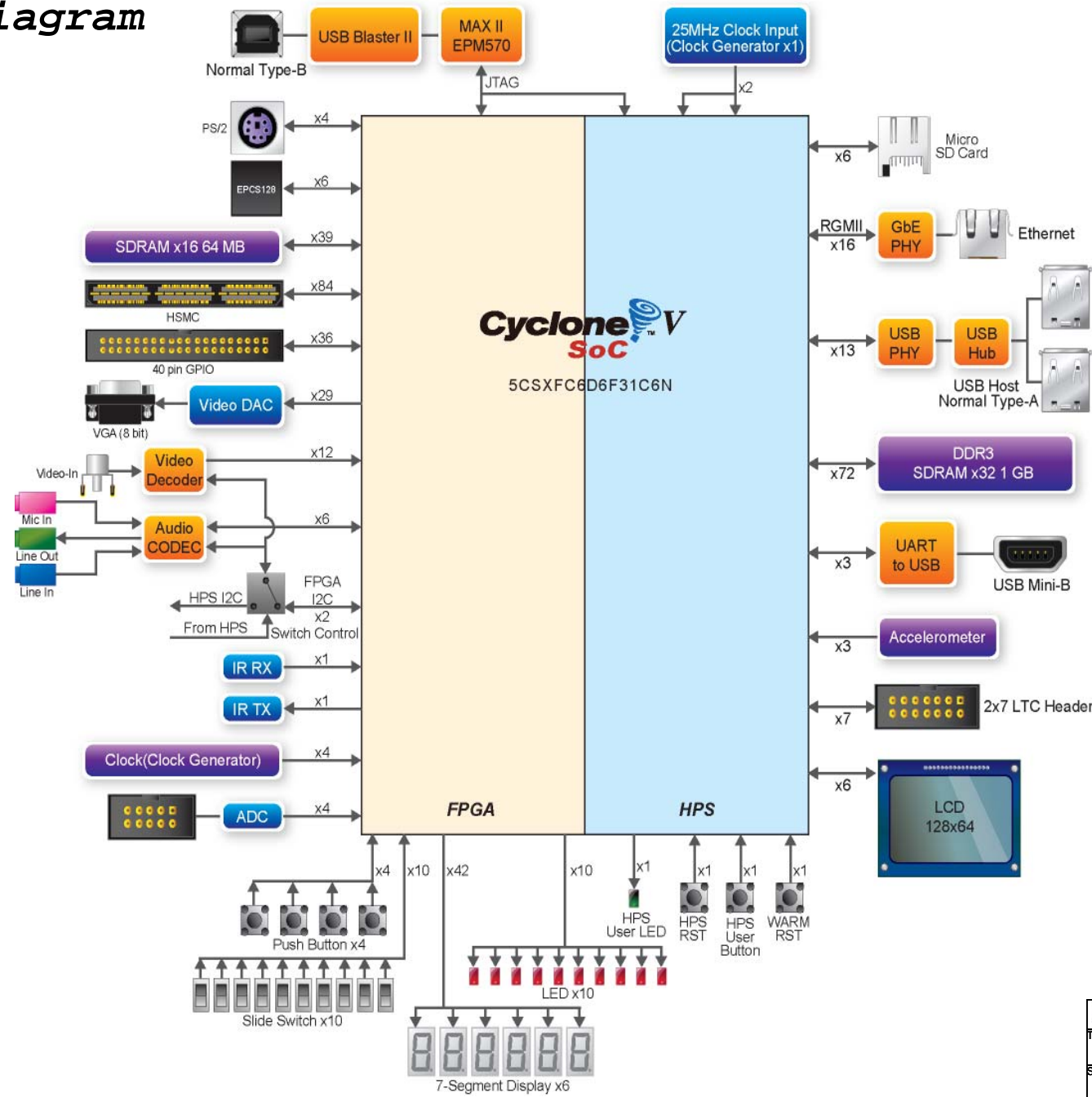
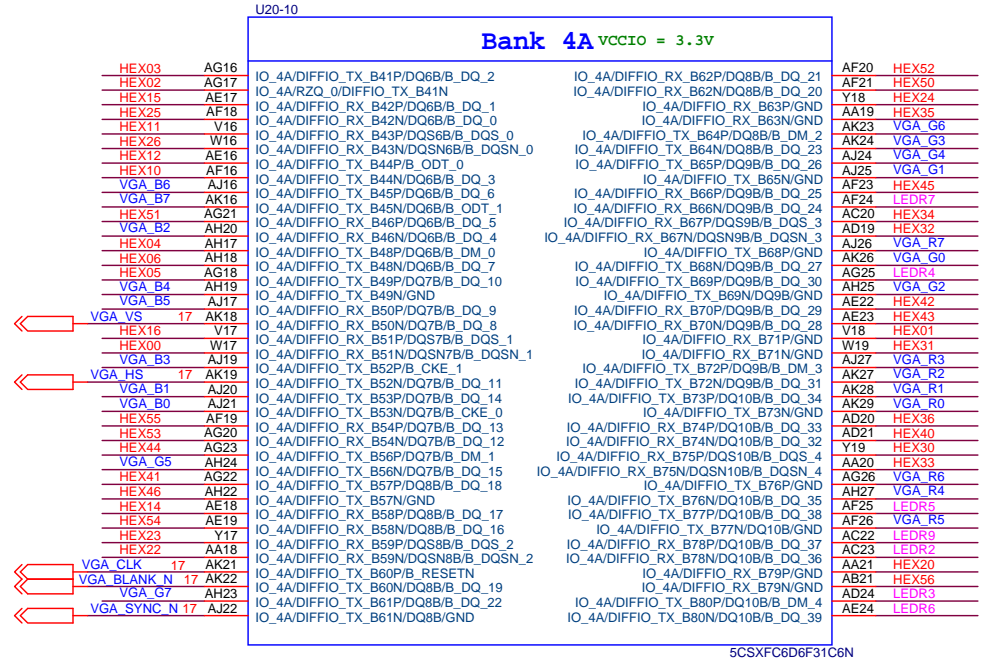
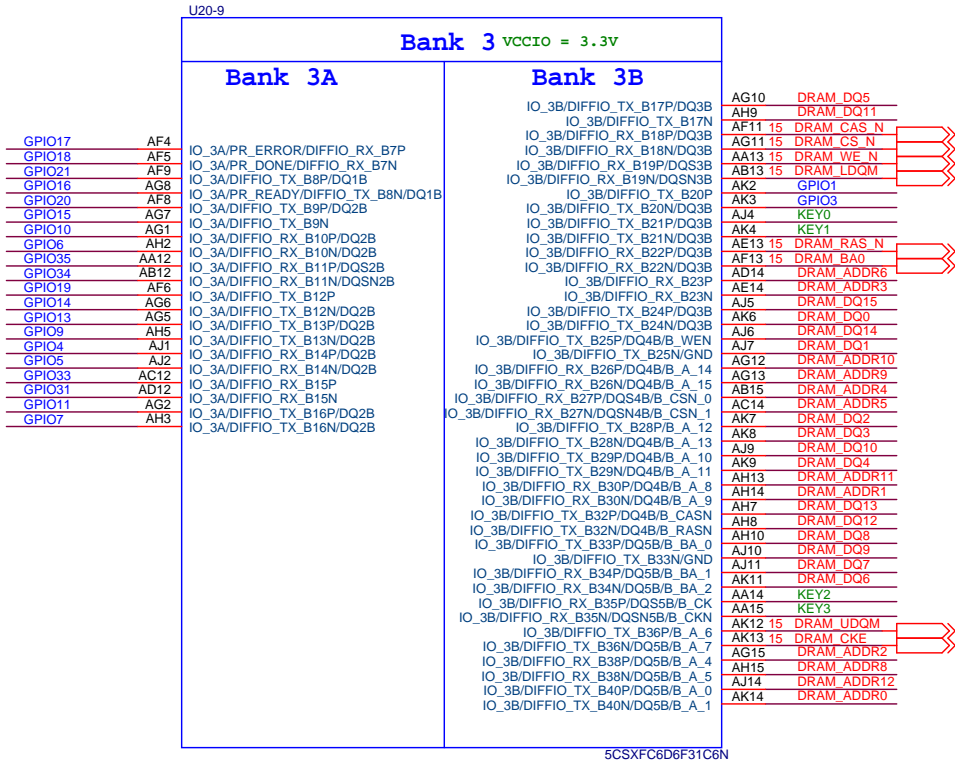
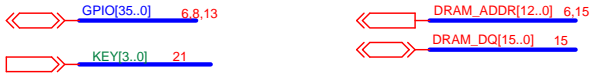


ALTERA Cyclone V SoC Development & Education Board (DE10-Standard)

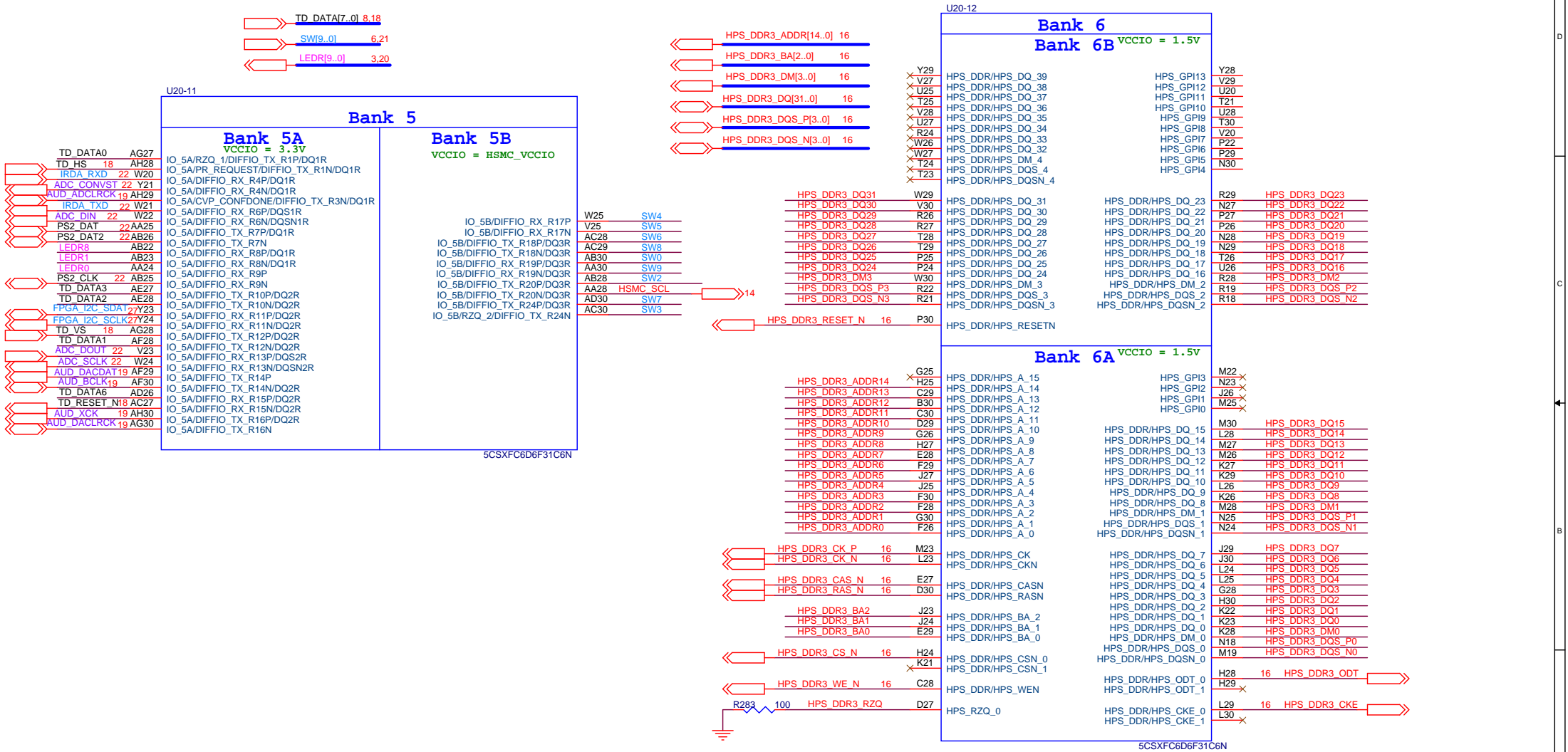
PAGE	CONTENT	PAGE	CONTENT
1	Cover Page	18	ADV7180 Video Decoder
2	Block Diagram	19	Audio CODEC
3	FPGA BANK 3, BANK 4	20	7-Segment Display, LED
4	FPGA BANK 5, BANK 6	21	FPGA BUTTON, Switch
5	FPGA BANK 7, BANK 8	22	ADC, PS2, IR Tx, IR Rx
6	FPGA Clocks, GND	23	2-port USB Host
7	Transceiver	24	1 Ggabit Ethernet
8	FPGA Configuration	25	UART to USB, SD CARD
9	FPGA Decoupling	26	Accelerometer, LTC Connector
10	FPGA Power	27	I2C Multiplexer, HPS BUTTON, HPS LED
11	USB Blaster II	28	LCD
12	JTAG Chain	29	Power - 1.1V
13	GPIO	30	Power - 5V, 3.3V
14	HSMC	31	Power - 9V, 2.5V, 1.5V
15	SDRAM, HPS QSPI Flash	32	Power - 1.2V, 1.8V, DDR3 VREF, DDR3 VTT
16	HPS DDR3 SDRAM	33	Power - VCCIO_HSMC & HSMC_VCCPD
17	ADV7123 VGA		

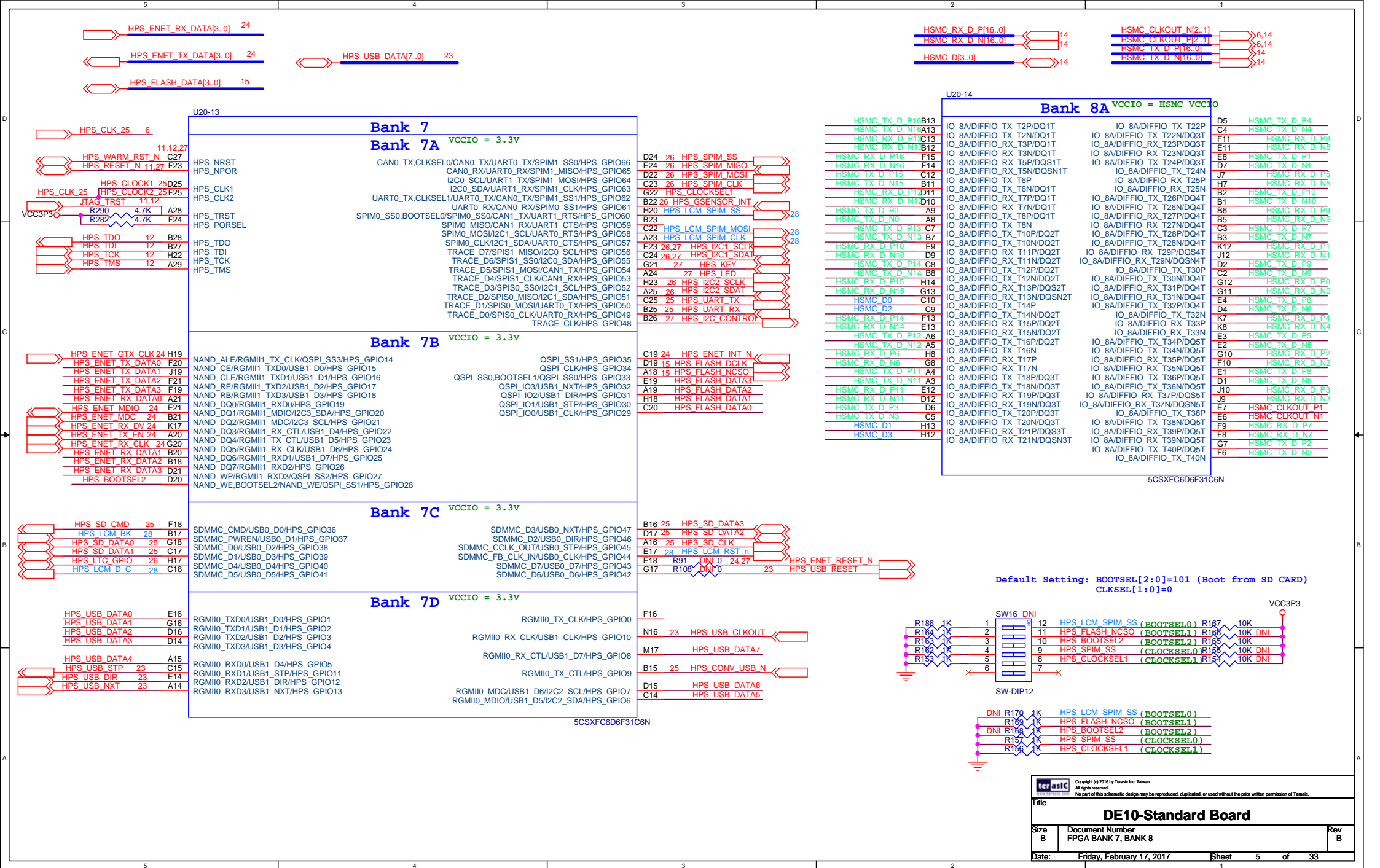
Block Diagram

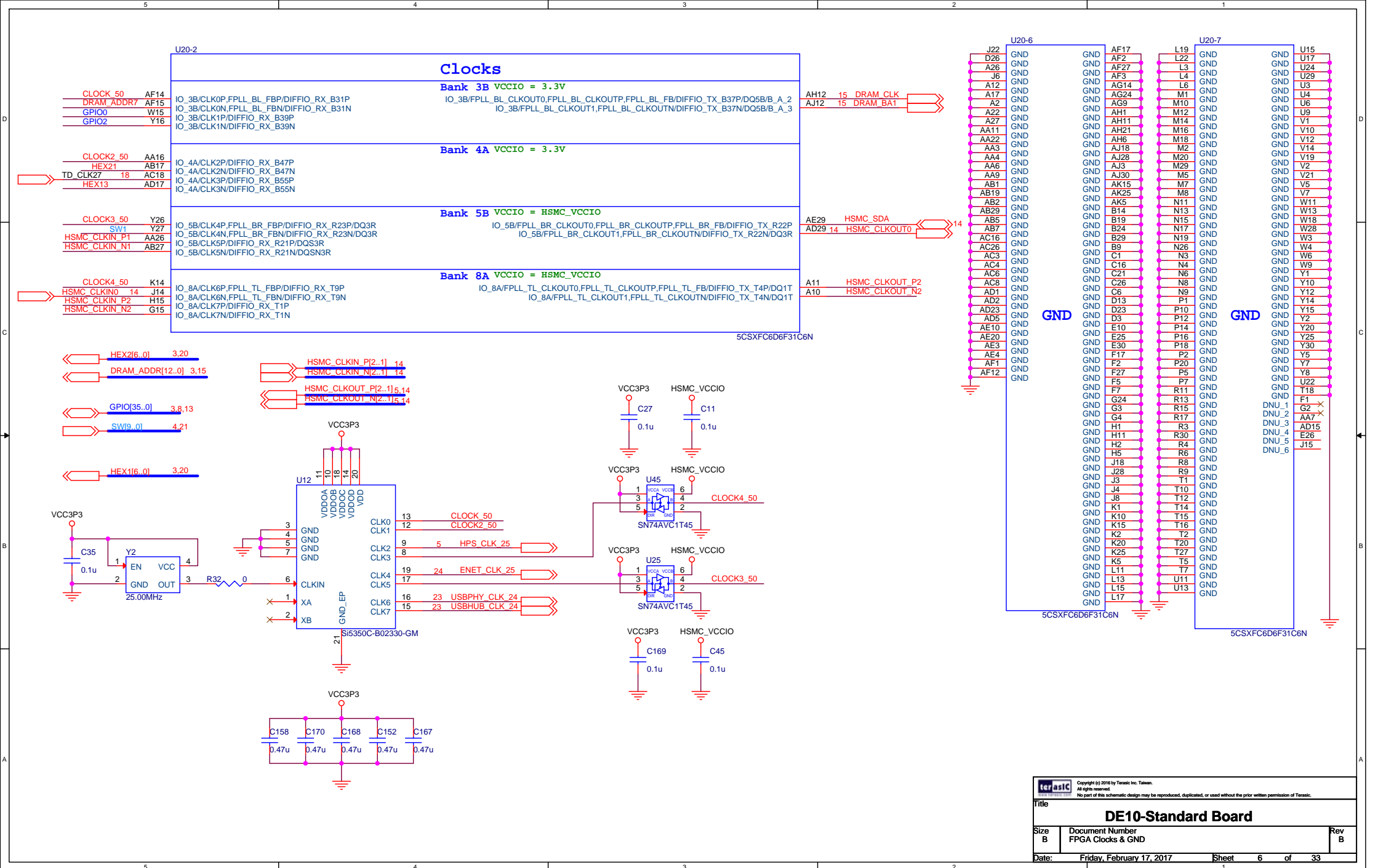


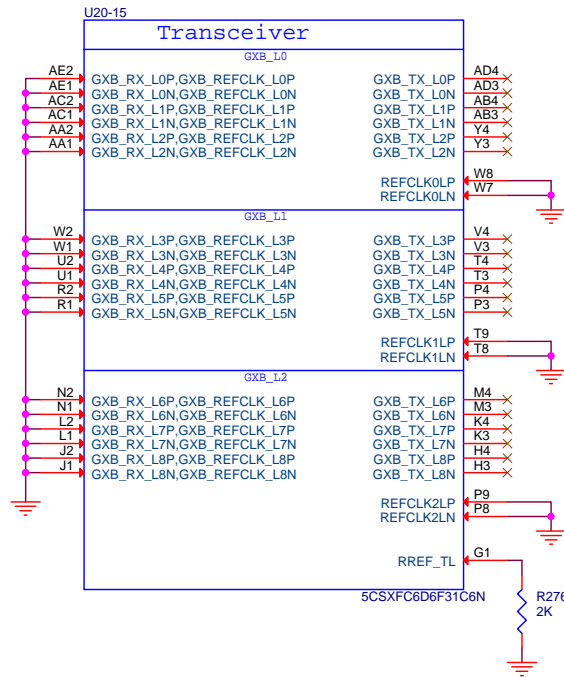


5CSXFC6D6F31C6N

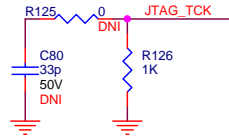
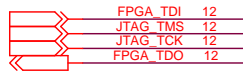






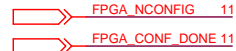
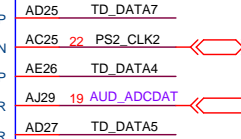
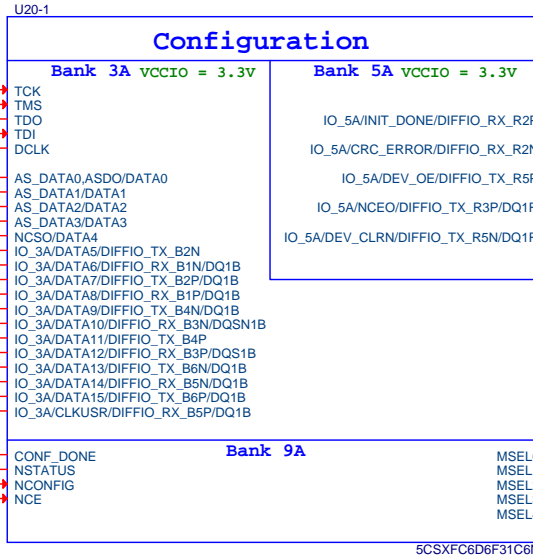
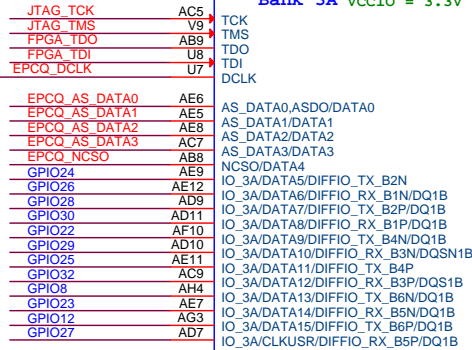
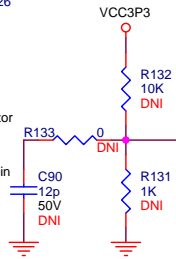


USB Blaster



Design Note:
Optional termination resistor
for DCLK

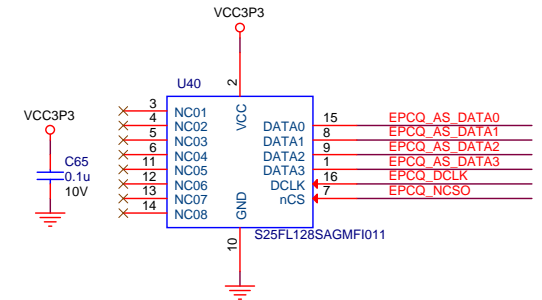
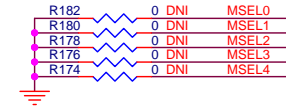
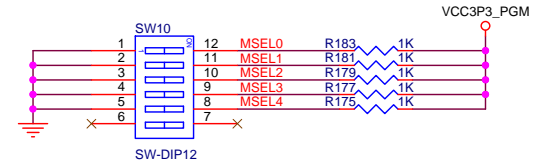
CAD Note:
Place near FPGA DCLK pin

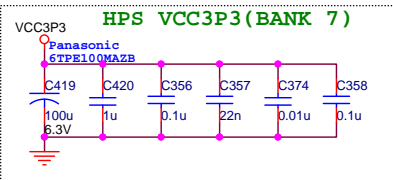
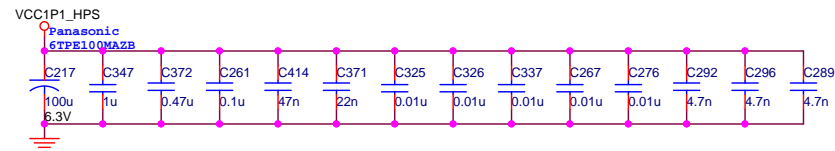
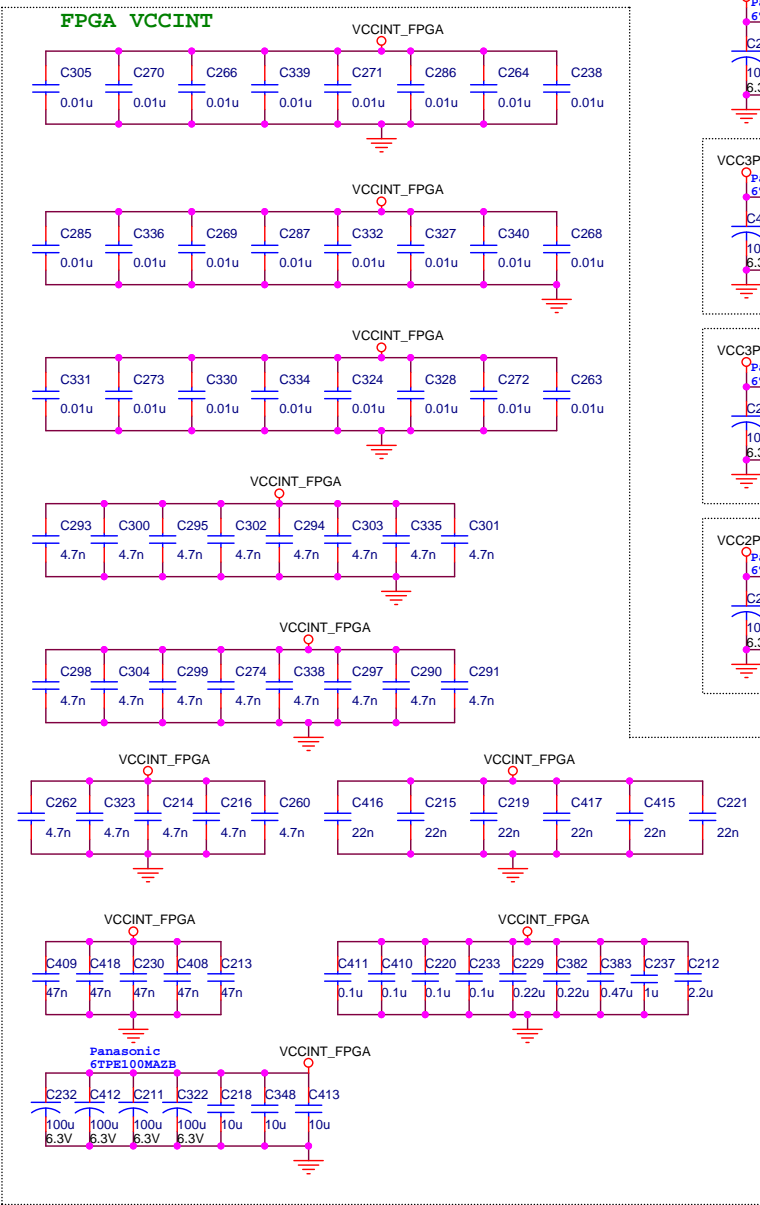


TD_DATA[7..0] 4,18

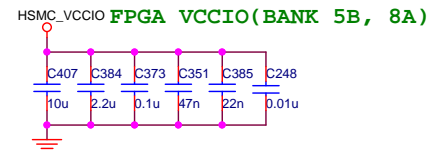
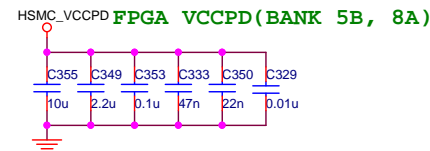
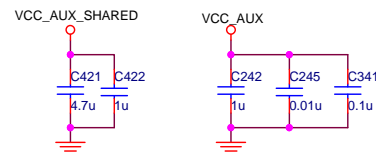
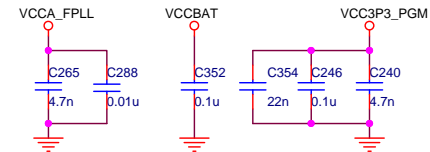
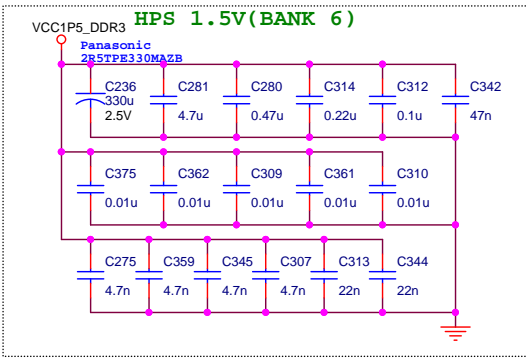
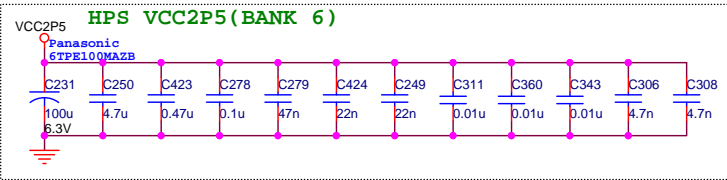
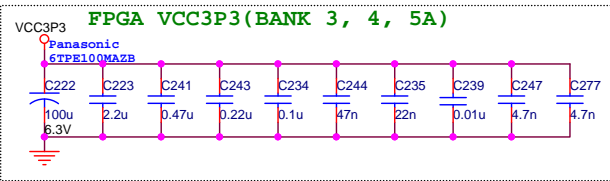
GPIO[35..0] 3,6,13

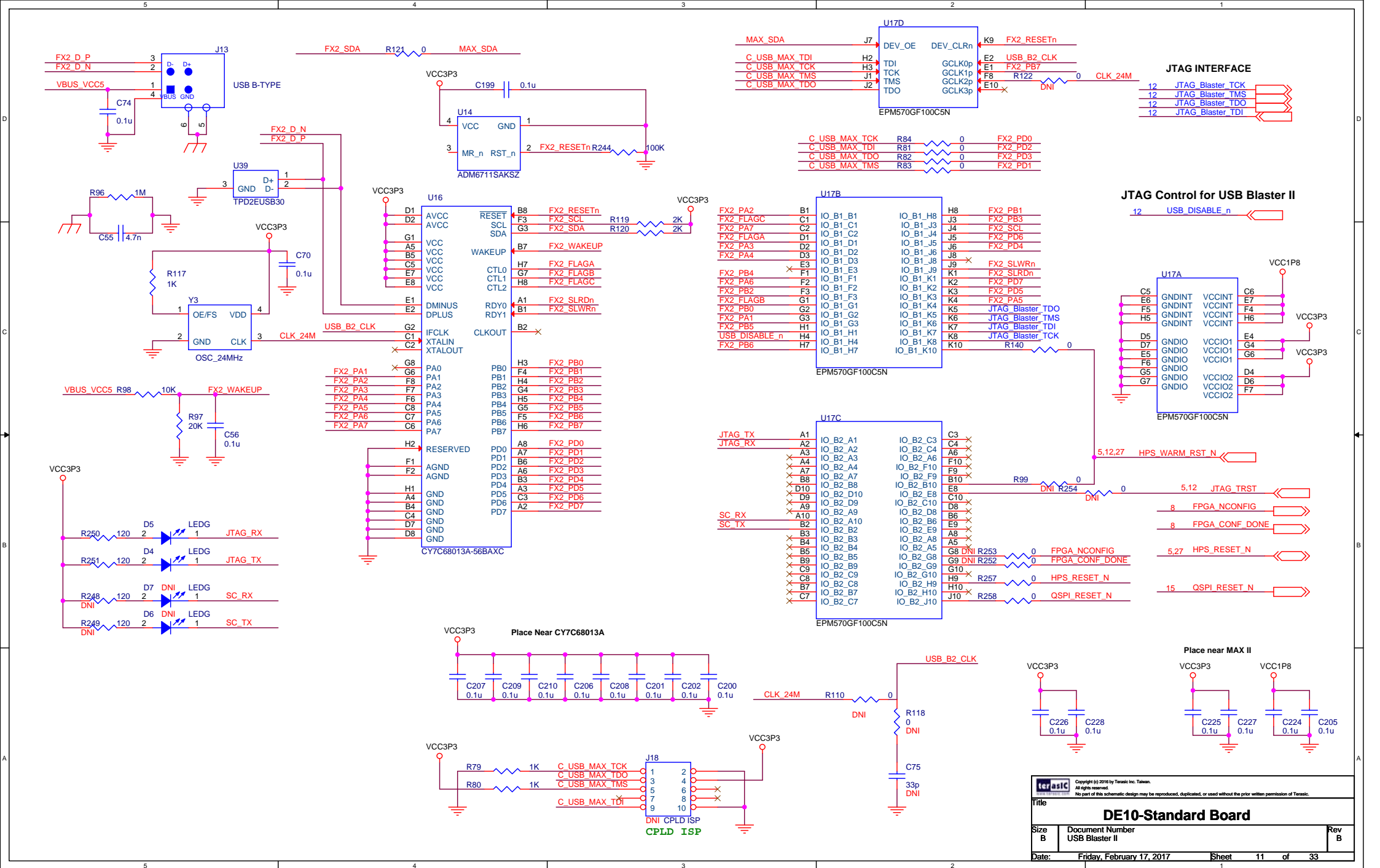
Fix MSEL[4:0]=10010 in AS Fast Mode

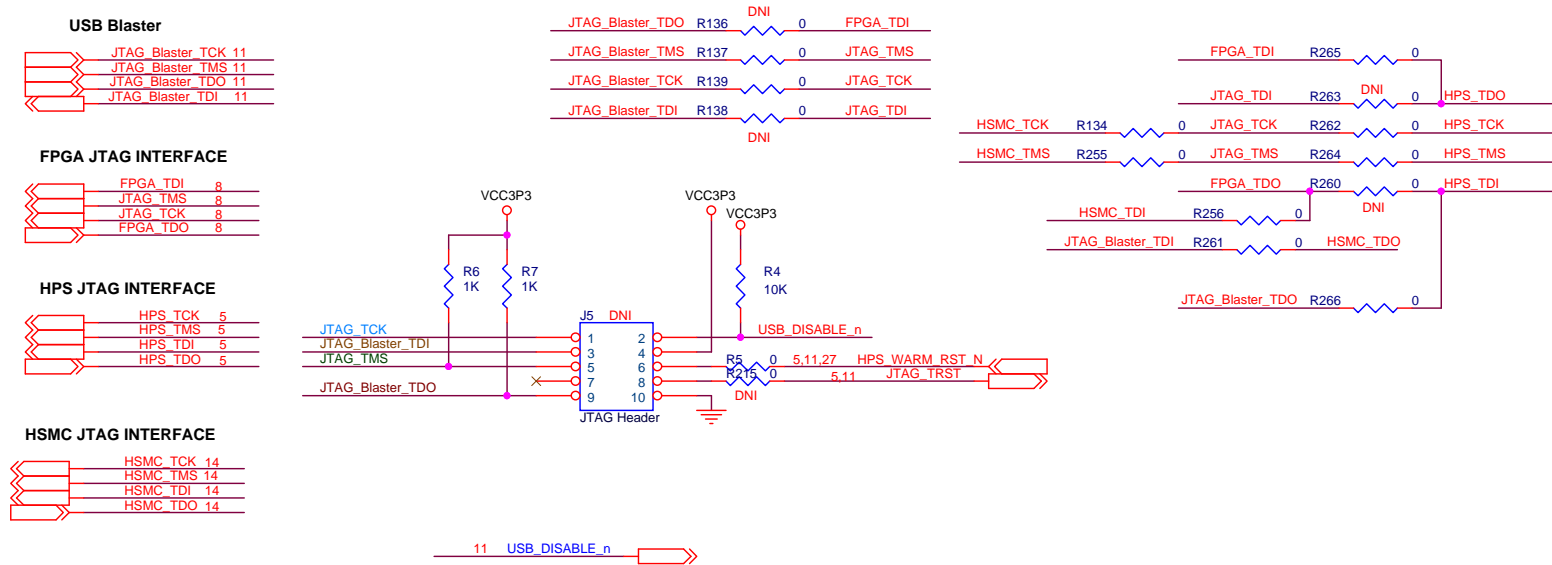




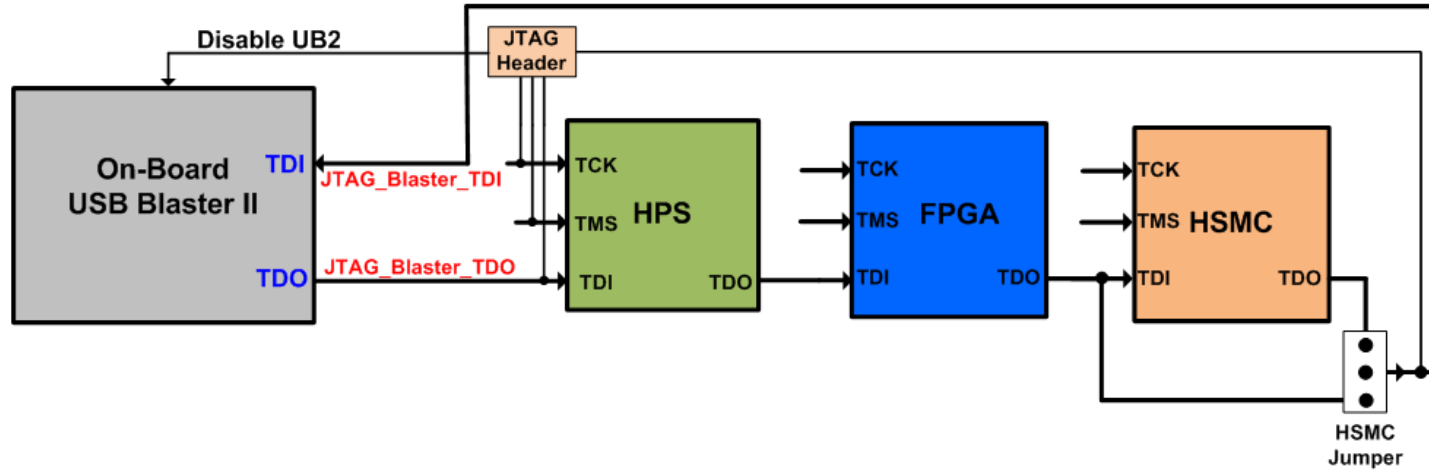
Place C394 close to J20/G23 pin

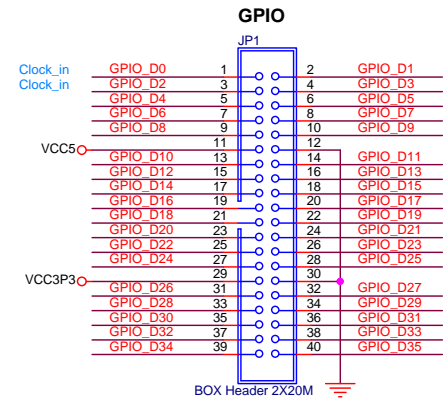
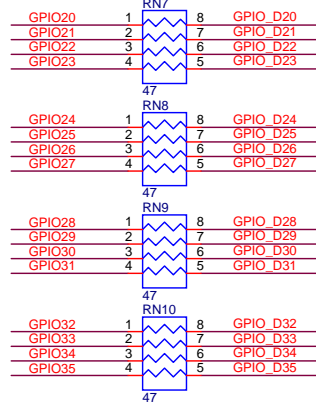
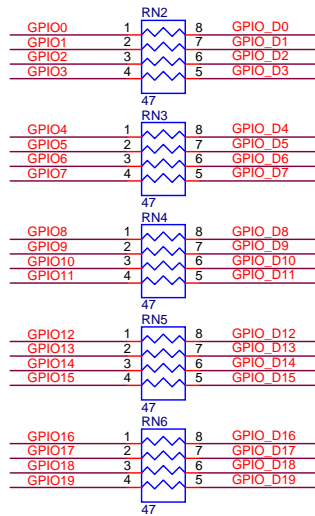
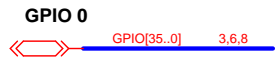
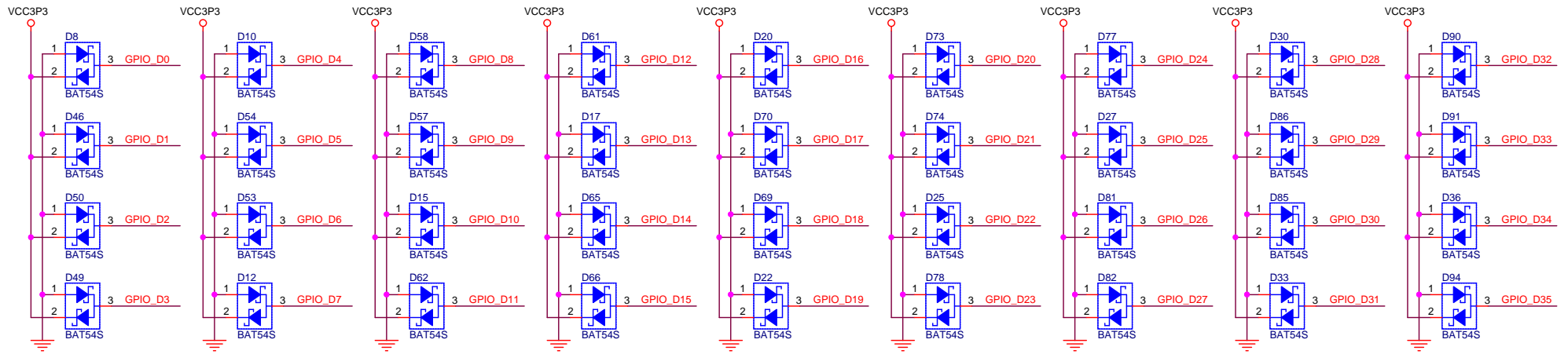


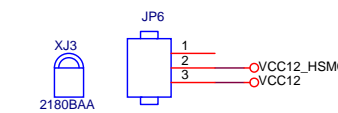
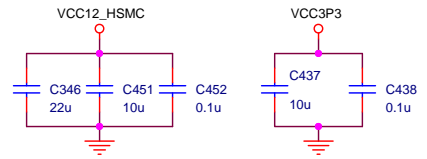
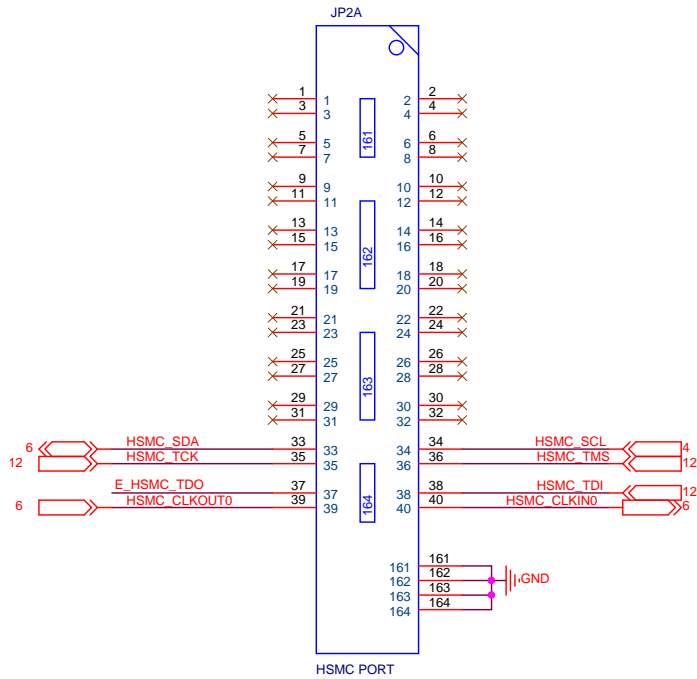




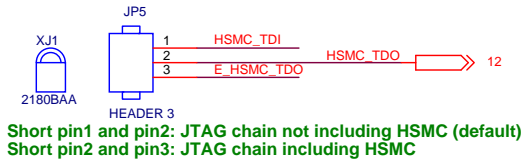
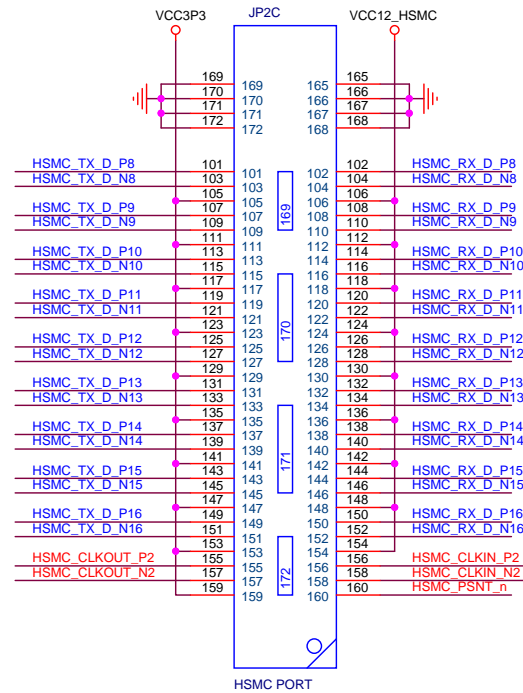
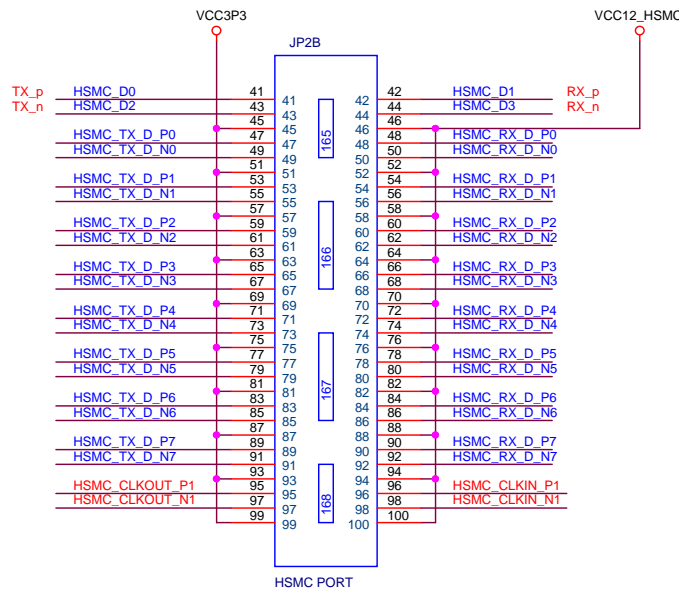
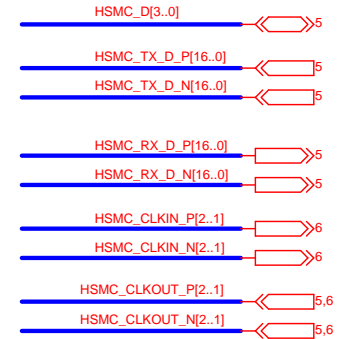
JTAG Chain



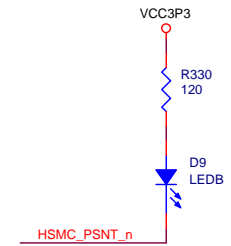




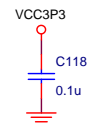
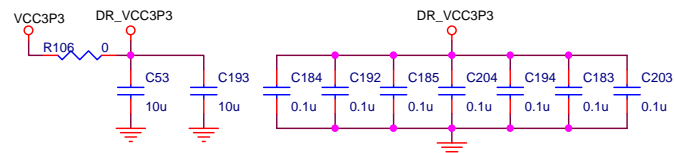
Short pin1 and pin2: without HSMC 12V power (default)
Short pin2 and pin3: with HSMC 12V power

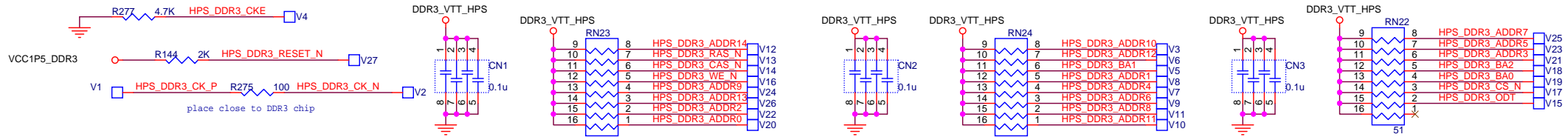


Short pin1 and pin2: JTAG chain not including HSMC (default)
Short pin2 and pin3: JTAG chain including HSMC

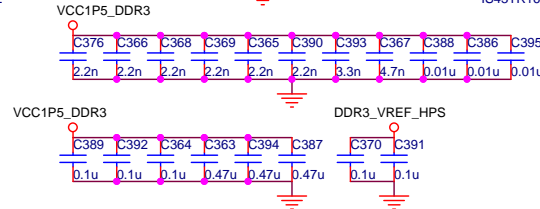
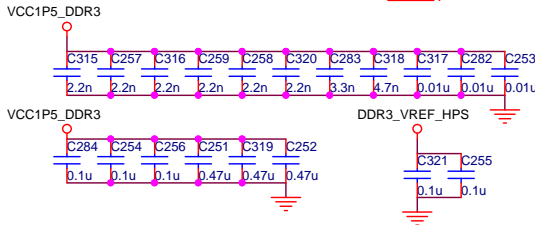
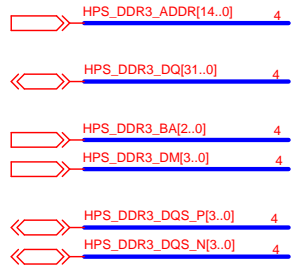


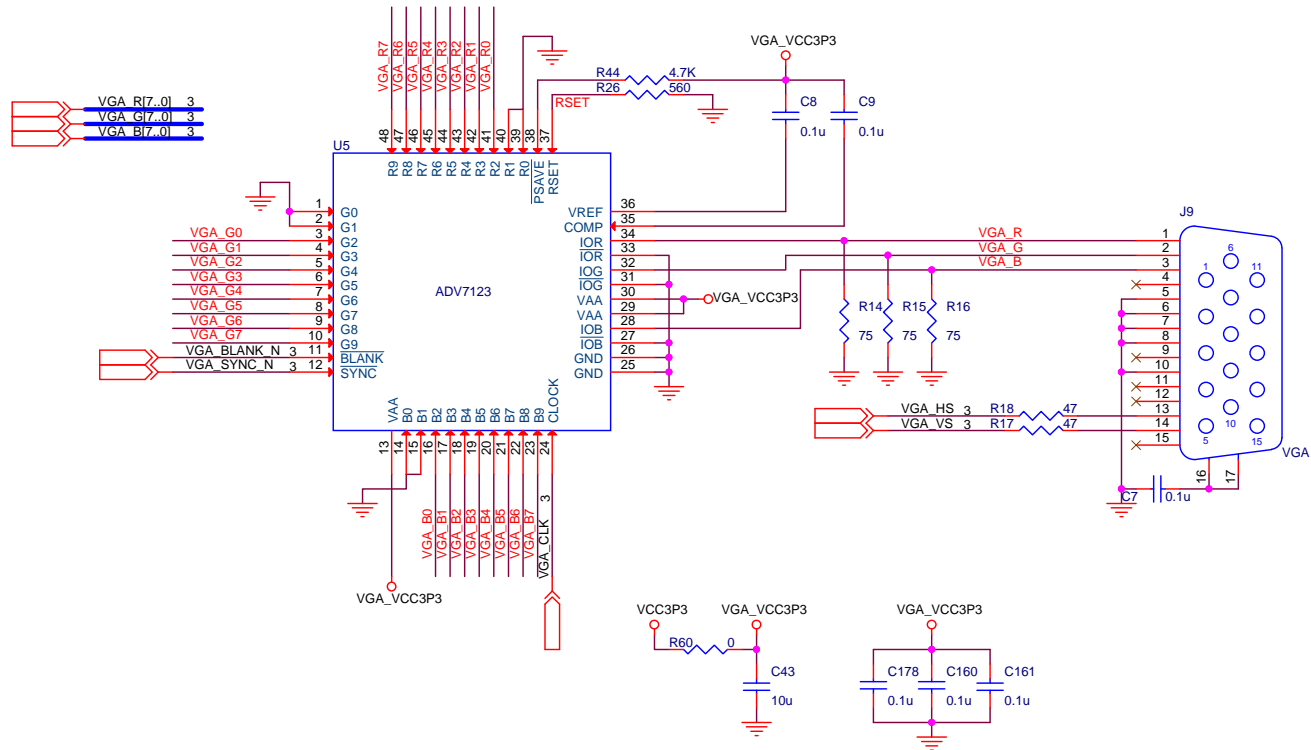
<div> <div>terasic</div> <div>Copyright (c) 2016 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.</div> </div>		
Title		
DE10-Standard Board		
Size B	Document Number HSMC	Rev B
Date:	Friday, February 17, 2017	Sheet 14 of 33

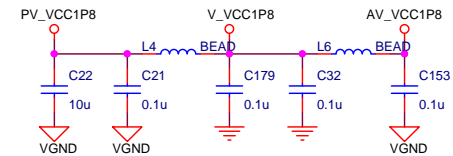
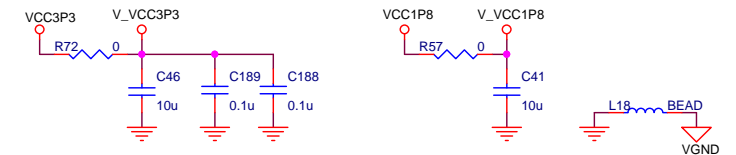
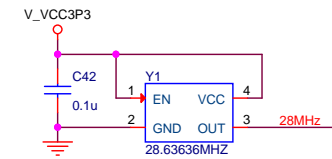
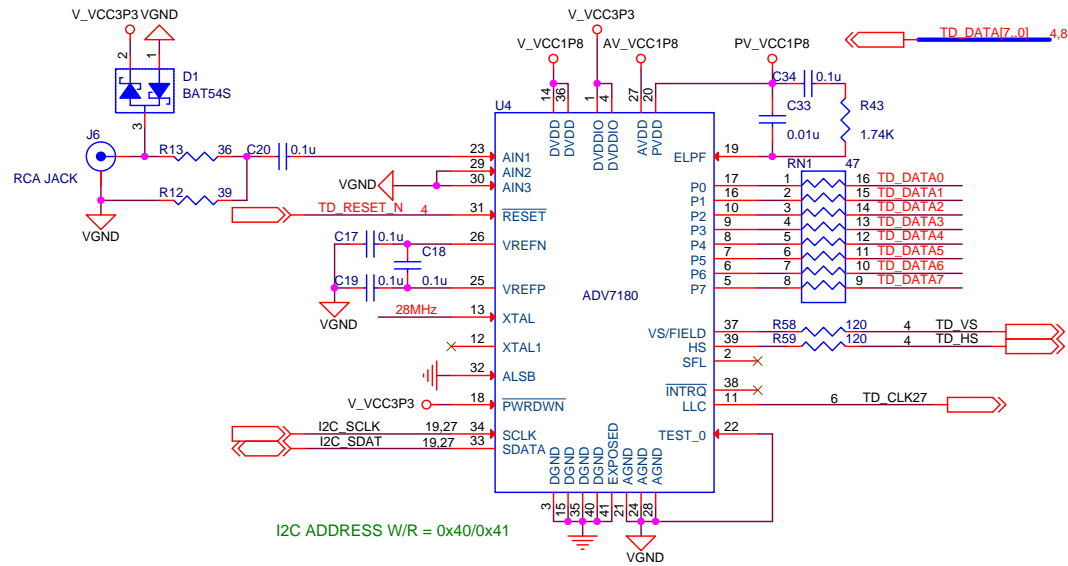


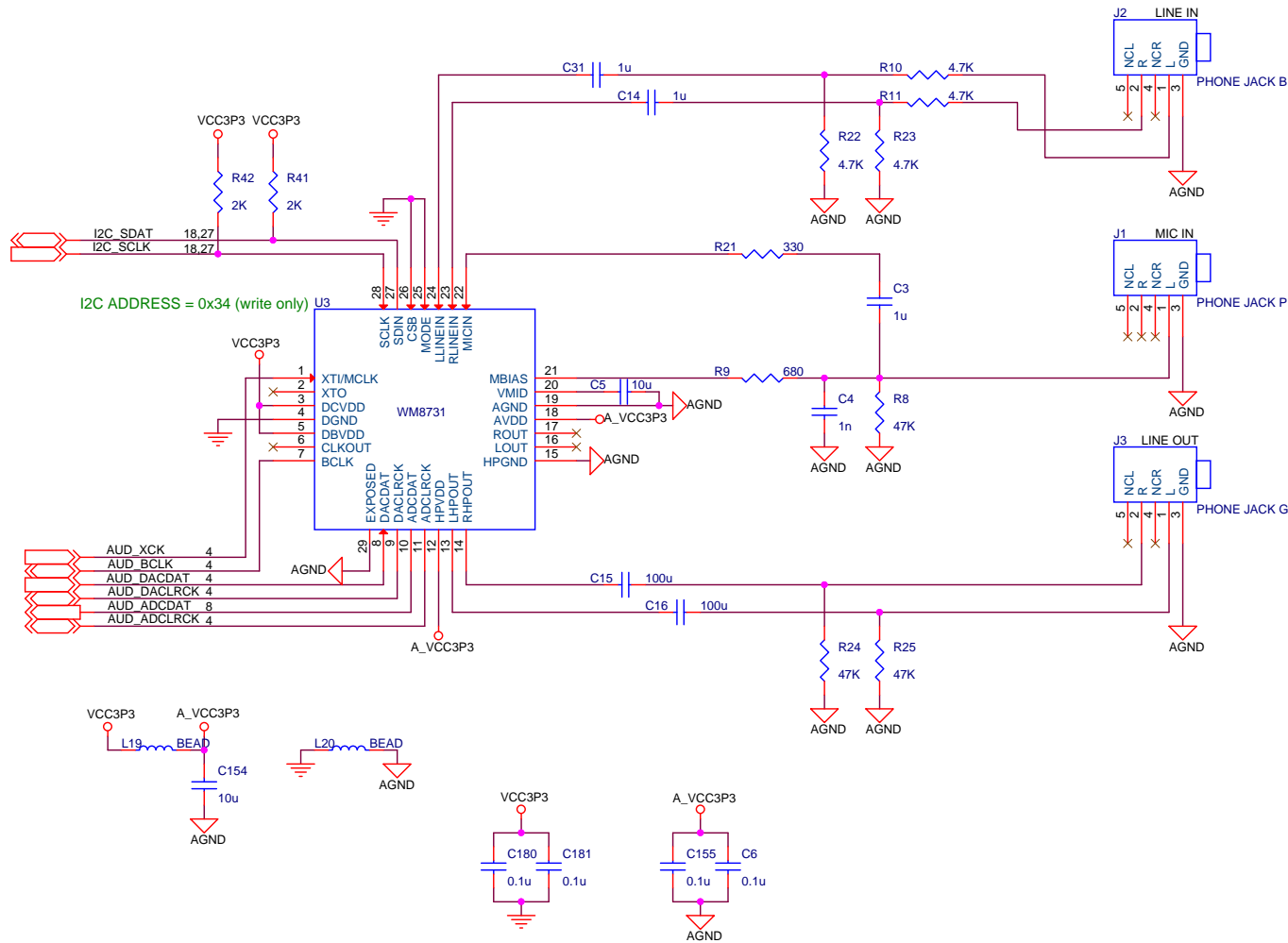


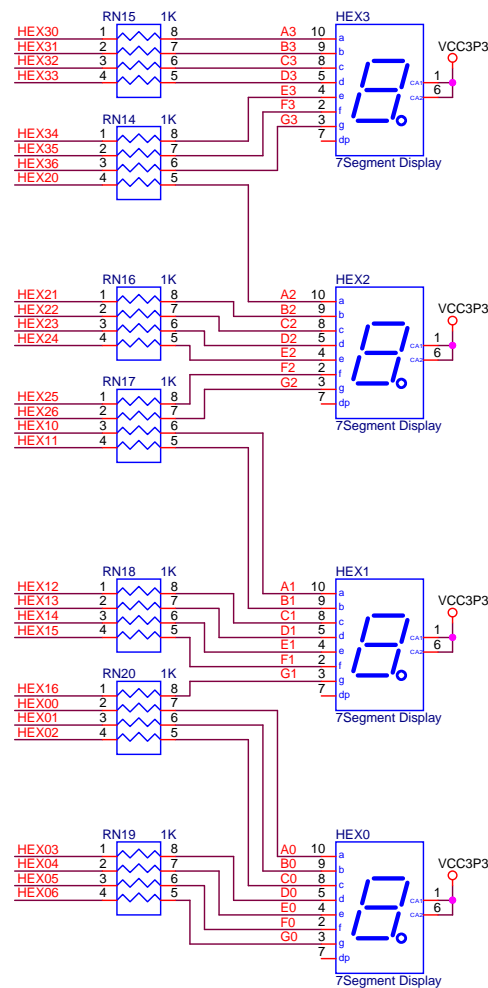
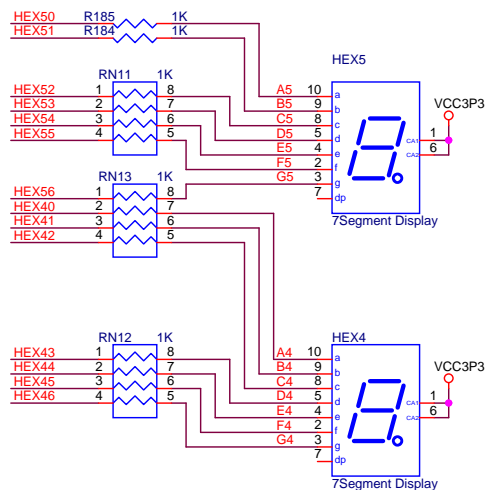
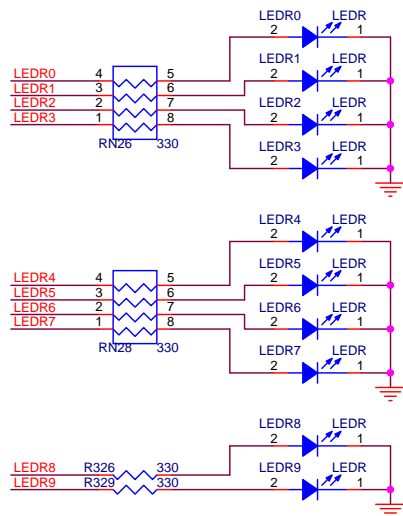
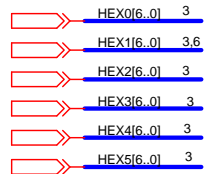
Note:you can only swap the DQ signals within x8 group (e.g. 0-7,8-15,16-23,24-31) on the DDR3 chips Note:you can swap the signals on the OCT resistor array(include NC pin)



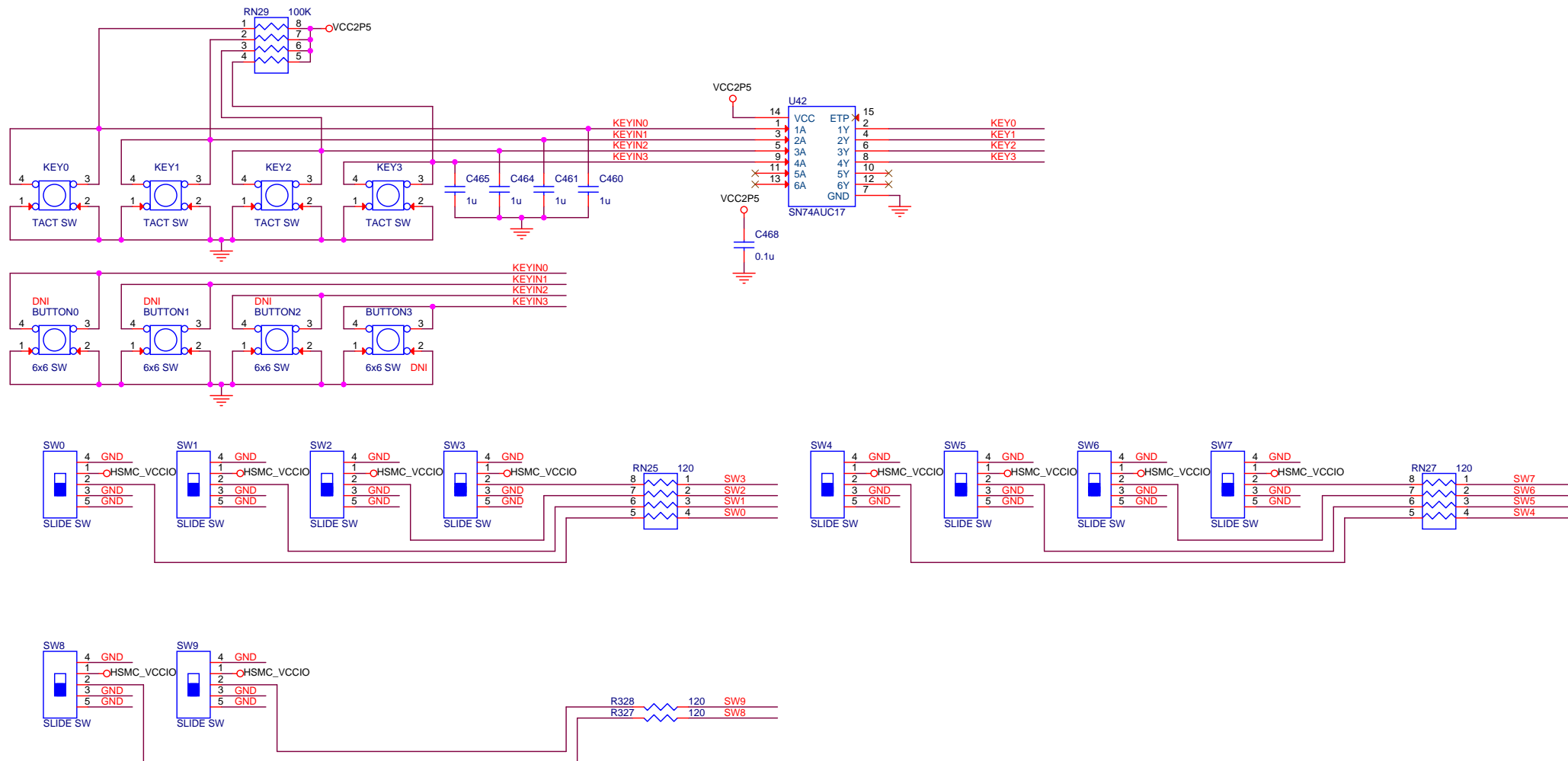


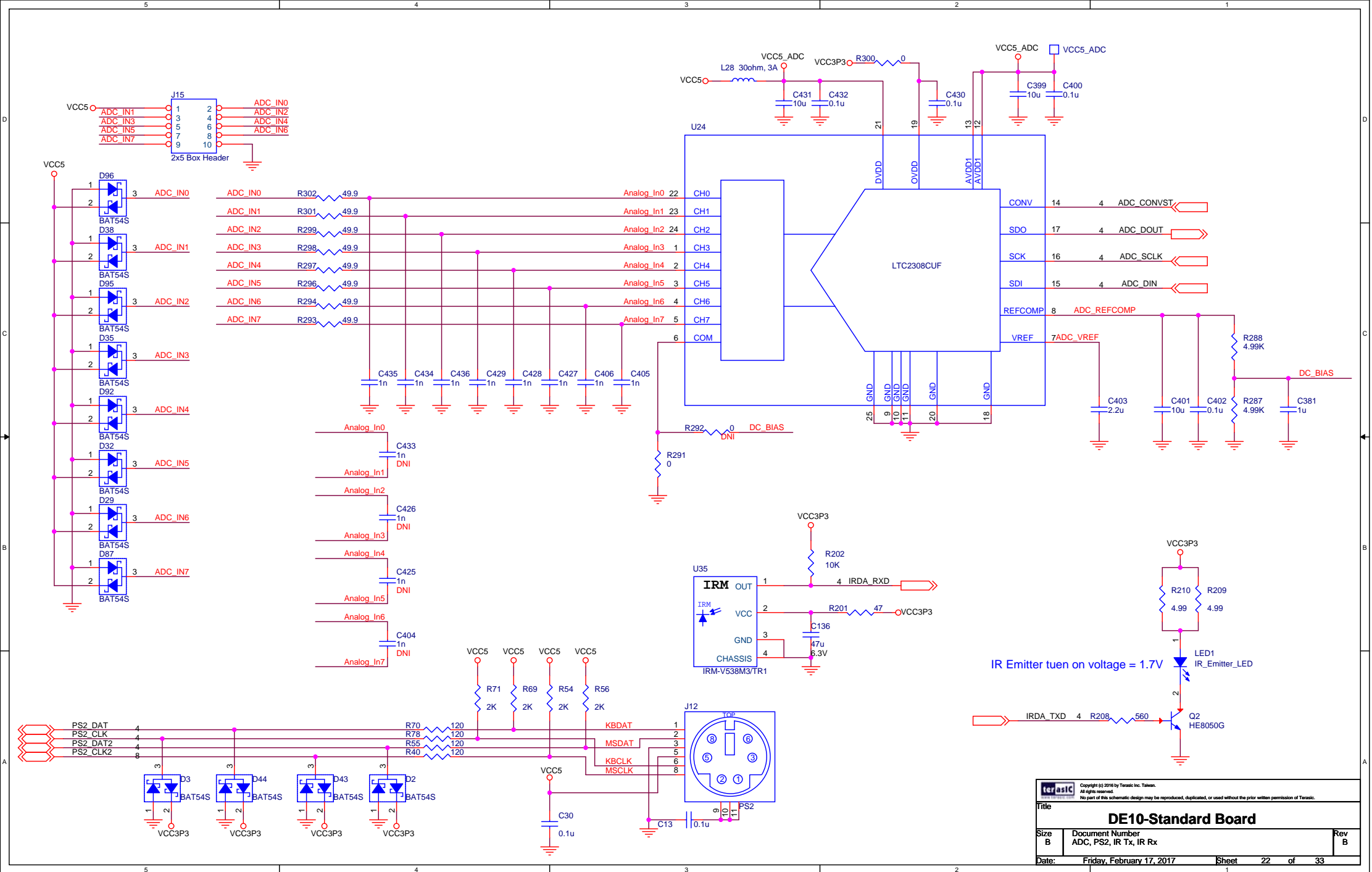


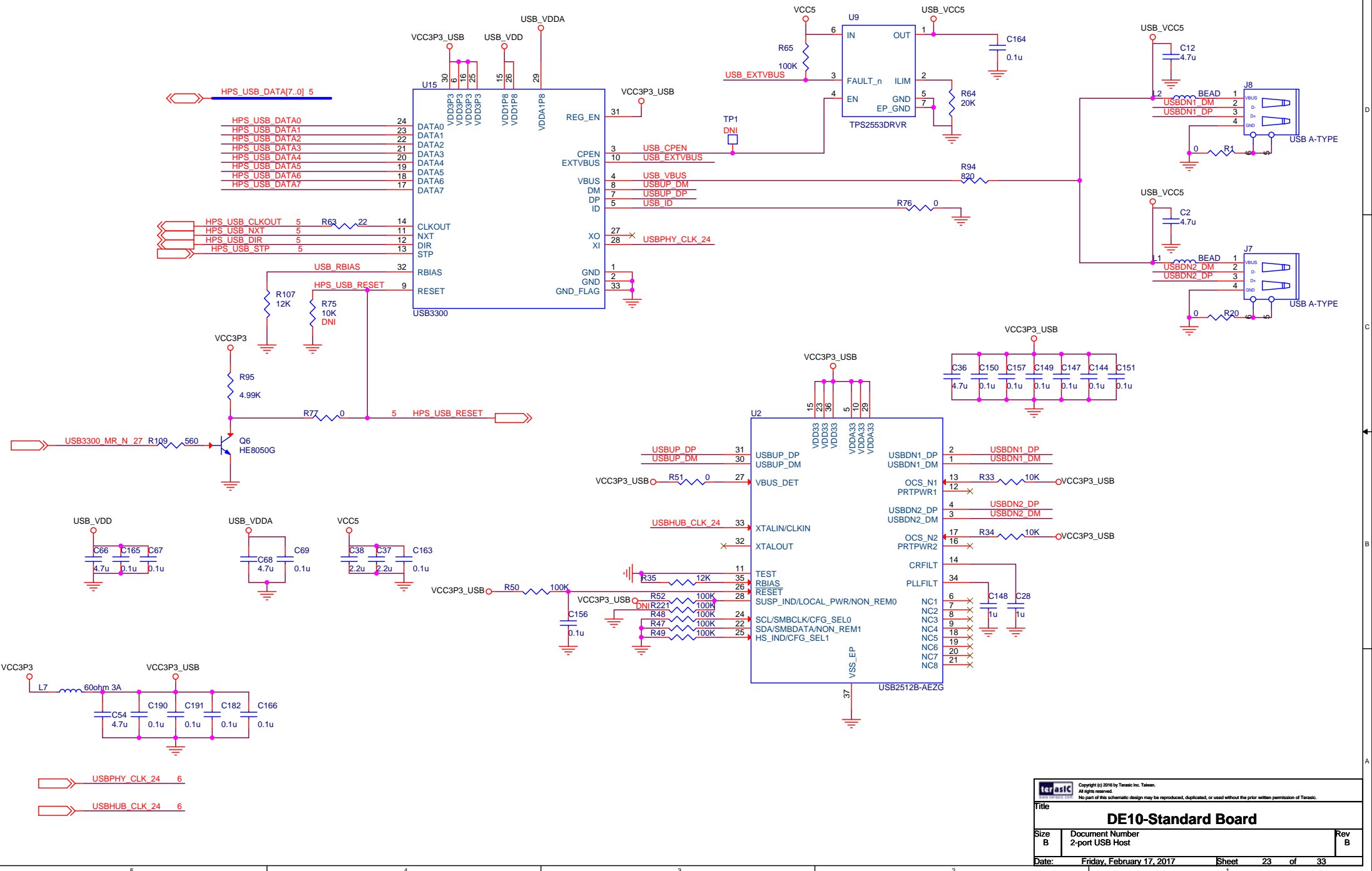


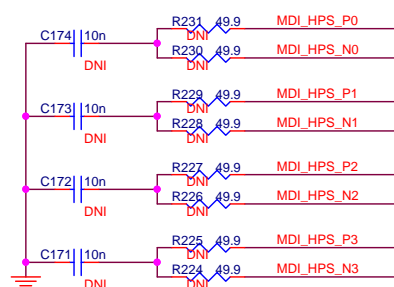
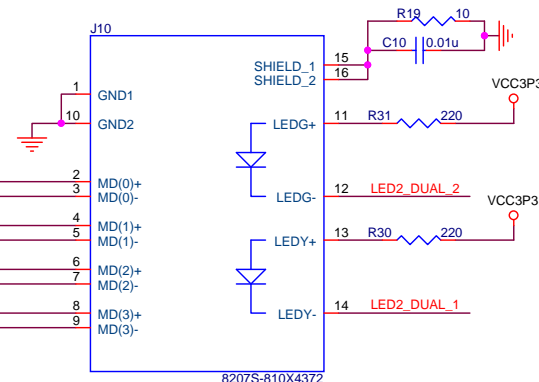
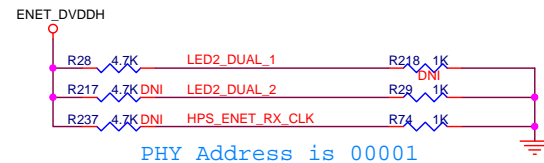
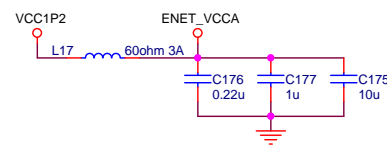
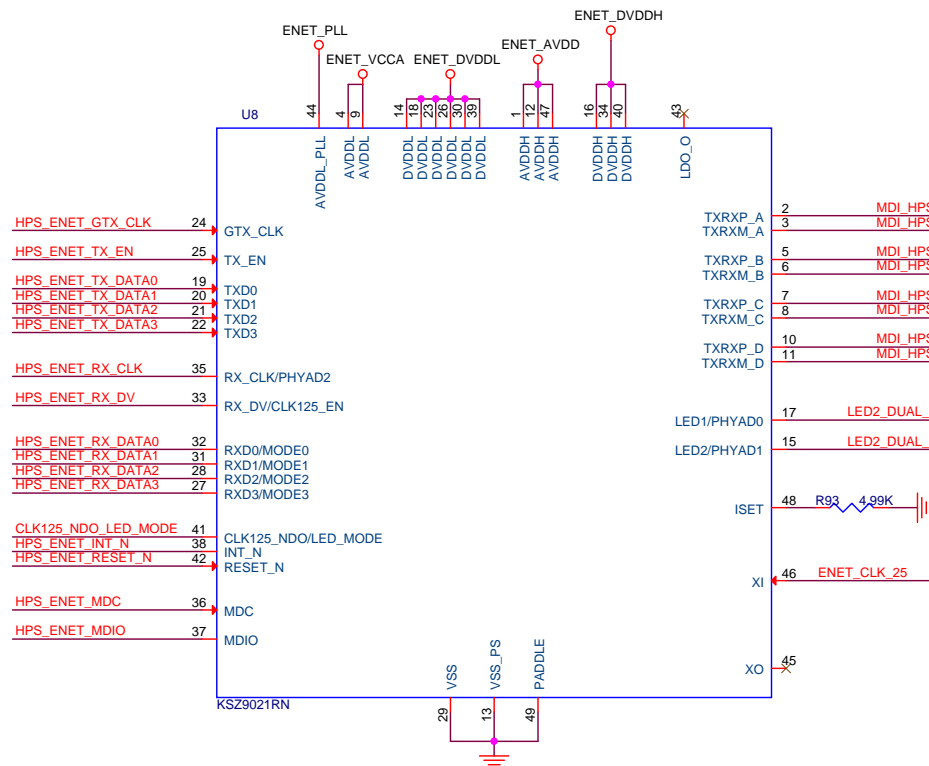
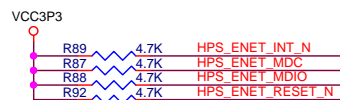
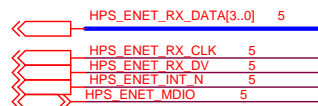


KEY[3..0] 3
SW[9..0] 4,6



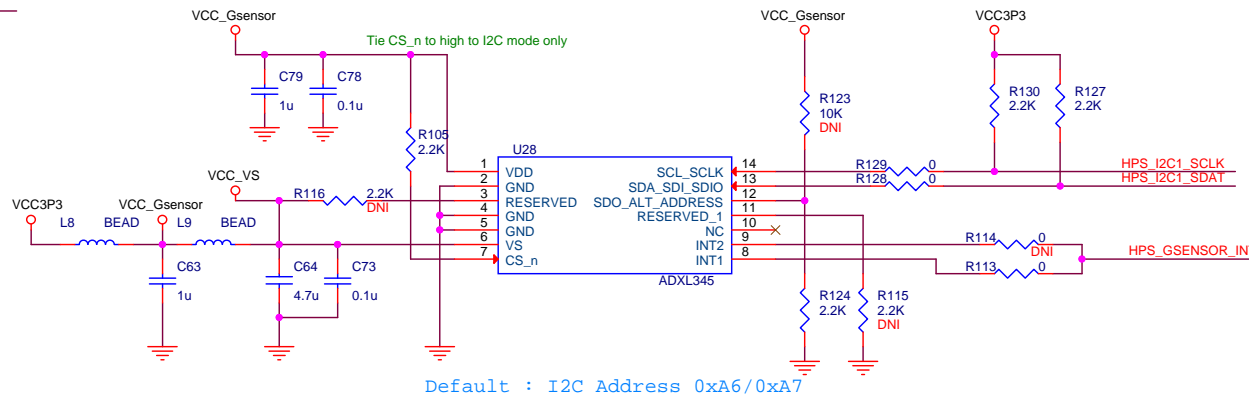




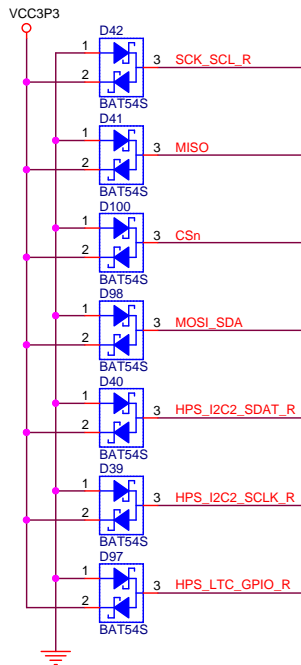


HPS_I2C1_SDAT 5,27
HPS_I2C1_SCLK 5,27
HPS_GSENSOR_INT 5

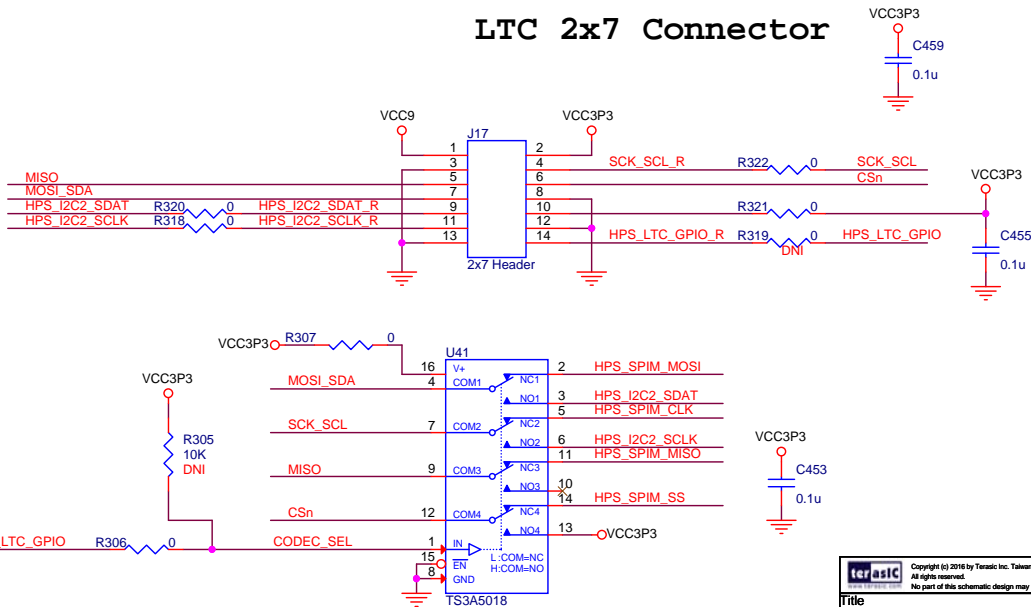
Digital Accelerometer



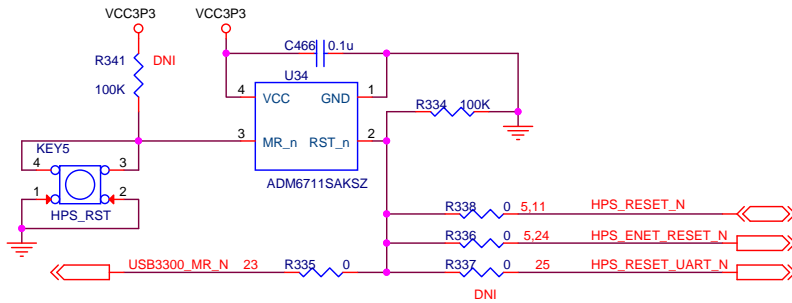
HPS_I2C2_SCLK 5
HPS_I2C2_SDAT 5
HPS_SPIM_MOSI 5
HPS_SPIM_CLK 5
HPS_SPIM_SS 5
HPS_SPIM_MISO 5
HPS_LTC_GPIO 5



LTC 2x7 Connector

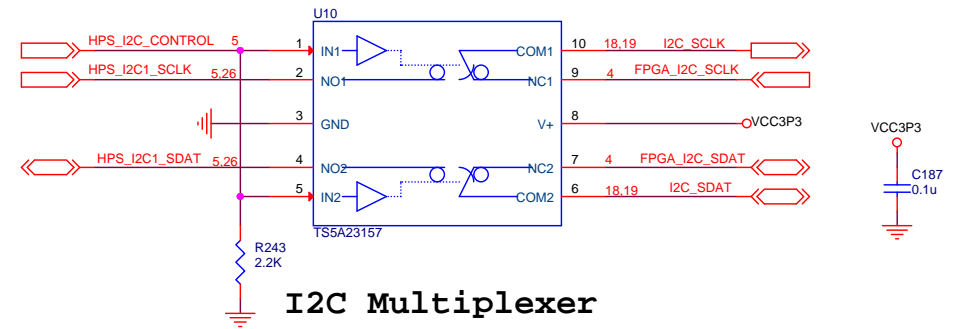


terasic Copyright (c) 2016 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE10-Standard Board		
Size	Document Number	Rev
B	Accelerometer, LTC Connector	B
Date:	Friday, February 17, 2017	Sheet 26 of 33

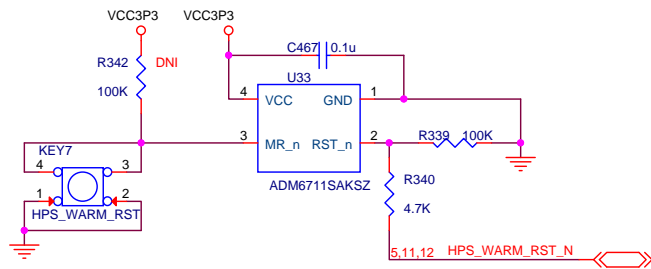


HPS Cold Reset

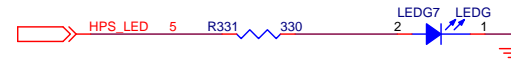
LOW --> NC to/from COM = ON and NO to/from COM = OFF
HIGH --> NC to/from COM = OFF and NO to/from COM = ON



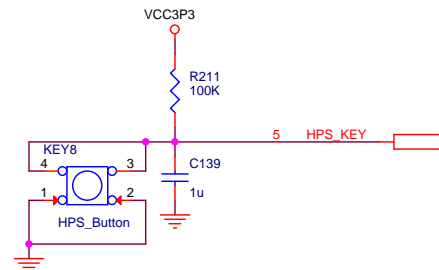
I2C Multiplexer



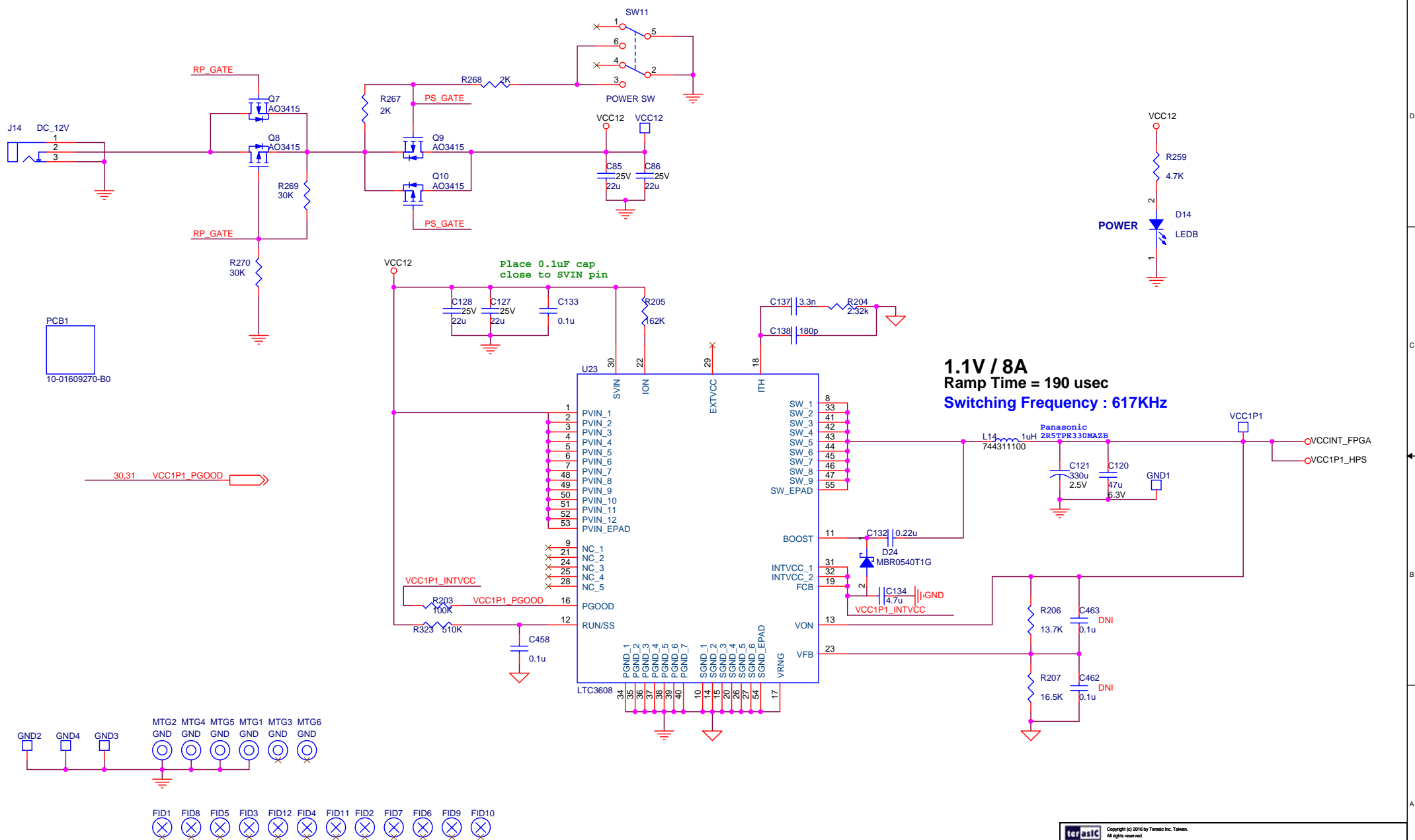
HPS Warm Reset

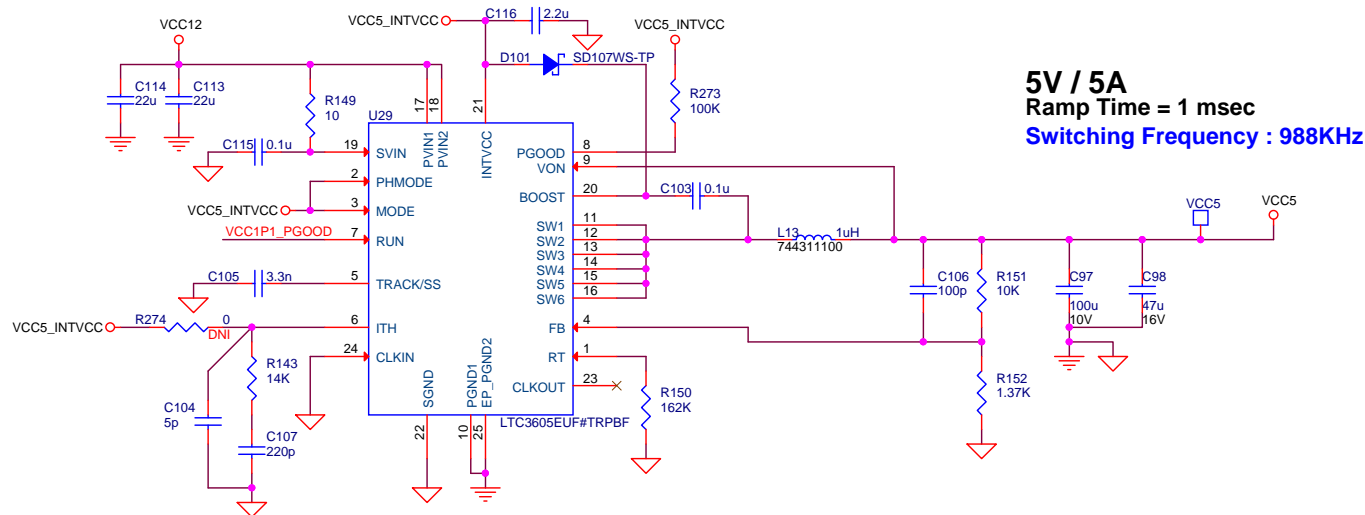
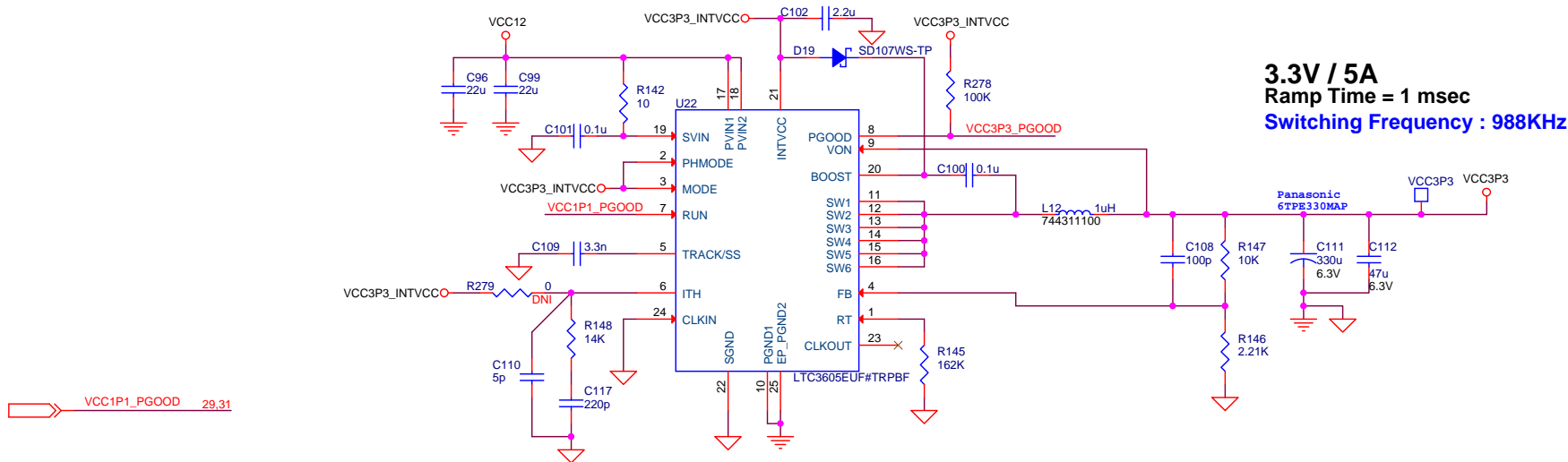


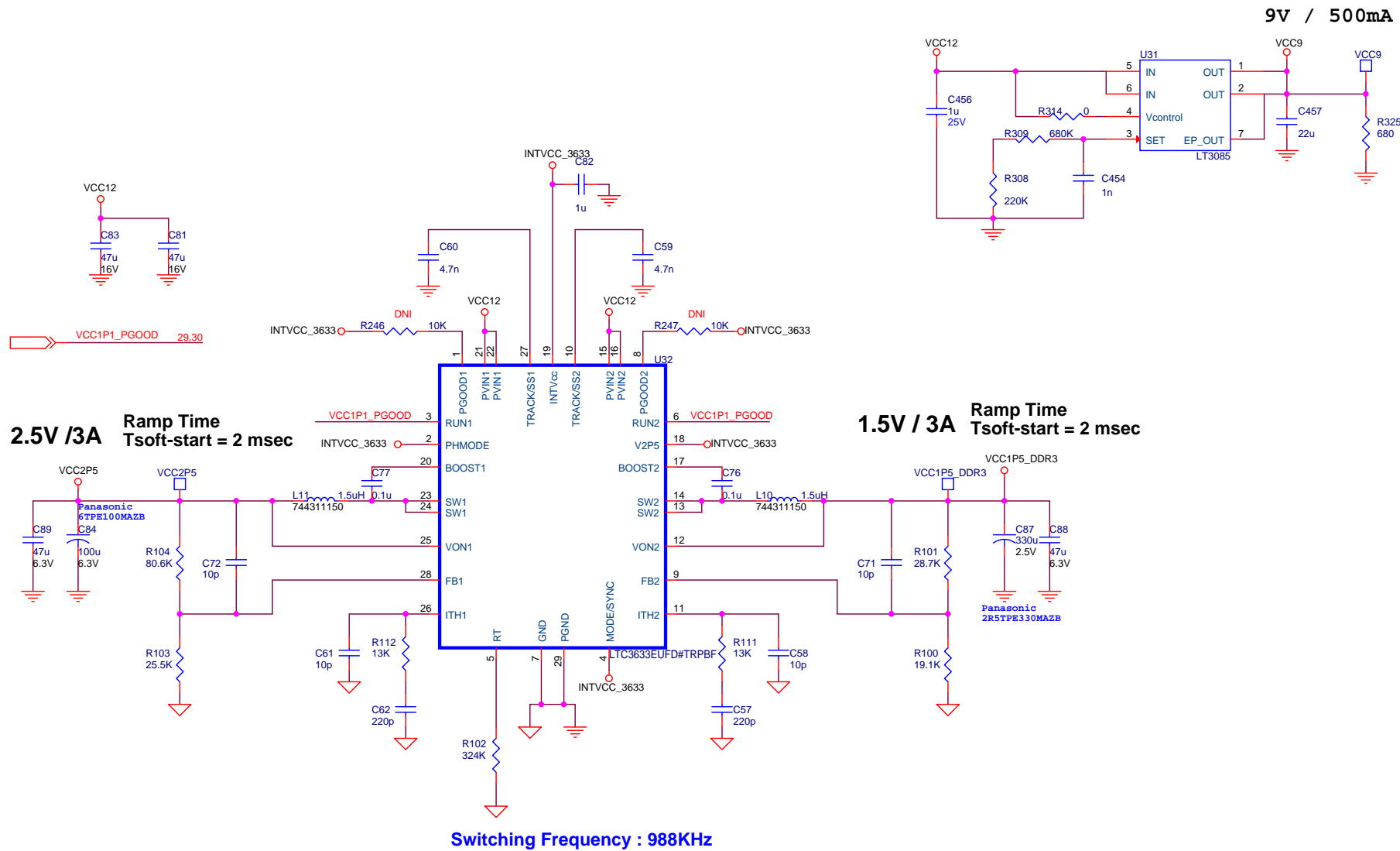
HPS User LED



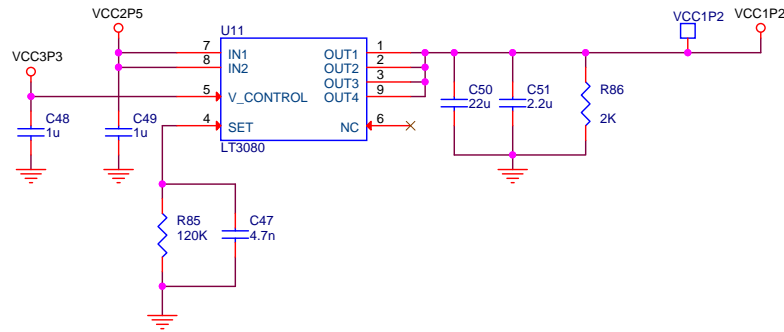
HPS User Button



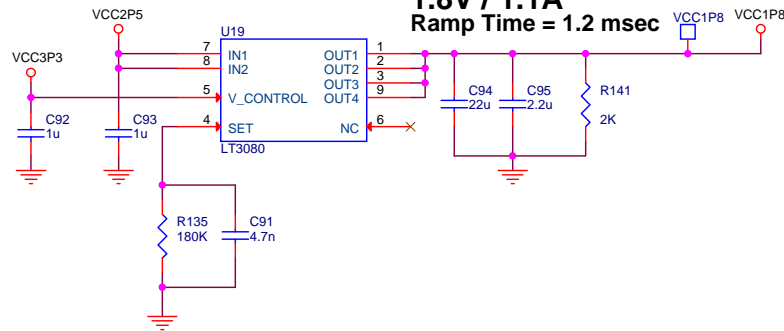




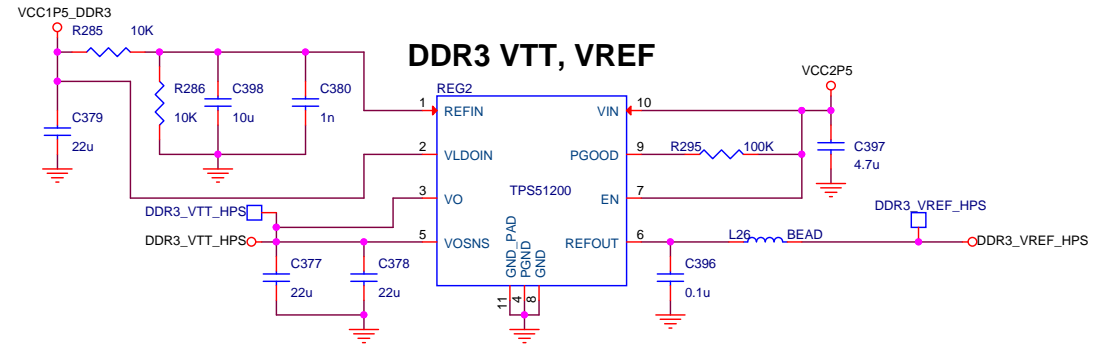
1.2V / 1.1A
Ramp Time = 0.8msec



1.8V / 1.1A
Ramp Time = 1.2 msec



DDR3 VTT, VREF



HSMC_VCCIO / 0.5A Adjustable: 3.3/2.5/1.8/1.5 V
Default: 2.5V

