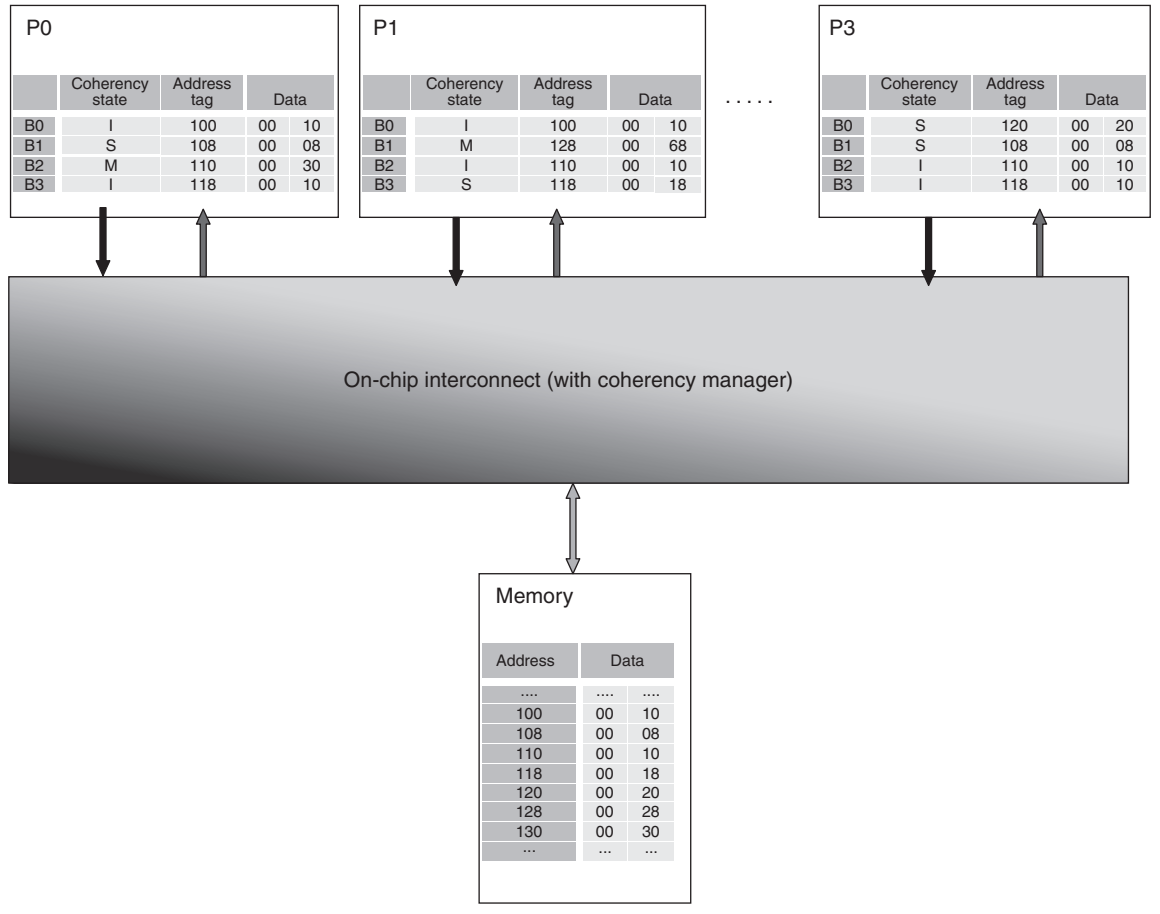
P0
Coherency state
Address tag
Data
B0 I 100 00 10
B1 S 108 00 08
B2 M 110 00 30
B3 I 118 00 10
P1
Coherency state
Address tag
Data
B0 I 100 00 10
B1 M 128 00 68
B2 I 110 00 10
B3 S 118 00 18
.....
P3
Coherency state
Address tag
Data
B0 S 120 00 20
B1 S 108 00 08
B2 I 110 00 10
B3 I 118 00 10
On-chip interconnect (with coherency manager)
Memory
Address
Data
....
100 00 10
108 00 08
110 00 10
118 00 18
120 00 20
128 00 28
130 00 30
... ...