

CMOS 7RF (CMRF7SF) 1.8 V (12-Track) Standard Cell Databook Foundry IP



© Copyright International Business Machines Corporation 2010

Printed in the United States of America February 2010

IBM, the IBM logo, and ibm.com are trademarks or registered trademarks of International Business Machines Corp., registered in many jurisdictions worldwide. Other product and service names might be trademarks of IBM or other companies. A current list of IBM trademarks is available on the Web at "Copyright and trademark information" at www.ibm.com/legal/copytrade.shtml.

All information contained in this document is subject to change without notice. The products described in this document are NOT intended for use in applications such as implantation, life support, or other hazardous uses where malfunction could result in death, bodily injury, or catastrophic property damage. The information contained in this document does not affect or change IBM product specifications or warranties. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of IBM or third parties. All information contained in this document was obtained in specific environments, and is presented as an illustration. The results obtained in other operating environments may vary.

While the information contained herein is believed to be accurate, such information is preliminary, and should not be relied upon for accuracy or completeness, and no representations or warranties of accuracy or completeness are made.

Note: This document contains information on products in the design, sampling and/or initial production phases of development. This information is subject to change without notice. Verify with your IBM field applications engineer that you have the latest version of this document before finalizing a design.

THE INFORMATION CONTAINED IN THIS DOCUMENT IS PROVIDED ON AN "AS IS" BASIS. In no event will IBM be liable for damages arising directly or indirectly from any use of the information contained in this document.

IBM Systems and Technology Group 2070 Route 52, Bldg. 330 Hopewell Junction, NY 12533-6351

The IBM home page can be found at **ibm.com**®. The IBM semiconductor solutions home page can be found at **ibm.com**/chips.

CMRF7SF1.8V12_title.fm February 22, 2010—IBM Confidential



Contents

List of Figures	11
List of Tables	13
Revision Log	19
1. Overview	21
1.1 Technology Features	21
1.2 Cell Naming Conventions	21
1.3 Pin Naming Conventions	22
1.4 Using Logic Symbols	23
1.5 Performance Levels	23
1.6 Truth Tables	24
1.7 Propagation Delay Tables	25
1.8 Setup and Hold Delays	26
1.9 Physical Design Cells	26
1.10 Optional Output Pins	26
1.11 Unused Input Pins	27
1.12 CMOS 7RF 1.8 V (12-Track) Cells and Functions	27
	~4
2. Standard Cell Primitive Logic	
2.1 AND2_{PL} Cell	
2.1.2 Description	
2.1.3 Propagation Delay Table	
2.1.4 Cell Specifications	
2.2 AND3 {PL} Cell	
2.2.1 Function	
2.2.2 Description	34
2.2.3 Propagation Delay Table	. 34
2.2.4 Cell Specifications	36
2.3 AND4_{PL} Cell	37
2.3.1 Function	
2.3.2 Description	
2.3.3 Propagation Delay Table	
2.3.4 Cell Specifications	
2.4 INVERT_{PL} Cell	
2.4.1 Function	
2.4.2 Description	
2.4.3 Propagation Delay Table	
2.4.4 Cell Specifications	
2.5.1 Function	
2.5.2 Description	
2.5.3 Propagation Delay Table	44
2.5.4 Cell Specifications	44



Α	М	1	9	n	^	0
_	ч	v	а		·	c

2.6 NAND2_{PL} Cell	
2.6.1 Function	
2.6.2 Description	
2.6.3 Propagation Delay Table	
2.6.4 Cell Specifications	48
2.7 NAND2BAL_{PL} Cell	49
2.7.1 Function	49
2.7.2 Description	49
2.7.3 Propagation Delay Table	49
2.7.4 Cell Specifications	50
2.8 NAND3_{PL} Cell	51
2.8.1 Function	51
2.8.2 Description	51
2.8.3 Propagation Delay Table	51
2.8.4 Cell Specifications	53
2.9 NAND4_{PL} Cell	55
2.9.1 Function	
2.9.2 Description	55
2.9.3 Propagation Delay Table	
2.9.4 Cell Specifications	
2.10 NOR2_{PL} Cell	
2.10.1 Function	
2.10.2 Description	
2.10.3 Propagation Delay Table	
2.10.4 Cell Specifications	
2.11 NOR3_{PL} Cell	
2.11.1 Function	
2.11.2 Description	
2.11.3 Propagation Delay Table	
2.11.4 Cell Specifications	
2.12 NOR4_{PL} Cell	
2.12.1 Function	
2.12.2 Description	
2.12.3 Propagation Delay Table	
2.12.4 Cell Specifications	
2.13 OR2 {PL} Cell	
2.13.1 Function	
2.13.2 Description	
2.13.3 Propagation Delay Table	
2.13.4 Cell Specifications	
2.14 OR3 {PL} Cell	
2.14.1 Function	
2.14.2 Description	
2.14.3 Propagation Delay Table	
2.14.4 Cell Specifications	
2.15 OR4 {PL} Cell	
2.15.1 Function	
2.15.1 Function	
2.15.3 Propagation Delay Table	
2.15.4 Cell Specifications	
2.10.7 Ooli Opeoliidations	, 5

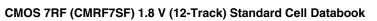


	2.16 XOR2_{PL} Cell	77
	2.16.1 Function	77
	2.16.2 Description	77
	2.16.3 Propagation Delay Table	
	2.16.4 Cell Specifications	79
	2.17 XOR3 {PL} Cell	81
	2.17.1 Function	
	2.17.2 Description	81
	2.17.3 Propagation Delay Table	
	2.17.4 Cell Specifications	
	2.18 XNOR2_{PL} Cell	85
	2.18.1 Function	
	2.18.2 Description	85
	2.18.3 Propagation Delay Table	
	2.18.4 Cell Specifications	
	2.19 XNOR3_{PL} Cell	
	2.19.1 Function	
	2.19.2 Description	
	2.19.3 Propagation Delay Table	
	2.19.4 Cell Specifications	92
3.	Standard Cell Complex Logic	93
	3.1 AO21 {PL} Cell	
	3.1.1 Function	
	3.1.2 Description	93
	3.1.3 Propagation Delay Table	93
	3.1.4 Cell Specifications	95
	3.2 AO22_{PL} Cell	97
	3.2.1 Function	
	3.2.2 Description	97
	3.2.3 Propagation Delay Table	97
	3.2.4 Cell Specifications	99
	3.3 AO33 {PL} Cell	101
	3.3.1 Function	101
	3.3.2 Description	101
	3.3.3 Propagation Delay Table	101
	3.3.3 Propagation Delay Table	-
		103
	3.3.4 Cell Specifications	103 104
	3.3.4 Cell Specifications	103 104 104
	3.3.4 Cell Specifications 3.4 AO44_{PL} Cell 3.4.1 Function	103 104 104 104
	3.3.4 Cell Specifications 3.4 AO44_{PL} Cell 3.4.1 Function 3.4.2 Description	103 104 104 104 104
	3.3.4 Cell Specifications 3.4 AO44_{PL} Cell 3.4.1 Function 3.4.2 Description 3.4.3 Propagation Delay Table 3.4.4 Cell Specifications	103 104 104 104 104 106
	3.3.4 Cell Specifications 3.4 AO44_{PL} Cell 3.4.1 Function 3.4.2 Description 3.4.3 Propagation Delay Table	103 104 104 104 104 106
	3.3.4 Cell Specifications 3.4 AO44_{PL} Cell 3.4.1 Function 3.4.2 Description 3.4.3 Propagation Delay Table 3.4.4 Cell Specifications 3.5 AO222_{PL} Cell	103 104 104 104 106 107
	3.3.4 Cell Specifications 3.4 AO44_{PL} Cell 3.4.1 Function 3.4.2 Description 3.4.3 Propagation Delay Table 3.4.4 Cell Specifications 3.5 AO222_{PL} Cell 3.5.1 Function	103 104 104 104 106 107 107



	_	١.			_	_
Α	а	V	а	n	С	E

3	.6 AO2222_{PL} Cell	111
	3.6.1 Function	
	3.6.2 Description	111
	3.6.3 Propagation Delay Table	111
	3.6.4 Cell Specifications	114
3	.7 AOI21_{PL} Cell	116
	3.7.1 Function	
	3.7.2 Description	116
	3.7.3 Propagation Delay Table	
	3.7.4 Cell Specifications	118
3	.8 AOI22_{PL} Cell	119
	3.8.1 Function	
	3.8.2 Description	
	3.8.3 Propagation Delay Table	
	3.8.4 Cell Specifications	
3	.9 AOI33_{PL} Cell	122
	3.9.1 Function	
	3.9.2 Description	
	3.9.3 Propagation Delay Table	
	3.9.4 Cell Specifications	
3	.10 AOI44 {PL} Cell	
Ū	3.10.1 Function	
	3.10.2 Description	
	3.10.3 Propagation Delay Table	
	3.10.4 Cell Specifications	
3	.11 AOI222 {PL} Cell	128
	3.11.1 Function	
	3.11.2 Description	128
	3.11.3 Propagation Delay Table	128
	3.11.4 Cell Specifications	130
3	.12 AOI2222_{PL} Cell	131
	3.12.1 Function	
	3.12.2 Description	131
	3.12.3 Propagation Delay Table	
	3.12.4 Cell Specifications	133
3	.13 OA21_{PL} Cell	134
	3.13.1 Function	134
	3.13.2 Description	134
	3.13.3 Propagation Delay Table	134
	3.13.4 Cell Specifications	136
3	.14 OA22_{PL} Cell	137
	3.14.1 Function	137
	3.14.2 Description	137
	3.14.3 Propagation Delay Table	137
	3.14.4 Cell Specifications	139
3	.15 OA222_{PL} Cell	141
	3.15.1 Function	
	3.15.2 Description	141
	3.15.3 Propagation Delay Table	141
	3.15.4 Cell Specifications	143





	3.16 OA2222_{PL} Cell	145
	3.16.1 Function	145
	3.16.2 Description	145
	3.16.3 Propagation Delay Table	146
	3.16.4 Cell Specifications	148
	3.17 OAI21_{PL} Cell	
	3.17.1 Function	
	3.17.2 Description	150
	3.17.3 Propagation Delay Table	
	3.17.4 Cell Specifications	
	3.18 OAI22_{PL} Cell	153
	3.18.1 Function	153
	3.18.2 Description	153
	3.18.3 Propagation Delay Table	153
	3.18.4 Cell Specifications	155
	3.19 OAI222_{PL} Cell	156
	3.19.1 Function	156
	3.19.2 Description	156
	3.19.3 Propagation Delay Table	156
	3.19.4 Cell Specifications	157
	3.20 OAI2222_{PL} Cell	158
	3.20.1 Function	158
	3.20.2 Description	158
	3.20.3 Propagation Delay Table	158
	3.20.4 Cell Specifications	159
л		
4.	Standard Cell Unique Logic	
4.	4.1 ADDF_{PL} Cell	161
4.	4.1 ADDF_{PL} Cell	161 161
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description	161 161 161
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table	161 161 161 161
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table	161 161 161 161 162
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table 4.1.5 Cell Specifications	161 161 161 161 162 165
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table 4.1.5 Cell Specifications 4.2 BUFFER_{PL} Cell	161 161 161 161 162 165 166
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table 4.1.5 Cell Specifications 4.2 BUFFER_{PL} Cell 4.2.1 Function	161 161 161 161 162 165 166
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table 4.1.5 Cell Specifications 4.2 BUFFER_{PL} Cell 4.2.1 Function 4.2.2 Description	161 161 161 162 165 166 166
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table 4.1.5 Cell Specifications 4.2 BUFFER_{PL} Cell 4.2.1 Function 4.2.2 Description 4.2.3 Propagation Delay Table	161 161 161 162 165 166 166 166
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table 4.1.5 Cell Specifications 4.2 BUFFER_{PL} Cell 4.2.1 Function 4.2.2 Description 4.2.3 Propagation Delay Table 4.2.4 Cell Specifications	161 161 161 162 165 166 166 166 167
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table 4.1.5 Cell Specifications 4.2 BUFFER_{PL} Cell 4.2.1 Function 4.2.2 Description 4.2.3 Propagation Delay Table 4.2.4 Cell Specifications 4.3 CLK_{PL} Cell	161 161 161 162 165 166 166 166 167
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table 4.1.5 Cell Specifications 4.2 BUFFER_{PL} Cell 4.2.1 Function 4.2.2 Description 4.2.3 Propagation Delay Table 4.2.4 Cell Specifications 4.3 CLK_{PL} Cell 4.3.1 Function	161 161 161 162 165 166 166 166 167 168
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table 4.1.5 Cell Specifications 4.2 BUFFER_{PL} Cell 4.2.1 Function 4.2.2 Description 4.2.3 Propagation Delay Table 4.2.4 Cell Specifications 4.3 CLK_{PL} Cell 4.3.1 Function 4.3.2 Description	161 161 161 162 165 166 166 166 168 168
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table 4.1.5 Cell Specifications 4.2 BUFFER_{PL} Cell 4.2.1 Function 4.2.2 Description 4.2.3 Propagation Delay Table 4.2.4 Cell Specifications 4.3 CLK_{PL} Cell 4.3.1 Function 4.3.2 Description 4.3.3 Truth Table	161 161 161 162 165 166 166 166 168 168 168 168
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table 4.1.5 Cell Specifications 4.2 BUFFER_{PL} Cell 4.2.1 Function 4.2.2 Description 4.2.3 Propagation Delay Table 4.2.4 Cell Specifications 4.3 CLK_{PL} Cell 4.3.1 Function 4.3.2 Description 4.3.2 Description 4.3.3 Truth Table 4.3.4 Propagation Delay Table	161 161 161 162 165 166 166 166 168 168 168 168
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table 4.1.5 Cell Specifications 4.2 BUFFER_{PL} Cell 4.2.1 Function 4.2.2 Description 4.2.3 Propagation Delay Table 4.2.4 Cell Specifications 4.3 CLK_{PL} Cell 4.3.1 Function 4.3.2 Description 4.3.2 Description 4.3.3 Truth Table 4.3.4 Propagation Delay Table 4.3.5 Cell Specifications	161 161 161 162 165 166 166 167 168 168 168 168
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table 4.1.5 Cell Specifications 4.2 BUFFER_{PL} Cell 4.2.1 Function 4.2.2 Description 4.2.3 Propagation Delay Table 4.2.4 Cell Specifications 4.3 CLK_{PL} Cell 4.3.1 Function 4.3.2 Description 4.3.2 Description 4.3.3 Truth Table 4.3.4 Propagation Delay Table 4.3.5 Cell Specifications 4.4 CLKI_{PL} Cell	161 161 161 162 165 166 166 167 168 168 168 168 169 170
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table 4.1.5 Cell Specifications 4.2 BUFFER_{PL} Cell 4.2.1 Function 4.2.2 Description 4.2.3 Propagation Delay Table 4.2.4 Cell Specifications 4.3 CLK_{PL} Cell 4.3.1 Function 4.3.2 Description 4.3.3 Truth Table 4.3.4 Propagation Delay Table 4.3.5 Cell Specifications 4.4 CLKI_{PL} Cell 4.5 Cell Specifications	161 161 161 162 165 166 166 167 168 168 168 168 169 170
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table 4.1.5 Cell Specifications 4.2 BUFFER_{PL} Cell 4.2.1 Function 4.2.2 Description 4.2.3 Propagation Delay Table 4.2.4 Cell Specifications 4.3 CLK_{PL} Cell 4.3.1 Function 4.3.2 Description 4.3.3 Truth Table 4.3.4 Propagation Delay Table 4.3.5 Cell Specifications 4.4 CLKI_{PL} Cell 4.4.1 Function 4.3.5 Description 4.4.1 Function 4.4.1 Function 4.4.2 Description	161 161 161 162 165 166 166 167 168 168 168 169 170 170
4.	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table 4.1.5 Cell Specifications 4.2 BUFFER_{PL} Cell 4.2.1 Function 4.2.2 Description 4.2.3 Propagation Delay Table 4.2.4 Cell Specifications 4.3 CLK_{PL} Cell 4.3.1 Function 4.3.2 Description 4.3.2 Description 4.3.3 Truth Table 4.3.4 Propagation Delay Table 4.3.5 Cell Specifications 4.4 CLKL_{PL} Cell 4.1 Function 4.2 Description 4.3 Truth Table 4.4 Teunction 4.4 Description 4.4 Teunction 4.4 Description 4.4 Truth Table	161 161 161 162 165 166 166 167 168 168 168 169 170 170 170
*-	4.1 ADDF_{PL} Cell 4.1.1 Function 4.1.2 Description 4.1.3 Truth Table 4.1.4 Propagation Delay Table 4.1.5 Cell Specifications 4.2 BUFFER_{PL} Cell 4.2.1 Function 4.2.2 Description 4.2.3 Propagation Delay Table 4.2.4 Cell Specifications 4.3 CLK_{PL} Cell 4.3.1 Function 4.3.2 Description 4.3.3 Truth Table 4.3.4 Propagation Delay Table 4.3.5 Cell Specifications 4.4 CLKI_{PL} Cell 4.4.1 Function 4.3.5 Description 4.4.1 Function 4.4.1 Function 4.4.2 Description	161 161 161 162 165 166 166 167 168 168 168 169 170 170 170



Α	Ы	v	2	n	^	_

	4.5 COMP2_{PL} Cell	172
	4.5.1 Function	172
	4.5.2 Description	172
	4.5.3 Truth Table	172
	4.5.4 Propagation Delay Table	173
	4.5.5 Cell Specifications	175
	4.6 DELAY4_{PL} Cell	177
	4.6.1 Function	
	4.6.2 Description	177
	4.6.3 Propagation Delay Table	177
	4.6.4 Cell Specifications	177
	4.7 DELAY6_{PL} Cell	179
	4.7.1 Function	
	4.7.2 Description	179
	4.7.3 Propagation Delay Table	179
	4.7.4 Cell Specifications	180
	4.8 MUX21_{PL} Cell	181
	4.8.1 Function	181
	4.8.2 Description	181
	4.8.3 Truth Table	181
	4.8.4 Propagation Delay Table	
	4.8.5 Cell Specifications	183
	4.9 MUX21BAL_{PL} Cell	184
	4.9.1 Function	
	4.9.2 Description	
	4.9.3 Truth Table	
	4.9.4 Propagation Delay Table	
	4.9.5 Cell Specifications	
	4.10 MUX21I_{PL} Cell	
	4.10.1 Function	
	4.10.2 Description	
	4.10.3 Truth Table	
	4.10.4 Propagation Delay Table	
	4.10.5 Cell Specifications	
	4.11 MUX41_{PL} Cell	
	4.11.1 Function	
	4.11.2 Description	
	4.11.3 Truth Table	
	4.11.4 Propagation Delay Table	
	4.11.5 Cell Specifications	
	4.12 TERM_{PL} Cell	
	4.12.1 Function	
	4.12.2 Description	
	4.12.3 Cell Specifications	195
5.	Standard Cell Sequential Logic	
	5.1 DFF_{PL} Cell	
	5.1.1 Function	
	5.1.2 Description	197



5.1.3 DFF Truth Table	. 19	7
5.1.4 Delay Tables	. 19	17
5.1.5 Cell Specifications	19	8
5.2 DFFR_{PL} Cell	. 19	9
5.2.1 Function	. 19	19
5.2.2 Description	. 19	19
5.2.3 DFF Truth Table	. 19	9
5.2.4 Delay Tables	20	Ю
5.2.5 Cell Specifications	20	11
5.3 DFFS_{PL} Cell	20)2
5.3.1 Function		
5.3.2 Description	20	2
5.3.3 DFF Truth Table	20	2
5.3.4 Delay Tables	20	3
5.3.5 Cell Specifications		
5.4 DFFSR_{PL} Cell	20)5
5.4.1 Function		
5.4.2 Description	20	15
5.4.3 DFF Truth Table	20	15
5.4.4 Delay Tables	20	16
5.4.5 Cell Specifications	20	17
5.5 LATSR_{PL} Cell	20	8
5.5.1 Function	20	8
5.5.2 Description	20	8
5.5.3 DFF Truth Table	20	18
5.5.4 Delay Tables	20	19
5.5.5 Cell Specifications	21	0
5.6 SDFF_{PL} Cell	21	1
5.6.1 Function	. 21	1
5.6.2 Description	21	1
5.6.3 DFF Truth Table	. 21	1
5.6.4 Delay Tables	. 21	2
5.6.5 Cell Specifications	21	2
5.7 SDFFR_{PL} Cell	21	4
5.7.1 Function	. 21	4
5.7.2 Description	. 21	4
5.7.3 DFF Truth Table	. 21	4
5.7.4 Delay Tables	21	5
5.7.5 Cell Specifications	. 21	6
5.8 SDFFS_{PL} Cell	21	7
5.8.1 Function		
5.8.2 Description		
5.8.3 DFF Truth Table		
5.8.4 Delay Tables		
5.8.5 Cell Specifications	21	



CMOS 7RF (CMRF7SF) 1.8 V (12-Track) Standard Cell Databook

	5.9 SDFFSR_{PL} Cell	220
	5.9.1 Function	220
	5.9.2 Description	220
	5.9.3 DFF Truth Table	220
	5.9.4 Delay Tables	221
	5.9.5 Cell Specifications	222
	5.10 SLATSR_{PL} Cell	223
	5.10.1 Function	
	5.10.2 Description	223
	5.10.3 DFF Truth Table	223
	5.10.4 Delay Tables	224
	5.10.5 Cell Specifications	226
ô.	. Physical Design Cells	229
	6.1 DECAP_{PL} Cell	
	6.1.1 Function	
	6.1.2 Description	229
	6.1.3 Truth Table	229
	6.2 FILL{1,2} Cell	230
	6.2.1 Function	
	6.2.2 Description	230
	6.2.3 Cell Specifications	
	6.3 FGTIE_{PL} Cell	231
	6.3.1 Function	
	6.3.2 Description	231
	6.3.3 Cell Specifications	231
	6.4 GAUNUSEDxxx Cell	
	6.4.1 Function	
	6.4.2 Description	
	6.4.3 Cell Specifications	232



List of Figures

	•	
Figure 1-1.	Cell Naming Convention Example	22
Figure 1-2.	Cell AND2_{PL} Symbols	23
Figure 2-1.	Cell AND2_{PL} Symbols	31
Figure 2-2.	Cell AND3_{PL} Symbols	34
Figure 2-3.	Cell AND4_{PL} Symbols	37
Figure 2-4.	Cell INVERT_{PL} Symbols	41
Figure 2-5.	Cell INVERTBAL_{PL} Symbols	44
Figure 2-6.	Cell NAND2_{PL} Symbols	46
Figure 2-7.	Cell NAND2BAL_{PL} Symbols	49
Figure 2-8.	Cell NAND3_{PL} Symbols	51
Figure 2-9.	Cell NAND4_{PL} Symbols	55
Figure 2-10.	Cell NOR2_{PL} Symbols	58
Figure 2-11.	Cell NOR3_{PL} Symbols	61
Figure 2-12.	Cell NOR4_{PL} Symbols	64
Figure 2-13.	Cell OR2_{PL} Symbols	67
Figure 2-14.	Cell OR3_{PL} Symbols	70
Figure 2-15.	Cell OR4_{PL} Symbols	73
Figure 2-16.	Cell XOR2_{PL} Symbols	77
Figure 2-17.	Cell XOR3_{PL} Symbols	81
Figure 2-18.	Cell XNOR2_{PL} Symbols	85
Figure 2-19.	Cell XNOR3_{PL} Symbols	89
Figure 3-1.	Cell AO21_{PL} Symbols	93
Figure 3-2.	Cell AO22_{PL} Symbols	97
Figure 3-3.	Cell AO33_{PL} Symbols	101
Figure 3-4.	Cell AO44_{PL} Symbols	104
Figure 3-5.	Cell AO222_{PL} Symbols	107
Figure 3-6.	Cell AO2222_{PL} Symbols	111
Figure 3-7.	Cell AOI21_{PL} Symbols	116
Figure 3-8.	Cell AOI22_{PL} Symbols	119
Figure 3-9.	Cell AOI33_{PL} Symbols	122
Figure 3-10.	Cell AOI44_{PL} Symbols	125
Figure 3-11.	Cell AOI222_{PL} Symbols	128
Figure 3-12.	Cell AOI2222_{PL} Symbols	131
Figure 3-13.	Cell OA21_{PL} Symbols	134
Figure 3-14.	Cell OA22_{PL} Symbols	137
Figure 3-15.	Cell OA222_{PL} Symbols	141
Figure 3-16.	Cell OA2222_{PL} Symbols	145
Figure 3-17.	Cell OAI21 {PL} Symbols	150

Foundry IP



CIVIOS / RF (C	SMRF/SF) 1.6 V (12-1 rack) Standard Cell Databook	Advanc
Figure 3-18.	Cell OAl22_{PL} Symbols	153
Figure 3-19.	Cell OAI222_{PL} Symbols	156
Figure 3-20.	Cell OAI2222_{PL} Symbols	158
Figure 4-1.	Cell ADDF_{PL} Symbols	161
Figure 4-2.	Cell BUFFER_{PL} Symbols	166
Figure 4-3.	Cell CLK_{PL} Symbols	168
Figure 4-4.	Cell CLKI_{PL} Symbols	170
Figure 4-5.	Cell COMP2_{PL} Symbols	172
Figure 4-6.	Cell DELAY4_{PL} Symbols	177
Figure 4-7.	Cell DELAY6_{PL} Symbols	179
Figure 4-8.	Cell MUX21_{PL} Symbols	181
Figure 4-9.	Cell MUX21BAL_{PL} Symbols	184
Figure 4-10.	Cell MUX21I_{PL} Symbols	187
Figure 4-11.	Cell MUX41_{PL} Symbols	191
Figure 4-12.	Cell TERM_{PL} Symbols	195
Figure 5-1.	Cell DFF_{PL} Symbols	197
Figure 5-2.	Cell DFFR_{PL} Symbols	199
Figure 5-3.	Cell DFFS_{PL} Symbols	202
Figure 5-4.	Cell DFFSR_{PL} Symbols	205
Figure 5-5.	Cell LATSR_{PL} Symbols	208
Figure 5-6.	Cell SDFF_{PL} Symbols	211
Figure 5-7.	Cell SDFFR_{PL} Symbols	214
Figure 5-8.	Cell SDFFS_{PL} Symbols	217
Figure 5-9.	Cell SDFFSR_{PL} Symbols	220
Figure 5-10.	Cell SLATSR_{PL} Symbols	223
Figure 6-1.	Cell DECAP_{PL} Symbols	229
Figure 6-2	Call FGTIF JPI \ Symbols	231



List of Tables

Table 1-1.	General Characteristics	21
Table 1-2.	I/O Pin Naming Conventions	22
Table 1-3.	Nominal Load Capacitance by Performance Level	23
Table 1-4.	Cell DFF_{PL} Truth Table Example	24
Table 1-5.	Truth Table Legend	24
Table 1-6.	Input Transition Times	25
Table 1-7.	Propagation Delay Table Terminology	25
Table 1-8.	Cell Propagation Delays	25
Table 1-9.	Cell DFF_{PL} Latch Setup and Hold Delays	26
Table 1-10.	CMOS 7RF Library Cells with "Optional" Outputs	26
Table 1-11.	CMOS 7RF 1.8 V (12-Track) Cell Functions	27
Table 2-1.	Cell AND2_{PL} Propagation Delays	31
Table 2-2.	Cell AND2_{PL} Capacitance	32
Table 2-3.	Cell AND2_{PL} Area	33
Table 2-4.	Cell AND3_{PL} Propagation Delays	34
Table 2-5.	Cell AND3_{PL} Capacitance	36
Table 2-6.	Cell AND3_{PL} Area	36
Table 2-7.	Cell AND4_{PL} Propagation Delays	37
Table 2-8.	Cell AND4_{PL} Capacitance	39
Table 2-9.	Cell AND4_{PL} Area	40
Table 2-10.	Cell INVERT_{PL} Propagation Delays	41
Table 2-11.	Cell INVERT_{PL} Capacitance	42
Table 2-12.	Cell INVERT_{PL} Area	43
Table 2-13.	Cell INVERTBAL_{PL} Propagation Delays	44
Table 2-14.	Cell INVERTBAL_{PL} Capacitance	44
Table 2-15.	Cell INVERTBAL_{PL} Area	45
Table 2-16.	Cell NAND2_{PL} Propagation Delays	46
Table 2-17.	Cell NAND2_{PL} Capacitance	48
Table 2-18.	Cell NAND2_{PL} Area	48
Table 2-19.	Cell NAND2BAL_{PL} Propagation Delays	49
Table 2-20.	Cell NAND2BAL_{PL} Capacitance	50
Table 2-21.	Cell NAND2BAL_{PL} Area	50
Table 2-22.	Cell NAND3_{PL} Propagation Delays	51
Table 2-23.	Cell NAND3_{PL} Capacitance	53
Table 2-24.	Cell NAND3_{PL} Area	54
Table 2-25.	Cell NAND4_{PL} Propagation Delays	55
Table 2-26.	Cell NAND4_{PL} Capacitance	57
Table 2-27.	Cell NAND4_{PL} Area	57



CMOS 7RF (CMRF7SF) 1.8 V (12-Track) Standard Cell Databook Advance Cell NOR2_{PL} Propagation Delays58 Table 2-28. Table 2-29. Table 2-30. Table 2-31. Cell NOR3 {PL} Propagation Delays61 Table 2-32. Cell NOR3 {PL} Capacitance62 Cell NOR3 _{PL} Area63 Table 2-33. Table 2-34. Cell NOR4 {PL} Propagation Delays64 Table 2-35. Cell NOR4 {PL} Capacitance65 Table 2-36. Table 2-37. Cell OR2 {PL} Propagation Delays67 Table 2-38. Cell OR2_{PL} Capacitance68 Table 2-39. Table 2-40. Cell OR3_{PL} Propagation Delays70 Table 2-41. Table 2-42. Table 2-43. Cell OR4 {PL} Propagation Delays73 Table 2-44. Table 2-45. Table 2-46. Cell XOR2 {PL} Propagation Delays77 Table 2-47. Cell XOR2 {PL} Capacitance79 Table 2-48. Cell XOR2 {PL} Area80 Table 2-49. Cell XOR3 {PL} Propagation Delays81 Table 2-50. Cell XOR3 {PL} Capacitance84 Table 2-51. Cell XOR3_{PL} Area84 Table 2-52. Cell XNOR2 {PL} Propagation Delays85 Table 2-53. Cell XNOR2 {PL} Capacitance87 Table 2-54. Table 2-55. Cell XNOR3 {PL} Propagation Delays89 Table 2-56. Cell XNOR3 {PL} Capacitance92 Table 2-57. Cell XNOR3_{PL} Area92 Table 3-1. Cell AO21 {PL} Propagation Delays93 Table 3-2. Cell AO21 {PL} Capacitance95 Table 3-3. Cell AO21_{PL} Area96 Table 3-4. Cell AO22_{PL} Propagation Delays97 Table 3-5. Cell AO22_{PL} Capacitance99 Table 3-6. Table 3-7. Cell AO33 {PL} Propagation Delays101 Table 3-8. Table 3-9.



Table 3-10.	Cell AO44_{PL} Propagation Delays	104
Table 3-11.	Cell AO44_{PL} Capacitance	106
Table 3-12.	Cell AO44_{PL} Area	106
Table 3-13.	Cell AO222_{PL} Propagation Delays	107
Table 3-14.	Cell AO222_{PL} Capacitance	110
Table 3-15.	Cell AO222_{PL} Area	110
Table 3-16.	Cell AO2222_{PL} Propagation Delays	111
Table 3-17.	Cell AO2222_{PL} Capacitance	114
Table 3-18.	Cell AO2222_{PL} Area	115
Table 3-19.	Cell AOI21_{PL} Propagation Delays	116
Table 3-20.	Cell AOI21_{PL} Capacitance	118
Table 3-21.	Cell AOI21_{PL} Area	118
Table 3-22.	Cell AOI22_{PL} Propagation Delays	119
Table 3-23.	Cell AOI22_{PL} Capacitance	121
Table 3-24.	Cell AOI22_{PL} Area	121
Table 3-25.	Cell AOI33_{PL} Propagation Delays	122
Table 3-26.	Cell AOI33_{PL} Capacitance	124
Table 3-27.	Cell AOI33_{PL} Area	124
Table 3-28.	Cell AOI44_{PL} Propagation Delays	125
Table 3-29.	Cell AOI44_{PL} Capacitance	127
Table 3-30.	Cell AOI44_{PL} Area	127
Table 3-31.	Cell AOI222_{PL} Propagation Delays	128
Table 3-32.	Cell AOI222_{PL} Capacitance	130
Table 3-33.	Cell AOI222_{PL} Area	130
Table 3-34.	Cell AOI2222_{PL} Propagation Delays	131
Table 3-35.	Cell AOI2222_{PL} Capacitance	133
Table 3-36.	Cell AOI2222_{PL} Area	133
Table 3-37.	Cell OA21_{PL} Propagation Delays	134
Table 3-38.	Cell OA21_{PL} Capacitance	136
Table 3-39.	Cell OA21_{PL} Area	136
Table 3-40.	Cell OA22_{PL} Propagation Delays	137
Table 3-41.	Cell OA22_{PL} Capacitance	139
Table 3-42.	Cell OA22_{PL} Area	140
Table 3-43.	Cell OA222_{PL} Propagation Delays	141
Table 3-44.	Cell OA222_{PL} Capacitance	143
Table 3-45.	Cell OA222_{PL} Area	144
Table 3-46.	Cell OA2222_{PL} Propagation Delays	146
Table 3-47.	Cell OA2222_{PL} Capacitance	148
Table 3-48.	Cell OA2222_{PL} Area	149



CMOS 7RF (CMRF7SF) 1.8 V (12-Track) Standard Cell Databook		Advance
Table 3-49.	Cell OAI21_{PL} Propagation Delays	150
Table 3-50.	Cell OAI21_{PL} Capacitance	152
Table 3-51.	Cell OAI21_{PL} Area	152
Table 3-52.	Cell OAI22_{PL} Propagation Delays	153
Table 3-53.	Cell OAI22_{PL} Capacitance	155
Table 3-54.	Cell OAI22_{PL} Area	155
Table 3-55.	Cell OAI222_{PL} Propagation Delays	156
Table 3-56.	Cell OAI222_{PL} Capacitance	157
Table 3-57.	Cell OAI222_{PL} Area	157
Table 3-58.	Cell OAI2222_{PL} Propagation Delays	158
Table 3-59.	Cell OAI2222_{PL} Capacitance	159
Table 3-60.	Cell OAI2222_{PL} Area	160
Table 4-1.	Cell ADDF_{PL} Truth Table	161
Table 4-2.	Cell ADDF_{PL} Propagation Delays	162
Table 4-3.	Cell ADDF_{PL} Capacitance	165
Table 4-4.	Cell ADDF_{PL} Area	165
Table 4-5.	Cell BUFFER_{PL} Propagation Delays	166
Table 4-6.	Cell BUFFER_{PL} Capacitance	167
Table 4-7.	Cell BUFFER_{PL} Area	167
Table 4-8.	Cell CLK_{PL} Truth Table	168
Table 4-9.	Cell CLK_{PL} Propagation Delays	168
Table 4-10.	Cell CLK_{PL} Capacitance	169
Table 4-11.	Cell CLK_{PL} Area	169
Table 4-12.	Cell CLKI_{PL} Truth Table	170
Table 4-13.	Cell CLKI_{PL} Propagation Delays	170
Table 4-14.	Cell CLKI_{PL} Capacitance	171
Table 4-15.	Cell CLKI_{PL} Area	171
Table 4-16.	Cell COMP2_{PL} Truth Table	172
Table 4-17.	Cell COMP2_{PL} Propagation Delays	173
Table 4-18.	Cell COMP2_{PL} Capacitance	175
Table 4-19.	Cell COMP2_{PL} Area	176
Table 4-20.	Cell DELAY4_{PL} Propagation Delays	177
Table 4-21.	Cell DELAY4_{PL} Capacitance	177
Table 4-22.	Cell DELAY4_{PL} Area	178
Table 4-23.	Cell DELAY6_{PL} Propagation Delays	179
Table 4-24.	Cell DELAY6_{PL} Capacitance	180
Table 4-25.	Cell DELAY6_{PL} Area	180
Table 4-26.	Cell MUX21_{PL} Truth Table	181
Table 4-27.	Cell MUX21_{PL} Propagation Delays	181



Table 4-28.	Cell MUX21_{PL} Capacitance	183
Table 4-29.	Cell MUX21_{PL} Area	183
Table 4-30.	Cell MUX21BAL_{PL} Truth Table	184
Table 4-31.	Cell MUX21BAL_{PL} Propagation Delays	185
Table 4-32.	Cell MUX21BAL_{PL} Capacitance	185
Table 4-33.	Cell MUX21BAL_{PL} Area	186
Table 4-34.	Cell MUX21I_{PL} Truth Table	187
Table 4-35.	Cell MUX21I_{PL} Propagation Delays	187
Table 4-36.	Cell MUX21I_{PL} Capacitance	189
Table 4-37.	Cell MUX21I_{PL} Area	190
Table 4-38.	Cell MUX41_{PL} Truth Table	191
Table 4-39.	Cell MUX41_{PL} Propagation Delays	192
Table 4-40.	Cell MUX41_{PL} Capacitance	193
Table 4-41.	Cell MUX41_{PL} Area	194
Table 4-42.	Cell TERM_{PL} Capacitance	195
Table 4-43.	Cell TERM_{PL} Area	195
Table 5-1.	Cell DFF_{PL} Truth Table	197
Table 5-2.	Cell DFF_{PL} Propagation Delays	197
Table 5-3.	Cell DFF_{PL} Latch Setup and Hold Delays	198
Table 5-4.	Cell DFF_{PL} Capacitance	198
Table 5-5.	Cell DFF_{PL} Area	198
Table 5-6.	Cell DFFR_{PL} Truth Table	199
Table 5-7.	Cell DFFR_{PL} Propagation Delays	200
Table 5-8.	Cell DFFR_{PL} Latch Setup and Hold Delays	200
Table 5-9.	Cell DFFR_{PL} Capacitance	201
Table 5-10.	Cell DFFR_{PL} Area	201
Table 5-11.	Cell DFFS_{PL} Truth Table	202
Table 5-12.	Cell DFFS_{PL} Propagation Delays	203
Table 5-13.	Cell DFFS_{PL} Latch Setup and Hold Delays	203
Table 5-14.	Cell DFFS_{PL} Capacitance	204
Table 5-15.	Cell DFFS_{PL} Area	204
Table 5-16.	Cell DFFSR_{PL} Truth Table	205
Table 5-17.	Cell DFFSR_{PL} Propagation Delays	206
Table 5-18.	Cell DFFSR_{PL} Latch Setup and Hold Delays	207
Table 5-19.	Cell DFFSR_{PL} Capacitance	
Table 5-20.	Cell DFFSR_{PL} Area	
Table 5-21.	Cell LATSR_{PL} Truth Table	208
Table 5-22.	Cell LATSR_{PL} Propagation Delays	
Table 5-23.	Cell LATSR_{PL} Latch Setup and Hold Delays	



CMOS 7RF (CMRF7SF) 1.8 V (12-Track) Standard Cell Databook Table 5-24. Cell LATSR_{PL} Area210 Table 5-25. Table 5-26. Cell SDFF_{PL} Truth Table211 Table 5-27. Cell SDFF {PL} Latch Setup and Hold Delays212 Table 5-28. Table 5-29. Table 5-30. Cell SDFFR {PL} Truth Table214 Table 5-31. Table 5-32. Cell SDFFR_{PL} Propagation Delays215 Table 5-33. Cell SDFFR {PL} Latch Setup and Hold Delays215 Table 5-34. Table 5-35. Table 5-36. Cell SDFFS_{PL} Truth Table217 Table 5-37. Table 5-38. Cell SDFFS_{PL} Latch Setup and Hold Delays218 Table 5-39. Table 5-40. Table 5-41. Table 5-42. Cell SDFFSR {PL} Propagation Delays221 Table 5-43. Cell SDFFSR {PL} Latch Setup and Hold Delays222 Table 5-44. Table 5-45. Table 5-46. Table 5-47. Cell SLATSR_{PL} Propagation Delays224 Table 5-48. Cell SLATSR {PL} Latch Setup and Hold Delays226 Table 5-49. Table 5-50. Table 6-1. Cell DECAP {PL} Truth Table229 Table 6-2. Table 6-3. Table 6-4. Cell FGTIE {PL} Area231 Table 6-5.



Revision Log

Revision Date	Pages	Description
February 22, 2010	_	Initial release (00).





1. Overview

This databook describes the IBM CMOS 7RF digital product family, which consists of standard cell products implemented in a 0.18 μm lithography process. CMOS 7RF uses up to six levels of metal wiring.

This section summarizes the standard cells, including logical and electrical information. The terminology, symbology, and data presented throughout this databook are defined. Five types of cells are presented in the following sections:

- Primitive logic
- Complex logic
- Unique logic
- · Sequential logic
- · Physical design cells

The databook is intended to be used in conjunction with the IBM CMRF7SF Design Kit. Contact your IBM technical representative for more information.

1.1 Technology Features

Table 1-1. General Characteristics

Characteristic	Description
Technology	CMOS 7RF
NFET L _{eff}	$0.145 \pm 0.017~\mu m$
PFET L _{eff}	$0.145 \pm 0.017 \mu m$
Supply voltage	1.8 V ± 10%
Ambient operating temperature range	-55°C to 100°C
Junction temperature range	-40°C to 125°C
Storage temperature range	-65°C to 150°C
Wiring levels	Four to eight for MA last metal Three to seven for AM / ML last metal
Cell length	6.72 μm

1.2 Cell Naming Conventions

There are two main parts to cell names.

- Function: Describes the basic Boolean function for the primitive, complex, unique, and latch cells (see Section 1.12 CMOS 7RF 1.8 V (12-Track) Cells and Functions on page 27).
- Performance level: Designates A through U with an underscore separating the performance level from the library type. In this databook, each cell name includes "{PL}" as a placeholder for the performance level. The delay and capacitance tables for each cell show the different values for each performance level offered for that cell. See Section 1.5 on page 23 for more information on performance cells.

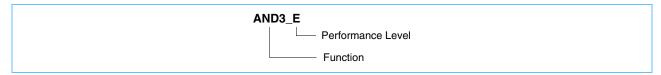


The full cell name is *Function_{Performance Level}*. *Figure 1-1* shows an example.

Cell name AND3_E

Description Three-way AND, performance level E

Figure 1-1. Cell Naming Convention Example



1.3 Pin Naming Conventions

Table 1-2 describes the functions of the cell pins used in the CMOS 7RF 1.8 V standard cells.

Table 1-2. I/O Pin Naming Conventions

A, A1, A2, A3, A4,		
B, B1, B2, B3, B4, C, C1, C2 D, D0, D1, D2, D3 J, K	Data input pins	1
CIN	Carry input pin for ADDF cells	
CLK, C	Clock pin for latches	1
COUT	Carry output pin for ADDF cells	
E	Enable pin for clock gating cells (input)	
GCK	Gated clock pin for clock gating cells (output)	
GND	Ground pin	
Q	Latch output pin	
QBAR	Latch output pin (Q complement)	
QN	Latch output pin (Q complement)	
RN	Asynchronous reset or clear (negative active)	
S	Set pin (input)	
SD, SD1, SD2	Multiplexer selection pin (input)	
SE	Scan enable pin (input)	
SI	Scan input pin	
SN	Asynchronous set of preset (negative active)	
SUM	Output pin for ADDF cells	
VDD	Power pin	
Z	Output pin	

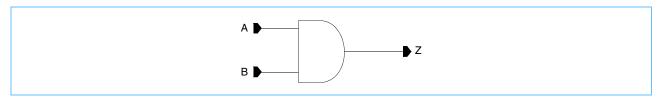
The C pin can be either a data input pin or a clock pin. See the description of the specific cell to verify the function of the C pin.



1.4 Using Logic Symbols

Each cell subsection includes a symbols figure that shows the input and output pins. These symbols correspond to the symbols available in the IBM CMRF7SF Design Kit.

Figure 1-2. Cell AND2_{PL} Symbols



1.5 Performance Levels

Most cells are available in multiple performance levels. The performance levels are identified by A through U. An "A" performance level is used to drive the smallest loads efficiently; a "U" performance level is used to drive the largest loads efficiently. Performance levels can also be used to denote nonoverlap (not drive strength) of clock splitters or delay elements. The delay tables and input pin capacitance tables display the data for each performance level of a given cell. *Table 1-3* can be used as a capacitance estimation for running electrical simulations. For accurate timing analysis, refer to the IBM CMOS 7RF 1.8 V Library (.lib) timing files.

Table 1-3. Nominal Load Capacitance by Performance Level

Performance Level	Capacitance (fF)
A	15
В	17
С	27
D	35
E	43
F	61
Н	74
I	89
J	114
К	130
L	141
M	185
N	221
0	247
Q	458
U	408



1.6 Truth Tables

Table 1-4 shows an example of a truth table for a typical cell. *Table 1-5* shows the symbols used to define several possible logic states in the tables.

Table 1-4. Cell DFF_{PL} Truth Table Example

Inputs		Outputs	
CLK	D	Q	QBAR
(01)	0	х	0
(01)	1	х	1
(1x)	х	х	-
(x0)	х	х	-

Table 1-5. Truth Table Legend

Logic Symbol	Meaning
0	Forcing a logic '0'
1	Forcing a logic '1'
_	No change
x	"Don't care" input state
(01)	Clock rising edge
(1x)	If the clock starts as a 1, the Q+ output does not change
(x0)	If the clock ends as a 0, the Q+ output does not change



1.7 Propagation Delay Tables

Note: The delay and timing information for each cell is provided for estimation purposes only. The delays shown are from the nominal case. Propagation delay timing calculations are representative values at the beginning of the product's life. This timing data can degrade over the product's lifetime.

Propagation delays are presented for each cell as a function of load capacitance. Please see the .lib timing files for details about load capacitance and input transition times.

Table 1-6. Input Transition Times

Cell Types	Transition Times
Latches	200 ps
Primitives, complex, and unique cells	

The delay table is used to estimate delays for a given path. *Table 1-7* defines the terms used in the delay tables and *Table 1-8* is an example of a propagation delay table.

Table 1-7. Propagation Delay Table Terminology

Term	Definition
Parameter	t_{PHH} = Input going high (from 0 to 1) and output going high (from 0 to 1) t_{PHL} = Input going high (from 0 to 1) and output going low (from 1 to 0) t_{PLH} = Input going low (from 1 to 0) and output going high (from 0 to 1) t_{PLL} = Input going low (from 1 to 0) and output going low (from 1 to 0)
Path	Input pin to output pin logic path.
Performance level	A, B, C

Table 1-8. Cell Propagation Delays

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) V _{DD} 1.8 V T _j 25°C
	A-Z	t _{PLH}	0.114
A	A-Z	t _{PHL}	0.120
^	B-Z	t _{PLH}	0.111
		t _{PHL}	0.129
	A-Z	t _{PLH}	0.120
В	A-Z	t _{PHL}	0.120
	B-Z	t _{PLH}	0.111
	D-Z	t _{PHL}	0.129



1.8 Setup and Hold Delays

Table 1-9 shows an example of sequential logic setup and hold delays using the standard cell D flip-flop (DFF). Setup and hold times are calculated using nominal case conditions, with the clock and data slew rate at 200 ps.

Table 1-9. Cell DFF_{PL} Latch Setup and Hold Delays

	Constraint (ps) by	Constraint (ps) by Performance Level			
Data / Clock	Condition ¹	E	Н	К	
D 01 / CL K	Setup	031	035	026	
D 01 / CLK Hold	009	014	002		
D 10 / CLK Hold	182	183	179		
	-149	-147	-151		
1. Setup and	hold are calculated	using nominal case co	nditions (1.8 V, 25°C; clock and o	lata slew rate = 200 ps.)	

1.9 Physical Design Cells

Special cells for physical design are included in the IBM CMRF7SF Design Kit. Use of these cells is specific to the physical design flow and is described in a separate application note for the CMOS 7RF physical design methodology. Contact your IBM technical representative for more information.

Cells available for physical design include:

- N-well/substrate contacts
- Floating-gate diodes (for correcting antenna violations)
- Filler cells
- Decoupling capacitors

Use of floating-gate diodes is optional. If used, they should exist in the schematic netlist for layout versus schematic (LVS) checking. Use of the n-well/substrate contacts and filler cells is governed by a set methodology; these cells are masked during LVS checking.

1.10 Optional Output Pins

The ADFF_{PL} cell has optional output pins. *Table 1-10* lists the optional pin group, affected pins, and the minimum and maximum number of pins that may be used. For example, an instantiation of a full adder can use SUM, COUT, or both SUM and COUT.

Table 1-10. CMOS 7RF Library Cells with "Optional" Outputs

Function	Cell Name	Outputs	(Pin Group): (Minimum number of pins, maximum number of pins)
Full adder	ADDF_{PL}	SUM, COUT	(SUM, COUT): (1,2)



1.11 Unused Input Pins

Input pins that are not used should be tied down. If an unused pin needs to be tied up, an inverter and tie-down cell combination is recommended. Contact your IBM technical representative for more information.

1.12 CMOS 7RF 1.8 V (12-Track) Cells and Functions

Table 1-11 lists the CMOS 7RF 1.8 V (12-track) library cells and their functions.

Table 1-11. CMOS 7RF 1.8 V (12-Track) Cell Functions (Page 1 of 3)

Cell	Function
Standard Cell Primitive Logic	
AND2_{PL}	Two-way AND
AND3_{PL}	Three-way AND
AND4_{PL}	Four-way AND
INVERT_{PL}	Inverter
NAND2_{PL}	Two-way NAND
NAND3_{PL}	Three-way NAND
NAND4_{PL}	Four-way NAND
NOR2_{PL}	Two-way NOR
NOR3_{PL}	Three-way NOR
NOR4_{PL}	Four-way NOR
OR2_{PL}	Two-way OR
OR3_{PL}	Three-way OR
OR4_{PL}	Four-way OR
XNOR2_{PL}	Two-way XNOR
XNOR3_{PL}	Three-way XNOR
XOR2_{PL}	Two-way XOR
XOR3_{PL}	Three-way XOR
Standard Cell Complex Logic	·
AO21_{PL}	2 × 1 AND OR
AO22_{PL}	2 × 2 AND OR
AO33_{PL}	3×3 AND OR
AO44_{PL}	4 × 4 AND OR
AO222_{PL}	2 × 2 × 2 AND OR
AO2222_{PL}	2 × 2 × 2 × 2 AND OR
AOI21_{PL}	2 × 1 AND OR inverter
AOI22_{PL}	2 × 2 AND OR inverter
AOI33_{PL}	3 × 3 AND OR inverter
AOI44_{PL}	4 × 4 AND OR inverter



Table 1-11. CMOS 7RF 1.8 V (12-Track) Cell Functions (Page 2 of 3)

Cell	Function	
AOI222_{PL}	2 × 2 × 2 AND OR inverter	
AOI2222_{PL}	2 × 2 × 2 × 2 AND OR inverter	
OA21_{PL}	2 × 1 OR AND	
OA22_{PL}	2 × 2 OR AND	
OA222_{PL}	2 × 2 × 2 OR AND	
OA2222_{PL}	× 2 × 2 × 2 OR AND	
OAI21_{PL}	2 × 1 OR AND inverter	
OAI22_{PL}	2 × 2 OR AND inverter	
OAI222_{PL}	2 × 2 × 2 OR AND inverter	
OAI2222_{PL}	2 × 2 × 2 × 2 OR AND inverter	
Standard Cell Unique Logic		
ADDF_{PL}	Full adder	
BUFFER_{PL}	Buffer	
CLK_{PL}	Clock driver	
CLKI_{PL}	Inverting clock driver	
COMP2_{PL}	Two-bit comparator	
DELAY4_{PL}	Delay line	
DELAY6_{PL}	Delay line	
MUX21_{PL}	2:1 multiplexer	
MUX21I_{PL}	2:1 multiplexer with inverted output	
MUX41_{PL}	4:1 multiplexer	
TERM_{PL}	Net terminator	
Standard Cell Sequential Logic		
DFF_{PL}	DFF with Q and QBAR outputs	
DFFR_{PL}	DFF with Q and QBAR outputs, -asynchronous reset	
DFFS_{PL}	DFF with Q and QBAR outputs, asynchronous set	
DFFSR_{PL}	DFF with Q and QBAR outputs, asynchronous set, -asynchronous reset	
SDFF_{PL}	Scannable DFF with Q and QBAR outputs	
SDFFR_{PL}	Scannable DFF with Q and QBAR outputs, -asynchronous reset	
SDFFS_{PL}	Scannable DFF with Q and QBAR outputs, asynchronous set	
SDFFSR_{PL}	Scannable DFF Q and QBAR outputs, asynchronous set, -asynchronous reset	
LATSR_{PL}	Latch with Q and QBAR outputs, asynchronous set, -asynchronous reset	
SLATSR_{PL}	Scannable latch with Q and QBAR outputs, asynchronous set, -asynchronous reset	



CMOS 7RF (CMRF7SF) 1.8 V (12-Track) Standard Cell Databook

Table 1-11. CMOS 7RF 1.8 V (12-Track) Cell Functions (Page 3 of 3)

Cell	Function		
Physical Design Cells			
FILL{1,2}	One- and two-cell post fill cells		
FGTIE_{PL}	Floating gate tie-off		
GAUNUSEDxxx	Gate array postfill cells		



2. Standard Cell Primitive Logic

2.1 AND2_{PL} Cell

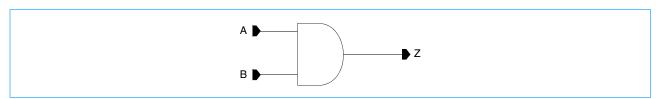
2.1.1 Function

Two-way AND

2.1.2 Description

This cell is a combinational gate, two-way AND. The Boolean expression for this cell is $Z = (A \times B)$.

Figure 2-1. Cell AND2_{PL} Symbols



2.1.3 Propagation Delay Table

Table 2-1. Cell AND2_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V_{DD} 1.8 V T_j 25°C
	A-Z	t _{PHH}	0.120
В	A-Z	t _{PLL}	0.120
Б	B–Z	t _{PHH}	0.111
	D-Z	t _{PLL}	0.129
	A-Z	t _{PHH}	0.101
С	A-Z	t _{PLL}	0.113
C	D 7	t _{PHH}	0.093
	B–Z	t _{PLL}	0.123
	۸.7	t _{PHH}	0.092
D	A–Z	t _{PLL}	0.099
D	B–Z	t _{PHH}	0.085
	D-Z	t _{PLL}	0.108
	A-Z	t _{PHH}	0.090
E	A-Z	t _{PLL}	0.098
	B-Z	t _{PHH}	0.083
	D-Z	t _{PLL}	0.107

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-1. Cell AND2_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A–Z	t _{PHH}	0.084
F	A-Z	t _{PLL}	0.096
F	B–Z	t _{PHH}	0.078
	D-Z	t _{PLL}	0.105
	A-Z	t _{PHH}	0.084
	A-Z	t _{PLL}	0.108
Н	D 7	t _{PHH}	0.079
	B–Z	t _{PLL}	0.120
	A–Z	t _{PHH}	0.091
ı	A-Z	t _{PLL}	0.106
I	D 7	t _{PHH}	0.084
	B–Z	t _{PLL}	0.115
	۸.7	t _{PHH}	0.096
	A–Z	t _{PLL}	0.121
J	D 7	t _{PHH}	0.089
	B–Z	t _{PLL}	0.130
	A-Z	t _{PHH}	0.106
К -	A-Z	t _{PLL}	0.121
	D 7	t _{PHH}	0.098
	B–Z	t _{PLL}	0.129

^{2.1.4} Cell Specifications

Table 2-2. Cell AND2_{PL} Capacitance

Input /	Capacitance (fF) by Performance Level								
Output Pins	В	С	D	E	F	Н	I	J	K
A	2.6	3.3	4.6	5.1	6.7	6.6	8.0	8.8	9.4
В	2.6	3.1	4.3	4.8	6.4	6.3	7.7	8.3	9.0
Z	51.9	109.4	172.9	238.7	356.5	454.9	707.4	959.1	1208.9

1. Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-3. Cell AND2_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
В			
С			
D			
E	3.36		
F		6.72	
Н			
I			
J	4.40		
К	4.48		



2.2 AND3_{PL} Cell

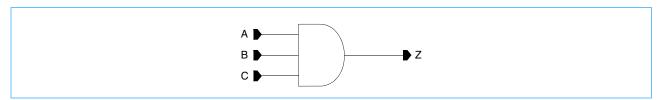
2.2.1 Function

Three-way AND

2.2.2 Description

This cell is a combinational gate, three-way AND. The Boolean expression for this cell is $Z = (A \times B \times C)$.

Figure 2-2. Cell AND3_{PL} Symbols



2.2.3 Propagation Delay Table

Table 2-4. Cell AND3_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A 7	t _{PHH}	0.132
	A-Z	t _{PLL}	0.143
В	B-Z	t _{PHH}	0.130
Б	D-Z	t _{PLL}	0.154
	C-Z	t _{PHH}	0.122
	U-Z	t _{PLL}	0.164
	A-Z	t _{PHH}	0.130
	A-Z	t _{PLL}	0.129
С	D 7	t _{PHH}	0.126
C	B–Z	t _{PLL}	0.136
	C 7	t _{PHH}	0.116
	C-Z	t _{PLL}	0.144
	A-Z	t _{PHH}	0.111
	A-Z	t _{PLL}	0.112
D	B-Z	t _{PHH}	0.107
D	D-Z	t _{PLL}	0.121
	C-Z	t _{PHH}	0.100
	U-Z	t _{PLL}	0.129

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-4. Cell AND3_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A 7	t _{PHH}	0.114
	A–Z	t _{PLL}	0.111
_	D 7	t _{PHH}	0.110
E	B–Z	t _{PLL}	0.120
	C–Z	t _{PHH}	0.103
	0-2	t _{PLL}	0.127
	A–Z	t _{PHH}	0.108
	A-L	t _{PLL}	0.108
F	B–Z	t _{PHH}	0.105
'	D-Z	t _{PLL}	0.117
	C–Z	t _{PHH}	0.098
	0-2	t _{PLL}	0.125
	A–Z	t _{PHH}	0.105
	A-2	t _{PLL}	0.116
н	B–Z	t _{PHH}	0.102
11	D-Z	t _{PLL}	0.126
	C–Z	t _{PHH}	0.097
	0-2	t _{PLL}	0.135
	A–Z	t _{PHH}	0.109
	A 2	t _{PLL}	0.118
I	B–Z	t _{PHH}	0.106
'	t _F	t _{PLL}	0.128
	C–Z	t _{PHH}	0.100
	∪ -∠	t _{PLL}	0.136
	A–Z	t _{PHH}	0.112
	7. 2	t _{PLL}	0.123
J	B–Z	t _{PHH}	0.109
J	D-Z	t _{PLL}	0.133
	C–Z	t _{PHH}	0.104
	U-L	t _{PLL}	0.142

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-4. Cell AND3_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A–Z	t _{РНН}	0.110
К	A-Z	t _{PLL}	0.127
	B–Z	t _{PHH}	0.108
	D-Z	t _{PLL}	0.136
	C-Z	t _{РНН}	0.102
	0-2	t _{PLL}	0.145

2.2.4 Cell Specifications

Table 2-5. Cell AND3_{PL} Capacitance

Input /	Capacitance (fF) by Performance Level								
Output Pins	В	С	D	E	F	Н	I	J	K
Α	2.7	3.2	4.5	4.8	6.0	7.1	8.1	9.9	11.1
В	2.5	2.9	4.1	4.4	5.7	6.7	7.7	10.3	11.5
С	2.5	2.9	4.0	4.3	5.5	6.3	7.3	10.0	11.1
Z	54.4	110.9	167.5	237.6	354.3	501.5	706.6	968.7	1257.2

Table 2-6. Cell AND3_{PL} Area

	Cell Dimensions (μm)			
Performance Level	Width	Length		
В				
С				
D				
Е	3.92			
F		6.72		
Н				
I				
J	5.00			
К	5.60			



2.3 AND4_{PL} Cell

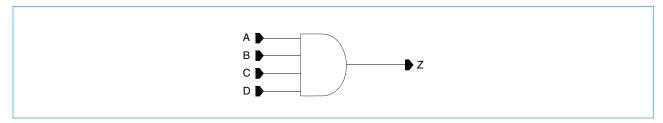
2.3.1 Function

Four-way AND

2.3.2 Description

This cell is a combinational gate, four-way AND. The Boolean expression for this cell is $Z = (A \times B \times C \times D)$.

Figure 2-3. Cell AND4_{PL} Symbols



2.3.3 Propagation Delay Table

Table 2-7. Cell AND4_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process $(ns)^1$ V_{DD} 1.8 V T_j 25°C
	A 7	t _{PHH}	0.148
	A–Z	t _{PLL}	0.127
	B–Z	t _{PHH}	0.148
В	D-Z	t _{PLL}	0.136
В	C–Z	t _{PHH}	0.146
	0-2	t _{PLL}	0.145
	D–Z	t _{PHH}	0.141
	D- <u>Z</u>	t _{PLL}	0.152
	A-Z	t _{PHH}	0.131
	A-2	t _{PLL}	0.128
	B–Z	t _{PHH}	0.132
С	υ-ζ	t _{PLL}	0.138
· ·	C–Z	t _{PHH}	0.130
	υ- Ζ	t _{PLL}	0.147
	D–Z	t _{PHH}	0.124
	D-Z	t _{PLL}	0.154

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.

CMOS 7RF (CMRF7SF) 1.8 V (12-Track) Standard Cell Databook



Table 2-7. Cell AND4_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A 7	t _{PHH}	0.125
	A–Z	t _{PLL}	0.125
	D 7	t _{PHH}	0.125
D	B–Z	t _{PLL}	0.136
D	0.7	t _{PHH}	0.123
	C–Z	t _{PLL}	0.145
	D 7	t _{PHH}	0.118
	D-Z	t _{PLL}	0.152
	A 7	t _{PHH}	0.120
	A-Z	t _{PLL}	0.121
	D 7	t _{PHH}	0.121
F	B–Z	t _{PLL}	0.131
E	C–Z	t _{PHH}	0.119
	0-2	t _{PLL}	0.141
	D–Z	t _{PHH}	0.115
	D-Z	t _{PLL}	0.148
	A-Z	t _{PHH}	0.118
	A-Z	t _{PLL}	0.120
	B–Z	t _{PHH}	0.119
F	D- <u>Z</u>	t _{PLL}	0.130
ľ	C–Z	t _{PHH}	0.117
	0-2	t _{PLL}	0.139
	D-Z	t _{PHH}	0.113
	D- <u>Z</u>	t _{PLL}	0.147
	A-Z	t _{PHH}	0.114
	Λ 4	t _{PLL}	0.117
	B-Z	t _{PHH}	0.115
Н	υ-Δ	t _{PLL}	0.128
11	C–Z	t _{PHH}	0.113
	∪− ∠	t _{PLL}	0.137
	D-Z	t _{PHH}	0.110
	D-Z	t _{PLL}	0.144

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . lib\ timing\ files\ for\ more\ information.$



Table 2-7. Cell AND4_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A–Z	t _{PHH}	0.145
	A-Z	t _{PLL}	0.138
	B-Z	t _{PHH}	0.144
I .	B-Z	t _{PLL}	0.147
1	C-Z	t _{PHH}	0.141
	0-2	t _{PLL}	0.154
	D-Z	t _{PHH}	0.139
	D-Z	t _{PLL}	0.162
	A-Z	t _{PHH}	0.138
	A-Z	t _{PLL}	0.142
	B–Z	t _{PHH}	0.138
	D-Z	t _{PLL}	0.151
J	C-Z	t _{PHH}	0.134
	0-2	t _{PLL}	0.159
	D-Z	t _{PHH}	0.133
	D-Z	t _{PLL}	0.168
	A–Z	t _{PHH}	0.139
	A-L	t _{PLL}	0.136
	B-Z	t _{PHH}	0.139
K	υ–∠	t _{PLL}	0.145
r\	C-Z	t _{PHH}	0.136
	U-Z	t _{PLL}	0.153
	D-Z	t _{PHH}	0.135
	υ–∠	t _{PLL}	0.161

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information

2.3.4 Cell Specifications

Table 2-8. Cell AND4_{PL} Capacitance

Input /	Capacitance	capacitance (fF) by Performance Level							
Output Pins	В	С	D	E	F	Н	I	J	K
Α	3.3	3.7	4.1	4.7	5.9	7.3	7.9	9.2	11.2
В	3.2	3.5	3.9	4.5	5.5	6.8	7.6	8.9	10.6
С	3.3	3.6	4.0	4.6	5.6	6.9	7.0	8.3	10.1
D	2.8	3.1	3.5	4.1	5.2	6.6	7.6	8.9	10.8
Z	61.6	115.5	173.5	233.6	374.5	499.9	745.9	995.2	1279.3



Table 2-9. Cell AND4_{PL} Area

	Cell Dimensions (μm)			
Performance Level	Width	Length		
В				
С	4.48			
D	4.46			
E				
F	5.04	6.72		
Н	5.04			
I				
J	8.96			
К				



2.4 INVERT_{PL} Cell

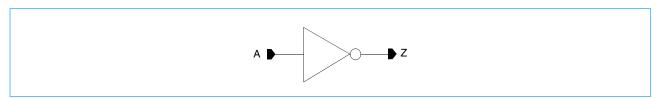
2.4.1 Function

Inverter

2.4.2 Description

This cell is a combinational gate inverter. The Boolean expression for this cell is $Z = \overline{A}$.

Figure 2-4. Cell INVERT_{PL} Symbols



2.4.3 Propagation Delay Table

Table 2-10. Cell INVERT_{PL} Propagation Delays (Page 1 of 2)

Path (Input to Output)	Performance Level	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	۸	t _{PLH}	0.099
	Α	t _{PHL}	0.035
	В	t _{PLH}	0.089
	В	t _{PHL}	0.037
	С	t _{PLH}	0.062
		t _{PHL}	0.035
	D	t _{PLH}	0.053
	U	t _{PHL}	0.030
A 7	_	t _{PLH}	0.049
A–Z	E	t _{PHL}	0.026
	F	t _{PLH}	0.051
	F	t _{PHL}	0.007
	.,	t _{PLH}	0.044
	Н –	t _{PHL}	0.012
		t _{PLH}	0.039
		t _{PHL}	0.016
	_	t _{PLH}	0.038
	J	t _{PHL}	0.017

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-10. Cell INVERT_{PL} Propagation Delays (Page 2 of 2)

Path (Input to Output)	Performance Level	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	К	t _{PLH}	0.038
	, ,	t _{PHL}	0.015
	ı	t _{PLH}	0.038
	L	t _{PHL}	0.014
	M	t _{PLH}	0.035
A 7	IVI	t _{PHL}	0.017
A–Z	N.	t _{PLH}	0.034
	N	t _{PHL}	0.018
	0	t _{PLH}	0.034
	0	t _{PHL}	0.018
		t _{PLH}	0.033
	U	t _{PHL}	0.018

2.4.4 Cell Specifications

Table 2-11. Cell INVERT_{PL} Capacitance

Input /	Capacit	ance (fF) by Perf	ormance	Level										
Output Pins	Α	В	С	D	Е	F	Н	I	J	K	L	М	N	0	U
Α	2.1	2.2	3.4	4.6	6.0	12.4	14.4	17.4	25.5	31.3	35.3	52.1	65.8	79.5	167.6
Z	40.1	48.4	98.5	148.9	201.8	337.2	448.1	595.8	859.6	1045.0	1183.4	1779.2	2322.4	2747.6	5834.8



Table 2-12. Cell INVERT_{PL} Area

	Cell Dimensions (μm)					
Performance Level	Width	Length				
А						
В						
С						
D	1.68					
E	1.00					
F						
Н						
I		6.72				
J						
К	2.80					
L						
М	4.48					
N	5.60					
0	7.28					
U	14.56					



2.5 INVERTBAL_{PL} Cell

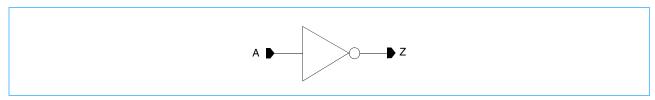
2.5.1 Function

Balanced inverter

2.5.2 Description

This cell is a combinational gate, balanced inverter. The Boolean expression for this cell is $Z = \overline{A}$.

Figure 2-5. Cell INVERTBAL_{PL} Symbols



2.5.3 Propagation Delay Table

Table 2-13. Cell INVERTBAL_{PL} Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Nominal Process $(ns)^1$ V_{DD} 1.8 V T_j 25°C
	E	t _{PLH}	0.038
		t _{PHL}	0.027
		t _{PLH}	0.034
A–Z	H	t _{PHL}	0.025
A-Z		t _{PLH}	0.032
	J	t _{PHL}	0.023
		t _{PLH}	0.032
	L	t _{PHL}	0.022

2.5.4 Cell Specifications

Table 2-14. Cell INVERTBAL_{PL} Capacitance

	Capacitance (fF) by Performance Level				
Input / Output Pins	Е	Н	J	L	
A	10.3	15.7	31.6	47.2	
Z	355.8	568.5	1128.6	1687.7	



Table 2-15. Cell INVERTBAL_{PL} Area

	Cell Dimensions (μm)			
Performance Level	Width	Length		
E	1.00			
Н	1.68	6.72		
J	3.36	0.72		
L	5.04			



2.6 NAND2_{PL} Cell

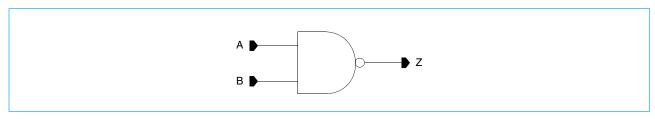
2.6.1 Function

Two-way NAND

2.6.2 Description

This cell is a combinational gate, two-way NAND. The Boolean expression for this cell is $Z = \overline{A \times B}$.

Figure 2-6. Cell NAND2_{PL} Symbols



2.6.3 Propagation Delay Table

Table 2-16. Cell NAND2_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A-Z	t _{PLH}	0.089
Δ	A-Z	t _{PHL}	0.060
Α	B–Z	t _{PLH}	0.098
	D-Z	t _{PHL}	0.052
	A-Z	t _{PLH}	0.085
В	A-Z	t _{PHL}	0.052
D	B–Z	t _{PLH}	0.095
	D- <u>Z</u>	t _{PHL}	0.045
	A–Z	t _{PLH}	0.064
С	A-Z	t _{PHL}	0.037
C	B–Z	t _{PLH}	0.076
	D-Z	t _{PHL}	0.034
	A-Z	t _{PLH}	0.057
D	M-L	t _{PHL}	0.032
	B–Z	t _{PLH}	0.070
	D- <u>/</u>	t _{PHL}	0.030

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-16. Cell NAND2_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
_	A 7	t _{PLH}	0.054
	A–Z	t _{PHL}	0.029
E		t _{PLH}	0.068
	B–Z	t _{PHL}	0.028
		t _{PLH}	0.054
_	A–Z	t _{PHL}	0.021
F		t _{PLH}	0.070
	B–Z	t _{PHL}	0.022
		t _{PLH}	0.052
	A–Z	t _{PHL}	0.020
Н		t _{PLH}	0.069
	B–Z	t _{PHL}	0.020
		t _{PLH}	0.054
	A–Z	t _{PHL}	0.017
I		t _{PLH}	0.072
	B–Z	t _{PHL}	0.019
		t _{PLH}	0.056
	A–Z	t _{PHL}	0.024
J -		t _{PLH}	0.056
	B–Z	t _{PHL}	0.024
		t _{PLH}	0.053
	A–Z		0.025
K		t _{PHL}	0.055
	B–Z	t _{PLH}	0.035
		t _{PHL}	
	A–Z	t _{PLH}	0.052
L		t _{PHL}	0.026
	B–Z	t _{PLH}	0.052
		t _{PHL}	0.026
	A-Z	t _{PLH}	0.055
M		t _{PHL}	0.023
	B–Z	t _{PLH}	0.055
		t _{PHL}	0.023

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



2.6.4 Cell Specifications

Table 2-17. Cell NAND2_{PL} Capacitance

Input /	Capacitar	Capacitance (fF) by Performance Level										
Output Pins	Α	В	С	D	E	F	Н	I	J	K	L	М
Α	2.4	2.6	4.7	6.6	8.5	12.7	24.8	26.2	30.7	39.8	48.9	61.8
В	2.5	2.7	4.4	6.3	8.2	12.9	24.7	26.0	30.4	39.7	48.9	61.4
Z	48.9	54.9	116.3	180.3	239.2	332.1	649.5	661.0	878.6	1165.9	1461.9	1754.9

Table 2-18. Cell NAND2_{PL} Area

	Cell Dimensions (μm)					
Performance Level	Width	Length				
А						
В						
С	2.24					
D	2.24					
E						
F		6.72				
Н						
I	4.48					
J						
К	6.16					
L	6.72					
М	8.96					



2.7 NAND2BAL_{PL} Cell

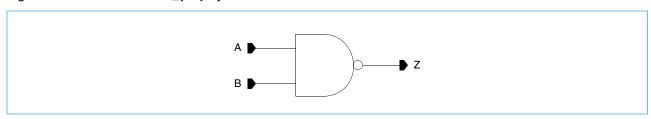
2.7.1 Function

Balanced two-way NAND

2.7.2 Description

This cell is a combinational gate, balanced two-way NAND. The Boolean expression for this cell is $Z = \overline{A \times B}$. The rising and falling delays are balanced; the A to Z delay is equal to the B to Z delay.

Figure 2-7. Cell NAND2BAL_{PL} Symbols



2.7.3 Propagation Delay Table

Table 2-19. Cell NAND2BAL_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A–Z	t _{PLH}	0.052
E	A-Z	t _{PHL}	0.039
<u> </u>	B–Z	t _{PLH}	0.052
	D- <u>Z</u>	t _{PHL}	0.040
	A–Z	t _{PLH}	0.049
н	A-Z	t _{PHL}	0.036
"	B–Z	t _{PLH}	0.048
	D- <u>Z</u>	t _{PHL}	0.036
	A–Z	t _{PLH}	0.048
J	A-Z	t _{PHL}	0.035
J	B–Z	t _{PLH}	0.047
	D-Z	t _{PHL}	0.035
	A–Z	t _{PLH}	0.048
	A-Z	t _{PHL}	0.034
L	B–Z	t _{PLH}	0.047
	υ-Ζ	t _{PHL}	0.034

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



2.7.4 Cell Specifications

Table 2-20. Cell NAND2BAL_{PL} Capacitance

	Capacitance (fF) by Performance Level					
Input / Output Pins	Е	Н	J	L		
A	11.1	17.1	34.4	51.7		
В	11.0	16.9	34.3	51.0		
Z	315.4	528.0	1047.8	1568.2		

Table 2-21. Cell NAND2BAL_{PL} Area

	Cell Dimensions (μm)				
Performance Level	Width	Length			
E	2.80				
Н	2.80	6.72			
J	5.60	0.72			
L	8.40				



2.8 NAND3_{PL} Cell

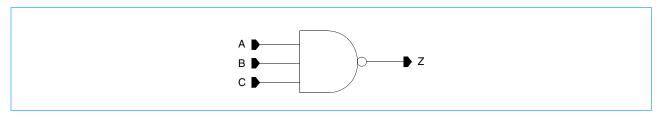
2.8.1 Function

Three-way NAND

2.8.2 Description

This cell is a combinational gate, three-way NAND. The Boolean expression for this cell is $Z = \overline{A \times B \times C}$.

Figure 2-8. Cell NAND3_{PL} Symbols



2.8.3 Propagation Delay Table

Table 2-22. Cell NAND3_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A-Z	t _{PLH}	0.108
	A-Z	t _{PHL}	0.080
Α	B–Z	t _{PLH}	0.118
A	D-Z	t _{PHL}	0.077
	C–Z	t _{PLH}	0.125
	0-2	t _{PHL}	0.068
	A–Z	t _{PLH}	0.091
	A-Z	t _{PHL}	0.058
В	B–Z	t _{PLH}	0.103
В	D-Z	t _{PHL}	0.058
	C–Z	t _{PLH}	0.114
	0-2	t _{PHL}	0.052
	A–Z	t _{PLH}	0.066
	A-Z	t _{PHL}	0.050
С	B–Z	t _{PLH}	0.079
C	D-Z	t _{PHL}	0.050
	C–Z	t _{PLH}	0.088
	U-Z	t _{PHL}	0.046

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-22. Cell NAND3_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V_{DD} 1.8 V T_j 25°C
	A 7	t _{PLH}	0.067
	A-Z	t _{PHL}	0.040
D	D 7	t _{PLH}	0.082
D	B–Z	t _{PHL}	0.041
	C-Z	t _{PLH}	0.093
	0-2	t _{PHL}	0.040
	A-Z	t _{PLH}	0.063
	A-Z	t _{PHL}	0.036
E	B-Z	t _{PLH}	0.079
L	υ-Δ	t _{PHL}	0.038
	C-Z	t _{PLH}	0.090
	0-2	t _{PHL}	0.037
	A-Z	t _{PLH}	0.061
	K-2	t _{PHL}	0.038
F	B–Z	t _{PLH}	0.075
,	D- <u>C</u>	t _{PHL}	0.038
	C-Z	t _{PLH}	0.087
	0-2	t _{PHL}	0.038
	A-Z	t _{PLH}	0.059
	K-2	t _{PHL}	0.036
н	B–Z	t _{PLH}	0.074
''	D- <u>Z</u>	t _{PHL}	0.036
	C-Z	t _{PLH}	0.086
	0 2	t _{PHL}	0.036
	A-Z	t _{PLH}	0.062
	N L	t _{PHL}	0.030
I	B-Z	t _{PLH}	0.079
!	υ- <u>/</u>	t _{PHL}	0.033
	C-Z	t _{PLH}	0.092
	0-2	t _{PHL}	0.033

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . lib\ timing\ files\ for\ more\ information.$



Table 2-22. Cell NAND3_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C		
	A-Z	t _{PLH}	0.059		
	A-Z	t _{PHL}	0.031		
1	D 7	t _{PLH}	0.076		
J	B–Z	t _{PHL}	0.034		
	C–Z	t _{PLH}	0.089		
	U-Z	t _{PHL}	0.034		
	۸.7	t _{PLH}	0.059		
	A–Z	t _{PHL}	0.034		
IZ.	D 7	t _{PLH}	0.074		
К	B–Z	t _{PHL}	0.036		
	0.7	t _{PLH}	0.086		
	C–Z	t _{PHL}	0.035		
. Minimum input transition and minimum output load. See .lib timing files for more information.					

2.8.4 Cell Specifications

Table 2-23. Cell NAND3_{PL} Capacitance

Input /	Capacitanc	Capacitance (fF) by Performance Level								
Output Pins	Α	В	С	D	E	F	Н	I	J	K
Α	2.1	3.2	5.3	7.6	10.2	16.0	20.2	33.0	41.5	50.8
В	2.3	3.1	5.3	8.0	10.7	15.7	19.8	32.0	41.3	49.5
С	2.4	3.1	5.2	7.8	10.3	15.5	19.4	31.8	41.0	49.8
Z	37.4	58.8	139.9	181.6	253.5	384.7	503.1	739.4	996.9	1241.9



Table 2-24. Cell NAND3_{PL} Area

	Cell Dimensions (μm)			
Performance Level	Width	Length		
Α				
В				
С	3.36			
D				
E		6.70		
F	F 60	6.72		
Н	5.60			
I	8.40			
J	9.52			
К	11.76			



2.9 NAND4_{PL} Cell

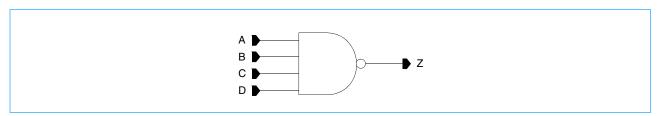
2.9.1 Function

Four-way NAND

2.9.2 Description

This cell is a combinational gate, four-way NAND. The Boolean expression for this cell is $Z = \overline{A \times B \times C \times D}$.

Figure 2-9. Cell NAND4_{PL} Symbols



2.9.3 Propagation Delay Table

Table 2-25. Cell NAND4_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A–Z	t _{PLH}	0.099
	A-Z	t _{PHL}	0.066
	B–Z	t _{PLH}	0.113
A	D-Z	t _{PHL}	0.068
A	C–Z	t _{PLH}	0.124
	D-Z	t _{PHL}	0.068
		t _{PLH}	0.133
		t _{PHL}	0.066
	A–Z	t _{PLH}	0.083
	A-Z	t _{PHL}	0.053
	B-Z	t _{PLH}	0.099
D	D-Z	t _{PHL}	0.056
В	C–Z	t _{PLH}	0.111
	U- ∠	t _{PHL}	0.057
	D 7	t _{PLH}	0.121
	D–Z	t _{PHL}	0.057

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-25. Cell NAND4_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A 7	t _{PLH}	0.078
	A-Z	t _{PHL}	0.044
	D 7	t _{PLH}	0.095
0	B–Z	t _{PHL}	0.048
С	C-Z	t _{PLH}	0.109
	0-2	t _{PHL}	0.050
	D-Z	t _{PLH}	0.122
	D-Z	t _{PHL}	0.052
	A 7	t _{PLH}	0.075
	A–Z	t _{PHL}	0.041
	B-Z	t _{PLH}	0.094
5	B-Z	t _{PHL}	0.045
D	C-Z	t _{PLH}	0.107
		t _{PHL}	0.048
	D-Z	t _{PLH}	0.121
		t _{PHL}	0.050
	A-Z	t _{PLH}	0.070
	A-Z	t _{PHL}	0.046
	B-Z	t _{PLH}	0.086
E	D-Z	t _{PHL}	0.050
E	C–Z	t _{PLH}	0.100
	0–2	t _{PHL}	0.054
	D-Z	t _{PLH}	0.110
	U-Z	t _{PHL}	0.053
	A-Z	t _{PLH}	0.066
	M-Z	t _{PHL}	0.043
	D 7	t _{PLH}	0.082
_	B–Z	t _{PHL}	0.047
F	C 7	t _{PLH}	0.097
	C–Z	t _{PHL}	0.051
	D 7	t _{PLH}	0.106
	D-Z		0.051

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



2.9.4 Cell Specifications

Table 2-26. Cell NAND4_{PL} Capacitance

Input /	Capacitance (fF	Capacitance (fF) by Performance Level					
Output Pins	Α	В	С	D	E	F	
Α	3.6	5.0	9.6	11.6	13.9	19.6	
В	3.4	4.8	9.2	11.1	13.5	19.1	
С	3.3	4.8	8.6	10.6	13.4	18.9	
D	3.3	4.6	9.2	11.1	13.4	19.0	
Z	56.9	95.4	174.5	218.2	296.1	448.3	

Table 2-27. Cell NAND4_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
А	3.36		
В			
С	5.60	6.70	
D		6.72	
E	7.04		
F	7.84		



2.10 NOR2_{PL} Cell

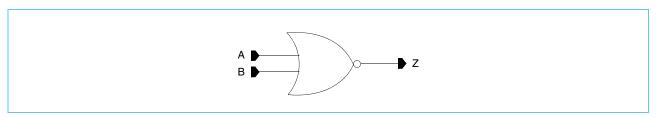
2.10.1 Function

Two-way NOR

2.10.2 Description

This cell is a combinational gate, two-way NOR. The Boolean expression for this cell is $Z = \overline{A + B}$.

Figure 2-10. Cell NOR2_{PL} Symbols



2.10.3 Propagation Delay Table

Table 2-28. Cell NOR2_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A-Z	t _{PLH}	0.121
Α	A-Z	t _{PHL}	0.039
^	B–Z	t _{PLH}	0.112
	D-Z	t _{PHL}	0.045
	A-Z	t _{PLH}	0.082
В	A-Z	t _{PHL}	0.049
J	B–Z	t _{PLH}	0.078
		t _{PHL}	0.061
	A–Z	t _{PLH}	0.062
С	A-Z	t _{PHL}	0.043
Ŭ	B–Z	t _{PLH}	0.061
	D-Z	t _{PHL}	0.060
	A–Z	t _{PLH}	0.053
D	H-Z	t _{PHL}	0.038
	B–Z	t _{PLH}	0.054
	υ-Σ	t _{PHL}	0.056

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-28. Cell NOR2_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A-Z	t _{PLH}	0.050
E	A-Z	t _{PHL}	0.037
_	B–Z	t _{PLH}	0.051
	D- <u>Z</u>	t _{PHL}	0.055
	A-Z	t _{PLH}	0.050
F	A-Z	t _{PHL}	0.035
ı	B–Z	t _{PLH}	0.051
	<i>D 2</i>	t _{PHL}	0.053
	A-Z	t _{PLH}	0.048
Н	A-L	t _{PHL}	0.034
''	B–Z	t _{PLH}	0.049
	D- <u>Z</u>	t _{PHL}	0.053
	A-Z	t _{PLH}	0.044
I -	A-2	t _{PHL}	0.032
ı	B–Z	t _{PLH}	0.047
	υ-∠	t _{PHL}	0.051
	A-Z	t _{PLH}	0.045
J	Λ-2	t _{PHL}	0.037
	B–Z	t _{PLH}	0.045
	<u>υ-</u> <u>κ</u>	t _{PHL}	0.046

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.

2.10.4 Cell Specifications

Table 2-29. Cell NOR2_{PL} Capacitance

Input /	Capacitance	(fF) by Perfor	mance Level						
Output Pins	Α	В	С	D	E	F	Н	I	J
Α	2.5	3.5	5.7	8.5	11.1	16.8	21.1	29.1	43.7
В	2.7	3.5	5.7	8.7	11.0	16.9	21.1	28.9	43.7
Z	27.0	53.3	110.2	168.4	229.8	331.9	434.0	617.6	941.5



Table 2-30. Cell NOR2_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
A			
В			
С	2.24		
D			
E		6.72	
F	2.00		
Н	3.92		
l	4.48		
J	6.72		



2.11 NOR3_{PL} Cell

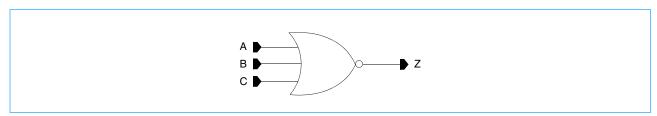
2.11.1 Function

Three-way NOR

2.11.2 Description

This cell is a combinational gate, three-way NOR. The Boolean expression for this cell is $Z = \overline{A + B + C}$.

Figure 2-11. Cell NOR3_{PL} Symbols



2.11.3 Propagation Delay Table

Table 2-31. Cell NOR3_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A-Z	t _{PLH}	0.099
	A-Z	t _{PHL}	0.059
Α	B–Z	t _{PLH}	0.103
A	D-Z	t _{PHL}	0.076
	C–Z	t _{PLH}	0.105
	0-2	t _{PHL}	0.082
	A–Z	t _{PLH}	0.084
	N-2	t _{PHL}	0.053
В	B–Z	t _{PLH}	0.091
В		t _{PHL}	0.072
	C–Z	t _{PLH}	0.094
	0-2	t _{PHL}	0.080
	A–Z	t _{PLH}	0.067
	A-Z	t _{PHL}	0.060
С	B–Z	t _{PLH}	0.077
C	D-Z	t _{PHL}	0.080
	C–Z	t _{PLH}	0.082
	U-Z	t _{PHL}	0.092

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-31. Cell NOR3_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V_{DD} 1.8 V T_j 25°C
	A-Z	t _{PLH}	0.062
	A-Z	t _{PHL}	0.053
D	B–Z	t _{PLH}	0.072
U	D-Z	t _{PHL}	0.074
	C–Z	t _{PLH}	0.078
	0-2	t _{PHL}	0.085
	A–Z	t _{PLH}	0.060
	A-Z	t _{PHL}	0.048
E	B–Z	t _{PLH}	0.069
E		t _{PHL}	0.067
	C–Z	t _{PLH}	0.075
	0-2	t _{PHL}	0.081
	A–Z	t _{PLH}	0.055
	A-Z	t _{PHL}	0.044
F	B–Z	t _{PLH}	0.065
F	D-Z	t _{PHL}	0.064
	C–Z	t _{PLH}	0.071
	0-2	t _{PHL}	0.077

2.11.4 Cell Specifications

Table 2-32. Cell NOR3_{PL} Capacitance

Input /	Capacitance (fF) by Performance Level					
Output Pins	Α	В	С	D	E	F
Α	3.9	5.3	9.9	13.6	18.2	28.3
В	3.8	5.1	9.3	12.9	17.3	27.2
С	3.6	4.9	9.5	13.1	17.8	28.4
Z	42.6	63.5	129.9	190.5	249.9	410.4



Table 2-33. Cell NOR3_{PL} Area

	Cell Dimensions (μm)			
Performance Level	Width	Length		
A	0.00			
В	2.80			
С	4.40	0.70		
D	4.48	6.72		
E	5.60			
F	6.16			



2.12 NOR4_{PL} Cell

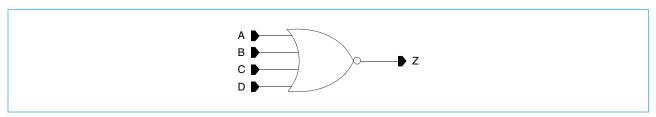
2.12.1 Function

Four-way NOR

2.12.2 Description

This cell is a combinational gate, four-way NOR. The Boolean expression for this cell is $Z = \overline{A + B + C + D}$.

Figure 2-12. Cell NOR4_{PL} Symbols



2.12.3 Propagation Delay Table

Table 2-34. Cell NOR4_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) 1 V _{DD} 1.8 V T $_j$ 25°C
	A 7	t _{PLH}	0.099
	A–Z	t _{PHL}	0.067
	B–Z	t _{PLH}	0.112
A	D-Z	t _{PHL}	0.091
Α .	C-Z	t _{PLH} 0.126 t _{PHL} 0.102 t _{PLH} 0.131 t _{PLH} 0.103	
	0-2	t _{PHL}	0.102
	D-Z	t _{PLH}	0.131
	D-Z	t _{PHL}	T _j 25°C 0.099 0.067 0.112 0.091 0.126 0.102
	A–Z	t _{PLH}	0.080
	A-Z	t _{PHL}	0.062
	B–Z	t _{PLH}	0.095
В	D-Z	t _{PHL}	0.086
D	C–Z	t _{PLH}	0.110
	0-2	Parameter Tj 25°C t _{PLH} 0.099 t _{PLH} 0.067 t _{PLH} 0.112 t _{PLH} 0.091 t _{PLH} 0.126 t _{PLH} 0.102 t _{PLH} 0.131 t _{PLH} 0.103 t _{PLH} 0.080 t _{PLH} 0.062 t _{PLH} 0.086 t _{PLH} 0.110 t _{PLH} 0.099 t _{PLH} 0.117	
	D-Z	t _{PLH}	0.117
	υ-Δ	t _{PHL}	0.103

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-34. Cell NOR4_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A–Z	t _{PLH}	0.072
	A-Z	t _{PHL}	0.058
	B–Z	t _{PLH}	0.087
С	D-Z	t _{PHL}	0.080
C	C–Z	t _{PLH}	0.102
	0–2	t _{PHL}	0.093
	D-Z	t _{PLH}	0.113
	D-Z	t _{PHL}	0.102
	A–Z	t _{PLH}	0.065
	A-Z	t _{PHL}	0.055
	B–Z	t _{PLH}	0.081
D	D-Z	t _{PHL}	0.079
D	C–Z	t _{PLH}	0.096
	0–2	t _{PHL}	0.092
	D–Z	t _{PLH}	0.106
	U-Z	t _{PHL}	0.096

2.12.4 Cell Specifications

Table 2-35. Cell NOR4_{PL} Capacitance

	Capacitance (fF) by Performance Level					
Input / Output Pins	Α	В	С	D		
A	4.2	6.4	14.1	28.6		
В	4.7	6.8	13.6	27.2		
С	4.6	6.7	13.2	26.9		
D	4.2	6.4	13.6	26.7		
Z	40.1	69.7	148.6	298.5		



Table 2-36. Cell NOR4_{PL} Area

	Cell Dimer	nsions (μm)
Performance Level	Width	Length
A	2.80	
В	2.80	6.72
С	5.60	0.72
D	9.52	



2.13 OR2_{PL} Cell

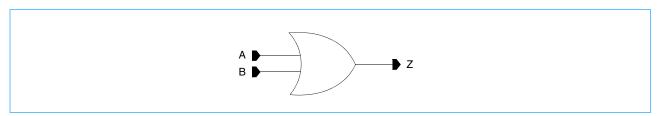
2.13.1 Function

Two-way OR

2.13.2 Description

This cell is a combinational gate, two-way OR. The Boolean expression for this cell is Z = A + B.

Figure 2-13. Cell OR2_{PL} Symbols



2.13.3 Propagation Delay Table

Table 2-37. Cell OR2_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A–Z	t _{PHH}	0.095
В	A-Z	t _{PLL}	0.148
Б	D 7	t _{PHH}	0.102
	D- <u>Z</u>	t _{PLL}	0.139
	Δ 7	t _{PHH}	0.091
С	N-2	t _{PLL}	0.134
Ŭ	B-Z A-Z A-Z B-Z	t _{PHH}	0.101
	<u>0-2</u>	t _{PLL}	0.127
	۸.7	t _{PHH}	0.096
D	A-Z	t _{PLL}	0.136
D	D 7	t _{PHH}	0.107
	D- <u>Z</u>	t _{PLL}	0.128
	A–Z	t _{PHH}	0.092
E	Λ-Δ	t _{PLL}	0.129
<u>_</u>	B–Z	t _{PHH}	0.103
	υ-Ζ	t _{PLL}	0.122

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-37. Cell OR2_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A-Z	t _{PHH}	0.090
F	A-Z	t _{PLL}	0.127
I.	B–Z	t _{PHH}	0.101
	D-Z	t _{PLL}	0.120
	A–Z	t _{PHH}	0.090
н	A-Z	t _{PLL}	0.135
11	B–Z	t _{PHH}	0.098
	D-Z	t _{PLL}	0.126
	A–Z	t _{PHH}	0.087
I	A-Z	t _{PLL}	0.124
ı	B–Z	t _{PHH}	0.099
	D-Z	t _{PLL}	0.117
	A–Z	t _{PHH}	0.088
J	A-Z	t _{PLL}	0.131
J	B–Z	t _{PHH}	0.099
	υ-Δ	t _{PLL}	0.123
	A-Z	t _{PHH}	0.099
K	M-Z	t _{PLL}	0.135
r.	B–Z	t _{PHH}	0.111
	D-Z	t _{PLL}	0.128

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.

2.13.4 Cell Specifications

Table 2-38. Cell OR2_{PL} Capacitance

Input /	Capacitance (fF) by Performance Level								
Output Pins	В	С	D	E	F	Н	I	J	K
Α	2.7	3.4	3.5	4.2	5.2	6.0	8.3	10.9	12.2
В	2.7	3.2	3.3	4.0	5.0	5.7	8.0	10.9	12.2
Z	52.1	107.2	168.4	231.9	356.3	477.2	711.2	979.7	1394.6



Table 2-39. Cell OR2_{PL} Area

	Cell Dimer	nsions (μm)
Performance Level	Width	Length
В		
С		
D		
Е	3.36	
F		6.72
Н		
I		
J	4.40	
К	4.48	



2.14 OR3_{PL} Cell

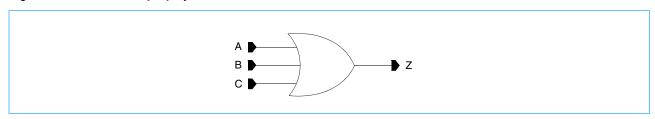
2.14.1 Function

Three-way OR

2.14.2 Description

This cell is a combinational gate, three-way OR. The Boolean expression for this cell is Z = A + B + C.

Figure 2-14. Cell OR3_{PL} Symbols



2.14.3 Propagation Delay Table

Table 2-40. Cell OR3_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A-Z	t _{РНН}	0.106
	A-Z	t _{PLL}	0.154
В	B–Z	t _{PHH}	0.117
В	D-Z	t _{PLL}	0.156
	C–Z	t _{РНН}	0.123
	0-2	t _{PLL}	0.157
	A–Z	t _{РНН}	0.102
	A-Z	t _{PLL}	0.152
С	B–Z	t _{PHH}	0.114
C	D-Z	t _{PLL}	0.154
	C–Z	t _{РНН}	0.122
	0-2	t _{PLL}	0.155
	A–Z	t _{РНН}	0.111
	A-Z	t _{PLL}	0.144
D	B–Z	t _{PHH}	0.124
U	D-Z	t _{PLL}	0.148
	C–Z	t _{РНН}	0.133
	U-Z	t _{PLL}	0.150

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-40. Cell OR3_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	۸.7	t _{PHH}	0.110
	A–Z	t _{PLL}	0.143
_	D 7	t _{PHH}	0.123
Е	B–Z	t _{PLL}	0.147
	0.7	t _{PHH}	0.132
	C-Z	t _{PLL}	0.149
	A 7	t _{PHH}	0.109
	A–Z	t _{PLL}	0.138
F	D 7	t _{PHH}	0.125
F	B–Z	t _{PLL}	0.144
	C–Z	t _{PHH}	0.134
	U-Z	t _{PLL}	0.145
	A-Z	t _{PHH}	0.103
	A-Z	t _{PLL}	0.135
	B–Z	t _{PHH}	0.119
Н	D-Z	t _{PLL}	0.141
	C-Z	t _{PHH}	0.128
	0-2	t _{PLL}	0.142
	A-Z	t _{PHH}	0.118
	A-Z	t _{PLL}	0.150
ı	B–Z	t _{PHH}	0.132
I	D-Z	t _{PLL}	0.155
	C-Z	t _{PHH}	0.147
	0-2	t _{PLL}	0.157
	A-Z	t _{PHH}	0.112
	Λ- Δ	t _{PLL}	0.147
J	B–Z	t _{PHH}	0.127
J	D-Z	t _{PLL}	0.152
	C-Z	t _{PHH}	0.140
	υ - <u>∠</u>	t _{PLL}	0.154

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-40. Cell OR3_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process $(ns)^1$ V_{DD} 1.8 V T_j 25°C
	A-Z	t _{РНН}	0.116
	A-Z	t _{PLL}	0.151
К	B–Z	t _{PHH}	0.131
N.	D-Z	t _{PLL}	0.158
	0.7	^t PHH	0.143
	C–Z	t _{PLL}	0.159

2.14.4 Cell Specifications

Table 2-41. Cell OR3_{PL} Capacitance

Input /	Capacitance (fF) by Performance Level								
Output Pins	В	С	D	E	F	Н	I	J	K
A	3.4	3.6	4.0	4.4	6.0	7.5	9.2	11.6	14.2
В	3.4	3.6	4.0	4.4	5.8	7.2	8.4	10.8	13.4
С	3.2	3.5	3.8	4.3	5.5	6.9	8.6	11.0	13.7
Z	57.2	109.2	165.2	221.3	359.5	475.5	710.3	947.8	1405.9

Table 2-42. Cell OR3_{PL} Area

	Cell Dimensions (μm)	
Performance Level	Width	Length
В	4.48	6.72
С		
D		
Е		
F		
Н		
I	7.28	
J		
К		



2.15 OR4_{PL} Cell

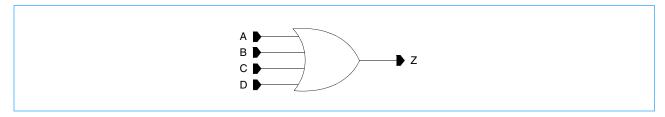
2.15.1 Function

Four-way OR

2.15.2 Description

This cell is a combinational gate, four-way OR. The Boolean expression for this cell is Z = A + B + C + D.

Figure 2-15. Cell OR4_{PL} Symbols



2.15.3 Propagation Delay Table

Table 2-43. Cell OR4_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A-Z	t _{РНН}	0.108
	A-Z	t _{PLL}	0.146
	B–Z	t _{РНН}	0.125
В	D-Z	t _{PLL}	0.159
ь	C–Z	t _{PHH}	0.135
	U-Z	t _{PLL}	0.171
	D–Z	t _{РНН}	0.136
	0-2	t _{PLL}	0.176
	A–Z	t _{РНН}	0.107
	A-Z	t _{PLL}	0.132
	B–Z	t _{PHH}	0.128
С	D-Z	t _{PLL}	0.148
C	C–Z	t _{РНН}	0.140
	U-Z	t _{PLL}	0.161
	D–Z	t _{РНН}	0.143
	U-Z	t _{PLL}	0.166

 $^{{\}bf 1.}\ \ {\bf Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ .lib\ timing\ files\ for\ more\ information.}$



Table 2-43. Cell OR4_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) [↑] V _{DD} 1.8 V T _j 25°C
	A 7	t _{PHH}	0.106
	A–Z	t _{PLL}	0.129
	D 7	t _{PHH}	0.127
D	B–Z	t _{PLL}	0.145
D	C-Z	t _{PHH}	0.140
	U-Z	t _{PLL}	0.158
	D-Z	t _{PHH}	0.144
	D-Z	t _{PLL}	0.163
	A-Z	t _{PHH}	0.106
	A-Z	t _{PLL}	0.128
	B-Z	t _{PHH}	0.127
E	B-Z	t _{PLL}	0.144
E	C–Z	t _{PHH}	0.140
		t _{PLL}	0.157
	D-Z	t _{PHH}	0.145
		t _{PLL}	0.163
	A–Z	t _{PHH}	0.081
		t _{PLL}	0.118
	B–Z	t _{PHH}	0.092
F	D- <u>Z</u>	t _{PLL}	0.112
ľ	C–Z	t _{PHH}	0.091
	0-2	t _{PLL}	0.124
	D-Z	t _{PHH}	0.101
	D- <u>Z</u>	t _{PLL}	0.117
	A-Z	t _{PHH}	0.085
	Λ- Δ	t _{PLL}	0.129
	B-Z	t _{PHH}	0.095
н	υ-Δ	t _{PLL}	0.123
	C–Z	t _{PHH}	0.093
	υ- Ζ	t _{PLL}	0.134
	D-Z	t _{PHH}	0.103
	U-L	t _{PLL}	0.127

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . lib\ timing\ files\ for\ more\ information.$



Table 2-43. Cell OR4_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A–Z	t _{РНН}	0.107
	A-Z	t _{PLL}	0.146
	B–Z	t _{РНН}	0.117
I .	D-Z	t _{PLL}	0.138
	C–Z	t _{РНН}	0.117
_	U-Z	t _{PLL}	0.150
	D-Z	t _{РНН}	0.126
	D-Z	t _{PLL}	0.142
	A-Z	t _{PHH}	0.111
	A-Z	t _{PLL}	0.155
	B–Z	t _{РНН}	0.121
ı	D-Z	t _{PLL}	0.147
J -	C–Z	t _{РНН}	0.120
		t _{PLL}	0.159
	D–Z	t _{PHH}	0.130
	D-Z	t _{PLL}	0.151
	A–Z	t _{РНН}	0.120
	A-2	t _{PLL}	0.161
	B-Z	t _{РНН}	0.131
К	υ–∠	t _{PLL}	0.153
r\	C-Z	t _{PHH}	0.129
	U-Z	t _{PLL}	0.166
	D–Z	t _{РНН}	0.139
	υ–∠	t _{PLL}	0.158

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information

2.15.4 Cell Specifications

Table 2-44. Cell OR4_{PL} Capacitance

Input /	Capacitance	Capacitance (fF) by Performance Level							
Output Pins	В	С	D	E	F	Н	I	J	K
Α	4.6	5.5	6.3	7.0	8.3	8.2	8.6	10.7	11.2
В	4.5	5.4	6.0	6.7	7.9	7.9	8.3	10.9	11.4
С	4.5	5.4	6.0	6.6	8.3	8.2	8.6	10.7	11.2
D	3.9	4.8	5.6	6.2	7.9	7.9	8.3	11.0	11.5
Z	56.9	116.0	175.1	239.9	382.9	530.7	779.8	1132.8	1431.9



Table 2-45. Cell OR4_{PL} Area

	Cell Dimer	nsions (μm)
Performance Level	Width	Length
В		
С	4.48	
D	4.40	
E		
F	5.60	6.72
Н	5.60	
I	7.84	
J	11.00	
К	11.20	



2.16 XOR2_{PL} Cell

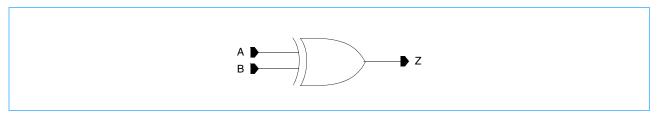
2.16.1 Function

Two-way XOR

2.16.2 Description

This cell is a combinational gate, two-way XOR. The Boolean expression for this cell is $Z = A \oplus B$.

Figure 2-16. Cell XOR2_{PL} Symbols



2.16.3 Propagation Delay Table

Table 2-46. Cell XOR2_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
		t _{PHH}	0.112
	A–Z	t _{PLL}	0.125
	A-Z	t _{PLH}	0.108
Α		t _{PHL}	0.082
^		t _{PHH}	0.098
	B–Z	t _{PLL}	0.123
	D- <u>Z</u>	t _{PLH}	0.129
		t _{PHL}	0.046
	A-Z	t _{PHH}	0.108
		t _{PLL}	0.119
		t _{PLH}	0.100
В		t _{PHL}	0.083
O D		t _{PHH}	0.096
	B–Z	t _{PLL}	0.117
	<u>υ-Σ</u>	t _{PLH}	0.120
		t _{PHL}	0.046

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-46. Cell XOR2_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) V _{DD} 1.8 V T _j 25°C
		t _{PHH}	0.093
	۸.7	t _{PLL}	0.102
	A–Z	t _{PLH}	0.085
0		t _{PHL}	0.073
С		t _{РНН}	0.085
	D 7	t _{PLL}	0.101
	B-Z	t _{PLH}	0.102
		t _{PHL}	0.039
		t _{PHH}	0.123
	A 7	t _{PLL}	0.138
	A-Z	t _{PLH}	0.154
		t _{PHL}	0.141
D		t _{РНН}	0.127
	B-Z	t _{PLL}	0.104
		t _{PLH}	0.150
		t _{PHL}	0.148
		t _{РНН}	0.118
	۸.7	t _{PLL}	0.135
	A-Z	t _{PLH}	0.148
Е		t _{PHL}	0.138
E		t _{PHH}	0.122
	D 7	t _{PLL}	0.102
	D-Z	B-Z tplH tpHL tpHL tpHH tpHH tpHL tpHH tpHH tpHH tpHH tpHH tpHH tpHH	0.144
		t _{PHL}	0.144
		t _{РНН}	0.113
	۸.7	t _{PLL}	0.130
	A-L	t _{PLH}	0.140
F		t _{PHL}	0.132
Г		t _{PHH}	0.117
	D 7	t _{PLL}	0.098
	D-Z	t _{PLH}	0.135
		t _{PHL}	0.138

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . lib\ timing\ files\ for\ more\ information.$



Table 2-46. Cell XOR2_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
		t _{PHH}	0.120
	A 7	t _{PLL}	0.129
	A–Z	t _{PLH}	0.142
		t _{PHL}	0.135
Н		t _{PHH}	0.126
	D 7	t _{PLL}	0.098
	B–Z	t _{PLH}	0.136
		t _{PHL}	0.141
		t _{PHH}	0.132
	A–Z	t _{PLL}	0.142
I -		t _{PLH}	0.155
		t _{PHL}	0.151
	B-Z	t _{PHH}	0.140
		t _{PLL}	0.110
		t _{PLH}	0.146
		t _{PHL}	0.158
		t _{PHH}	0.149
	A–Z	t _{PLL}	0.161
	A-L	t _{PLH}	0.173
,		t _{PHL}	0.176
J		t _{PHH}	0.158
	B–Z	t _{PLL}	0.128
	D-Z	t _{PLH}	0.159
		t _{PHL}	0.181

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information

2.16.4 Cell Specifications

Table 2-47. Cell XOR2_{PL} Capacitance

Input /	Capacitance	Capacitance (fF) by Performance Level							
Output Pins	Α	В	С	D	E	F	Н	I	J
Α	4.2	4.7	7.8	4.7	5.3	6.9	7.4	7.4	7.3
В	5.3	5.8	9.5	6.9	7.8	10.1	10.9	10.9	10.9
Z	59.4	72.7	144.8	163.4	224.6	355.6	444.6	708.3	1017.7



Table 2-48. Cell XOR2_{PL} Area

	Cell Dimer	nsions (μm)
Performance Level	Width	Length
А		
В	3.92	
С		
D		
E		6.72
F	5.60	
Н		
I		
J	7.28	



2.17 XOR3_{PL} Cell

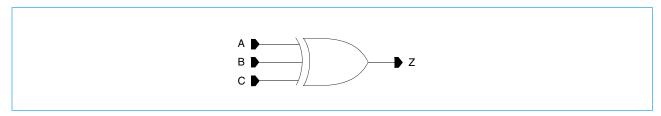
2.17.1 Function

Three-way XOR

2.17.2 Description

This cell is a combinational gate, three-way XOR. The Boolean expression for this cell is $Z = A \oplus B \oplus C$.

Figure 2-17. Cell XOR3_{PL} Symbols



2.17.3 Propagation Delay Table

Table 2-49. Cell XOR3_{PL} Propagation Delays (Page 1 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
		t _{РНН}	0.182
	A-Z	t _{PLL}	0.184
	A-Z	t _{PLH}	0.188
		t _{PHL}	0.151
		t _{РНН}	0.198
	B–Z	t _{PLL}	0.213
В	D-Z	t _{PLH}	0.198
		t _{PHL}	0.184
	C-Z	t _{PHH}	0.096
		t _{PLL}	0.120
		t _{PLH}	0.124
		t _{PHL}	0.126
С		t _{РНН}	0.177
	A–Z	t _{PLL}	0.183
		t _{PLH}	0.182
		t _{PHL}	0.151

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-49. Cell XOR3_{PL} Propagation Delays (Page 2 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
		t _{PHH}	0.192
	D 7	t _{PLL}	0.212
	B-Z	t _{PLH}	0.192
0		t _{PHL}	0.183
C		t _{PHH}	0.095
	0.7	t _{PLL}	0.120
	C-2	t _{PLH}	0.119
		t _{PHL}	0.128
		t _{PHH}	0.175
	A 7	t _{PLL}	0.183
	A-Z	t _{PLH}	0.181
		t _{PHL}	0.148
	B-Z	t _{PHH}	0.192
D		t _{PLL}	0.213
		t _{PLH}	0.193
		t _{PHL}	0.184
	C-Z A-Z B-Z C-Z	t _{PHH}	0.092
		t _{PLL}	0.118
		t _{PLH}	0.117
		t _{PHL}	0.127
		t _{PHH}	0.179
	A 7	t _{PLL}	0.186
	A-Z	t _{PLH}	0.186
		t _{PHL}	0.148
		t _{PHH}	0.192
F	D 7	t _{PLL}	0.213
E	B-∠	t _{PLH}	0.194
		t _{PHL}	0.176
		t _{PHH}	0.103
	0.7	t _{PLL}	0.121
	A-Z B-Z A-Z B-Z	t _{PLH}	0.122
		t _{PHL}	0.131

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-49. Cell XOR3_{PL} Propagation Delays (Page 3 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V_{DD} 1.8 V T_j 25°C
		t _{PHH}	0.179
	A–Z	t _{PLL}	0.194
		t _{PLH}	0.183
		t _{PHL}	0.156
		t _{PHH}	0.201
_		t _{PLL}	0.216
F	B–Z	t _{PLH}	0.201
		t _{PHL}	0.189
		t _{PHH}	0.108
		t _{PLL}	0.116
	C–Z	t _{PLH}	0.121
		t _{PHL}	0.124
	A-Z	t _{PHH}	0.183
		t _{PLL}	0.201
		t _{PLH}	0.188
		t _{PHL}	0.166
	_	t _{PHH}	0.208
		t _{PLL}	0.221
Н	B–Z	t _{PLH}	0.207
		t _{PHL}	0.199
		t _{PHH}	0.115
	0.7	t _{PLL}	0.126
	C–Z	t _{PLH}	0.125
		t _{PHL}	0.135
		t _{PHH}	0.201
	۸.7	t _{PLL}	0.221
	A–Z	t _{PLH}	0.207
ı		t _{PHL}	0.182
l -		t _{PHH}	0.222
	D 7	t _{PLL}	0.244
	B–Z	t _{PLH}	0.224
		t _{PHL}	0.220

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-49. Cell XOR3_{PL} Propagation Delays (Page 4 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	C-Z	t _{PHH}	0.133
1		t _{PLL}	0.138
ı		t _{PLH}	0.138
		t _{PHL}	0.151
Minimum input transition and	d minimum output load. See .lib tin	ning files for more information.	

2.17.4 Cell Specifications

Table 2-50. Cell XOR3_{PL} Capacitance

Input /	Capacitance (fF	Capacitance (fF) by Performance Level					
Output Pins	В	С	D	E	F	Н	I
Α	11.3	11.3	11.7	11.7	13.1	13.1	13.1
В	8.0	8.0	8.0	8.9	8.9	8.9	8.9
С	8.5	8.6	9.0	9.0	11.6	11.6	12.7
Z	64.9	121.5	172.9	238.6	385.3	512.7	761.3

Table 2-51. Cell XOR3_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
В			
С			
D	9.52		
Е	9.52	6.72	
F			
Н			
I	10.64		



2.18 XNOR2_{PL} Cell

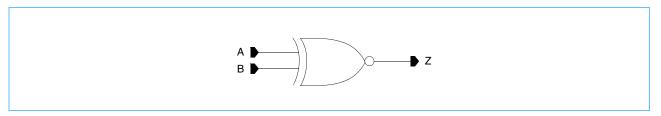
2.18.1 Function

Two-way XNOR

2.18.2 Description

This cell is a combinational gate, two-way XNOR. The Boolean expression for this cell is $Z = \overline{A \oplus B}$.

Figure 2-18. Cell XNOR2_{PL} Symbols



2.18.3 Propagation Delay Table

Table 2-52. Cell XNOR2_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
		t _{PLH}	0.105
	A–Z	t _{PHL}	0.086
	A-Z	t _{PHH}	0.114
А		t _{PLL}	0.122
A		t _{PLH}	0.073
	B–Z	t _{PHL}	0.095
		t _{PHH}	0.122
		t _{PLL}	0.116
	A–Z	t _{PLH}	0.098
		t _{PHL}	0.085
		t _{PHH}	0.109
В		t _{PLL}	0.116
D		t _{PLH}	0.067
	B–Z	t _{PHL}	0.093
	υ - Ζ	t _{PHH}	0.115
		t _{PLL}	0.111

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-52. Cell XNOR2_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V_{DD} 1.8 V T_{j} 25°C
		t _{PLH}	0.083
	A 7	t _{PHL}	0.077
	A–Z	t _{PHH}	0.094
0		t _{PLL}	0.100
C		t _{PLH}	0.055
	D 7	t _{PHL}	0.083
	B–Z	t _{PHH}	0.098
		t _{PLL}	0.097
		t _{PLH}	0.144
	A 7	t _{PHL}	0.130
	A-Z	t _{PHH}	0.110
5		t _{PLL}	0.134
D	B-Z	t _{PLH}	0.142
		t _{PHL}	0.118
		t _{PHH}	0.074
		t _{PLL}	0.153
	A-Z	t _{PLH}	0.151
		t _{PHL}	0.136
		t _{PHH}	0.114
_		t _{PLL}	0.140
E		t _{PLH}	0.149
	D 7	t _{PHL}	0.123
	B–Z	t _{PHH}	0.078
		t _{PLL}	0.161
		t _{PLH}	0.142
	A 7	t _{PHL}	0.131
	A-Z	t _{PHH}	0.110
_		t _{PLL}	0.133
F		t _{PLH}	0.140
	D 7	t _{PHL}	0.118
	B–Z	t _{PHH}	0.075
		t _{PLL}	0.153

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-52. Cell XNOR2_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V_{DD} 1.8 V T_j 25°C
		t _{PLH}	0.144
	A 7	t _{PHL}	0.133
	A–Z	t _{PHH}	0.120
н		t _{PLL}	0.127
П		t _{PLH}	0.142
	B–Z	t _{PHL}	0.120
	D-Z	t _{PHH}	0.082
		t _{PLL}	0.145
		t _{PLH}	0.157
	A-Z	t _{PHL}	0.146
	K-L	t _{PHH}	0.133
ı		t _{PLL}	0.138
ı	B-Z	t _{PLH}	0.154
		t _{PHL}	0.129
		t _{PHH}	0.094
		t _{PLL}	0.160
		t _{PLH}	0.175
	A-Z	t _{PHL}	0.169
	A-Z	t _{PHH}	0.150
J		t _{PLL}	0.157
J		t _{PLH}	0.173
	B–Z	t _{PHL}	0.145
	υ-Δ	t _{PHH}	0.112
		t _{PLL}	0.183

2.18.4 Cell Specifications

Table 2-53. Cell XNOR2_{PL} Capacitance

Input /	Capacitance	Capacitance (fF) by Performance Level							
Output Pins	Α	В	С	D	E	F	Н	I	J
Α	4.1	4.6	7.7	5.9	5.2	6.8	7.7	7.7	7.6
В	6.1	6.9	11.7	7.7	6.7	8.7	9.6	9.6	9.5
Z	59.0	72.9	145.8	233.8	224.3	350.6	439.3	706.3	1011.9



Table 2-54. Cell XNOR2_{PL} Area

	Cell Dime	nsions (μm)
Performance Level	Width	Length
Α		
В	3.92	
С		
D		
E	5.04	6.72
F	5.04	
Н		
I	5.60	
J	6.72	



2.19 XNOR3_{PL} Cell

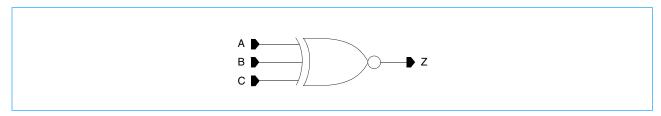
2.19.1 Function

Three-way XNOR

2.19.2 Description

This cell is a combinational gate, three-way XNOR. The Boolean expression for this cell is $Z = \overline{A \oplus B \oplus C}$.

Figure 2-19. Cell XNOR3_{PL} Symbols



2.19.3 Propagation Delay Table

Table 2-55. Cell XNOR3_{PL} Propagation Delays (Page 1 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
		t _{PLH}	0.175
	A–Z	t _{PHL}	0.172
	A-Z	t _{PHH}	0.148
		t _{PLL}	0.176
		t _{PLH}	0.204
В	B–Z	t _{PHL}	0.186
В		t _{PHH}	0.175
		t _{PLL}	0.185
	C–Z	t _{PLH}	0.130
		t _{PHL}	0.116
		t _{PHH}	0.089
		t _{PLL}	0.122
		t _{PLH}	0.168
0	A–Z	t _{PHL}	0.172
С	M-2	t _{PHH}	0.142
		t _{PLL}	0.176

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 2-55. Cell XNOR3_{PL} Propagation Delays (Page 2 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process $(ns)^1$ V_{DD} 1.8 V T_j 25°C
		t _{PLH}	0.198
	D 7	t _{PHL}	0.185
	B–Z	t _{PHH}	0.168
•		t _{PLL}	0.185
С		t _{PLH}	0.124
		t _{PHL}	0.117
	C-Z	t _{PHH}	0.088
		t _{PLL}	0.122
		t _{PLH}	0.165
	A 7	t _{PHL}	0.167
	A-Z	t _{PHH}	0.137
		t _{PLL}	0.170
	B-Z	t _{PLH}	0.196
D		t _{PHL}	0.182
D		t _{PHH}	0.167
		t _{PLL}	0.182
	C-Z	t _{PLH}	0.123
		t _{PHL}	0.116
		t _{PHH}	0.085
		t _{PLL}	0.120
		t _{PLH}	0.172
	A-Z	t _{PHL}	0.166
	A-Z	t _{PHH}	0.142
		t _{PLL}	0.172
		t _{PLH}	0.200
E	B–Z	t _{PHL}	0.177
Ē	D-Z	t _{PHH}	0.162
		t _{PLL}	0.177
		t _{PLH}	0.129
	0.7	t _{PHL}	0.120
	C–Z	t _{PHH}	0.095
		t _{PLL}	0.123



Table 2-55. Cell XNOR3_{PL} Propagation Delays (Page 3 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V_{DD} 1.8 V T_j 25°C
		t _{PLH}	0.179
		t _{PHL}	0.157
	A–Z	t _{PHH}	0.153
		t _{PLL}	0.164
		t _{PLH}	0.204
_		t _{PHL}	0.181
F	B–Z	t _{PHH}	0.177
		t _{PLL}	0.179
		t _{PLH}	0.129
		t _{PHL}	0.119
	C–Z	t _{PHH}	0.099
		t _{PLL}	0.116
	A-Z	t _{PLH}	0.180
		t _{PHL}	0.169
		t _{PHH}	0.159
		t _{PLL}	0.176
		t _{PLH}	0.202
		t _{PHL}	0.195
Н	B–Z	t _{PHH}	0.184
		t _{PLL}	0.191
		t _{PLH}	0.133
		t _{PHL}	0.129
	C–Z	t _{PHH}	0.105
		t _{PLL}	0.126
		t _{PLH}	0.198
		t _{PHL}	0.186
	A-Z	t _{PHH}	0.177
		t _{PLL}	0.193
I		t _{PLH}	0.223
		t _{PHL}	0.211
	B–Z	t _{PHH}	0.204
		t _{PLL}	0.209

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . lib\ timing\ files\ for\ more\ information.$

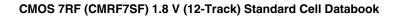




Table 2-55. Cell XNOR3_{PL} Propagation Delays (Page 4 of 4)

t _{PLH}	0.155
t _{PHL}	0.141
t _{PHH}	0.118
t _{PLL}	0.140

2.19.4 Cell Specifications

Table 2-56. Cell XNOR3_{PL} Capacitance

Input /	Capacitance (fF) by Performance Level								
Output Pins	В	С	D	E	F	Н	I		
Α	11.3	11.3	11.7	11.7	13.1	13.0	13.1		
В	8.0	8.0	8.0	8.9	8.8	8.8	8.8		
С	8.0	8.0	8.3	8.3	10.8	10.8	11.9		
Z	64.6	120.8	172.0	239.0	387.6	512.7	764.0		

Table 2-57. Cell XNOR3_{PL} Area

	Cell Dimensions (μm)					
Performance Level	Width	Length				
В						
С						
D	0.50					
Е	9.52	6.72				
F						
Н						
I	10.64					

3. Standard Cell Complex Logic

3.1 AO21_{PL} Cell

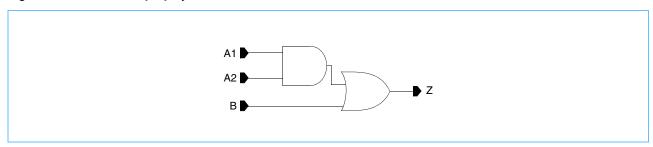
3.1.1 Function

 2×1 AND OR

3.1.2 Description

This cell is a combinational gate, 2×1 AND OR. The Boolean expression for this cell is $Z = (A1 \times A2) + B$.

Figure 3-1. Cell AO21_{PL} Symbols



3.1.3 Propagation Delay Table

Table 3-1. Cell AO21_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A1–Z	t _{PHH}	0.125
	AI-Z	t _{PLL}	0.141
В	A2-Z	t _{РНН}	0.116
ь	AZ-Z	t _{PLL}	0.151
	B–Z	t _{PHH}	0.126
	D-Z	t _{PLL}	0.100
	A1–Z	t _{РНН}	0.124
	AI-Z	t _{PLL}	0.130
С	A2-Z	t _{РНН}	0.112
O	MZ-Z	t _{PLL}	0.138
	D 7	t _{PHH}	0.130
	B–Z	t _{PLL}	0.093

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . lib\ timing\ files\ for\ more\ information.$



Table 3-1. Cell AO21_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	7	t _{PHH}	0.113
	A1–Z	t _{PLL}	0.119
D	40.7	t _{PHH}	0.103
	A2–Z	t _{PLL}	0.128
	D 7	t _{PHH}	0.150
	B-Z	t _{PLL}	0.084
	A1 7	t _{PHH}	0.107
	A1–Z	t _{PLL}	0.115
_	40.7	t _{PHH}	0.097
E	A2–Z	t _{PLL}	0.124
	D 7	t _{PHH}	0.156
	B-Z	t _{PLL}	0.080
	A1–Z	^t РНН	0.098
	AI-Z	t _{PLL}	0.110
_	40.7	t _{PHH}	0.090
F	A2–Z	t _{PLL}	0.120
	B-Z	t _{РНН}	0.151
	D-Z	t _{PLL}	0.075
	A1–Z	t _{РНН}	0.102
	AI-Z	t _{PLL}	0.122
	40.7	t _{PHH}	0.094
Н	A2–Z	t _{PLL}	0.133
	B-Z	t _{РНН}	0.149
	υ-Δ	t _{PLL}	0.080
	A1–Z	t _{РНН}	0.103
	MI-Z	t _{PLL}	0.131
ı	A2-Z	t _{PHH}	0.095
ı	AZ-Z	t _{PLL}	0.142
	B-Z	t _{РНН}	0.148
	D-Z	t _{PLL}	0.085

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 3-1. Cell AO21_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A1–Z	t _{PHH}	0.115
	AI-Z	t _{PLL}	0.127
,	A2-Z	t _{PHH}	0.106
J	AZ-Z	t _{PLL}	0.137
	B–Z	t _{PHH}	0.174
	D-Z	t _{PLL}	0.117
	A1–Z	t _{PHH}	0.120
	AI-Z	t _{PLL}	0.122
K	A2-Z	t _{PHH}	0.110
r.	AZ-Z	t _{PLL}	0.131
	B–Z	t _{PHH}	0.184
	D-Z	t _{PLL}	0.114

3.1.4 Cell Specifications

Table 3-2. Cell AO21_{PL} Capacitance

Input /	Capacitance (fF) by Performance Level								
Output Pins	В	С	D	E	F	Н	I	J	K
A1	3.0	3.5	4.6	5.6	7.6	7.5	8.5	12.3	16.1
A2	2.7	3.2	4.4	5.3	7.2	7.2	8.1	11.6	15.3
В	4.6	5.6	7.1	8.4	11.4	11.0	12.5	10.6	13.9
Z	56.6	113.7	174.9	235.6	356.0	474.9	708.3	942.6	1374.2



Table 3-3. Cell AO21_{PL} Area

	Cell Dimensions (μm)				
Performance Level	Width	Length			
В					
С					
D					
Е	3.92				
F		6.72			
Н					
I					
J	0.16				
К	6.16				



3.2 AO22_{PL} Cell

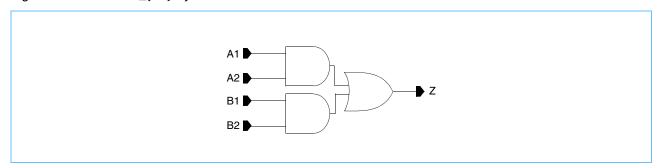
3.2.1 Function

 2×2 AND OR

3.2.2 Description

This cell is a combinational gate, 2×2 AND OR. The Boolean expression for this cell is $Z = (A1 \times A2) + (B1 \times B2)$.

Figure 3-2. Cell AO22_{PL} Symbols



3.2.3 Propagation Delay Table

Table 3-4. Cell AO22_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A1 7	t _{PHH}	0.108
	A1–Z	t _{PLL}	0.114
	A2–Z	t _{PHH}	0.101
В	AZ-Z	t _{PLL}	0.125
Б	B1–Z	t _{PHH}	0.137
	D1-Z	t _{PLL}	0.128
	B2-Z	t _{PHH}	0.128
	DZ-Z	t _{PLL}	0.139
	A1–Z	t _{PHH}	0.088
	AI-L	t _{PLL}	0.093
С	A2–Z	t _{PHH}	0.083
O	MZ-Z	t _{PLL}	0.104
	B1–Z	t _{PHH}	0.124
	DI-Z	t _{PLL}	0.111

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.

CMOS 7RF (CMRF7SF) 1.8 V (12-Track) Standard Cell Databook



Table 3-4. Cell AO22_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process $(ns)^1$ V_{DD} 1.8 V T_j 25°C
С	D0. 7	t _{PHH}	0.116
C	B2–Z	t _{PLL}	0.120
	A4. 7	t _{PHH}	0.083
D	A1–Z	t _{PLL}	0.092
	40.7	t _{PHH}	0.078
	A2–Z	t _{PLL}	0.103
	D4 7	t _{PHH}	0.117
	B1–Z	t _{PLL}	0.108
	Do 7	t _{PHH}	0.110
	B2–Z	t _{PLL}	0.118
	A4.7	t _{PHH}	0.082
	A1–Z	t _{PLL}	0.092
	AO 7	t _{PHH}	0.077
F	A2–Z	t _{PLL}	0.103
E	D4 7	t _{PHH}	0.115
	B1–Z	t _{PLL}	0.108
	D0. 7	t _{PHH}	0.107
	B2–Z	t _{PLL}	0.118
	A1–Z	t _{PHH}	0.091
	AI-Z	t _{PLL}	0.104
	40.7	t _{PHH}	0.084
F	A2–Z	t _{PLL}	0.115
Г	B1–Z	t _{PHH}	0.117
	DI-Z	t _{PLL}	0.115
	B2–Z	t _{PHH}	0.109
	D2-Z	t _{PLL}	0.126
	A4.7	t _{PHH}	0.096
	A1–Z	t _{PLL}	0.105
	A0. 7	t _{PHH}	0.088
П	A2–Z	t _{PLL}	0.114
Н	D1 7	t _{PHH}	0.125
	B1–Z	t _{PLL}	0.117
	D0. 7	t _{PHH}	0.116
	B2–Z	t _{PLL}	0.126



Table 3-4. Cell AO22_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process $(ns)^1$ V_{DD} 1.8 V T_j 25°C
	A1–Z	t _{PHH}	0.093
	AI-Z	t _{PLL}	0.110
	A2–Z	t _{PHH}	0.087
I	AZ-Z	t _{PLL}	0.120
	B1–Z	t _{PHH}	0.118
	DI-Z	t _{PLL}	0.119
	B2–Z	t _{PHH}	0.109
	D2-Z	t _{PLL}	0.129
	A1–Z	t _{PHH}	0.098
	A1-Z	t _{PLL}	0.105
	A2–Z	t _{PHH}	0.091
J	AZ-Z	t _{PLL}	0.114
J	B1–Z	t _{PHH}	0.127
	D1-Z	t _{PLL}	0.116
	B2–Z	t _{PHH}	0.118
	DZ-Z	t _{PLL}	0.124
	A1–Z	t _{PHH}	0.103
	AI-Z	t _{PLL}	0.115
	A2–Z	t _{PHH}	0.096
К	MZ-Z	t _{PLL}	0.124
r\	B1–Z	t _{PHH}	0.131
	DI-Z	t _{PLL}	0.125
	B2–Z	t _{PHH}	0.122
	טב–2	t _{PLL}	0.132

3.2.4 Cell Specifications

Table 3-5. Cell AO22_{PL} Capacitance

Input /	Capacitance (fF) by Performance Level									
Output Pins	В	С	D	E	F	Н	I	J	K	
A1	4.5	8.4	9.1	9.5	8.8	9.6	15.2	18.0	17.9	
A2	3.9	7.8	8.6	8.9	8.1	9.0	14.9	17.6	17.6	
B1	4.3	7.9	8.6	9.0	8.3	9.1	14.7	17.3	17.3	
B2	4.1	7.6	8.3	8.6	8.1	8.9	14.3	16.9	17.0	
Z	54.5	114.1	177.7	236.9	392.1	553.4	780.5	1058.9	1407.4	



Table 3-6. Cell AO22_{PL} Area

	Cell Dimensions (μm)			
Performance Level	Width	Length		
В				
С				
D	4.48			
E	4.40			
F		6.72		
Н				
I				
J	8.40			
К				



3.3 AO33_{PL} Cell

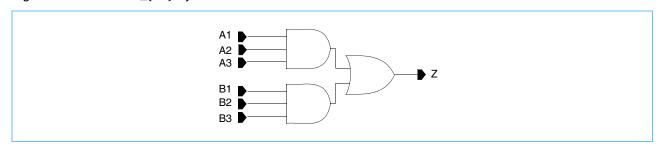
3.3.1 Function

 3×3 AND OR

3.3.2 Description

This cell is a combinational gate, 3×3 AND OR. The Boolean expression for this cell is $Z = (A1 \times A2 \times A3) + (B1 \times B2 \times B3)$.

Figure 3-3. Cell AO33_{PL} Symbols



3.3.3 Propagation Delay Table

Table 3-7. Cell AO33_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A1 7	t _{PHH}	0.157
	A1–Z	t _{PLL}	0.169
	A2-Z	t _{РНН}	0.152
	AZ-Z	t _{PLL}	0.176
	A3-Z	t _{PHH}	0.142
С		t _{PLL}	0.184
C	B1-Z	t _{РНН}	0.171
		t _{PLL}	0.171
	D0 7	t _{РНН}	0.167
_	B2-Z	t _{PLL}	0.179
	Do 7	t _{PHH}	0.156
	B3-Z	t _{PLL}	0.187

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 3-7. Cell AO33_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ $V_{DD} \qquad 1.8 \text{ V}$ $T_{j} \qquad 25^{\circ}\text{C}$
	A1–Z	t _{PHH}	0.165
	AI-Z	t _{PLL}	0.164
	A2–Z	t _{PHH}	0.159
	AZ-Z	t _{PLL}	0.170
	A3–Z	t _{PHH}	0.150
E	A3-Z	t _{PLL}	0.177
E	B1–Z	t _{PHH}	0.179
	81–2	t _{PLL}	0.167
	DO 7	t _{PHH}	0.175
	B2-Z	t _{PLL}	0.175
	B3-Z	t _{PHH}	0.163
		t _{PLL}	0.182
	A1–Z	t _{PHH}	0.143
		t _{PLL}	0.147
	A2–Z	t _{PHH}	0.138
		t _{PLL}	0.156
	A3–Z	t _{PHH}	0.131
н	A3-Z	t _{PLL}	0.163
П	D4 7	t _{PHH}	0.154
	B1–Z	t _{PLL}	0.151
	D0 7	t _{PHH}	0.149
	B2-Z	t _{PLL}	0.160
		t _{PHH}	0.140
	B3–Z	t _{PLL}	0.168

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



3.3.4 Cell Specifications

Table 3-8. Cell AO33_{PL} Capacitance

	Capacitance (fF) by Performance Level			
Input / Output Pins	С	Е	Н	
A1	2.7	3.0	4.8	
A2	2.3	2.7	4.5	
A3	2.4	2.8	4.5	
B1	2.6	3.0	4.7	
B2	2.3	2.7	4.6	
B3	2.4	2.8	4.5	
Z	111.7	239.8	497.2	

Table 3-9. Cell AO33_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
С			
E	8.96	6.72	
Н			



3.4 AO44_{PL} Cell

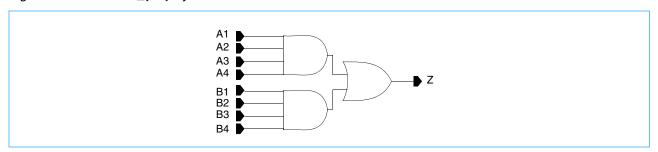
3.4.1 Function

 4×4 AND OR

3.4.2 Description

This cell is a combinational gate, 4×4 AND OR. The Boolean expression for this cell is $Z = (A1 \times A2 \times A3 \times A4) + (B1 \times B2 \times B3 \times B4)$.

Figure 3-4. Cell AO44_{PL} Symbols



3.4.3 Propagation Delay Table

Table 3-10. Cell AO44_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process $(ns)^1$ V_{DD} 1.8 V T_j 25°C
	A1–Z	t _{PHH}	0.194
	A1-Z	t _{PLL}	0.181
	A2–Z	t _{PHH}	0.194
	MZ-Z	t _{PLL}	0.190
	A3–Z	t _{PHH}	0.190
	A3-Z	t _{PLL}	0.197
С	A4–Z	t _{PHH}	0.184
O		t _{PLL}	0.204
	B1–Z	t _{PHH}	0.212
	DI-Z	t _{PLL}	0.184
	B2–Z	t _{PHH}	0.211
_	D2-L	t _{PLL}	0.192
	B3–Z	t _{PHH}	0.207
	D)-Z	t _{PLL}	0.199

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 3-10. Cell AO44_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process $(ns)^1$ V_{DD} 1.8 V T_j 25°C
С	B4–Z	t _{PHH}	0.201
C	D4-Z	t _{PLL}	0.207
	A4. 7	t _{PHH}	0.197
	A1–Z	t _{PLL}	0.189
	40.7	t _{PHH}	0.196
	A2–Z	t _{PLL}	0.197
	40.7	t _{PHH}	0.193
	A3–Z	t _{PLL}	0.205
		t _{PHH}	0.187
_	A4–Z	t _{PLL}	0.213
E	D4 7	t _{PHH}	0.213
	B1–Z	t _{PLL}	0.194
	D0. 7	t _{PHH}	0.213
	B2–Z	t _{PLL}	0.203
	Do 7	t _{PHH}	0.209
	B3-Z	t _{PLL}	0.210
	D4 7	t _{PHH}	0.204
	B4-Z	t _{PLL}	0.218
	A1–Z	t _{PHH}	0.162
		t _{PLL}	0.168
	A2-Z	t _{PHH}	0.162
		t _{PLL}	0.178
		t _{PHH}	0.159
	A3–Z	t _{PLL}	0.187
	A 4 7	t _{PHH}	0.156
	A4–Z	t _{PLL}	0.195
Н	D4 7	t _{PHH}	0.175
	B1–Z	t _{PLL}	0.172
	DO 7	t _{PHH}	0.175
	B2–Z	t _{PLL}	0.182
	D0. 7	t _{PHH}	0.172
	B3–Z	t _{PLL}	0.190
		t _{PHH}	0.168
	B4–Z	t _{PLL}	0.199

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



3.4.4 Cell Specifications

Table 3-11. Cell AO44_{PL} Capacitance

	Capacitance (fF) by Performance Level		
Input / Output Pins	С	Е	Н
A1	2.6	2.8	4.3
A2	2.6	2.8	4.3
A3	2.5	2.8	4.2
A4	2.4	2.7	4.1
B1	2.6	2.8	4.3
B2	2.6	2.8	4.3
B3	2.5	2.7	4.2
B4	2.4	2.6	4.1
Z	115.3	255.2	521.2

Table 3-12. Cell AO44_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
С			
Е	9.52	6.72	
Н			

3.5 AO222_{PL} Cell

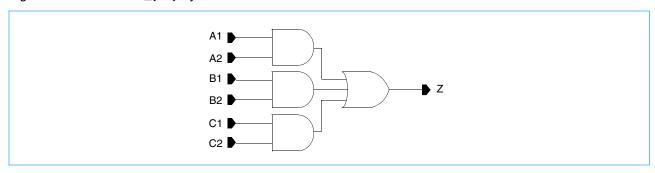
3.5.1 Function

 $2 \times 2 \times 2$ AND OR

3.5.2 Description

This cell is a combinational gate, $2 \times 2 \times 2$ AND OR. The Boolean expression for this cell is $Z = (A1 \times A2) + (B1 \times B2) + (C1 \times C2)$.

Figure 3-5. Cell AO222_{PL} Symbols



3.5.3 Propagation Delay Table

Table 3-13. Cell AO222_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	$\begin{array}{cc} \text{Nominal Process (ns)}^1 \\ \text{V}_{\text{DD}} & \text{1.8 V} \\ \text{T}_{j} & \text{25}^{\circ}\text{C} \end{array}$
	A	t _{PHH}	0.121
	A1–Z	t _{PLL}	0.132
	A2–Z	t _{PHH}	0.112
	A2-Z	t _{PLL}	0.142
	B1–Z	t _{PHH}	0.112
В		t _{PLL}	0.110
Ь	D0. 7	t _{PHH}	0.106
	B2–Z	t _{PLL}	0.122
	C1–Z	t _{PHH}	0.146
	01-2	t _{PLL}	0.128
	C2. 7	t _{PHH}	0.138
	C2–Z	t _{PLL}	0.137



Table 3-13. Cell AO222_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
		t _{PHH}	0.115
	A1–Z	t _{PLL}	0.126
	40.7	t _{PHH}	0.104
	A2–Z	t _{PLL}	0.135
	D4 7	t _{PHH}	0.093
•	B1–Z	t _{PLL}	0.099
С	D0. 7	t _{PHH}	0.089
	B2–Z	t _{PLL}	0.111
	04.7	t _{PHH}	0.125
	C1–Z	t _{PLL}	0.115
	00.7	t _{PHH}	0.118
	C2–Z	t _{PLL}	0.125
	A4 7	t _{PHH}	0.113
	A1–Z	t _{PLL}	0.121
	A2–Z	t _{PHH}	0.103
		t _{PLL}	0.130
	B1–Z	t _{PHH}	0.093
D		t _{PLL}	0.100
U	B2-Z	t _{PHH}	0.089
		t _{PLL}	0.112
	04.7	t _{PHH}	0.125
	C1–Z	t _{PLL}	0.115
	C2–Z	t _{PHH}	0.117
	02–2	t _{PLL}	0.125
	A1–Z	t _{PHH}	0.122
	M1-Z	t _{PLL}	0.130
	AQ 7	t _{PHH}	0.111
_	A2–Z	t _{PLL}	0.138
E	B1–Z	t _{PHH}	0.097
	DI-Z	t _{PLL}	0.100
	B2–Z	t _{PHH}	0.092
	D2-L	t _{PLL}	0.111

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 3-13. Cell AO222_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process $(ns)^1$ V_{DD} 1.8 V T_j 25°C
	C1–Z	t _{PHH}	0.129
E	CI-Z	t _{PLL}	0.115
E	C2-Z	t _{PHH}	0.121
	02-2	t _{PLL}	0.124
	A1–Z	t _{PHH}	0.163
	A1-Z	t _{PLL}	0.156
	A2-Z	t _{PHH}	0.150
	AZ-Z	t _{PLL}	0.162
	B1–Z	t _{PHH}	0.100
F	DI-Z	t _{PLL}	0.104
ŗ	B2-Z	t _{PHH}	0.093
		t _{PLL}	0.114
	C1-Z - C2-Z -	t _{PHH}	0.131
		t _{PLL}	0.117
		t _{PHH}	0.122
	02-2	t _{PLL}	0.126
	A1–Z	t _{PHH}	0.174
	A1-Z	t _{PLL}	0.168
	A2-Z	t _{PHH}	0.161
	AZ-Z	t _{PLL}	0.174
	B1–Z	t _{PHH}	0.104
Н	DI-Z	t _{PLL}	0.110
11	B2-Z	t _{PHH}	0.097
	DZ-Z	t _{PLL}	0.120
	C1–Z	t _{PHH}	0.134
	-	t _{PLL}	0.122
	C2-Z	t _{PHH}	0.125
	U2-L	t _{PLL}	0.131

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



3.5.4 Cell Specifications

Table 3-14. Cell AO222_{PL} Capacitance

Input /	Capacitance (fF) by Performance Level						
Input / Output Pins	В	С	D	E	F	Н	
A1	2.9	3.4	3.5	3.5	3.8	3.8	
A2	2.7	3.2	3.7	3.7	3.5	3.5	
B1	6.0	8.9	9.1	9.3	9.5	9.5	
B2	5.8	8.6	8.8	9.0	9.2	9.2	
C1	5.8	8.6	8.8	9.3	9.2	9.2	
C2	5.8	8.4	8.6	8.8	9.1	9.1	
Z	58.5	121.6	188.2	252.6	376.9	471.3	

Table 3-15. Cell AO222_{PL} Area

	Cell Dimensions (μm)				
Performance Level	Width	Length			
В					
С	6.72				
D	6.72			6.70	
E		6.72			
F	7.00				
Н	7.28				

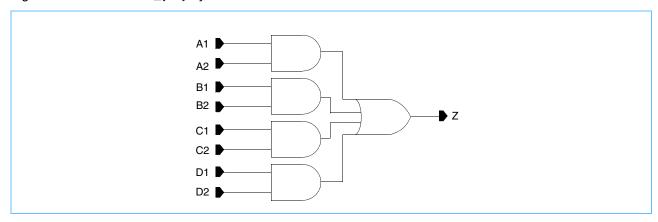
3.6 AO2222_{PL} Cell

3.6.1 Function

 $2 \times 2 \times 2 \times 2$ AND OR

3.6.2 Description

Figure 3-6. Cell AO2222_{PL} Symbols



3.6.3 Propagation Delay Table

Table 3-16. Cell AO2222_{PL} Propagation Delays (Page 1 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V_{DD} 1.8 V T_j 25°C
	A 1 7	t _{PHH}	0.110
	A1–Z	t _{PLL}	0.114
	40.7	t _{PHH}	0.105
	A2–Z	t _{PLL}	0.125
	B1-Z	t _{PHH}	0.144
D		t _{PLL}	0.131
В	D0. 7	t _{PHH}	0.136
	B2–Z	t _{PLL}	0.140
	C1 7	t _{PHH}	0.104
	C1–Z	t _{PLL}	0.114
	00.7	t _{PHH}	0.098
	C2–Z	t _{PLL}	0.125

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 3-16. Cell AO2222_{PL} Propagation Delays (Page 2 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	D. 7	t _{PHH}	0.137
Б	D1–Z	t _{PLL}	0.132
В	D0 7	t _{PHH}	0.128
	D2–Z	t _{PLL}	0.141
	A1–Z	t _{PHH}	0.091
	AI-Z	t _{PLL}	0.101
	A2–Z	tpнн tpнн	0.087
	AZ-Z	t _{PLL}	0.113
	D4 7	t _{PHH}	0.122
С	B1–Z	t _{PLL}	0.115
	D0 7	t _{PHH}	0.115
	B2–Z	t _{PLL}	0.126
	C1–Z	t _{PHH}	0.084
	01–2	t _{PLL}	0.100
	C2–Z	t _{PHH}	0.080
	G2-Z	t _{PLL}	0.112
	D1 7	t _{PHH}	0.115
	D1–Z	t _{PLL}	0.115
	D0. 7	t _{PHH}	0.108
	D2–Z	t _{PLL}	0.125
	A4 7	t _{PHH}	0.093
	A1–Z	t _{PLL}	0.101
	40.7	t _{PHH}	0.088
	A2–Z	t _{PLL}	0.112
	B1–Z	t _{PHH}	0.123
D	DI-Z	t _{PLL}	0.115
D	D0 7		0.116
	B2–Z	t _{PLL}	0.125
	01.7	t _{PHH}	0.085
	C1–Z	t _{PLL}	0.099
	C2 7	t _{PHH}	0.081
	C2–Z	t _{PLL}	0.111

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 3-16. Cell AO2222_{PL} Propagation Delays (Page 3 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	D4 7	t _{PHH}	0.116
	D1–Z	t _{PLL}	0.113
D		t _{PHH}	0.108
	D2–Z	t _{PLL}	0.124
	7	t _{PHH}	0.096
	A1–Z	t _{PLL}	0.101
		t _{PHH}	0.091
	A2–Z	t _{PLL}	0.112
		t _{PHH}	0.127
	B1–Z	t _{PLL}	0.115
		t _{PHH}	0.119
_	B2–Z	t _{PLL}	0.125
E		t _{PHH}	0.088
	C1–Z	t _{PLL}	0.099
		t _{PHH}	0.083
	C2–Z	t _{PLL}	0.110
	- · -	t _{PHH}	0.119
	D1–Z	t _{PLL}	0.113
		t _{PHH}	0.112
	D2–Z	t _{PLL}	0.123
		t _{PHH}	0.099
	A1–Z	t _{PLL}	0.105
		t _{PHH}	0.092
	A2–Z	t _{PLL}	0.115
	D4 7	t _{PHH}	0.129
_	B1–Z	t _{PLL}	0.118
F	D0. 7	t _{PHH}	0.120
	B2–Z	t _{PLL}	0.126
	01.7	t _{PHH}	0.110
	C1–Z	t _{PLL}	0.109
	00.7	t _{PHH}	0.103
	C2–Z	t _{PLL}	0.119

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . \\ Iib\ timing\ files\ for\ more\ information.$



Table 3-16. Cell AO2222_{PL} Propagation Delays (Page 4 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) V _{DD} 1.8 V T _j 25°C	
	D1–Z	t _{PHH}	0.140	
F	DI-Z	t _{PLL}	0.122	
1	D2–Z	t _{PHH}	0.132	
	UZ-Z	t _{PLL}	0.130	
	A1–Z	t _{PHH}	0.103	
	AI-Z	t _{PLL}	0.112	
	A2–Z	t _{PHH}	0.096	
	AL L	t _{PLL}	0.121	
	B1–Z	t _{PHH}	0.132	
	D1-2	t _{PLL}	0.124	
	B2–Z	t _{PHH}	0.123	
Н	D2-Z	t _{PLL}	0.133	
11	C1–Z	t _{PHH}	0.113	
	01-2	t _{PLL}	0.116	
	C2–Z	t _{PHH}	0.106	
	02-2	t _{PLL}	0.125	
	D1–Z	t _{PHH}	0.143	
	D1-2	t _{PLL}	0.128	
	D2–Z	t _{PHH}	0.134	
	<i>DL</i> -L	t _{PLL}	0.136	

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.

3.6.4 Cell Specifications

Table 3-17. Cell AO2222_{PL} Capacitance

Input /	Capacitance ((fF) by Performand	ce Level			
Output Pins	В	С	D	E	F	Н
A1	6.0	9.0	9.1	9.2	9.3	9.2
A2	5.7	8.7	8.8	8.9	9.0	8.9
B1	5.7	8.7	8.8	9.2	9.3	9.3
B2	5.9	8.8	8.9	8.9	8.9	8.9
C1	5.9	9.0	9.1	9.2	9.2	9.2
C2	5.7	8.7	8.8	8.9	9.0	9.0
D1	5.7	8.8	8.8	9.2	9.3	9.2
D2	5.8	8.6	8.7	8.8	8.9	8.9
Z	58.6	121.6	183.7	253.0	380.0	493.4



Table 3-18. Cell AO2222_{PL} Area

	Cell Dimensions (μm)				
Performance Level	Width	Length			
В					
С	7.84 6.	7.04			
D		0.70			
Е		6.72			
F	0.00				
Н	8.96				



3.7 AOI21_{PL} Cell

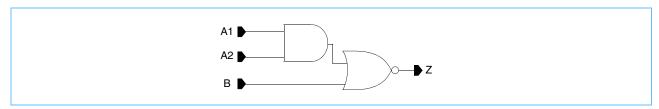
3.7.1 Function

2 × 1 AND OR inverter

3.7.2 Description

This cell is a combinational gate, 2×1 AND OR inverter. The Boolean expression for this cell is $Z = \overline{(A1 \times A2) + B}$.

Figure 3-7. Cell AOI21_{PL} Symbols



3.7.3 Propagation Delay Table

Table 3-19. Cell AOI21_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A1–Z	t _{PLH}	0.114
	AI-Z	t _{PHL}	0.068
٨	40.7	t _{PLH}	0.123
Α	A2–Z	t _{PHL}	0.058
	D 7	t _{PLH}	0.072
	B–Z	t _{PHL}	0.070
	A 1 7	t _{PLH}	0.081
	A1–Z	t _{PHL}	0.068
В	40.7	t _{PLH}	0.090
В	A2–Z	t _{PHL}	0.059
	D 7	t _{PLH}	0.053
	B–Z	t _{PHL}	0.096
Minimum input transition and	d minimum output load. See, lib tim	ning files for more information	

Minimum input transition and minimum output load. See .lib timing files for more information.



Table 3-19. Cell AOI21_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A1–Z	t _{PLH}	0.066
	A1-Z	t _{PHL}	0.054
0	40.7	t _{PLH}	0.077
С	A2–Z	t _{PHL}	0.048
	B–Z	t _{PLH}	0.044
	D-Z	t _{PHL}	0.102
	A1–Z	t _{PLH}	0.068
	A1-Z	t _{PHL}	0.043
D	A2–Z	t _{PLH}	0.081
U	AZ-Z	t _{PHL}	0.040
	B-Z	t _{PLH}	0.069
		t _{PHL}	0.074
E	A1–Z	t _{PLH}	0.066
	A1-Z	t _{PHL}	0.040
	A2–Z	t _{PLH}	0.080
	MZ-Z	t _{PHL}	0.037
	B-Z	t _{PLH}	0.067
		t _{PHL}	0.069
	A1–Z	t _{PLH}	0.063
	MI-L	t _{PHL}	0.039
F	A2–Z	t _{PLH}	0.077
'	<i>∩∟</i> −∠	t _{PHL}	0.037
	B–Z	t _{PLH}	0.064
	υ-Δ	t _{PHL}	0.069
	A1–Z	t _{PLH}	0.065
	Λ1 ⁻ Δ	t _{PHL}	0.038
Н	A2–Z	t _{PLH}	0.079
11	M2-L	t _{PHL}	0.036
	B–Z	t _{PLH}	0.065
	D-Z	t _{PHL}	0.063

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



3.7.4 Cell Specifications

Table 3-20. Cell AOI21_{PL} Capacitance

Input /	Capacitance (fF) by Performance Level						
Output Pins	Α	В	С	D	E	F	Н
A1	2.8	4.1	7.2	11.8	15.1	24.3	34.2
A2	2.6	3.8	6.9	11.3	14.8	24.0	34.6
В	4.5	6.5	11.2	11.2	14.2	20.6	30.8
Z	31.9	61.9	128.3	191.8	251.4	417.4	580.3

Table 3-21. Cell AOI21_{PL} Area

	Cell Dimensions (μm)			
Performance Level	Width	Length		
Α				
В	2.80			
С				
D		6.72		
Е	3.92			
F	6.16			
Н	8.96			



3.8 AOI22_{PL} Cell

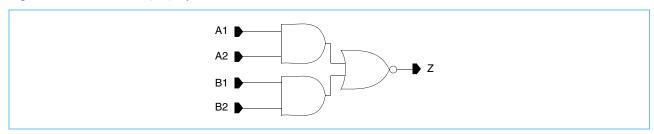
3.8.1 Function

2 × 2 AND OR inverter

3.8.2 Description

This cell is a combinational gate, 2×2 AND OR inverter. The Boolean expression for this cell is $Z = \overline{(A1 \times A2) + (B1 \times B2)}$.

Figure 3-8. Cell AOI22_{PL} Symbols



3.8.3 Propagation Delay Table

Table 3-22. Cell AOI22_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process $(ns)^1$ V_{DD} 1.8 V T_j 25°C
	A4 7	t _{PLH}	0.100
	A1–Z	t _{PHL}	0.076
	A2–Z	t _{PLH}	0.108
۸	AZ-Z	t _{PHL}	0.066
А	D4 7	t _{PLH}	0.114
	B1–Z	t _{PHL}	0.104
	B2-Z	t _{PLH}	0.122
		t _{PHL}	0.092
	A1–Z	t _{PLH}	0.075
		t _{PHL}	0.057
	A2-Z	t _{PLH}	0.085
В		t _{PHL}	0.050
D	B1–Z	t _{PLH}	0.089
	DI-Z	t _{PHL}	0.087
	D0. 7	t _{PLH}	0.099
	B2–Z	t _{PHL}	0.077

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 3-22. Cell AOI22_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A4 7	t _{PLH}	0.062
	A1–Z	t _{PHL}	0.045
	40.7	t _{PLH}	0.074
0	A2–Z	t _{PHL}	0.041
C	D4 7	t _{PLH}	0.076
	B1–Z	t _{PHL}	0.075
	B2–Z	t _{PLH}	0.086
	D2-Z	t _{PHL}	0.068
	A4 7	t _{PLH}	0.062
	A1–Z	t _{PHL}	0.049
	A2-Z	t _{PLH}	0.073
D	AZ-Z	t _{PHL}	0.044
D	B1–Z	t _{PLH}	0.076
	DI-Z	t _{PHL}	0.081
	B2-Z	t _{PLH}	0.085
		t _{PHL}	0.073
	A1–Z	t _{PLH}	0.059
		t _{PHL}	0.046
	A2–Z	t _{PLH}	0.070
E		t _{PHL}	0.042
_	B1–Z	t _{PLH}	0.073
	D1-2	t _{PHL}	0.079
	B2-Z	t _{PLH}	0.082
	DE Z	t _{PHL}	0.071
	A1–Z	t _{PLH}	0.055
	Α1. Έ	t _{PHL}	0.047
	A2-Z	t _{PLH}	0.066
F	<u> Λ</u> 2−2	t _{PHL}	0.043
l l	B1–Z	t _{PLH}	0.071
	υ i – Δ	t _{PHL}	0.081
	B2-Z	t _{PLH}	0.080
	UZ-Z	t _{PHL}	0.073

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . lib\ timing\ files\ for\ more\ information.$



Table 3-22. Cell AOI22_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	$\begin{array}{cc} \text{Nominal Process (ns)}^1 \\ \text{V}_{\text{DD}} & \text{1.8 V} \\ \text{T}_{j} & \text{25}^{\circ}\text{C} \end{array}$
	A1–Z	t _{PLH}	0.054
	AI-Z	t _{PHL}	0.048
	A2-Z	t _{PLH}	0.064
ш		t _{PHL}	0.043
Н	B1-Z B2-Z	t _{PLH}	0.070
		t _{PHL}	0.084
		t _{PLH}	0.078
		t _{PHL}	0.076

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.

3.8.4 Cell Specifications

Table 3-23. Cell AOI22_{PL} Capacitance

Input /	Capacitance (fF) by Performance Level						
Output Pins	A	В	С	D	Е	F	Н
A1	3.0	4.7	8.4	12.4	16.4	23.7	31.5
A2	2.6	4.4	8.0	12.6	16.4	23.9	31.7
B1	3.1	4.8	8.2	12.2	16.2	23.7	30.9
B2	3.2	4.7	8.2	12.2	16.1	23.6	31.0
Z	46.1	90.4	181.1	277.9	380.2	554.4	735.4

Table 3-24. Cell AOI22_{PL} Area

	Cell Dimensions (μm)			
Performance Level	Width	Length		
А				
В	3.36			
С				
D	6.16	6.72		
E	6.16			
F	8.96			
Н	11.20			



3.9 AOI33_{PL} Cell

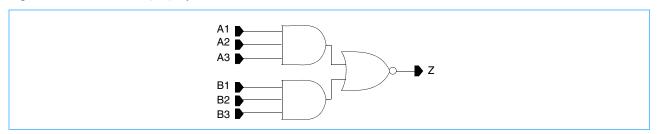
3.9.1 Function

3 × 3 AND OR inverter

3.9.2 Description

This cell is a combinational gate, 3×3 AND OR inverter. The Boolean expression for this cell is $Z = \overline{(A1 \times A2 \times A3) + (B1 \times B2 \times B3)}$.

Figure 3-9. Cell AOI33_{PL} Symbols



3.9.3 Propagation Delay Table

Table 3-25. Cell AOI33_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A1–Z	t _{PLH}	0.212
	AI-Z	t _{PHL}	0.190
	A2-Z	t _{PLH}	0.220
	AZ-Z	t _{PHL}	0.185
	A3-Z	t _{PLH}	0.229
С		t _{PHL}	0.176
C	B1-Z	t _{PLH}	0.231
		t _{PHL}	0.199
	B2-Z	t _{PLH}	0.239
		t _{PHL}	0.194
	B3-Z	t _{PLH}	0.248
	DJ-Z	t _{PHL}	0.184

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . lib\ timing\ files\ for\ more\ information.$



Table 3-25. Cell AOI33_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A1–Z	t _{PLH}	0.193
	A1-Z	t _{PHL}	0.184
	A2–Z	t _{PLH}	0.201
	MZ-Z	t _{PHL}	0.179
	A3–Z	t _{PLH}	0.210
E	AJ-Z	t _{PHL}	0.171
<u> </u>	B1–Z	t _{PLH}	0.207
	DI-Z	t _{PHL}	0.190
	B2–Z	t _{PLH}	0.214
	D2-Z	t _{PHL}	0.186
	B3-Z	t _{PLH}	0.223
		t _{PHL}	0.176
	A1–Z	t _{PLH}	0.163
		t _{PHL}	0.160
	A2-Z	t _{PLH}	0.173
		t _{PHL}	0.158
	A3–Z	t _{PLH}	0.183
н	A3-Z	t _{PHL}	0.152
П	B1–Z	t _{PLH}	0.169
	DI-Z	t _{PHL}	0.159
	B2–Z	t _{PLH}	0.180
	D2-L	t _{PHL}	0.156
	B3–Z	t _{PLH}	0.189
	D)-L	t _{PHL}	0.150

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



3.9.4 Cell Specifications

Table 3-26. Cell AOI33_{PL} Capacitance

	Capacitance (fF) by Performance Level			
Input / Output Pins	С	Е	Н	
A1	2.7	3.1	4.8	
A2	2.6	3.0	4.7	
A3	2.4	2.8	4.5	
B1	2.7	3.0	4.8	
B2	2.5	2.9	4.6	
B3	2.4	2.8	4.4	
Z	116.5	245.7	450.2	

Table 3-27. Cell AOI33_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
С			
E	9.52	6.72	
Н			



3.10 AOI44_{PL} Cell

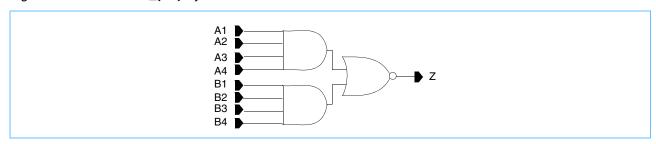
3.10.1 Function

4 × 4 AND OR inverter

3.10.2 Description

This cell is a combinational gate, 4×4 AND OR inverter. The Boolean expression for this cell is $Z = \overline{(A1 \times A2 \times A3 \times A4) + (B1 \times B2 \times B3 \times B4)}$.

Figure 3-10. Cell AOI44_{PL} Symbols



3.10.3 Propagation Delay Table

Table 3-28. Cell AOI44_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A1–Z	t _{PLH}	0.212
	A1-Z	t _{PHL}	0.200
	A2–Z	t _{PLH}	0.222
	MZ-Z	t _{PHL}	0.200
	A3–Z	t _{PLH}	0.231
	AJ-Z	t _{PHL}	0.198
	A4-Z	t _{PLH}	0.239
С		t _{PHL}	0.193
C	B1-Z B2-Z	t _{PLH}	0.221
		t _{PHL}	0.224
		t _{PLH}	0.231
	D2-Z	t _{PHL}	0.223
	B3–Z	t _{PLH}	0.240
	D3-Z	t _{PHL}	0.221
	B4–Z	t _{PLH}	0.249
	D4-Z	t _{PHL}	0.217

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 3-28. Cell AOI44_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V_{DD} 1.8 V T_j 25°C
	A4.7	t _{PLH}	0.206
	A1–Z	t _{PHL}	0.191
	40.7	t _{PLH}	0.217
	A2–Z	t _{PHL}	0.192
	A3–Z	t _{PLH}	0.227
	A3-Z	t _{PHL}	0.190
	A4–Z	t _{PLH}	0.235
E	A4-Z	t _{PHL}	0.186
E	D4 7	t _{PLH}	0.212
	B1–Z	t _{PHL}	0.208
	B2–Z	t _{PLH}	0.223
	D2-Z	t _{PHL}	0.209
	D0. 7	t _{PLH}	0.232
	B3-Z	t _{PHL}	0.207
	B4–Z	t _{PLH}	0.242
		t _{PHL}	0.204
	A1–Z	t _{PLH}	0.176
		t _{PHL}	0.166
	40.7	t _{PLH}	0.189
	A2–Z	t _{PHL}	0.168
	A3–Z	t _{PLH}	0.200
	A3-Z	t _{PHL}	0.168
	A4–Z	t _{PLH}	0.210
Н	A4- 2	t _{PHL}	0.166
П	B1–Z	t _{PLH}	0.181
	טו–∠	t _{PHL}	0.180
	P2 7	t _{PLH}	0.194
	B2–Z	t _{PHL}	0.183
	P2 7	t _{PLH}	0.205
	B3–Z	t _{PHL}	0.183
	P4 7	t _{PLH}	0.215
B4–Z	D 4 -L	t _{PHL}	0.181

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



3.10.4 Cell Specifications

Table 3-29. Cell AOI44_{PL} Capacitance

	Capacitance (fF) by Performance Level		
Input / Output Pins	С	Е	Н
A1	2.6	2.9	4.6
A2	2.5	2.7	4.3
A3	2.4	2.7	4.2
A4	2.2	2.5	4.1
B1	2.6	2.8	4.5
B2	2.4	2.7	4.3
В3	2.3	2.6	4.1
B4	2.3	2.6	4.1
Z	121.1	245.3	469.1

Table 3-30. Cell AOI44_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
С			
E	10.64	6.72	
Н			



3.11 AOI222_{PL} Cell

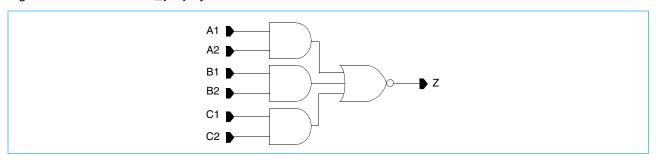
3.11.1 Function

 $2 \times 2 \times 2$ AND OR inverter

3.11.2 Description

This cell is a combinational gate, $2 \times 2 \times 2$ AND OR inverter. The Boolean expression for this cell is $Z = \overline{(A1 \times A2) + (B1 \times B2) + (C1 \times C2)}$.

Figure 3-11. Cell AOI222_{PL} Symbols



3.11.3 Propagation Delay Table

Table 3-31. Cell AOI222_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A 1 7	t _{PLH}	0.138
	A1–Z	t _{PHL}	0.179
	40.7	t _{PLH}	0.144
	A2–Z	t _{PHL}	0.167
	D4 7	t _{PLH}	0.140
F	B1–Z	t _{PHL}	0.163
Г	D0. 7	t _{PLH}	0.148
	B2–Z	t _{PHL}	0.155
	C1–Z	t _{PLH}	0.159
	Ο1 - Ζ	t _{PHL}	0.210
	C2 7	t _{PLH}	0.166
	C2–Z	t _{PHL}	0.201

1. Minimum input transition and minimum output load. See .lib timing files for more information.



Table 3-31. Cell AOI222_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	۸1 7	t _{PLH}	0.139
	AI-Z	t _{PHL}	0.168
	40.7	t _{PLH}	0.147
	AZ-Z	t _{PHL}	0.157
	D1 7	t _{PLH}	0.135
н	D1-Z	t _{PHL}	0.156
П	P0 7	t _{PLH}	0.145
	D2-L	t _{PHL}	0.151
	C1 7	t _{PLH}	0.150
	01–2	t _{PHL}	0.190
	C0. 7	t _{PLH}	0.159
	02–2	t _{PHL}	0.182
	۸1 7	t _{PLH}	0.145
	AI-Z	t _{PHL}	0.159
	40.7	t _{PLH}	0.153
	AZ-Z	t _{PHL}	0.150
	D4 7	A1-Z tpHL tpLH tpLH tpHL tpHL	0.141
	DI-Z		0.152
I	P2 7		0.152
	D2-L	t _{PHL}	0.147
	C1 7	t _{PLH}	0.156
	U1-Z	t _{PHL}	0.184
	C0. 7	t _{PLH}	0.166
	U2-Z	tpHL tpHH tpHL tpHH tpHL tpHH tpHH tpHH	0.176

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



3.11.4 Cell Specifications

Table 3-32. Cell AOI222_{PL} Capacitance

	Capacitance (fF) by Performance Level		
Input / Output Pins	F	Н	I
A1	4.8	4.7	5.1
A2	4.3	4.3	4.6
B1	8.3	9.1	9.2
B2	8.0	8.7	8.8
C1	7.9	8.8	8.9
C2	8.2	8.9	9.0
Z	389.7	502.7	716.2

Table 3-33. Cell AOI222_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
F			
Н	7.84	6.72	
I			

3.12 AOI2222_{PL} Cell

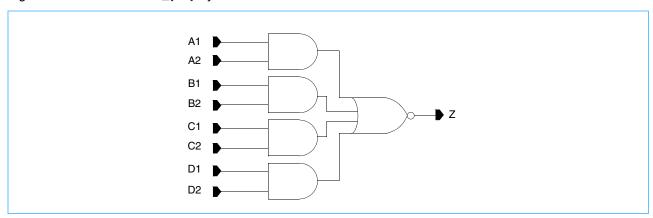
3.12.1 Function

 $2 \times 2 \times 2 \times 2$ AND OR inverter

3.12.2 Description

This cell is a combinational gate, $2 \times 2 \times 2 \times 2$ AND OR inverter. The Boolean expression for this cell is $Z = \overline{(A1 \times A2) + (B1 \times B2) + (C1 \times C2) + (D1 \times D2)}$.

Figure 3-12. Cell AOI2222_{PL} Symbols



3.12.3 Propagation Delay Table

Table 3-34. Cell AOI2222_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process $(ns)^1$ V_{DD} 1.8 V T_j 25°C
	A1 7	t _{PLH}	0.140
	A1–Z	t _{PHL}	0.165
	AQ 7	t _{PLH}	0.148
	A2–Z	t _{PHL}	0.157
	D4 7	t _{PLH}	0.160
F	B1–Z	t _{PHL}	0.212
F	D0. 7	t _{PLH}	0.166
	B2–Z	t _{PHL}	0.202
	C1 7	t _{PLH}	0.136
	C1–Z	t _{PHL}	0.153
	CO 7	t _{PLH}	0.144
	C2–Z	t _{PHL}	0.145

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . lib\ timing\ files\ for\ more\ information.$

CMOS 7RF (CMRF7SF) 1.8 V (12-Track) Standard Cell Databook



Table 3-34. Cell AOI2222_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) V _{DD} 1.8 V T _j 25°C
	D1–Z	t _{PLH}	0.158
F	DI-Z	t _{PHL}	0.200
F	D2–Z	t _{PLH}	0.164
	D2-Z	t _{PHL}	0.191
	۸1 7	t _{PLH}	0.135
	A1–Z	t _{PHL}	0.158
	A2–Z	t _{PLH}	0.146
	MZ-Z	t _{PHL}	0.153
	D4 7	t _{PLH}	0.151
	B1–Z	t _{PHL}	0.191
	B2–Z	t _{PLH}	0.160
	DZ-Z	t _{PHL}	0.183
Н	C1–Z	t _{PLH}	0.131
	01-2	t _{PHL}	0.143
	C0. 7	t _{PLH}	0.142
	C2–Z	t _{PHL}	0.138
	D1–Z	t _{PLH}	0.148
	DI-Z	t _{PHL}	0.177
	D0. 7	t _{PLH}	0.157
	D2–Z	t _{PHL}	0.169
	A1–Z	t _{PLH}	0.142
	A1-Z	t _{PHL}	0.153
	A2–Z	t _{PLH}	0.152
	MZ-Z	t _{PHL}	0.148
	B1–Z	t _{PLH}	0.157
I	DI-Z	t _{PHL}	0.185
ı	B2–Z	t _{PLH}	0.166
	DZ-Z	t _{PHL}	0.177
	C1–Z	t _{PLH}	0.138
	Ο1-Z	t _{PHL}	0.140
	C2-Z	t _{PLH}	0.149
	<i>0L-L</i>	t _{PHL}	0.136

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 3-34. Cell AOI2222_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	D1–Z	t _{PLH} 0.155	0.155
1	D1-Z	t _{PHL}	0.173
ı	D2–Z	t _{PLH}	0.165
	U2-Z	t _{PHL}	0.165
Minimum input transition and	d minimum output load. See .lib tin		31,100

3.12.4 Cell Specifications

Table 3-35. Cell AOI2222_{PL} Capacitance

	Capacitance (fF) by Performance Level		
Input / Output Pins	F	Н	I
A1	8.2	9.0	9.2
A2	8.0	8.8	8.9
B1	7.9	8.8	8.9
B2	8.1	8.9	9.0
C1	8.2	9.0	9.2
C2	8.0	8.8	8.9
D1	7.9	8.8	8.9
D2	7.9	8.7	8.8
Z	389.2	501.2	715.7

Table 3-36. Cell AOI2222_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
F			
Н	8.96	6.72	
I			



3.13 OA21_{PL} Cell

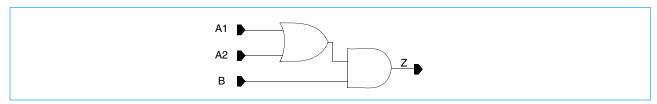
3.13.1 Function

 2×1 OR AND

3.13.2 Description

This cell is a combinational gate, 2×1 OR AND. The Boolean expression for this cell is $Z = (A1 + A2) \times B$.

Figure 3-13. Cell OA21_{PL} Symbols



3.13.3 Propagation Delay Table

Table 3-37. Cell OA21_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A1–Z	tРНН tРLL tРНН tРLL	0.118
	AI-Z	t _{PLL}	0.155
В	A2-Z	t _{PHH}	0.128
В	AZ-Z	t _{PLL}	0.147
	B–Z	t _{PHH}	0.112
	D-Z	t _{PLL}	0.132
	A1–Z		0.114
	AI-L	t _{PLL}	0.157
С	A2–Z	t _{PHH}	0.124
C	AZ-Z	t _{PLL}	0.148
	B–Z	t _{PHH}	0.105
	D- <u>Z</u>	t _{PLL}	0.142
	A1–Z	t _{PHH}	0.125
	AI-Z	t _{PLL}	0.148
D	A2-Z	tрнн tpll tpll tpнн tpнн	0.137
U	M2-L	t _{PLL}	0.140
	B–Z	t _{PHH}	0.114
	υ-ζ	t _{PLL}	0.152

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . lib\ timing\ files\ for\ more\ information.$



Table 3-37. Cell OA21_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A4 7	t _{PHH}	0.135
	A1–Z	t _{PLL}	0.145
E	40.7	t _{PHH}	0.148
	A2–Z	t _{PLL}	0.137
	D 7	t _{PHH}	0.122
	B–Z	t _{PLL}	0.164
	A1–Z	t _{PHH}	0.128
	A1-Z	t _{PLL}	0.139
F	40.7	t _{PHH}	0.142
F	A2–Z	t _{PLL}	0.132
	B–Z	t _{PHH}	0.115
	D-Z	t _{PLL}	0.157
	A1–Z	t _{PHH}	0.120
		t _{PLL}	0.135
н	A2–Z B–Z	t _{PHH}	0.135
''		t _{PLL}	0.128
		t _{PHH}	0.107
		t _{PLL}	0.156
	A1–Z	t _{PHH}	0.115
	7.1 2	t _{PLL}	0.131
I	A2–Z	^t PHH	0.130
•	ne e	t _{PLL}	0.124
	B–Z	t _{PHH}	0.103
	5.2	t _{PLL}	0.152
	A1–Z	t _{РНН}	0.110
	, <u>L</u>	t _{PLL}	0.132
J	A2–Z	t _{PHH}	0.124
Ŭ	, v. Z	t _{PLL}	0.125
	B–Z	t _{РНН}	0.101
	5 2	t _{PLL}	0.157

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 3-37. Cell OA21_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A1–Z	t _{PHH}	0.108
	AI-Z	t _{PLL}	0.129
K	A2-Z	t _{PHH}	0.122
K	AZ-Z	t _{PLL}	0.123
	B-Z	t _{PHH}	0.100
	D-Z	t _{PLL}	0.155

3.13.4 Cell Specifications

Table 3-38. Cell OA21_{PL} Capacitance

Input /	Capacitance (fF) by Performance Level								
Output Pins	В	С	D	E	F	Н	I	J	K
A1	2.9	3.0	3.3	3.6	4.8	6.1	7.8	12.3	15.8
A2	2.7	2.8	3.1	3.4	4.4	5.7	7.3	12.3	15.6
В	3.9	3.9	3.9	4.0	5.0	6.2	7.6	8.9	11.0
Z	54.9	111.4	176.2	245.2	385.8	521.4	704.5	1043.2	1394.0

Table 3-39. Cell OA21_{PL} Area

	Cell Dimer	nsions (μm)
Performance Level	Width	Length
В		
С		
D		
Е	3.92	
F		6.72
Н		
I		
J	0.40	
К	8.40	

3.14 OA22_{PL} Cell

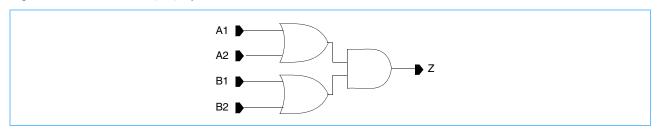
3.14.1 Function

 $2 \times 2 \text{ OR AND}$

3.14.2 Description

This cell is a combinational gate, 2×2 OR AND. The Boolean expression for this cell is $Z = (A1 + A2) \times (B1 + B2)$.

Figure 3-14. Cell OA22_{PL} Symbols



3.14.3 Propagation Delay Table

Table 3-40. Cell OA22_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A1–Z	t _{PHH}	0.128
	AI-Z	t _{PLL}	0.133
	A2-Z	t _{PHH}	0.144
В	AZ-Z	t _{PLL}	0.129
В	B1–Z	t _{PHH}	0.133
	D1-Z	t _{PLL}	0.162
	B2–Z	t _{PHH}	0.145
	DZ-Z	t _{PLL}	0.152
	A1–Z	t _{PHH}	0.114
	A1-2	t _{PLL}	0.132
	A2-Z	t _{PHH}	0.129
С	A2-2	t _{PLL}	0.127
	B1–Z	t _{PHH}	0.116
	טו–ב	t _{PLL}	0.158
	B2-Z	t _{PHH}	0.129
	D2-Z	t _{PLL}	0.149

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 3-40. Cell OA22_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	7	t _{PHH}	0.110
D	A1–Z	t _{PLL}	0.127
		t _{PHH}	0.124
	A2–Z	t _{PLL}	0.122
U	D	t _{PHH}	0.111
	B1–Z	t _{PLL}	0.151
	Do 7	t _{PHH}	0.123
	B2–Z	t _{PLL}	0.142
		t _{PHH}	0.106
	A1–Z	t _{PLL}	0.126
		t _{PHH}	0.120
_	A2–Z	t _{PLL}	0.120
E		t _{PHH}	0.106
	B1–Z	t _{PLL}	0.148
	DO 7	t _{PHH}	0.118
	B2–Z	t _{PLL}	0.140
	A4 7	t _{PHH}	0.101
	A1–Z	t _{PLL}	0.123
	A2-Z	t _{PHH}	0.114
F	AZ-Z	t _{PLL}	0.117
F	B1–Z	t _{PHH}	0.100
	D1-Z	t _{PLL}	0.143
	B2-Z	t _{PHH}	0.111
	DZ-Z	t _{PLL}	0.135
	A1–Z	t _{PHH}	0.096
	Α1. Έ	t _{PLL}	0.119
	A2-Z	t _{PHH}	0.109
н	Λ <u>ζ</u> - <u>ζ</u>	t _{PLL}	0.113
Н	B1–Z	t _{PHH}	0.095
	υ i – Z	t _{PLL}	0.139
	B2-Z	t _{PHH}	0.106
	υz- ∠	t _{PLL}	0.131

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . lib\ timing\ files\ for\ more\ information.$



Table 3-40. Cell OA22_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V_{DD} 1.8 V T_j 25°C
	A1–Z	t _{PHH}	0.107
	A1-Z	t _{PLL}	0.133
	A2–Z	t _{PHH}	0.119
I	AZ-Z	t _{PLL}	0.126
·	B1–Z	t _{PHH}	0.105
	DI-Z	t _{PLL}	0.152
	B2–Z	t _{PHH}	0.116
	D2-L	t _{PLL}	0.143
	A1–Z	t _{PHH}	0.105
		t _{PLL}	0.129
	A2-Z	t _{PHH}	0.119
J	MZ-Z	t _{PLL}	0.122
J	B1–Z	t _{PHH}	0.104
		t _{PLL}	0.149
	B2–Z	t _{PHH}	0.116
	DZ-Z	t _{PLL}	0.140
	A1–Z	t _{PHH}	0.108
	AI-Z	t _{PLL}	0.132
	A2–Z	t _{PHH}	0.121
К	n . L	t _{PLL}	0.125
IX	B1–Z	t _{PHH}	0.106
	D1-2	t _{PLL}	0.151
	B2–Z	t _{PHH}	0.118
	DL L	t _{PLL}	0.144

3.14.4 Cell Specifications

Table 3-41. Cell OA22_{PL} Capacitance

Input /	Capacitance	(fF) by Perfor	mance Level						
Output Pins	В	С	D	E	F	Н	I	J	K
A1	3.2	3.6	4.2	4.8	6.5	8.4	8.4	13.4	16.4
A2	3.5	3.9	4.4	5.0	6.3	8.1	8.1	13.2	16.1
B1	3.6	4.1	4.6	5.2	6.8	8.7	8.7	13.1	16.0
B2	3.1	3.5	4.0	4.5	6.0	7.7	7.7	12.8	15.6
Z	59.1	110.9	167.5	226.4	364.2	485.7	706.2	978.4	1392.0



Table 3-42. Cell OA22_{PL} Area

	Cell Dimer	nsions (μm)
Performance Level	Width	Length
В		
С		
D		
Е	4.48	
F		6.72
Н		
I		
J	10.00	
К	10.08	

3.15 OA222_{PL} Cell

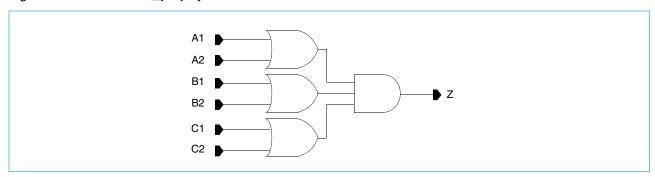
3.15.1 Function

 $2 \times 2 \times 2$ OR AND

3.15.2 Description

This cell is a combinational gate, $2 \times 2 \times 2$ OR AND. The Boolean expression for this cell is $Z = (A1 + A2) \times (B1 + B2) \times (C1 + C2)$.

Figure 3-15. Cell OA222_{PL} Symbols



3.15.3 Propagation Delay Table

Table 3-43. Cell OA222_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A4 7	t _{PHH}	0.106
	A1–Z	t _{PLL}	0.175
	40.7	t _{PHH}	0.113
	A2–Z	t _{PLL}	0.166
	B1–Z	t _{PHH}	0.132
В		t _{PLL}	0.180
В	D0. 7	t _{PHH}	0.144
	B2–Z	t _{PLL}	0.173
	04.7	t _{PHH}	0.139
	C1–Z	t _{PLL}	0.218
	00.7	t _{PHH}	0.146
	C2–Z	t _{PLL}	0.206

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 3-43. Cell OA222_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	7	t _{PHH}	0.115
	A1–Z	t _{PLL}	0.178
	40.7	t _{PHH}	0.122
	A2–Z	t _{PLL}	0.169
	D	t _{PHH}	0.141
_	B1–Z	t _{PLL}	0.176
C	B2-Z	t _{PHH}	0.154
	B2-Z	t _{PLL}	0.170
	04.7	t _{PHH}	0.144
	C1–Z	t _{PLL}	0.204
	00.7	t _{PHH}	0.153
	C2–Z	t _{PLL}	0.194
	A1–Z	t _{PHH}	0.119
	AI-Z	t _{PLL}	0.156
	A2-Z	t _{PHH}	0.130
	A2-L	t _{PLL}	0.149
	B1-Z	t _{PHH}	0.150
D		t _{PLL}	0.154
U	B2-Z	t _{PHH}	0.167
	DZ-Z	t _{PLL}	0.148
	C1–Z	t _{PHH}	0.150
	01-2	t _{PLL}	0.173
	C2–Z	t _{PHH}	0.162
	02-2	t _{PLL}	0.164
	A1–Z	t _{PHH}	0.115
	A1-2	t _{PLL}	0.153
	A2-Z	t _{PHH}	0.127
E	Λ <u>ζ</u> - <u>ζ</u>	t _{PLL}	0.147
E	D4.7	t _{PHH}	0.144
	B1–Z	t _{PLL}	0.151
	B2-Z	t _{PHH}	0.159
	D2-L	t _{PLL}	0.144

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . lib\ timing\ files\ for\ more\ information.$



Table 3-43. Cell OA222_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	C1–Z	t _{PHH}	0.142
E	G1–Z	t _{PLL}	0.167
<u> </u>	C0. 7	t _{PHH}	0.154
	C2–Z	t _{PLL}	0.159
	A1–Z	t _{PHH}	0.108
	AI-Z	t _{PLL}	0.147
	A2–Z	t _{PHH}	0.119
	AZ-Z	t _{PLL}	0.141
	B1-Z	t _{PHH}	0.131
F		t _{PLL}	0.144
I .	B2-Z	t _{PHH}	0.147
	DZ-Z	t _{PLL}	0.138
	C1–Z	t _{PHH}	0.128
	01-2	t _{PLL}	0.160
	C2-Z	t _{PHH}	0.141
	02-Z	t _{PLL}	0.152

^{1.} Millinum input transition and millimum output load. See the timing lifes for more information

3.15.4 Cell Specifications

Table 3-44. Cell OA222_{PL} Capacitance

	Capacitance (fF) by Performance Level				
Input / Output Pins	В	С	D	Е	F
A1	2.9	3.3	4.8	5.8	7.5
A2	2.7	3.0	4.5	5.4	7.1
B1	2.9	3.3	4.9	5.9	7.6
B2	3.0	3.3	4.7	5.6	7.2
C1	3.4	3.7	5.2	6.2	7.9
C2	2.7	3.0	4.4	5.4	6.9
Z	61.7	129.9	209.9	277.2	363.5



Table 3-45. Cell OA222_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
В	7.04		
С	7.84	6.72	
D			
E	8.40		
F			



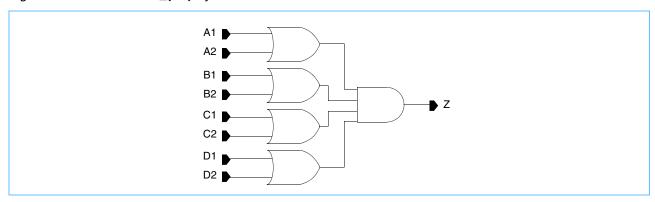
3.16 OA2222_{PL} Cell

3.16.1 Function

 $2 \times 2 \times 2 \times 2$ OR AND

3.16.2 Description

Figure 3-16. Cell OA2222_{PL} Symbols





3.16.3 Propagation Delay Table

Table 3-46. Cell OA2222_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) V _{DD} 1.8 V T _j 25°C
	A1–Z	t _{PHH}	0.136
	A1-Z	t _{PLL}	0.184
	40.7	t _{PHH}	0.147
	A2–Z	t _{PLL}	0.178
	D4 7	t _{PHH}	0.143
	B1–Z	t _{PLL}	0.222
	Do 7	t _{PHH}	0.150
_	B2–Z	t _{PLL}	0.211
В	04.7	t _{PHH}	0.132
	C1–Z	t _{PLL}	0.180
		t _{PHH}	0.144
	C2–Z	t _{PLL}	0.173
		t _{PHH}	0.139
	D1–Z	t _{PLL}	0.218
	D2-Z	t _{PHH}	0.146
		t _{PLL}	0.206
	A1–Z	t _{PHH}	0.147
		t _{PLL}	0.184
	A2-Z	t _{PHH}	0.160
		t _{PLL}	0.178
	D4 7	t _{PHH}	0.150
	B1–Z	t _{PLL}	0.213
	Do 7	t _{PHH}	0.159
0	B2–Z	t _{PLL}	0.203
С	01.7	t _{PHH}	0.141
	C1–Z	t _{PLL}	0.176
	00.7	t _{PHH}	0.154
	C2–Z	t _{PLL}	0.170
	D4 7	t _{PHH}	0.144
	D1–Z	t _{PLL}	0.204
	D0. 7	t _{PHH}	0.153
	D2–Z	t _{PLL}	0.194



Table 3-46. Cell OA2222_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A1–Z	t _{PHH}	0.152
	A1-Z	t _{PLL}	0.160
	A2-Z	t _{PHH}	0.168
	AZ-Z	t _{PLL}	0.155
	B1–Z	t _{PHH}	0.151
	DI-Z	t _{PLL}	0.180
	D0 7	t _{PHH}	0.166
D	B2–Z	t _{PLL}	0.172
D	04.7	t _{PHH}	0.149
	C1–Z	t _{PLL}	0.154
	00.7	t _{PHH}	0.166
	C2–Z	t _{PLL}	0.148
	D1–Z	t _{PHH}	0.149
		t _{PLL}	0.172
	D2-Z	t _{PHH}	0.161
		t _{PLL}	0.164
	A1–Z	t _{PHH}	0.147
		t _{PLL}	0.157
	A2–Z	t _{PHH}	0.162
		t _{PLL}	0.152
		t _{PHH}	0.144
	B1–Z	t _{PLL}	0.175
		t _{PHH}	0.159
_	B2–Z	t _{PLL}	0.167
Е	0	t _{PHH}	0.143
	C1–Z	t _{PLL}	0.150
		t _{PHH}	0.159
	C2–Z	t _{PLL}	0.144
		t _{PHH}	0.141
	D1–Z	t _{PLL}	0.167
	P	t _{PHH}	0.153
	D2–Z	t _{PLL}	0.159

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 3-46. Cell OA2222_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) V _{DD} 1.8 V T _j 25°C
	A1–Z	t _{PHH}	0.137
	A1-Z	t _{PLL}	0.151
	A2–Z	t _{PHH}	0.151
	MZ-Z	t _{PLL}	0.145
	B1–Z	t _{PHH}	0.134
	D1-Z	t _{PLL}	0.168
	B2–Z	t _{PHH}	0.147
F	D2-L	t _{PLL}	0.160
	C1-Z	t _{PHH}	0.131
		t _{PLL}	0.144
	C2-Z	t _{PHH}	0.146
	02-L	t _{PLL}	0.137
	D1–Z	t _{PHH}	0.128
	D1-Z	t _{PLL}	0.160
	D2–Z	t _{PHH}	0.141
	U2-Z	t _{PLL}	0.152

^{3.16.4} Cell Specifications

Table 3-47. Cell OA2222_{PL} Capacitance

	Capacitance (fF) by Performance Level					
Input / Output Pins	В	С	D	Е	F	
A1	2.9	3.3	4.9	5.9	7.6	
A2	3.0	3.3	4.7	5.6	7.2	
B1	3.4	3.7	5.3	6.2	7.9	
B2	2.7	3.0	4.4	5.4	7.0	
C1	2.9	3.3	4.9	5.9	7.6	
C2	3.0	3.3	4.7	5.6	7.2	
D1	3.3	3.7	5.2	6.2	7.9	
D2	2.7	3.0	4.5	5.4	6.9	
Z	61.6	130.3	210.3	277.7	363.5	



Table 3-48. Cell OA2222_{PL} Area

	Cell Dimensions (μm)				
Performance Level	Width	Length			
В					
С					
D	9.52	6.72			
Е					
F					



3.17 OAI21_{PL} Cell

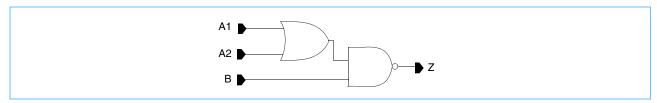
3.17.1 Function

2 × 1 OR AND inverter

3.17.2 Description

This cell is a combinational gate, 2×1 OR AND inverter. The Boolean expression for this cell is $Z = \overline{(A1 + A2) \times B}$.

Figure 3-17. Cell OAI21_{PL} Symbols



3.17.3 Propagation Delay Table

Table 3-49. Cell OAI21_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process $(ns)^1$ V_{DD} 1.8 V T_j 25°C
	A 1 7	t _{PLH}	0.108
	A1–Z	t _{PHL}	0.067
۸	A0. 7	t _{PLH}	0.101
Α	A2–Z	t _{PHL}	0.078
	B–Z	t _{PLH}	0.105
		t _{PHL}	0.057
	A1-Z	t _{PLH}	0.086
		t _{PHL}	0.054
D	40.7	t _{PLH}	0.081
В	A2–Z	t _{PHL}	0.067
	D 7	t _{PLH}	0.089
	B–Z	t _{PHL}	0.046

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . lib\ timing\ files\ for\ more\ information.$



Table 3-49. Cell OAI21_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A1–Z	t _{PLH}	0.072
	AI-Z	t _{PHL}	0.042
0	A2–Z	t _{PLH}	0.069
С	AZ-Z	t _{PHL}	0.056
	B–Z	t _{PLH}	0.080
	D-Z	t _{PHL}	0.036
	A1–Z	t _{PLH}	0.071
	A1-Z	t _{PHL}	0.041
D	A2–Z	t _{PLH}	0.068
D	AZ-Z	t _{PHL}	0.059
	B-Z	t _{PLH}	0.085
		t _{PHL}	0.040
_	A1–Z	t _{PLH}	0.065
		t _{PHL}	0.039
	A2–Z	t _{PLH}	0.063
Е		t _{PHL}	0.053
	B–Z	t _{PLH}	0.090
	D-Z	t _{PHL}	0.035
	A1–Z	t _{PLH}	0.061
	MI-L	t _{PHL}	0.041
F	A2–Z	t _{PLH}	0.060
Γ	M2-L	t _{PHL}	0.057
	B–Z	t _{PLH}	0.074
	υ-Δ	t _{PHL}	0.036
	A1–Z	t _{PLH}	0.063
	M1-Z	t _{PHL}	0.053
Ц	A2–Z	t _{PLH}	0.065
Н	AZ-Z	t _{PHL}	0.038
	D 7	t _{PLH}	0.076
	B–Z	t _{PHL}	0.054

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



3.17.4 Cell Specifications

Table 3-50. Cell OAI21_{PL} Capacitance

Input /	Capacitance (fF) by Performance Level						
Output Pins	Α	В	С	D	E	F	Н
A1	3.0	4.2	7.1	11.3	15.3	21.1	28.1
A2	3.0	4.1	6.9	10.5	14.8	21.0	28.7
В	3.8	5.1	8.2	7.7	10.8	16.8	22.7
Z	34.1	60.9	118.7	181.7	265.3	390.9	488.1

Table 3-51. Cell OAI21_{PL} Area

	Cell Dimensions (μm)				
Performance Level	Width	Length			
Α					
В	2.80				
С					
D	3.92	6.72			
E	3.92				
F	5.60				
Н	7.28				



3.18 OAI22_{PL} Cell

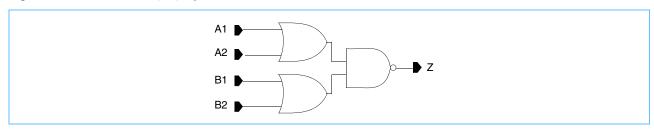
3.18.1 Function

2 × 2 OR AND inverter

3.18.2 Description

This cell is a combinational gate, 2×2 OR AND inverter. The Boolean expression for this cell is $Z = \overline{(A1 + A2) \times (B1 + B2)}$.

Figure 3-18. Cell OAI22_{PL} Symbols



3.18.3 Propagation Delay Table

Table 3-52. Cell OAI22_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A1–Z	t _{PLH}	0.095
	AI-Z	t _{PHL}	0.074
	A2-Z	t _{PLH}	0.091
۸	AZ-Z	t _{PHL}	0.089
Α	D4 7	t _{PLH}	0.120
	B1–Z	t _{PHL}	0.078
	B2–Z	t _{PLH}	0.110
	D2-Z	t _{PHL}	0.089
	A1–Z	t _{PLH}	0.077
		t _{PHL}	0.060
		t _{PLH}	0.075
В	A2–Z	t _{PHL}	0.076
D	D4 7	t _{PLH}	0.099
	B1–Z	t _{PHL}	0.061
	B2-Z	t _{PLH}	0.092
	DZ-Z	t _{PHL}	0.074

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 3-52. Cell OAI22_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A4 7	t _{PLH}	0.069
	A1–Z	t _{PHL}	0.054
	40.7	t _{PLH}	0.068
0	A2–Z	t _{PHL}	0.071
C	D4 7	t _{PLH}	0.089
	B1–Z	t _{PHL}	0.054
	D0. 7	t _{PLH}	0.084
	B2–Z	t _{PHL}	0.070
	A4. 7	t _{PLH}	0.067
	A1–Z	t _{PHL}	0.052
	40.7	t _{PLH}	0.066
D	A2–Z	t _{PHL}	0.068
	B1–Z	t _{PLH}	0.087
		t _{PHL}	0.054
	B2-Z	t _{PLH}	0.083
	B2-Z	t _{PHL}	0.067
	A1–Z	t _{PLH}	0.065
		t _{PHL}	0.049
	40.7	t _{PLH}	0.064
E	A2–Z	t _{PHL}	0.065
_	B1–Z	t _{PLH}	0.085
	DI-Z	t _{PHL}	0.050
	B2-Z	t _{PLH}	0.081
	D2-Z	t _{PHL}	0.064
	A1–Z	t _{PLH}	0.062
	M1-Z	t _{PHL}	0.047
	A2-Z	t _{PLH}	0.061
F	MZ-Z	t _{PHL}	0.063
Г	B1–Z	t _{PLH}	0.083
	DI-L	t _{PHL}	0.048
	P0 7	t _{PLH}	0.079
	B2–Z	t _{PHL}	0.063

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . lib\ timing\ files\ for\ more\ information.$



3.18.4 Cell Specifications

Table 3-53. Cell OAI22_{PL} Capacitance

Input /	Capacitance (fF) by Performance Level					
Output Pins A	Α	В	С	D	E	F
A1	3.4	4.9	9.0	13.7	17.6	30.4
A2	3.5	4.8	9.3	13.9	17.6	30.4
B1	3.8	5.3	8.8	13.8	17.5	29.6
B2	3.2	4.6	9.0	13.7	17.4	29.7
Z	45.2	80.5	160.5	237.3	313.4	551.3

Table 3-54. Cell OAI22_{PL} Area

	Cell Dimensions (μm)			
Performance Level	Width Length			
А	3.92			
В	3.92			
С	5.04	6.72		
D	7.00	0.72		
E	7.28			
F	10.08			



3.19 OAI222_{PL} Cell

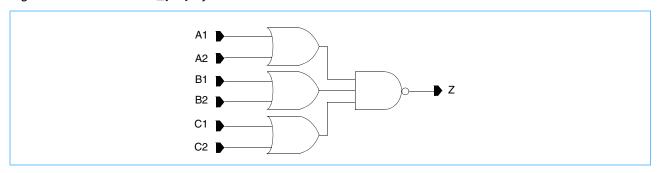
3.19.1 Function

 $2 \times 2 \times 2$ OR AND inverter

3.19.2 Description

This cell is a combinational gate, $2 \times 2 \times 2$ OR AND inverter. The Boolean expression for this cell is $Z = \overline{(A1 + A2) \times (B1 + B2) \times (C1 + C2)}$.

Figure 3-19. Cell OAI222_{PL} Symbols



3.19.3 Propagation Delay Table

Table 3-55. Cell OAI222_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A1–Z	t _{PLH}	0.213
	AI-Z	t _{PHL}	0.147
	A2–Z	t _{PLH}	0.204
	AZ-Z	t _{PHL}	0.150
	B1–Z	t _{PLH}	0.248
E		t _{PHL}	0.175
<u> </u>	D0. 7	t _{PLH}	0.241
	B2–Z	t _{PHL}	0.184
	04.7	t _{PLH}	0.290
	C1–Z	t _{PHL}	0.180
	C2-Z	t _{PLH}	0.279
		t _{PHL}	0.184



Table 3-55. Cell OAI222_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A1 7	t _{PLH}	0.190
	A1–Z	t _{PHL}	0.130
	A2–Z	t _{PLH}	0.182
	AZ-Z	t _{PHL}	0.136
	B1–Z	t _{PLH}	0.217
Н	BI-Z	t _{PHL}	0.153
П	DO 7	t _{PLH}	0.209
	B2–Z	t _{PHL}	0.162
	C1–Z	t _{PLH}	0.249
	01-2	t _{PHL}	0.156
	C2. 7	t _{PLH}	0.240
	C2–Z	t _{PHL}	0.161

3.19.4 Cell Specifications

Table 3-56. Cell OAI222_{PL} Capacitance

	Capacitance (fF) by Performance Level		
Input / Output Pins	E	Н	
A1	3.0	4.6	
A2	2.8	4.3	
B1	3.2	5.0	
B2	3.2	4.9	
C1	3.5	5.2	
C2	2.9	4.5	
z	236.5	467.1	

Table 3-57. Cell OAI222_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
E	8.96	6.72	
Н	8.90	6.72	



3.20 OAI2222_{PL} Cell

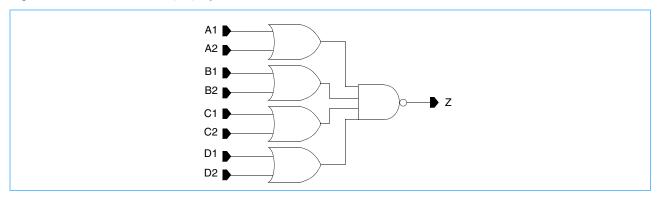
3.20.1 Function

 $2 \times 2 \times 2 \times 2$ OR AND inverter

3.20.2 Description

This cell is a combinational gate, $2 \times 2 \times 2 \times 2$ OR AND inverter. The Boolean expression for this cell is $Z = \overline{(A1 + A2) \times (B1 + B2) \times (C1 + C2) \times (D1 + D2)}$.

Figure 3-20. Cell OAI2222_{PL} Symbols



3.20.3 Propagation Delay Table

Table 3-58. Cell OAI2222_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process $(ns)^1$ V_{DD} 1.8 V T_j 25°C
	A1–Z	t _{PLH}	0.227
	AI-Z	t _{PHL}	0.162
	A2-Z	t _{PLH}	0.220
	AZ-Z	t _{PHL}	0.171
	B1-Z	t _{PLH}	0.270
E		t _{PHL}	0.170
<u> </u>	B2-Z	t _{PLH}	0.258
	DZ-Z	t _{PHL}	0.172
	01.7	t _{PLH}	0.249
	C1–Z	t _{PHL}	0.177
C2-Z	C0. 7	t _{PLH}	0.242
	t _{PHL}	0.185	



Table 3-58. Cell OAI2222_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) V _{DD} 1.8 V T _j 25°C
	D1–Z	t _{PLH}	0.290
Е	DI-Z	t _{PHL}	0.182
E	D2–Z	t _{PLH}	0.280
	DZ-Z	t _{PHL}	0.186
	A1–Z	t _{PLH}	0.202
	AI-Z	t _{PHL}	0.141
	A2–Z	t _{PLH}	0.194
	A2-Z	t _{PHL}	0.150
	B1–Z	t _{PLH}	0.235
		t _{PHL}	0.145
	B2–Z	t _{PLH}	0.225
Н	DZ-Z	t _{PHL}	0.150
11	C1–Z	t _{PLH}	0.217
	01 2	t _{PHL}	0.155
	C2–Z	t _{PLH}	0.209
	U2-L	t _{PHL}	0.163
	D1–Z	t _{PLH}	0.250
	υ1–Ζ	t _{PHL}	0.157
	D2–Z	t _{PLH}	0.240
	D2-L	t _{PHL}	0.162

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.

3.20.4 Cell Specifications

Table 3-59. Cell OAI2222_{PL} Capacitance

	Capacitance (fF) by Performance Level	
Input / Output Pins	E	Н
A1	3.1	4.9
A2	3.2	4.9
B1	3.6	5.3
B2	2.9	4.5
C1	3.1	4.9
C2	3.2	4.9
D1	3.5	5.2
D2	2.9	4.5
Z	236.4	469.1

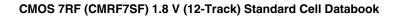




Table 3-60. Cell OAI2222_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
E	10.64	10.64	
Н	10.64	10.64	

4. Standard Cell Unique Logic

4.1 ADDF_{PL} Cell

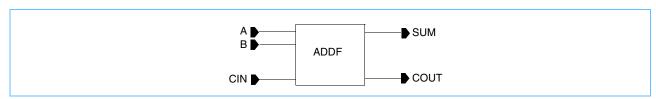
4.1.1 Function

Full adder

4.1.2 Description

This cell is a full, three-bit adder with sum (SUM) and carry (COUT) as outputs.

Figure 4-1. Cell ADDF_{PL} Symbols



4.1.3 Truth Table

Table 4-1. Cell ADDF_{PL} Truth Table

	Inputs		Out	puts
Α	В	CIN	COUT	SUM
0	0	0	0	0
0	1	0	0	1
1	0	0	0	1
1	1	0	1	0
0	0	1	0	1
0	1	1	1	0
1	0	1	1	0
1	1	1	1	1



4.1.4 Propagation Delay Table

Table 4-2. Cell ADDF_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	A 00UT	t _{PHH}	0.186
	A-COUT	t _{PLL}	0.230
	D COUT	t _{PHH}	0.219
	B-COUT	t _{PLL}	0.188
	OIN COLIT	t _{PHH}	0.118
	CIN-COUT	t _{PLL}	0.118
		t _{PHH}	0.211
	4 01114	t _{PLL}	0.196
5	A-SUM	t _{PLH}	0.221
В		t _{PHL}	0.175
		t _{PHH}	0.254
		t _{PLL}	0.222
	B-SUM	t _{PLH}	0.236
		t _{PHL}	0.207
	CIN-SUM	t _{PHH}	0.090
		t _{PLL}	0.125
		t _{PLH}	0.141
		t _{PHL}	0.145
		t _{PHH}	0.179
	A-COUT	t _{PLL}	0.225
	D. COLUT	t _{PHH}	0.217
	B-COUT	t _{PLL}	0.200
	011.001.7	t _{PHH}	0.112
	CIN-COUT	t _{PLL}	0.118
		t _{PHH}	0.205
С	4 01	t _{PLL}	0.192
	A-SUM	t _{PLH}	0.216
		t _{PHL}	0.169
		t _{PHH}	0.254
	D 01	t _{PLL}	0.218
	B-SUM	t _{PLH}	0.235
		t _{PHL}	0.206

Standard Cell Unique Logic Page 162 of 232



Table 4-2. Cell ADDF_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
		t _{PHH}	0.090
С	CINI CLIM	t _{PLL}	0.123
C	CIN-SUM	t _{PLH}	0.140
		^t РНН t _{PLL}	0.143
	A COLIT	t _{PHH}	0.186
	A-COUT	t _{PLL}	0.221
	B-COUT	t _{PHH}	0.226
	B-COUT	t _{PLL}	0.208
	CIN COLIT	t _{PHH}	0.116
	CIN-COUT	t _{PLL}	0.120
		t _{PHH}	0.194
	A-SUM	t _{PLL}	0.193
D	A-SUM	t _{PLH}	0.204
D		t _{PHL}	0.169
	B-SUM	t _{PHH}	0.245
		t _{PLL}	0.220
		t _{PLH}	0.225
		t _{PHL}	0.209
		t _{PHH}	0.089
	CINI CLIM	t _{PLL}	0.121
	CIN-SUM	t _{PLH}	0.138
		t _{PHL}	0.142
	A-COUT	t _{PHH}	0.192
	A-0001	t _{PLL}	0.224
	P COUT	t _{PHH}	0.232
	B-COUT	t _{PLL}	0.212
F	OIN COLIT		0.120
E	CIN-COUT		0.122
		t _{PHH}	0.201
	A 01114		0.198
	A-SUM		0.212
		t _{PHL}	0.175

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 4-2. Cell ADDF_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
		t _{PHH}	0.256
	D. CLIM	t _{PLL}	0.226
	B-SUM	t _{PLH}	0.235
Е		t _{PHL}	0.215
E		t _{PHH}	0.100
	CINI CLIM	t _{PLL}	0.125
	CIN-SUM	t _{PLH}	0.147
		t _{PHL}	0.147
	A COULT	t _{PHH}	0.224
	A-COUT	t _{PLL}	0.231
	B-COUT	t _{PHH}	0.270
		t _{PLL}	0.229
	CIN-COUT	t _{PHH}	0.150
		t _{PLL}	0.132
	A-SUM	t _{PHH}	0.203
		t _{PLL}	0.226
F		t _{PLH}	0.217
F		t _{PHL}	0.199
		t _{PHH}	0.274
	D CLIM	t _{PLL}	0.257
	B-SUM	t _{PLH}	0.251
		t _{PHL}	0.245
		t _{PHH}	0.107
	CIN-SUM	t _{PLL}	0.147
	CIN-20M	t _{PLH}	0.160
		t _{PHL}	0.170

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



4.1.5 Cell Specifications

Table 4-3. Cell ADDF_{PL} Capacitance

	Capacitance (fF) by P	Capacitance (fF) by Performance Level						
Input / Output Pins	В	С	D	Е	F			
A	11.5	11.9	12.2	12.2	13.6			
В	8.1	8.1	8.0	8.0	8.4			
CIN	10.6	10.7	10.8	10.9	11.6			
SUM	67.4	123.7	182.0	246.5	482.7			
COUT	67.0	127.0	186.6	252.4	647.6			

Table 4-4. Cell ADDF_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
В			
С	10.44		
D	13.44	6.72	
E			
F	14.00		



4.2 BUFFER_{PL} Cell

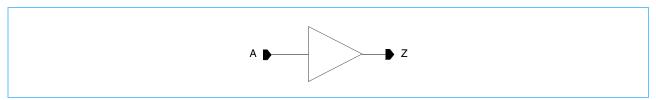
4.2.1 Function

Buffer

4.2.2 Description

This cell is a buffer combinational gate. The Boolean expression for this cell is Z = A.

Figure 4-2. Cell BUFFER_{PL} Symbols



4.2.3 Propagation Delay Table

Table 4-5. Cell BUFFER_{PL} Propagation Delays (Page 1 of 2)

Path (Input to Output)	Performance Level	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	С	t _{PHH}	0.087
	C	t _{PLL}	0.107
	D	t _{PHH}	0.081
	U	t _{PLL}	0.103
	E	t _{PHH}	0.084
	_	t _{PLL}	0.102
	F	t _{PHH}	0.087
	Г	t _{PLL}	0.107
A–Z	Н	t _{PHH}	0.075
A-Z		t _{PLL}	0.109
		t _{PHH}	0.081
	'	t _{PLL}	0.119
	ı	t _{РНН}	0.085
	J	t _{PLL}	0.123
	V	t _{PHH}	0.092
	К	t _{PLL}	0.115
	L	t _{РНН}	0.075
	L	t _{PLL}	0.092

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 4-5. Cell BUFFER_{PL} Propagation Delays (Page 2 of 2)

Path (Input to Output)	Performance Level	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C	
	M	t _{РНН}	0.079	
	IVI	t _{PLL}	0.100	
A 7	N	t _{PHH}	0.106	
A–Z		t _{PLL}	0.121	
	0	t _{PHH}	0.104	
		t _{PLL}	0.120	
Minimum input transition and minimum output load. See .lib timing files for more information.				

^{4.2.4} Cell Specifications

Table 4-6. Cell BUFFER_{PL} Capacitance

Input /	Capacitar	Capacitance (fF) by Performance Level										
Output Pins	С	D	Е	F	Н	I	J	K	L	М	N	0
А	3.1	3.6	3.9	4.3	5.6	6.1	7.3	8.6	17.1	17.9	14.8	17.4
Z	107.4	167.0	225.1	342.4	452.2	710.0	895.4	1149.0	1460.2	1835.6	2359.6	2822.0

Table 4-7. Cell BUFFER_{PL} Area

	Cell Dimensions (μm)			
Performance Level	Width	Length		
С				
D				
E	2.90			
F	2.80			
Н				
I		6.72		
J	3.92	0.72		
К				
L				
М	6.16			
N	7.00			
0	7.28			



4.3 CLK_{PL} Cell

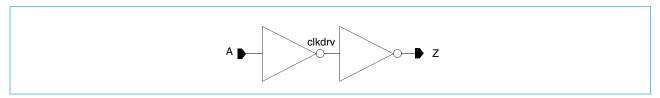
4.3.1 Function

Clock driver

4.3.2 Description

This cell is a clock driver combinational gate. The Boolean expression for this cell is Z = A.

Figure 4-3. Cell CLK_{PL} Symbols



4.3.3 Truth Table

Table 4-8. Cell CLK_{PL} Truth Table

Input	Output
А	Z
1	0
0	1

4.3.4 Propagation Delay Table

Table 4-9. Cell CLK_{PL} Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Nominal Process (ns) V _{DD} 1.8 V T _j 25°C
	ı	t _{PHH}	0.119
	'	t _{PLL}	0.107
	K	t _{PHH}	0.134
	, ,	t _{PLL}	0.120
۸1 7	M	t _{PHH}	0.124
A1–Z -	IVI	t _{PLL}	0.114
	0	t _{PHH}	0.128
		t _{PLL}	0.116
	0	t _{PHH}	0.128
	Q	t _{PLL}	0.119

1. Minimum input transition and minimum output load. See .lib timing files for more information.



4.3.5 Cell Specifications

Table 4-10. Cell CLK_{PL} Capacitance

	Capacitance (fF) by Performance Level					
Input / Output Pins	I	К	М	0	Q	
Α	10.1	13.2	24.3	32.8	46.4	
Z	1161.7	2119.3	3524.2	4912.3	6931.8	

Table 4-11. Cell CLK_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
I	3.92		
К	5.04		
М	8.96	6.72	
0	13.44		
Q	17.36		



4.4 CLKI_{PL} Cell

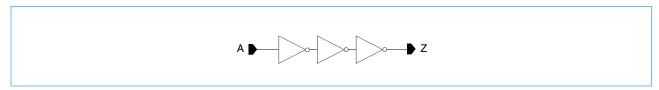
4.4.1 Function

Inverting clock driver

4.4.2 Description

This cell is an inverting clock driver combinational gate. The Boolean expression for this cell is $Z = \overline{A}$.

Figure 4-4. Cell CLKI_{PL} Symbols



4.4.3 Truth Table

Table 4-12. Cell CLKI_{PL} Truth Table

Input	Output
A	Z
1	0
0	1

4.4.4 Propagation Delay Table

Table 4-13. Cell CLKI_{PL} Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
		t _{PLH}	0.165
	'	t _{PHL}	0.178
	V	t _{PLH}	0.177
	K	t _{PHL}	0.186
A1–Z	M	t _{PLH}	0.180
AI-Z	IVI	t _{PHL}	0.184
	0	t _{PLH}	0.179
	0	t _{PHL}	0.180
	0	t _{PLH}	0.202
	Q	t _{PHL}	0.189



4.4.5 Cell Specifications

Table 4-14. Cell CLKI_{PL} Capacitance

	Capacitance (fF) by Performance Level				
Input / Output Pins	I	К	М	0	Q
Α	5.7	6.4	8.3	12.2	14.0
Z	1089.0	1997.6	2995.2	4896.9	6935.2

Table 4-15. Cell CLKI_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
I	5.60		
К	6.72		
M	10.08	6.72	
0	14.00		
Q	19.04		



4.5 COMP2_{PL} Cell

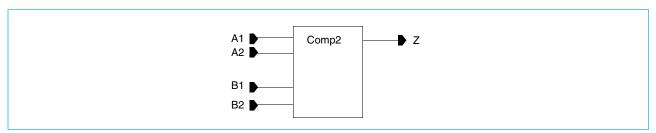
4.5.1 Function

Two-bit comparator

4.5.2 Description

This cell is a two-bit comparator combinational gate. The output of the two-bit comparator is '1' when the A1/B1 and the A2/B2 pairs are the same. The A1/B1 pair does not need to have the same value as the A2/B2 pair.

Figure 4-5. Cell COMP2_{PL} Symbols



4.5.3 Truth Table

Table 4-16. Cell COMP2_{PL} Truth Table

	Inputs				
A1	A2	B1	B2	Z	
0	-	1	-	0	
1	-	0	-	0	
-	0	_	1	0	
-	1	_	0	0	
0	0	0	0	1	
0	1	0	1	1	
1	0	1	0	1	
1	1	1	1	1	



4.5.4 Propagation Delay Table

Table 4-17. Cell COMP2_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process $(ns)^1$ V_{DD} 1.8 V T_j 25°C
		t _{PLH}	0.197
		t _{PHL}	0.180
	A1–Z	t _{PHH}	0.142
		t _{PLL}	0.188
		t _{PLH}	0.214
		t _{PHL}	0.203
	A2–Z	t _{PHH}	0.157
_		t _{PLL}	0.210
В		t _{PLH}	0.195
		t _{PHL}	0.158
	B1–Z	t _{PHH}	0.106
		t _{PLL}	0.217
	B2-Z	t _{PLH}	0.212
		t _{PHL}	0.178
		t _{PHH}	0.122
		t _{PLL}	0.241
		t _{PLH}	0.176
		t _{PHL}	0.171
	A1–Z	t _{PHH}	0.126
		t _{PLL}	0.179
		t _{PLH}	0.191
		t _{PHL}	0.191
	A2–Z	t _{PHH}	0.139
		t _{PLL}	0.199
С		t _{PLH}	0.174
		t _{PHL}	0.150
	B1–Z	т _{РНН}	0.092
	-		0.208
		t _{PLL}	0.189
		t _{PLH}	0.168
	B2–Z	t _{PHL}	0.106
	_	t _{PHH}	0.106
		t _{PLL}	0.228



Table 4-17. Cell COMP2_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
		t _{PLH}	0.167
	A4 7	t _{PHL}	0.165
	A1–Z	t _{PHH}	0.119
		t _{PLL}	0.175
		t _{PLH}	0.180
	40.7	t _{PHL}	0.183
	A2–Z	t _{PHH}	0.131
		t _{PLL}	0.193
D		t _{PLH}	0.164
	D4 7	t _{PHL}	0.145
	B1–Z	t _{PHH}	0.086
		t _{PLL}	0.204
		t _{PLH}	0.178
	B2–Z	t _{PHL}	0.161
		t _{PHH}	0.099
		t _{PLL}	0.222
		t _{PLH}	0.160
	A4 7	t _{PHL}	0.159
	A1–Z	t _{PHH}	0.115
		t _{PLL}	0.169
		t _{PLH}	0.173
	40.7	t _{PHL}	0.174
	A2–Z	t _{PHH}	0.126
_		t _{PLL}	0.185
E		t _{PLH}	0.157
	D4 7	t _{PHL}	0.139
	B1–Z	t _{PHH}	0.083
		t _{PLL}	0.197
		t _{PLH}	0.170
	P0. 7	t _{PHL}	0.154
	B2–Z	t _{PHH}	0.095
		t _{PLL}	0.213

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 4-17. Cell COMP2_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
		t _{PLH}	0.171
	A1–Z	t _{PHL}	0.176
	A1-Z	t _{PHH}	0.128
		t _{PLL}	0.179
		t _{PLH}	0.183
	A2–Z	t _{PHL}	0.191
	AZ-Z	t _{PHH}	0.138
F		t _{PLL}	0.194
	B1–Z	t _{PLH}	0.168
		t _{PHL}	0.149
		t _{PHH}	0.096
		t _{PLL}	0.214
		t _{PLH}	0.180
	B2–Z	t _{PHL}	0.163
	טב-ב	t _{PHH}	0.108
		t _{PLL}	0.229

4.5.5 Cell Specifications

Table 4-18. Cell COMP2_{PL} Capacitance

Input /	Capacitance (fF) by Performance Level				
Output Pins	В	С	D	E	F
A1	3.3	4.0	4.9	5.8	5.8
A2	3.3	4.0	4.8	5.8	5.8
B1	4.6	5.5	6.5	7.7	7.8
B2	4.6	5.5	6.6	7.8	7.8
Z	64.0	122.3	187.4	247.5	360.2



Table 4-19. Cell COMP2_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
В	10.08		
С		6.72	
D			
E			
F	11.20		



4.6 DELAY4_{PL} Cell

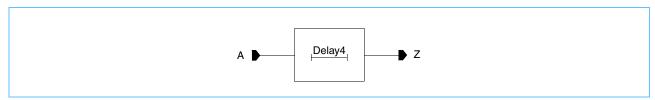
4.6.1 Function

Delay line

4.6.2 Description

This cell is a delay line combinational gate. The Boolean expression for this cell is Z = A.

Figure 4-6. Cell DELAY4_{PL} Symbols



4.6.3 Propagation Delay Table

Table 4-20. Cell DELAY4_{PL} Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	0	t _{PHH}	0.259
	С	t _{PLL}	0.239
۸.7	A–Z F	t _{PHH}	0.214
A-Z		t _{PLL}	0.198
		t _{РНН}	0.182
	J	t _{PLL}	0.178

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.

4.6.4 Cell Specifications

Table 4-21. Cell DELAY4_{PL} Capacitance

	Capacitance (fF) by Performance Level			
Input / Output Pins	С	F	J	
Α	5.7	5.7	5.7	
Z	617.4	593.0	567.2	



Table 4-22. Cell DELAY4_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
С			
F	5.60	6.72	
J			



4.7 DELAY6_{PL} Cell

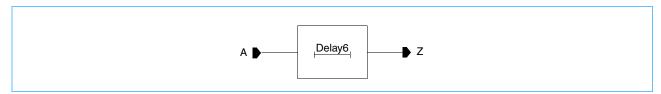
4.7.1 Function

Delay line

4.7.2 Description

This cell is a delay line combinational gate. The Boolean expression for this cell is Z = A.

Figure 4-7. Cell DELAY6_{PL} Symbols



4.7.3 Propagation Delay Table

Table 4-23. Cell DELAY6_{PL} Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C		
A-Z	А	t _{РНН}	1.633		
	^	t _{PLL}	1.635		
	В	t _{PHH}	1.028		
	Ь	t _{PLL}	1.036		
	С	t _{РНН}	0.509		
		t _{PLL}	0.486		
	F	t _{РНН}	0.419		
	F	t _{PLL}	0.399		
		t _{PHH}	0.347		
	J	t _{PLL}	0.338		
		t _{PHH}	0.252		
	M	t _{PLL}	0.244		
Minimum input transition and minimum output load. See .lib timing files for more information.					



4.7.4 Cell Specifications

Table 4-24. Cell DELAY6_{PL} Capacitance

	Capacitance (fF) by Performance Level					
Input / Output Pins	Α	В	С	F	J	М
Α	4.0	5.5	5.7	5.7	5.7	5.7
Z	672.3	597.6	603.5	594.2	592.7	581.0

Table 4-25. Cell DELAY6_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
А		6.72	
В	8.40		
С			
F			
J			
М			



4.8 MUX21_{PL} Cell

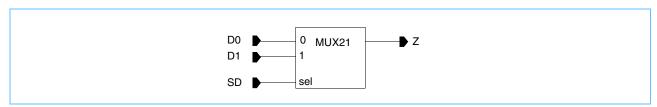
4.8.1 Function

2:1 Multiplexer

4.8.2 Description

This cell is a 2:1 multiplexer combinational gate. The cell selects data from D0 or D1 based on the value of the SD input pin.

Figure 4-8. Cell MUX21_{PL} Symbols



4.8.3 Truth Table

Table 4-26. Cell MUX21_{PL} Truth Table

Inputs			Output
D0	D1	SD	Z
0	-	0	0
1	_	0	1
-	0	1	0
_	1	1	1

4.8.4 Propagation Delay Table

Table 4-27. Cell MUX21_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	D0-Z	t _{PHH}	0.086
	D0-Z	t _{PLL}	0.132
_	D1-Z	t _{PHH}	0.085
		t _{PLL}	0.134
С	SD-Z	t _{PHH}	0.075
		t _{PLL}	0.120
		t _{PLH}	0.172
		t _{PHL}	0.165



Table 4-27. Cell MUX21_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
		t _{PHH}	0.085
	D0–Z	t _{PLL}	0.132
	D4 7	t _{PHH}	0.085
	D1–Z	t _{PLL}	0.133
D		t _{PHH}	0.075
	-	t _{PLL}	0.120
	SD-Z	t _{PLH}	0.171
		t _{PHL}	0.164
		t _{PHH}	0.087
	D0-Z	t _{PLL}	0.132
	D	t _{PHH}	0.086
_	D1–Z	t _{PLL}	0.133
E		t _{PHH}	0.077
	SD-Z	t _{PLL}	0.122
		t _{PLH}	0.173
		t _{PHL}	0.165
	D0-Z	t _{PHH}	0.095
		t _{PLL}	0.135
	D1–Z	t _{PHH}	0.094
F		t _{PLL}	0.136
F		t _{PHH}	0.086
	SD-Z	t _{PLL}	0.127
	30-2	t _{PLH}	0.182
		t _{PHL}	0.170
	D0-Z	t _{PHH}	0.094
	υ-2	t _{PLL}	0.134
	D1–Z	t _{PHH}	0.093
Н	υI-L	t _{PLL}	0.135
П		t _{PHH}	0.087
	SD-Z	t _{PLL}	0.126
	3D-Z	t _{PLH}	0.178
		t _{PHL}	0.179

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . lib\ timing\ files\ for\ more\ information.$



Table 4-27. Cell MUX21_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process $(ns)^1$ V_{DD} 1.8 V T_j 25°C
	D0-Z	t _{РНН}	0.103
	D0-Z	t _{PLL}	0.135
ſ	D1-Z SD-Z	t _{PHH}	0.102
		t _{PLL}	0.136
		t _{РНН}	0.095
		t _{PLL}	0.128
		t _{PLH}	0.172
		t _{PHL}	0.171

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.

4.8.5 Cell Specifications

Table 4-28. Cell MUX21_{PL} Capacitance

Input /	Capacitance (fF) by Performance Level					
Output Pins	С	D	E	F	Н	I
D0	6.0	6.0	6.2	6.5	7.7	8.8
D1	6.3	6.3	6.4	6.8	7.8	8.8
SD	8.1	8.1	8.2	8.5	9.6	11.1
Z	116.0	165.0	226.4	360.0	460.3	715.4

Table 4-29. Cell MUX21_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
С	5.04	-	
D			
E		0.70	
F		6.72	
Н			
I			



4.9 MUX21BAL_{PL} Cell

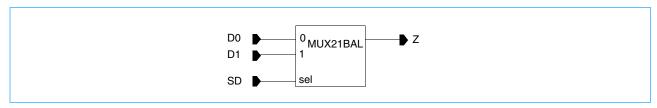
4.9.1 Function

Balanced 2:1 multiplexer

4.9.2 Description

This cell selects data from D0 or D1 based on the value of the SD input. The delay of D0 to Z equals the delay of D1 to Z. The rising data delay equals the falling data delay. The rising select delay equals the falling select delay.

Figure 4-9. Cell MUX21BAL_{PL} Symbols



4.9.3 Truth Table

Table 4-30. Cell MUX21BAL_{PL} Truth Table

Inputs			Output
D0	D1	SD	Z
0	-	0	0
1	-	0	1
_	0	1	0
-	1	1	1

4.9.4 Propagation Delay Table

Table 4-31. Cell MUX21BAL_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) V _{DD} 1.8 V T _j 25°C
	D0–Z	t _{PHH}	0.130
	D0-Z	t _{PLL}	0.132
	D1–Z	t _{PHH}	0.130
н	DI-Z	t _{PLL}	0.133
П		t _{PHH}	0.188
	SD-Z	t _{PLL}	0.194
	30-2	t _{PLH}	0.200
		t _{PHL}	0.191
	D0–Z	t _{PHH}	0.160
	DU-Z	t _{PLL}	0.161
	D1–Z	t _{PHH}	0.162
J		t _{PLL}	0.163
J	SD-Z	t _{PHH}	0.225
		t _{PLL}	0.221
		t _{PLH}	0.227
		t _{PHL}	0.222
	Do 7	t _{PHH}	0.188
	D0–Z	t _{PLL}	0.189
	D1–Z	t _{PHH}	0.192
1	υI-Z	t _{PLL}	0.192
L		t _{PHH}	0.255
	SD-Z	t _{PLL}	0.246
	JU−Z	t _{PLH}	0.255
		t _{PHL}	0.247

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.

4.9.5 Cell Specifications

Table 4-32. Cell MUX21BAL_{PL} Capacitance (Page 1 of 2)

	Capacitance (fF) by Performance Level			
Input / Output Pins	Н	J	L	
D0	8.4	8.6	8.7	

CMOS 7RF (CMRF7SF) 1.8 V (12-Track) Standard Cell Databook

Advance

Table 4-32. Cell MUX21BAL_{PL} Capacitance (Page 2 of 2)

	Capacitance (fF) by Performance Level			
Input / Output Pins	Н	J	L	
D1	9.1	9.3	9.3	
SD	18.5	18.3	18.3	
Z	703.0	1390.6	2025.8	

Table 4-33. Cell MUX21BAL_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
Н	8.96		
J	10.64	6.72	
L	12.32		



4.10 MUX21I_{PL} Cell

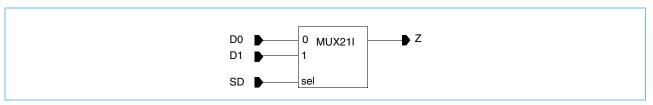
4.10.1 Function

2:1 Multiplexer with inverted output

4.10.2 Description

This cell is a 2:1 multiplexer with inverted output combinational gate. This cell selects data from D0 or D1 based on the value of the SD input pin.

Figure 4-10. Cell MUX21I_{PL} Symbols



4.10.3 Truth Table

Table 4-34. Cell MUX21I_{PL} Truth Table

Inputs			Output
D0	D1	SD	Z
0	-	0	0
1	-	0	1
-	0	1	0
-	1	1	1

4.10.4 Propagation Delay Table

Table 4-35. Cell MUX21I_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C		
	D0-Z	t _{PLH}	0.091		
	D0–Z	t _{PHL}	0.047		
	D1 7	t _{PLH}	0.093		
D	D1–Z	t _{PHL}	0.047		
В	SD-Z	t _{PLH}	0.078		
		t _{PHL}	0.035		
		t _{PHH}	0.103		
		t _{PLL}	0.137		
t _{PLL} 0.137 1. Minimum input transition and minimum output load. See .lib timing files for more information.					



Table 4-35. Cell MUX211_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	D0 7	t _{PLH}	0.081
	D0–Z	t _{PHL}	0.054
	D4 7	t _{PLH}	0.082
0	D1–Z	t _{PHL}	0.055
C		t _{PLH}	0.068
	00.7	t _{PHL}	0.040
	SD-Z	t _{PHH}	0.087
		t _{PLL}	0.133
	D0 7	t _{PLH}	0.075
	D0–Z	t _{PHL}	0.054
	D1–Z	t _{PLH}	0.076
D	D1-Z	t _{PHL}	0.055
D		t _{PLH}	0.062
	SD-Z	t _{PHL}	0.040
		t _{PHH}	0.094
		t _{PLL}	0.127
	D0-Z	t _{PLH}	0.078
	D0-Z	t _{PHL}	0.060
	D1–Z	t _{PLH}	0.082
E	D1-2	t _{PHL}	0.058
_		t _{PLH}	0.065
	SD-Z	t _{PHL}	0.042
	OD Z	t _{PHH}	0.123
		t _{PLL}	0.162
	D0-Z	t _{PLH}	0.161
	D0 -Z	t _{PHL}	0.135
	D1–Z	t _{PLH}	0.161
F	DI-L	t _{PHL}	0.134
'		t _{PLH}	0.149
	SD-Z	t _{PHL}	0.123
	2N-7	t _{PHH}	0.162
		t _{PLL}	0.208

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . lib\ timing\ files\ for\ more\ information.$



Table 4-35. Cell MUX211_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	D0-Z	t _{PLH}	0.156
	D0-Z	t _{PHL}	0.138
	D1 7	t _{PLH}	0.156
Н	D1–Z	t _{PHL}	0.138
П		t _{PLH}	0.145
	SD-Z	t _{PHL}	0.128
	SD-Z	t _{PHH}	0.156
		t _{PLL}	0.210
	D0-Z	t _{PLH}	0.157
	D0-Z	t _{PHL}	0.149
	D1–Z	t _{PLH}	0.157
	DI-Z	t _{PHL}	0.149
1		t _{PLH}	0.146
	SD-Z	t _{PHL}	0.140
	2D-7	t _{PHH}	0.157
		t _{PLL}	0.221

^{4.10.5} Cell Specifications

Table 4-36. Cell MUX21I_{PL} Capacitance

Input /	Capacitance (fF	Capacitance (fF) by Performance Level					
Output Pins	В	С	D	E	F	Н	I
D0	5.7	6.6	8.3	16.6	6.9	7.0	7.0
D1	6.0	6.9	8.7	16.0	7.0	7.0	7.0
SD	8.6	10.1	12.1	17.8	10.0	10.0	10.1
Z	81.9	107.2	148.4	287.2	343.8	450.9	712.3



Table 4-37. Cell MUX21I_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
В			
С	3.92		
D			
Е	8.40	6.72	
F			
Н	6.72		
I			



4.11 MUX41_{PL} Cell

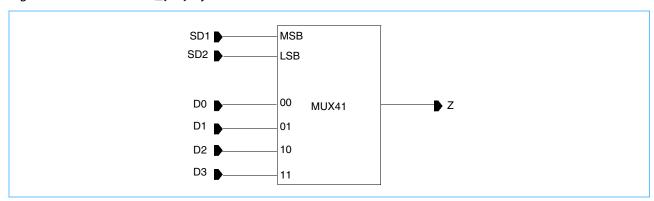
4.11.1 Function

4:1 Multiplexer

4.11.2 Description

This cell is a 4:1 multiplexer combinational gate. This cell selects data from D0, D1, D2, or D3 based on the values of the SD1 and SD2 input pins.

Figure 4-11. Cell MUX41_{PL} Symbols



4.11.3 Truth Table

Table 4-38. Cell MUX41_{PL} Truth Table

Inputs		Outputs
SD1	SD2	Z
0	0	
0	1	
1	0	
1	1	



4.11.4 Propagation Delay Table

Table 4-39. Cell MUX41_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
		t _{PHH}	0.131
	D0–Z	t _{PLL}	0.160
		t _{PHH}	0.120
	D1–Z	t _{PLL}	0.158
		t _{PHH}	0.137
	D2–Z	t _{PLL}	0.168
		t _{PHH}	0.124
_	D3–Z	t _{PLL}	0.165
D		t _{PHH}	0.107
		t _{PLL}	0.144
	SD1-Z	t _{PLH}	0.156
		t _{PHL}	0.140
		t _{PHH}	0.119
	SD2-Z	t _{PLL}	0.194
		t _{PLH}	0.211
		t _{PHL}	0.170
		t _{PHH}	0.139
	D0-Z	t _{PLL}	0.160
		t _{PHH}	0.139
	D1–Z	t _{PLL}	0.164
		t _{PHH}	0.142
	D2–Z	t _{PLL}	0.166
		t _{PHH}	0.141
	D3–Z	t _{PLL}	0.170
F		t _{PHH}	0.117
		t _{PLL}	0.150
	SD1-Z	t _{PLH}	0.160
		t _{PHL}	0.142
		t _{PHH}	0.138
		t _{PLL}	0.195
	SD2-Z	t _{PLH}	0.218
		t _{PHL}	0.177



Table 4-39. Cell MUX41_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) V _{DD} 1.8 V T _j 25°C
	D0-Z	t _{PHH}	0.176
	D0-Z	t _{PLL}	0.204
	D1–Z	t _{PHH}	0.177
	DI-Z	t _{PLL}	0.207
	D2-Z	t _{PHH}	0.177
	DZ-Z	t _{PLL}	0.207
	D3-Z	t _{PHH}	0.177
J	D3-Z	t _{PLL}	0.210
		t _{PHH}	0.122
	SD1-Z	t _{PLL}	0.152
		t _{PLH}	0.169
		t _{PHL}	0.143
		t _{PHH}	0.163
	SD2-Z	t _{PLL}	0.204
	302-2	t _{PLH}	0.223
		t _{PHL}	0.175

^{1.} Minimum input transition and minimum output load. See .iib timing files for more information

4.11.5 Cell Specifications

Table 4-40. Cell MUX41_{PL} Capacitance

	Capacitance (fF)	Capacitance (fF) by Performance Level		
Input / Output Pins	D	F	J	
D0	7.5	7.8	7.7	
D1	7.8	8.0	8.1	
D2	7.7	7.9	7.8	
D3	7.9	8.1	8.1	
SD1	5.9	6.8	13.3	
SD2	10.1	11.2	20.3	
Z	166.8	385.5	925.1	

Table 4-41. Cell MUX41_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
D	12.32		
F		6.72	
J	13.44		



4.12 TERM_{PL} Cell

4.12.1 Function

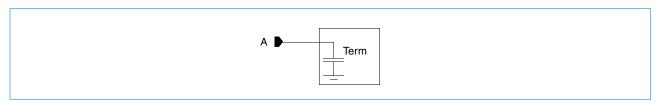
Net terminator

4.12.2 Description

This cell is a net terminator combinational gate. The net terminator is used to add capacitive load to a net. The additional load will modify the rise and fall time of the net.

Capacitive loads vary by performance level, as shown in *Table 4-42*.

Figure 4-12. Cell TERM_{PL} Symbols



4.12.3 Cell Specifications

Table 4-42. Cell TERM_{PL} Capacitance

	Capacitance (fF) by Performance Level				
Input Pin	Α	В	С	D	
Α	5.90	9.10	14.10	18.29	

Table 4-43. Cell TERM_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
A	1.68		
В		0.70	
С		6.72	
D			



5. Standard Cell Sequential Logic

5.1 DFF_{PL} Cell

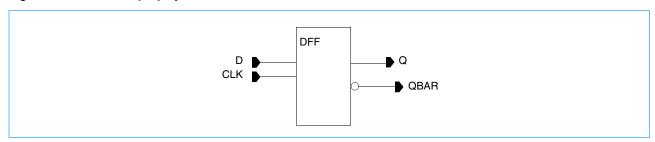
5.1.1 Function

DFF, Q, and QBAR outputs

5.1.2 Description

This cell is a positive edge-triggered D flip-flop with true and complement outputs.

Figure 5-1. Cell DFF_{PL} Symbols



5.1.3 DFF Truth Table

Table 5-1. Cell DFF_{PL} Truth Table

Inputs		Outputs	
CLK	D	Q	QBAR
(01)	0	0	1
(01)	1	1	0
(1x)	х	-	-
(x0)	х	-	-

5.1.4 Delay Tables

Table 5-2. Cell DFF_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
_	CLK-Q	t _{PHH}	0.226
		t _{PHL}	0.160
E	CLK-QBAR	t _{PHH}	0.106
	CLK-QBAR	t _{PHL}	0.164

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 5-2. Cell DFF_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process $(ns)^1$ V_{DD} 1.8 V T_j 25°C
	CLK-Q	t _{PHH}	0.261
11	OLK-Q	t _{PHL}	0.196
Н	CLK ODAD	t _{PHH}	0.124
	CLK-QBAR	t _{PHL}	0.168
	OLK O	t _{PHH}	0.264
17	CLK-Q	t _{PHL}	0.188
К	OLIV ODAD	t _{PHH}	0.274
	CLK-QBAR	t _{PHL}	0.345

Table 5-3. Cell DFF_{PL} Latch Setup and Hold Delays

		Constraint (ps) by I			
Data / Clock	Condition ¹	E	Н	K	
D 01 / CL K	Setup	31	35	26	
D 01 / CLK	Hold	9	14	2	
D 10 / OL K	Setup	182	183	179	
D 10 / CLK	Hold	-149	-147	-151	

^{1.} Setup and hold are calculated using nominal case conditions (1.8 V, 25°C; clock and data slew rate = 200 ps).

5.1.5 Cell Specifications

Table 5-4. Cell DFF_{PL} Capacitance

	Capacitance (fF) by Performance Level				
Input / Output Pins	Е	Н	К		
CLK	11.1	11.0	11.0		
D	4.6	4.8	4.7		
Q	236.9	463.9	1159.8		
QBAR	248.0	517.3	1184.6		

Table 5-5. Cell DFF_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
E	7.84		
Н	8.96	6.72	
К	12.32		



5.2 DFFR_{PL} Cell

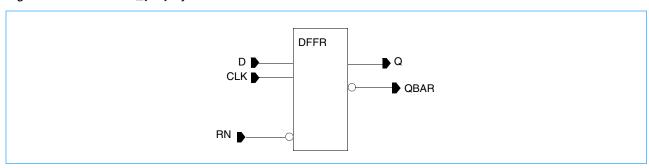
5.2.1 Function

DFF, Q, and QBAR outputs, -asynchronous reset

5.2.2 Description

This cell is a positive edge-triggered D flip-flop with asynchronous inputs and a reset function. If RN = 0, the Q output is forced to '0' (reset) and the QBAR output is forced to '1'.

Figure 5-2. Cell DFFR_{PL} Symbols



5.2.3 DFF Truth Table

Table 5-6. Cell DFFR_{PL} Truth Table

Inputs			Outputs	
CLK	D	RN	Q	QBAR
Х	х	0	0	1
(01)	1	1	1	0
(1x)	х	1	_	_
(x0)	x	1	_	-
(01)	0	х	0	1



5.2.4 Delay Tables

Table 5-7. Cell DFFR_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	RN-Q	t _{PLL}	0.238
	OLK O	t _{PHH}	0.289
E -	CLK-Q	t _{PHL}	0.181
_	RN-QBAR	t _{PLH}	0.184
	CLK-QBAR	t _{PHH}	0.120
	CLK-QDAR	t _{PHL}	0.187
	RN-Q	t _{PLL}	0.266
	CLK-Q	t _{PHH}	0.344
н	CLK-Q	t _{PHL}	0.220
11	RN-QBAR	t _{PLH}	0.195
	CLK-QBAR	t _{PHH}	0.140
	OLK-QDAN	t _{PHL}	0.198
	RN-Q	t _{PLL}	0.283
	CLK-Q	t _{PHH}	0.332
K	OLN-Q	t _{PHL}	0.216
IX.	RN-QBAR	t _{PLH}	0.373
	CLK-QBAR	t _{PHH}	0.306
	ULK-WDAN	t _{PHL}	0.419

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-8. Cell DFFR_{PL} Latch Setup and Hold Delays

		Constraint (ps) b	Constraint (ps) by Performance Level		
Data / Clock	Condition ¹	E	Н	К	
D 01 / CLK	Setup	103	122	58	
D 01 / CLK	Hold	4	9	-2	
D 10 / CL K	Setup	184	185	183	
D 10 / CLK	Hold	-148	-145	-151	
1. Setup and	1. Setup and hold are calculated using nominal case conditions (1.8 V, 25°C; clock and data slew rate = 200 ps).				



5.2.5 Cell Specifications

Table 5-9. Cell DFFR_{PL} Capacitance

	Capacitance (fF) by Performance Level			
Input / Output Pins	Е	Н	К	
CLK	12.3	12.2	12.2	
D	4.8	4.7	4.7	
Q	236.1	488.6	1265.3	
QBAR	261.6	516.3	1181.7	
RN	7.6	7.7	7.6	

Table 5-10. Cell DFFR_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
E	9.52		
Н	10.64	6.72	
К	14.00		



5.3 DFFS_{PL} Cell

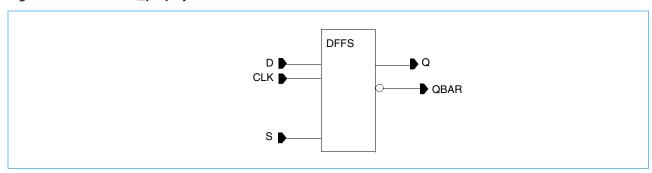
5.3.1 Function

DFF, Q, and QBAR outputs, asynchronous set

5.3.2 Description

This cell is a positive edge-triggered D flip-flop with asynchronous inputs and a set function. If S = 1, the Q output is forced to '1' (set) and the QBAR output is forced to '0'.

Figure 5-3. Cell DFFS_{PL} Symbols



5.3.3 DFF Truth Table

Table 5-11. Cell DFFS_{PL} Truth Table

Inputs			Out	puts
CLK	D	S	Q	QBAR
(01)	0	0	0	1
(01)	1	x	1	0
(1x)	х	0	_	-
(x0)	х	0	-	-
х	х	1	0	1



5.3.4 Delay Tables

Table 5-12. Cell DFFS_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	$\begin{array}{cc} \text{Nominal Process (ns)}^1 \\ \text{V}_{\text{DD}} & 5.0 \text{ V} \\ \text{T}_{j} & 25^{\circ}\text{C} \end{array}$
	S-Q	t _{PHH}	0.229
	CLK-Q	t _{PHH}	0.277
E	CLK-Q	t _{PHL}	0.183
_	S-QBAR	t _{PHL}	0.167
	CLK-QBAR	t _{PHH}	0.125
	OLK-QDAN	t _{PHL}	0.196
	S-Q	t _{PHH}	0.272
	CLK-Q	t _{PHH}	0.331
н	OLN-Q	t _{PHL}	0.226
11	S-QBAR	t _{PHL}	0.176
	CLK-QBAR	t _{PHH}	0.147
	OLN-QDAN	t _{PHL}	0.193
	S-Q	t _{PHH}	0.276
	CLK-Q	t _{PHH}	0.319
К	OLN-Q	t _{PHL}	0.216
IX	S-QBAR	t _{PHL}	0.359
	CLK-QBAR	t _{PHH}	0.304
	ULN-UDAN	t _{PHL}	0.404

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-13. Cell DFFS_{PL} Latch Setup and Hold Delays

		Constraint (ps) by Pe	Constraint (ps) by Performance Level			
Data / Clock	Condition ¹	E	Н	K		
D 01 / CLK	Setup	55	89	45		
D 01 / CLK	Hold	4	8	-2		
D 10 / OLK	Setup	189	188	185		
D 10 / CLK	Hold	-158	-15	-157		

^{1.} Setup and hold are calculated using nominal case conditions (1.8 V, 25°C; clock and data slew rate = 200 ps).



5.3.5 Cell Specifications

Table 5-14. Cell DFFS_{PL} Capacitance

	Capacitance (fF) by Performance Level			
Input / Output Pins	Е	Н	К	
CLK	11.5	11.8	11.7	
D	4.8	4.8	4.8	
Q	235.9	489.5	1265.2	
QBAR	244.9	545.1	1181.3	
S	7.7	7.5	7.5	

Table 5-15. Cell DFFS_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
Е	10.08		
Н	11.20	6.72	
К	14.56		

5.4 DFFSR_{PL} Cell

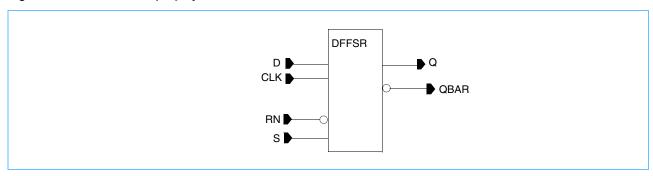
5.4.1 Function

DFF, Q, and QBAR outputs, asynchronous set, -asynchronous reset

5.4.2 Description

This cell is a positive edge-triggered D flip-flop with asynchronous inputs, and set and reset functions. S and RN are the set and reset inputs, respectively. If S = 1, the Q output is forced to '1' (set). If RN = 0, the Q output is forced to '0' (reset). The set function is dominant.

Figure 5-4. Cell DFFSR_{PL} Symbols



5.4.3 DFF Truth Table

Table 5-16. Cell DFFSR_{PL} Truth Table

Inputs				Out	puts
CLK	D	RN	S	Q	QBAR
х	х	0	0	0	1
(1x)	x	1	0	-	_
(x0)	x	1	0	-	_
(01)	0	х	0	0	1
х	x	х	1	1	0
(01)	1	1	х	1	0



5.4.4 Delay Tables

Table 5-17. Cell DFFSR_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) V _{DD} 1.8 V T _j 25°C
	RN-Q	t _{PLL}	0.256
	S-Q	t _{PHH}	0.275
	CLK-Q	t _{PHH}	0.260
E	OLN-Q	t _{PHL}	0.163
E	RN-QBAR	t _{PLH}	0.223
	S-QBAR	t _{PHL}	0.197
	CLK-QBAR	t _{PHH}	0.126
	CLK-QDAN	t _{PHL}	0.173
	RN-Q	t _{PLL}	0.303
	S-Q	t _{PHH}	0.312
	CLK-Q	t _{PHH}	0.298
н	OLN-Q	t _{PHL}	0.221
П	RN-QBAR	t _{PLH}	0.222
	S-QBAR	t _{PHL}	0.218
	CLK-QBAR	t _{PHH}	0.136
	CLK-QDAN	t _{PHL}	0.189
	RN-Q	t _{PLL}	0.329
	S-Q	t _{PHH}	0.327
	CLK-Q	t _{PHH}	0.315
к	OLN-Q	t _{PHL}	0.229
r.	RN-QBAR	t _{PLH}	0.422
	S-QBAR	t _{PHL}	0.410
	CLK-QBAR	t _{PHH}	0.322
	ULN-QDAN	t _{PHL}	0.400

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 5-18. Cell DFFSR_{PL} Latch Setup and Hold Delays

	Constraint (ps) by Performance Level		erformance Level		
Data / Clock	Condition ¹	E	Н	K	
D 04 / OL K	Setup	5	68	42	
D 01 / CLK	Hold	6	14	2	
D 40 / OL 14	Setup	196	199	196	
D 10 / CLK Hold	-162	-153	-163		

^{1.} Setup and hold are calculated using nominal case conditions (1.8 V, 25°C; clock and data slew rate = 200 ps).

5.4.5 Cell Specifications

Table 5-19. Cell DFFSR_{PL} Capacitance

	Capacitance (fF) by Performance Level				
Input / Output Pins	Е	Н	К		
CLK	11.6	11.6	11.6		
D	5.2	5.2	5.2		
Q	128.3	475.1	1275.6		
QBAR	128.9	516.5	1169.1		
RN	5.3	5.4	5.4		
S	5.2	5.3	5.3		

Table 5-20. Cell DFFSR_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
E	12.32		
Н	13.44	6.72	
К	16.79		



5.5 LATSR_{PL} Cell

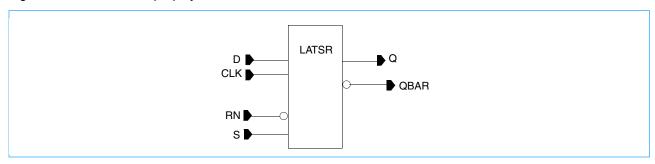
5.5.1 Function

Latch with Q and QBAR outputs, asynchronous set, and -asynchronous reset

5.5.2 Description

This is a polarity-hold latch with asynchronous set and reset functions. S and RN are the set and reset inputs respectively. If S = 1, the Q output is forced to a '1' (set). If RN = 0, the Q output is forced to a '0' (reset). The set function is dominant.

Figure 5-5. Cell LATSR_{PL} Symbols



5.5.3 DFF Truth Table

Table 5-21. Cell LATSR_{PL} Truth Table

Inputs				Out	puts
CLK	D	RN	S	Q	QBAR
х	х	0	0	0	1
0	х	1	0	-	-
1	0	x	0	0	1
х	х	x	1	1	0
1	1	1	х	1	0



5.5.4 Delay Tables

Table 5-22. Cell LATSR_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process $(ns)^1$ V_{DD} 1.8 V T_j 25°C
	011/ 0	t _{PHH}	0.145
	CLK-Q	t _{PHL}	0.162
	5.0	t _{PHH}	0.198
	D-Q	t _{PLL}	0.212
	RN-Q	t _{PLL}	0.340
_	S-Q	t _{PHH}	0.184
E	OLIK ODAD	t _{PHH}	0.280
	CLK-QBAR	t _{PHL}	0.225
	5.0545	t _{PLH}	0.332
	D–QBAR	t _{PHL}	0.278
	RN-QBAR	t _{PLH}	0.491
	S-QBAR	t _{PHL}	0.260
		t _{PHH}	0.173
	CLK-Q	t _{PHL}	0.175
	D-Q	t _{PHH}	0.224
		t _{PLL}	0.230
	RN-Q	t _{PLL}	0.385
	S-Q	t _{PHH}	0.204
Н		t _{PHH}	0.362
	CLK-QBAR	t _{PHL}	0.290
		t _{PLH}	0.418
	D-QBAR	t _{PHL}	0.342
	RN-QBAR	t _{PLH}	0.628
	S-QBAR	t _{PHL}	0.313
	011/ 0	t _{PHH}	0.291
	CLK-Q	t _{PHL}	0.339
	2.5	t _{PHH}	0.346
.,	D-Q	t _{PLL}	0.389
K	RN-Q	t _{PLL}	0.552
	S-Q	t _{PHH}	0.320
	011/ 0-:-	t _{PHH}	0.249
	CLK-QBAR	t _{PHL}	0.223

CMRF7SF1.8V12_sequential.fm February 22, 2010—IBM Confidential



Table 5-22. Cell LATSR_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C		
	D-QBAR	t _{PLH}	0.300		
K	D-QDAN	t _{PHL}	0.277		
N	RN-QBAR	t _{PLH}	0.453		
	S-QBAR	t _{PHL}	0.252		
Minimum input transition and minimum output load. See .lib timing files for more information.					

Table 5-23. Cell LATSR_{PL} Latch Setup and Hold Delays

		Constraint (ps) by F	Constraint (ps) by Performance Level			
Data / Clock	Condition ¹	E	Н	К		
D 01 / CLK	Setup	239	274	245		
D 01 / CLK	Hold	-227	-270	-238		
D 40 / OL K	Setup	225	281	224		
D 10 / CLK	Hold	-217	-278	-222		

5.5.5 Cell Specifications

Table 5-24. Cell LATSR_{PL} Capacitance

	Capacitance (fF) by Performance Level			
Input / Output Pins	Е	Н	К	
CLK	5.8	5.8	5.8	
D	7.7	7.6	7.6	
Q	262.0	565.0	922.2	
QBAR	239.5	498.0	971.2	
RN	5.6	5.6	5.6	
S	10.4	10.3	10.4	

Table 5-25. Cell LATSR_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
E	7.84		
Н	8.96	6.72	
К	12.88		



5.6 SDFF_{PL} Cell

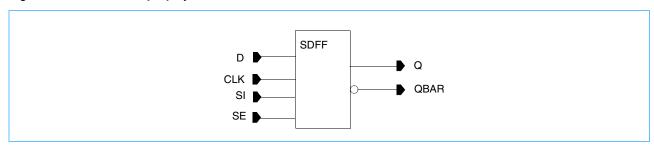
5.6.1 Function

Scannable DFF, Q, and QBAR outputs

5.6.2 Description

This cell is a positive edge-triggered scannable D flip-flop with true and complement outputs. When the scan enable pin is high, the latch is in scan mode. Setting the scan enable pin low enables the latch for normal operation.

Figure 5-6. Cell SDFF_{PL} Symbols



5.6.3 DFF Truth Table

Table 5-26. Cell SDFF_{PL} Truth Table

	Inputs			Out	puts
CLK	D	SE	SI	Q	QBAR
(01)	0	х	0	0	1
(01)	x	1	0	0	1
(01)	1	х	1	1	0
(01)	x	1	1	1	0
(01)	0	0	х	0	1
(01)	1	0	х	1	0
(1x)	х	х	х	_	_
(x0)	x	х	х	_	_



5.6.4 Delay Tables

Table 5-27. Cell SDFF_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	$\begin{array}{cc} \text{Nominal Process (ns)}^1 \\ \text{V}_{DD} & \text{1.8 V} \\ \text{T}_j & \text{25}^{\circ}\text{C} \end{array}$
	CLK-Q	t _{PHH}	0.226
E	CLK-Q	t _{PHL}	0.160
E	CLK-QBAR	t _{PHH}	0.106
	OLK-QDAN	t _{PHL}	0.165
	CLK-Q	t _{PHH}	0.261
Н		t _{PHL}	0.197
П	CLK-QBAR	t _{PHH}	0.125
		t _{PHL}	0.169
	CLK-Q	t _{PHH}	0.264
К	OLN-Q	t _{PHL}	0.188
K	CLK-QBAR	t _{PHH}	0.274
	OLN-QDAN	t _{PHL}	0.345

Table 5-28. Cell SDFF_{PL} Latch Setup and Hold Delays

		Constraint (ps) by I	y Performance Level		
Data / Clock	Condition ¹	E	Н	К	
D 01 / CL K	Setup	57	62	47	
D 01 / CLK	Hold	-15	-9	-19	
D 10 / CL K	Setup	208	210	201	
D 10 / CLK	Hold	-178	-176	-177	
1. Setup and	hold are calculated	using nominal case con-	ditions (1.8 V, 25°C; clock and o	lata slew rate = 200 ps).	

5.6.5 Cell Specifications

Table 5-29. Cell SDFF_{PL} Capacitance

	Capacitance (fF) by Performance Level			
Input / Output Pins	E	Н	К	
CLK	11.1	11.0	10.9	
D	11.0	11.2	10.8	
Q	236.7	462.2	1157.9	
QBAR	247.7	516.5	1182.3	
SE	6.8	6.8	7.4	
SI	9.6	9.7	9.0	



Table 5-30. Cell SDFF_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
E	11.20		
Н	12.32	6.72	
К	15.68		



5.7 SDFFR_{PL} Cell

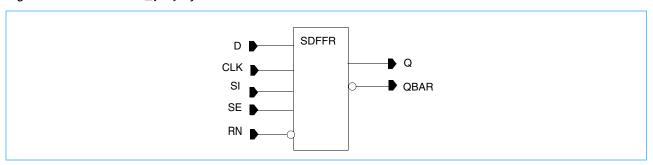
5.7.1 Function

Scannable DFF, Q, and QBAR outputs, -asynchronous reset

5.7.2 Description

This cell is a positive edge-triggered scannable D flip-flop with asynchronous inputs and a reset function. If RN = 0, the Q output is forced to '0' (reset) and the QBAR output is forced to '1'.

Figure 5-7. Cell SDFFR_{PL} Symbols



5.7.3 DFF Truth Table

Table 5-31. Cell SDFFR_{PL} Truth Table

	Inputs					puts
CLK	D	RN	SE	SI	Q	QBAR
х	х	0	х	х	0	1
(01)	1	1	x	1	1	0
(01)	x	1	1	1	1	0
(01)	1	1	0	х	1	0
(1x)	x	1	x	x	-	-
(x0)	x	1	x	x	-	-
(01)	0	x	x	0	0	1
(01)	x	х	1	0	0	1
(01)	0	х	0	x	0	1



5.7.4 Delay Tables

Table 5-32. Cell SDFFR_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	$ \begin{array}{ccc} \text{Nominal Process (ns)}^1 \\ \text{V}_{\text{DD}} & \text{1.8 V} \\ \text{T}_{j} & \text{25}^{\circ}\text{C} \end{array} $
	RN-Q	t _{PLL}	0.238
	CLK-Q	t _{PHH}	0.289
E -	CLK-Q	t _{PHL}	0.182
<u> </u>	RN-QBAR	t _{PLH}	0.184
	CLK-QBAR	t _{PHH}	0.121
	CLK-QDAN	t _{PHL}	0.188
	RN-Q	t _{PLL}	0.266
	CLK-Q	t _{PHH}	0.344
Н		t _{PHL}	0.221
11	RN-QBAR	t _{PLH}	0.195
	CLK-QBAR	t _{PHH}	0.141
	OLN-QDAN	t _{PHL}	0.198
	RN-Q	t _{PLL}	0.284
	CLK-Q	t _{PHH}	0.333
К	OLN-Q	t _{PHL}	0.217
K	RN-QBAR	t _{PLH}	0.373
	CLK-QBAR	t _{PHH}	0.306
	OLN-QDAN	t _{PHL}	0.419

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-33. Cell SDFFR_{PL} Latch Setup and Hold Delays

		Constraint (ps) by Performance Level			
Data / Clock	Condition ¹	E	Н	К	
D 01 / CLK	Setup	122	15	81	
D 01 / CLK	Hold	-17	-11	-25	
D 10 / CL K	Setup	204	206	207	
D 10 / CLK	Hold	-172	-168	-175	

^{1.} Setup and hold are calculated using nominal case conditions (1.8 V, 25°C; clock and data slew rate = 200 ps).



5.7.5 Cell Specifications

Table 5-34. Cell SDFFR_{PL} Capacitance

	Capacitance (fF) by Performance Level			
Input / Output Pins	Е	Н	К	
CLK	12.2	12.2	12.2	
D	10.8	10.8	10.8	
Q	236.1	483.3	1271.0	
QBAR	261.2	515.5	1179.0	
RN	7.6	7.7	7.6	
SE	7.5	7.5	7.5	
SI	9.0	9.0	9.0	

Table 5-35. Cell SDFFR_{PL} Area

	Cell Dimensions (μm)	
Performance Level	Width	Length
E	12.88	
Н	14.00	6.72
К	17.36	



5.8 SDFFS_{PL} Cell

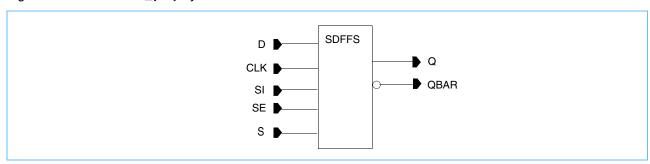
5.8.1 Function

Scannable DFF, Q, and QBAR outputs, asynchronous set

5.8.2 Description

This cell is a positive edge-triggered scannable D flip-flop with asynchronous inputs and a set function. If S = 1, the Q output is forced to '1' (set) and the QBAR output is forced to '0'.

Figure 5-8. Cell SDFFS_{PL} Symbols



5.8.3 DFF Truth Table

Table 5-36. Cell SDFFS_{PL} Truth Table

	Inputs					puts
CLK	D	S	SE	SI	Q	QBAR
(01)	0	0	х	0	0	1
(01)	х	0	1	0	0	1
(01)	0	0	0	х	0	1
(01)	1	x	x	1	1	0
(01)	х	х	1	1	1	0
(01)	1	x	0	х	1	0
(1x)	x	0	x	х	-	-
(x0)	х	0	х	х	-	-
х	x	1	x	х	1	0



5.8.4 Delay Tables

Table 5-37. Cell SDFFS_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	S–Q	t _{PHH}	0.229
	CLK-Q	t _{PHH}	0.278
E -	CLK-Q	t _{PHL}	0.183
_	S-QBAR	t _{PHL}	0.167
	CLK-QBAR	t _{PHH}	0.125
	CLN-QDAN	t _{PHL}	0.197
	S-Q	t _{PHH}	0.272
	CLK-Q	t _{PHH}	0.331
н	CLK-Q	t _{PHL}	0.226
П	S-QBAR	t _{PHL}	0.177
	CLK-QBAR	t _{PHH}	0.147
	ULK-QDAN	t _{PHL}	0.193
	S-Q	t _{РНН}	0.276
	CLK O	t _{PHH}	0.319
K	CLK-Q	t _{PHL}	0.216
r\	S-QBAR	t _{PHL}	0.360
	CLK-QBAR	t _{PHH}	0.304
	ULN-WDAN	t _{PHL}	0.404

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-38. Cell SDFFS_{PL} Latch Setup and Hold Delays

		Constraint (ps) by P	Constraint (ps) by Performance Level				
Data / Clock	Condition ¹	E	Н	К			
D 01 / CLK Setup	80	111	69				
	-18	-14	-25				
Setup	Setup	212	210	206			
D 10 / CLK	Hold	-185	-177	-183			

^{1.} Setup and hold are calculated using nominal case conditions (1.8 V, 25°C; clock and data slew rate = 200 ps).



5.8.5 Cell Specifications

Table 5-39. Cell SDFFS_{PL} Capacitance

	Capacitance (fF) by Performance Level				
Input / Output Pins	Е	Н	K		
CLK	11.5	11.8	11.7		
D	11.1	10.8	10.8		
Q	235.8	489.0	1261.7		
QBAR	244.9	545.1	1179.5		
S	7.7	7.5	7.5		
SE	6.9	7.5	7.5		
SI	9.6	9.0	9.0		

Table 5-40. Cell SDFFS_{PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
E	13.44		
Н	14.56	6.72	
К	17.92		



5.9 SDFFSR_{PL} Cell

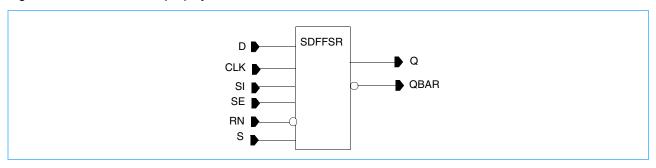
5.9.1 Function

Scannable DFF, Q, and QBAR outputs, asynchronous set, -asynchronous reset

5.9.2 Description

This cell is a positive edge-triggered scannable D flip-flop with asynchronous inputs, and set and reset functions. S and RN are the set and reset inputs, respectively. If S = 1, the Q output is forced to '1' (set). If RN = 0, the Q output is forced to '0' (reset). The set function is dominant.

Figure 5-9. Cell SDFFSR_{PL} Symbols



5.9.3 DFF Truth Table

Table 5-41. Cell SDFFSR_{PL} Truth Table

	Inputs					Out	puts
CLK	D	RN	S	SE	SI	Q	QBAR
х	Х	0	0	х	х	0	1
(1x)	х	1	0	х	х	_	_
(x0)	х	1	0	х	х	_	_
(01)	0	х	0	х	0	0	1
(01)	х	х	0	1	0	0	1
(01)	0	х	0	0	х	0	1
х	х	х	1	х	х	1	0
(01)	1	1	х	х	1	1	0
(01)	х	1	х	1	1	1	0
(01)	1	1	х	0	х	1	0



5.9.4 Delay Tables

Table 5-42. Cell SDFFSR_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	RN-Q	t _{PLL}	0.256
	S-Q	t _{PHH}	0.276
	CLK-Q	t _{PHH}	0.261
E	CLN-Q	t _{PHL}	0.163
<u> </u>	RN-QBAR	t _{PLH}	0.223
	S-QBAR	t _{PHL}	0.197
	CLK-QBAR	t _{PHH}	0.126
	CLK-QDAN	t _{PHL}	0.174
	RN-Q	t _{PLL}	0.303
	S-Q	t _{PHH}	0.312
	CLK-Q	t _{PHH}	0.297
Н	OLK-Q	t _{PHL}	0.220
П	RN-QBAR	t _{PLH}	0.223
	S-QBAR	t _{PHL}	0.218
	CLK-QBAR	t _{PHH}	0.136
	CLK-QBAR	t _{PHL}	0.188
	RN-Q	t _{PLL}	0.329
	S-Q	t _{PHH}	0.327
	CLK-Q	t _{PHH}	0.315
ĸ	ULN-W	t _{PHL}	0.229
r,	RN-QBAR	t _{PLH}	0.423
	S-QBAR	t _{PHL}	0.410
	CLK-QBAR	t _{PHH}	0.322
	ULK-UBAH	t _{PHL}	0.399

^{1.} Minimum input transition and minimum output load. See .lib timing files for more information.



Table 5-43. Cell SDFFSR_{PL} Latch Setup and Hold Delays

		Constraint (ps) by Performance Level				
Data / Clock	Condition ¹	E	Н	К		
D 01 / CLK Setup	73	91	65			
	Hold	-15	-8	-18		
D 10 / CLK Setup Hold	Setup	220	218	216		
	Hold	-184	-18	-186		

5.9.5 Cell Specifications

Table 5-44. Cell SDFFSR_{PL} Capacitance

	Capacitance (fF) by Performance Level				
Input / Output Pins	E	Н	К		
CLK	11.6	11.6	11.6		
D	10.8	10.8	10.8		
Q	128.2	474.6	1273.4		
QBAR	128.8	515.8	1171.3		
RN	5.4	5.4	5.4		
S	5.2	5.3	5.3		
SE	7.5	7.5	7.5		
SI	9.0	9.0	9.0		

Table 5-45. Cell SDFFSR_{PL} Area

	Cell Dimensions (μm)			
Performance Level	Width	Length		
E	15.68			
Н	16.80	6.72		
К	20.16			



5.10 SLATSR_{PL} Cell

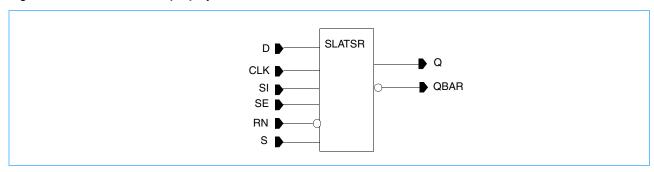
5.10.1 Function

Scannable latch with Q and QBAR outputs, asynchronous set, -asynchronous reset

5.10.2 Description

This cell is a scannable polarity-hold latch with asynchronous set and reset functions. S and RN are the set and reset inputs, respectively. The scan enable pin selects data or scan input. If S = 1, the Q output is forced to '1' (set). If RN = 0, the Q output is forced to '0' (reset). The set function is dominant.

Figure 5-10. Cell SLATSR_{PL} Symbols



5.10.3 DFF Truth Table

Table 5-46. Cell SLATSR_{PL} Truth Table

	Inputs						puts
CLK	D	RN	S	SE	SI	Q	QBAR
Х	х	0	0	х	х	0	1
0	х	1	0	х	х	_	-
1	0	х	0	х	0	0	1
1	х	х	0	1	0	0	1
1	0	х	0	0	х	0	1
Х	х	х	1	х	х	1	0
1	1	1	х	х	1	1	0
1	х	1	х	1	1	1	0
1	1	1	х	0	х	1	0



5.10.4 Delay Tables

Table 5-47. Cell SLATSR_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V_{DD} 1.8 V T_j 25°C
	CLK-Q	t _{PHH}	0.145
	CLK-Q	t _{PHL}	0.162
	D-Q	t _{PHH}	0.236
	D-Q	t _{PLL}	0.244
	RN-Q	t _{PLL}	0.341
	S-Q	t _{PHH}	0.184
		t _{PHH}	0.390
	SE-Q	t _{PLL}	0.304
	5E-Q	t _{PLH}	0.262
		t _{PHL}	0.311
	SI-Q	t _{PHH}	0.332
E	SI-Q	t _{PLL}	0.300
E	CLK ODAD	t _{PHH}	0.281
	CLK-QBAR	t _{PHL}	0.225
	D-QBAR	^t PLH	0.364
	D-QBAR	t _{PHL}	0.316
	RN-QBAR	t _{PLH}	0.493
	S-QBAR	t _{PHL}	0.260
		t _{PLH}	0.424
	CE OBAD	t _{PHL}	0.471
	SE-QBAR	t _{PHH}	0.432
		t _{PLL}	0.342
	SI-QBAR	t _{PLH}	0.420
	3I-QDAN	t _{PHL}	0.412
	CLK-Q	t _{РНН}	0.172
н	OLN-Q	t _{PHL}	0.175
П	D-Q	t _{РНН}	0.261
	D-Ø	t _{PLL}	0.262

 $^{1. \ \} Minimum\ input\ transition\ and\ minimum\ output\ load.\ See\ . lib\ timing\ files\ for\ more\ information.$



Table 5-47. Cell SLATSR_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns V _{DD} 1.8 V T _j 25°C
	RN-Q	t _{PLL}	0.386
	S-Q	t _{PHH}	0.205
		t _{PHH}	0.418
	SE-Q	t _{PLL}	0.322
	SE-Q	t _{PLH}	0.288
		t _{PHL}	0.329
	SI-Q	t _{PHH}	0.360
	SI-Q	t _{PLL}	0.318
	CLK ODAD	t _{PHH}	0.362
11	CLK-QBAR	t _{PHL}	0.290
Н	D. ODAD	t _{PLH}	0.450
	D-QBAR	t _{PHL}	0.380
	RN-QBAR	t _{PLH}	0.631
	S-QBAR	t _{PHL}	0.314
		t _{PLH}	0.510
	CE ODAD	t _{PHL}	0.536
	SE-QBAR	t _{PHH}	0.518
		t _{PLL}	0.407
	SI-QBAR	t _{PLH}	0.506
		t _{PHL}	0.478
	CLK-Q	t _{PHH}	0.291
		t _{PHL}	0.339
	D 0	t _{PHH}	0.384
	D-Q	t _{PLL}	0.422
	RN-Q	t _{PLL}	0.553
	S-Q	t _{PHH}	0.321
V		t _{PHH}	0.538
К	05.0	t _{PLL}	0.481
	SE-Q	t _{PLH}	0.410
		t _{PHL}	0.488
	01.0	t _{PHH}	0.481
	SI-Q	t _{PLL}	0.477
	CLK CDAD	t _{PHH}	0.249
	CLK-QBAR	t _{PHL}	0.223

CMRF7SF1.8V12_sequential.fm February 22, 2010—IBM Confidential



Table 5-47. Cell SLATSR_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) ¹ V _{DD} 1.8 V T _j 25°C
	D-QBAR	t _{PLH}	0.332
	D-QDAN	t _{PHL}	0.315
	RN-QBAR	t _{PLH}	0.455
	S-QBAR	t _{PHL}	0.253
к		t _{PLH}	0.391
	SE-QBAR	t _{PHL}	0.470
		t _{PHH}	0.399
		t _{PLL}	0.341
	SI-QBAR	t _{PLH}	0.387
	SI-QDAN	t _{PHL}	0.412

Table 5-48. Cell SLATSR_{PL} Latch Setup and Hold Delays

		Constraint (ps) by Performance Level			
Data / Clock	Condition ¹	E	Н	К	
D 01 / CL K	Setup	276	313	281	
D 01 / CLK	Hold	-265	-310	-274	
D 40 / OL K	Setup	259	316	258	
D 10 / CLK	Hold	-253	-314	-257	

5.10.5 Cell Specifications

Table 5-49. Cell SLATSR_{PL} Capacitance

	Capacitance (fF) by Performance Level		
Input / Output Pins	E	Н	K
CLK	5.8	5.8	5.8
D	13.6	13.6	13.6
Q	261.7	564.1	917.1
QBAR	240.9	495.5	969.2
RN	5.7	5.6	5.6
S	10.5	10.3	10.4
SE	6.1	6.1	6.1
SI	11.2	11.2	11.1



Table 5-50. Cell SLATSR_{PL} Area

	Cell Dimensions (μm)	
Performance Level	Width	Length
E	11.20	
Н	12.32	6.72
К	16.24	





6. Physical Design Cells

6.1 DECAP_{PL} Cell

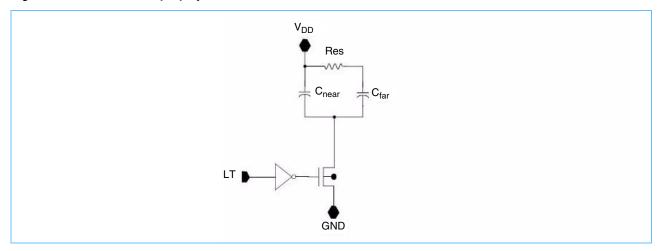
6.1.1 Function

V_{DD}-to-GND decoupling capacitor

6.1.2 Description

This cell is an NFET in n-well capacitor that can be placed on a chip to provide local noise decoupling from V_{DD} to GND. It should be uniformly distributed about the chip but placed near switching circuits. The LT pin is used at test to eliminate potential leakage current. The slew of the LT pin is noncritical. The DECAP cell is modeled as a pi network, where C_{near} is defined as the capacitance closest to the switching event. Be aware that these cells have high a polysilicon density that can cause checking concerns at the chip level. Blocks of DECAP cells should not exceed 3 mm² because they could affect the lithography of neighboring devices.

Figure 6-1. Cell DECAP_{PL} Symbols



6.1.3 Truth Table

Table 6-1. Cell DECAP_{PL} Truth Table

Input	
LT	Mode
0	Decoupling, normal mode
1	Leakage test, decoupling off



6.2 FILL{1,2} Cell

6.2.1 Function

One- and two-cell postfill cells

6.2.2 Description

One- and two-cell postfill cells are used during the physical design process. After design placement is completed, there are gaps left in unused areas of the layout. These gaps must be filled to provide n-well and power bus continuity. The available filler cells come in various sizes to fit different gaps. A typical physical design postfill strategy is to fill the largest gaps first with the largest filler cells, then repeat the process with subsequently smaller filler cells. By the time the process is repeated with the one-cell filler cell, all unused gaps in the layout are filled.

There are no active devices in FILL1 or FILL2. See *Section 6.4 GAUNUSEDxxx Cell* on page 232 for larger filler cells.

6.2.3 Cell Specifications

Table 6-2. Cell FILL{1,2} Area

	Cell Dimensions (μm)		
Cell	Width	Length	
FILL1	0.56	6.72	
FILL2	1.12	6.72	



6.3 FGTIE_{PL} Cell

6.3.1 Function

Floating gate tie-off

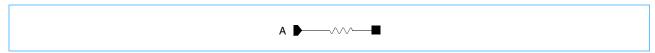
6.3.2 Description

This cell is used during physical design to correct antenna violations. Antenna violations can occur when large amounts of metal wiring are tied to polysilicon gates without being tied to diffusion for a specified length. During manufacturing, charge can build up on the metal and be discharged to the floating gate and damage the thin oxide under the gate.

Most physical design tools correct antenna violations in one of two ways. One way is to alter the wiring levels used in order to prevent large sections of M1 from being tied directly to a gate. The other way is to insert a diode near the gate to dissipate the charge into the substrate. This cell can be used to accomplish the latter. The input is essentially tied to a floating diffusion, which forms a diode with the substrate.

Physical design software typically inserts this cell automatically when necessary. However, these cells can also be manually placed in close proximity to cells with antenna violations.

Figure 6-2. Cell FGTIE_{PL} Symbols



6.3.3 Cell Specifications

Table 6-3. Cell FGTIE_{PL} Capacitance

	Capacitance (fF) by Performance Level	
Input Pin	A	
A	0	

Table 6-4. Cell FGTIE {PL} Area

	Cell Dimensions (μm)		
Performance Level	Width	Length	
А	1.68	6.72	



6.4 GAUNUSEDxxx Cell

6.4.1 Function

Gate array postfill cells

6.4.2 Description

Gate array post-fill cells are used during the postfill physical design process. After design placement is completed, there are gaps left in unused areas of the layout. These gaps must be filled to provide n-well and power bus continuity. Available filler cells come in various sizes to fit different gaps. A typical physical design post-fill strategy is to fill the largest gaps first with the largest filler cells, then repeat the process with subsequently smaller filler cells. By the time the process is repeated with the one-cell filler cell, all unused gaps in the layout are filled.

The GAUNUSED cells contain gate array background shapes, including spare transistors. A supported engineering change order physical design methodology replaces these spare cells with gate array cells, requiring only a back-end of the line mask change. See *Section 6.2 FILL{1,2} Cell* for smaller fill cells.

6.4.3 Cell Specifications

Table 6-5. Cell GAUNUSEDxxx Area

	Cell Dimer	Cell Dimensions (μm)	
Cell	Width	Length	
GAUNUSED003	1.68		
GAUNUSED006	3.36	6.72	
GAUNUSED012	6.72		
GAUNUSED024	13.44		
GAUNUSED048	26.88		
GAUNUSED096	53.76		