CMOS 7RF (CMRF7SF) 1.8 V (12-Track) Standard Cell Databook

Foundry IP

Advance

February 22, 2010—IBM Confidential

Printed in the United States of America February 2010

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CMRF7SF1.8V12_title.fm
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Revision Log

Revision Date	Pages	Description
February 22, 2010	–	Initial release (00).

1. Overview

This databook describes the IBM CMOS 7RF digital product family, which consists of standard cell products implemented in a 0.18 μm lithography process. CMOS 7RF uses up to six levels of metal wiring.

This section summarizes the standard cells, including logical and electrical information. The terminology, symbology, and data presented throughout this databook are defined. Five types of cells are presented in the following sections:

- Primitive logic
- Complex logic
- Unique logic
- Sequential logic
- Physical design cells

The databook is intended to be used in conjunction with the IBM CMRF7SF Design Kit. Contact your IBM technical representative for more information.

1.1 Technology Features

Table 1-1. General Characteristics

Characteristic	Description
Technology	CMOS 7RF
NFET L_{eff}	0.145 ± 0.017 μm
PFET L_{eff}	0.145 ± 0.017 μm
Supply voltage	1.8 V ± 10%
Ambient operating temperature range	-55°C to 100°C
Junction temperature range	-40°C to 125°C
Storage temperature range	-65°C to 150°C
Wiring levels	Four to eight for MA last metal Three to seven for AM / ML last metal
Cell length	6.72 μm

1.2 Cell Naming Conventions

There are two main parts to cell names.

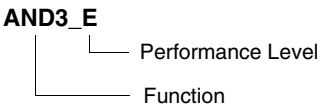
- Function: Describes the basic Boolean function for the primitive, complex, unique, and latch cells (see *Section 1.12 CMOS 7RF 1.8 V (12-Track) Cells and Functions* on page 27).
- Performance level: Designates A through U with an underscore separating the performance level from the library type. In this databook, each cell name includes “{PL}” as a placeholder for the performance level. The delay and capacitance tables for each cell show the different values for each performance level offered for that cell. See *Section 1.5* on page 23 for more information on performance cells.

The full cell name is *Function_{Performance Level}. Figure 1-1* shows an example.

Cell name AND3_E

Description Three-way AND, performance level E

Figure 1-1. Cell Naming Convention Example



1.3 Pin Naming Conventions

Table 1-2 describes the functions of the cell pins used in the CMOS 7RF 1.8 V standard cells.

Table 1-2. I/O Pin Naming Conventions

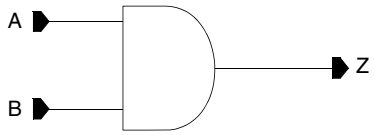
Pin	Description	Notes
A, A1, A2, A3, A4, B, B1, B2, B3, B4, C, C1, C2 D, D0, D1, D2, D3 J, K	Data input pins	1
CIN	Carry input pin for ADDF cells	
CLK, C	Clock pin for latches	1
COUT	Carry output pin for ADDF cells	
E	Enable pin for clock gating cells (input)	
GCK	Gated clock pin for clock gating cells (output)	
GND	Ground pin	
Q	Latch output pin	
QBAR	Latch output pin (Q complement)	
QN	Latch output pin (Q complement)	
RN	Asynchronous reset or clear (negative active)	
S	Set pin (input)	
SD, SD1, SD2	Multiplexer selection pin (input)	
SE	Scan enable pin (input)	
SI	Scan input pin	
SN	Asynchronous set of preset (negative active)	
SUM	Output pin for ADDF cells	
VDD	Power pin	
Z	Output pin	

1. The C pin can be either a data input pin or a clock pin. See the description of the specific cell to verify the function of the C pin.

1.4 Using Logic Symbols

Each cell subsection includes a symbols figure that shows the input and output pins. These symbols correspond to the symbols available in the IBM CMRF7SF Design Kit.

Figure 1-2. Cell AND2_{PL} Symbols



1.5 Performance Levels

Most cells are available in multiple performance levels. The performance levels are identified by A through U. An “A” performance level is used to drive the smallest loads efficiently; a “U” performance level is used to drive the largest loads efficiently. Performance levels can also be used to denote nonoverlap (not drive strength) of clock splitters or delay elements. The delay tables and input pin capacitance tables display the data for each performance level of a given cell. *Table 1-3* can be used as a capacitance estimation for running electrical simulations. For accurate timing analysis, refer to the IBM CMOS 7RF 1.8 V Library (.lib) timing files.

Table 1-3. Nominal Load Capacitance by Performance Level

Performance Level	Capacitance (fF)
A	15
B	17
C	27
D	35
E	43
F	61
H	74
I	89
J	114
K	130
L	141
M	185
N	221
O	247
Q	458
U	408

1.6 Truth Tables

Table 1-4 shows an example of a truth table for a typical cell. *Table 1-5* shows the symbols used to define several possible logic states in the tables.

Table 1-4. Cell DFF_{PL} Truth Table Example

Inputs		Outputs	
CLK	D	Q	QBAR
(01)	0	x	0
(01)	1	x	1
(1x)	x	x	–
(x0)	x	x	–

Table 1-5. Truth Table Legend

Logic Symbol	Meaning
0	Forcing a logic ‘0’
1	Forcing a logic ‘1’
–	No change
x	“Don’t care” input state
(01)	Clock rising edge
(1x)	If the clock starts as a 1, the Q+ output does not change
(x0)	If the clock ends as a 0, the Q+ output does not change

1.7 Propagation Delay Tables

Note: The delay and timing information for each cell is provided for estimation purposes only. The delays shown are from the nominal case. Propagation delay timing calculations are representative values at the beginning of the product's life. This timing data can degrade over the product's lifetime.

Propagation delays are presented for each cell as a function of load capacitance. Please see the .lib timing files for details about load capacitance and input transition times.

Table 1-6. Input Transition Times

Cell Types	Transition Times
Latches	200 ps
Primitives, complex, and unique cells	

The delay table is used to estimate delays for a given path. *Table 1-7* defines the terms used in the delay tables and *Table 1-8* is an example of a propagation delay table.

Table 1-7. Propagation Delay Table Terminology

Term	Definition
Parameter	t_{PHH} = Input going high (from 0 to 1) and output going high (from 0 to 1) t_{PHL} = Input going high (from 0 to 1) and output going low (from 1 to 0) t_{PLH} = Input going low (from 1 to 0) and output going high (from 0 to 1) t_{PLL} = Input going low (from 1 to 0) and output going low (from 1 to 0)
Path	Input pin to output pin logic path.
Performance level	A, B, C

Table 1-8. Cell Propagation Delays

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns) V_{DD} 1.8 V T_j 25°C
A	A-Z	t_{PLH}	0.114
		t_{PHL}	0.120
	B-Z	t_{PLH}	0.111
		t_{PHL}	0.129
B	A-Z	t_{PLH}	0.120
		t_{PHL}	0.120
	B-Z	t_{PLH}	0.111
		t_{PHL}	0.129

1.8 Setup and Hold Delays

Table 1-9 shows an example of sequential logic setup and hold delays using the standard cell D flip-flop (DFF). Setup and hold times are calculated using nominal case conditions, with the clock and data slew rate at 200 ps.

Table 1-9. Cell DFF_{PL} Latch Setup and Hold Delays

Data / Clock	Condition[1]	Constraint (ps) by Performance Level		
		E	H	K
D 01 / CLK	Setup	031	035	026
	Hold	009	014	002
D 10 / CLK	Setup	182	183	179
	Hold	-149	-147	-151

1. Setup and hold are calculated using nominal case conditions (1.8 V, 25°C; clock and data slew rate = 200 ps.)

1.9 Physical Design Cells

Special cells for physical design are included in the IBM CMRF7SF Design Kit. Use of these cells is specific to the physical design flow and is described in a separate application note for the CMOS 7RF physical design methodology. Contact your IBM technical representative for more information.

Cells available for physical design include:

- N-well/substrate contacts
- Floating-gate diodes (for correcting antenna violations)
- Filler cells
- Decoupling capacitors

Use of floating-gate diodes is optional. If used, they should exist in the schematic netlist for layout versus schematic (LVS) checking. Use of the n-well/substrate contacts and filler cells is governed by a set methodology; these cells are masked during LVS checking.

1.10 Optional Output Pins

The ADFF_{PL} cell has optional output pins. *Table 1-10* lists the optional pin group, affected pins, and the minimum and maximum number of pins that may be used. For example, an instantiation of a full adder can use SUM, COUT, or both SUM and COUT.

Table 1-10. CMOS 7RF Library Cells with “Optional” Outputs

Function	Cell Name	Outputs	(Pin Group): (Minimum number of pins, maximum number of pins)
Full adder	ADDF_{PL}	SUM, COUT	(SUM, COUT): (1,2)

1.11 Unused Input Pins

Input pins that are not used should be tied down. If an unused pin needs to be tied up, an inverter and tie-down cell combination is recommended. Contact your IBM technical representative for more information.

1.12 CMOS 7RF 1.8 V (12-Track) Cells and Functions

Table 1-11 lists the CMOS 7RF 1.8 V (12-track) library cells and their functions.

Table 1-11. CMOS 7RF 1.8 V (12-Track) Cell Functions (Page 1 of 3)

Cell	Function
Standard Cell Primitive Logic	
AND2_{PL}	Two-way AND
AND3_{PL}	Three-way AND
AND4_{PL}	Four-way AND
INVERT_{PL}	Inverter
NAND2_{PL}	Two-way NAND
NAND3_{PL}	Three-way NAND
NAND4_{PL}	Four-way NAND
NOR2_{PL}	Two-way NOR
NOR3_{PL}	Three-way NOR
NOR4_{PL}	Four-way NOR
OR2_{PL}	Two-way OR
OR3_{PL}	Three-way OR
OR4_{PL}	Four-way OR
XNOR2_{PL}	Two-way XNOR
XNOR3_{PL}	Three-way XNOR
XOR2_{PL}	Two-way XOR
XOR3_{PL}	Three-way XOR
Standard Cell Complex Logic	
AO21_{PL}	2 × 1 AND OR
AO22_{PL}	2 × 2 AND OR
AO33_{PL}	3 × 3 AND OR
AO44_{PL}	4 × 4 AND OR
AO222_{PL}	2 × 2 × 2 AND OR
AO2222_{PL}	2 × 2 × 2 × 2 AND OR
AOI21_{PL}	2 × 1 AND OR inverter
AOI22_{PL}	2 × 2 AND OR inverter
AOI33_{PL}	3 × 3 AND OR inverter
AOI44_{PL}	4 × 4 AND OR inverter

Table 1-11. CMOS 7RF 1.8 V (12-Track) Cell Functions (Page 2 of 3)

Cell	Function
AOI222_{PL}	2 × 2 × 2 AND OR inverter
AOI2222_{PL}	2 × 2 × 2 × 2 AND OR inverter
OA21_{PL}	2 × 1 OR AND
OA22_{PL}	2 × 2 OR AND
OA222_{PL}	2 × 2 × 2 OR AND
OA2222_{PL}	2 × 2 × 2 × 2 OR AND
OAI21_{PL}	2 × 1 OR AND inverter
OAI22_{PL}	2 × 2 OR AND inverter
OAI222_{PL}	2 × 2 × 2 OR AND inverter
OAI2222_{PL}	2 × 2 × 2 × 2 OR AND inverter
Standard Cell Unique Logic	
ADDF_{PL}	Full adder
BUFFER_{PL}	Buffer
CLK_{PL}	Clock driver
CLKI_{PL}	Inverting clock driver
COMP2_{PL}	Two-bit comparator
DELAY4_{PL}	Delay line
DELAY6_{PL}	Delay line
MUX21_{PL}	2:1 multiplexer
MUX21I_{PL}	2:1 multiplexer with inverted output
MUX41_{PL}	4:1 multiplexer
TERM_{PL}	Net terminator
Standard Cell Sequential Logic	
DFF_{PL}	DFF with Q and QBAR outputs
DFFR_{PL}	DFF with Q and QBAR outputs, -asynchronous reset
DFFS_{PL}	DFF with Q and QBAR outputs, asynchronous set
DFFSR_{PL}	DFF with Q and QBAR outputs, asynchronous set, -asynchronous reset
SDFF_{PL}	Scannable DFF with Q and QBAR outputs
SDFFR_{PL}	Scannable DFF with Q and QBAR outputs, -asynchronous reset
SDFFS_{PL}	Scannable DFF with Q and QBAR outputs, asynchronous set
SDFFSR_{PL}	Scannable DFF Q and QBAR outputs, asynchronous set, -asynchronous reset
LATSR_{PL}	Latch with Q and QBAR outputs, asynchronous set, -asynchronous reset
SLATSR_{PL}	Scannable latch with Q and QBAR outputs, asynchronous set, -asynchronous reset

Table 1-11. CMOS 7RF 1.8 V (12-Track) Cell Functions (Page 3 of 3)

Cell	Function
Physical Design Cells	
FILL{1,2}	One- and two-cell post fill cells
FGTIE_{PL}	Floating gate tie-off
GAUNUSEDxxx	Gate array postfill cells

2. Standard Cell Primitive Logic

2.1 AND2_{PL} Cell

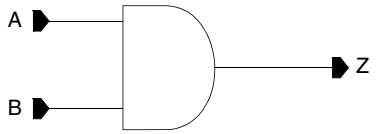
2.1.1 Function

Two-way AND

2.1.2 Description

This cell is a combinational gate, two-way AND. The Boolean expression for this cell is $Z = (A \times B)$.

Figure 2-1. Cell AND2_{PL} Symbols



2.1.3 Propagation Delay Table

Table 2-1. Cell AND2_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A–Z	t_{PHH}	0.120
		t_{PLL}	0.120
	B–Z	t_{PHH}	0.111
		t_{PLL}	0.129
C	A–Z	t_{PHH}	0.101
		t_{PLL}	0.113
	B–Z	t_{PHH}	0.093
		t_{PLL}	0.123
D	A–Z	t_{PHH}	0.092
		t_{PLL}	0.099
	B–Z	t_{PHH}	0.085
		t_{PLL}	0.108
E	A–Z	t_{PHH}	0.090
		t_{PLL}	0.098
	B–Z	t_{PHH}	0.083
		t_{PLL}	0.107

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-1. Cell AND2_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
F	A–Z	t_{PHH}	0.084
		t_{PLL}	0.096
	B–Z	t_{PHH}	0.078
		t_{PLL}	0.105
H	A–Z	t_{PHH}	0.084
		t_{PLL}	0.108
	B–Z	t_{PHH}	0.079
		t_{PLL}	0.120
I	A–Z	t_{PHH}	0.091
		t_{PLL}	0.106
	B–Z	t_{PHH}	0.084
		t_{PLL}	0.115
J	A–Z	t_{PHH}	0.096
		t_{PLL}	0.121
	B–Z	t_{PHH}	0.089
		t_{PLL}	0.130
K	A–Z	t_{PHH}	0.106
		t_{PLL}	0.121
	B–Z	t_{PHH}	0.098
		t_{PLL}	0.129

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.1.4 Cell Specifications

Table 2-2. Cell AND2_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level								
	B	C	D	E	F	H	I	J	K
A	2.6	3.3	4.6	5.1	6.7	6.6	8.0	8.8	9.4
B	2.6	3.1	4.3	4.8	6.4	6.3	7.7	8.3	9.0
Z	51.9	109.4	172.9	238.7	356.5	454.9	707.4	959.1	1208.9

Table 2-3. Cell AND2_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
B	3.36	6.72
C		
D		
E		
F		
H		
I		
J	4.48	
K		

2.2 AND3_{PL} Cell

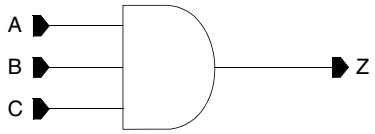
2.2.1 Function

Three-way AND

2.2.2 Description

This cell is a combinational gate, three-way AND. The Boolean expression for this cell is $Z = (A \times B \times C)$.

Figure 2-2. Cell AND3_{PL} Symbols



2.2.3 Propagation Delay Table

Table 2-4. Cell AND3_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A–Z	t_{PHH}	0.132
		t_{PLL}	0.143
	B–Z	t_{PHH}	0.130
		t_{PLL}	0.154
	C–Z	t_{PHH}	0.122
		t_{PLL}	0.164
C	A–Z	t_{PHH}	0.130
		t_{PLL}	0.129
	B–Z	t_{PHH}	0.126
		t_{PLL}	0.136
	C–Z	t_{PHH}	0.116
		t_{PLL}	0.144
D	A–Z	t_{PHH}	0.111
		t_{PLL}	0.112
	B–Z	t_{PHH}	0.107
		t_{PLL}	0.121
	C–Z	t_{PHH}	0.100
		t_{PLL}	0.129

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-4. Cell AND3_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	A–Z	t_{PHH}	0.114
		t_{PLL}	0.111
	B–Z	t_{PHH}	0.110
		t_{PLL}	0.120
	C–Z	t_{PHH}	0.103
		t_{PLL}	0.127
F	A–Z	t_{PHH}	0.108
		t_{PLL}	0.108
	B–Z	t_{PHH}	0.105
		t_{PLL}	0.117
	C–Z	t_{PHH}	0.098
		t_{PLL}	0.125
H	A–Z	t_{PHH}	0.105
		t_{PLL}	0.116
	B–Z	t_{PHH}	0.102
		t_{PLL}	0.126
	C–Z	t_{PHH}	0.097
		t_{PLL}	0.135
I	A–Z	t_{PHH}	0.109
		t_{PLL}	0.118
	B–Z	t_{PHH}	0.106
		t_{PLL}	0.128
	C–Z	t_{PHH}	0.100
		t_{PLL}	0.136
J	A–Z	t_{PHH}	0.112
		t_{PLL}	0.123
	B–Z	t_{PHH}	0.109
		t_{PLL}	0.133
	C–Z	t_{PHH}	0.104
		t_{PLL}	0.142

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-4. Cell AND3_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
K	A–Z	t_{PHH}	0.110
		t_{PLL}	0.127
	B–Z	t_{PHH}	0.108
		t_{PLL}	0.136
	C–Z	t_{PHH}	0.102
		t_{PLL}	0.145

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.2.4 Cell Specifications

Table 2-5. Cell AND3_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level								
	B	C	D	E	F	H	I	J	K
A	2.7	3.2	4.5	4.8	6.0	7.1	8.1	9.9	11.1
B	2.5	2.9	4.1	4.4	5.7	6.7	7.7	10.3	11.5
C	2.5	2.9	4.0	4.3	5.5	6.3	7.3	10.0	11.1
Z	54.4	110.9	167.5	237.6	354.3	501.5	706.6	968.7	1257.2

Table 2-6. Cell AND3_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
B	3.92	6.72
C		
D		
E		
F		
H		
I		
J	5.60	
K		

2.3 AND4_{PL} Cell

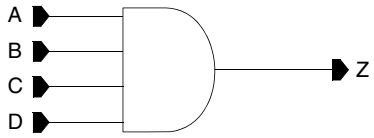
2.3.1 Function

Four-way AND

2.3.2 Description

This cell is a combinational gate, four-way AND. The Boolean expression for this cell is $Z = (A \times B \times C \times D)$.

Figure 2-3. Cell AND4_{PL} Symbols



2.3.3 Propagation Delay Table

Table 2-7. Cell AND4_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A–Z	t_{PHH}	0.148
		t_{PLL}	0.127
	B–Z	t_{PHH}	0.148
		t_{PLL}	0.136
	C–Z	t_{PHH}	0.146
		t_{PLL}	0.145
	D–Z	t_{PHH}	0.141
		t_{PLL}	0.152
C	A–Z	t_{PHH}	0.131
		t_{PLL}	0.128
	B–Z	t_{PHH}	0.132
		t_{PLL}	0.138
	C–Z	t_{PHH}	0.130
		t_{PLL}	0.147
	D–Z	t_{PHH}	0.124
		t_{PLL}	0.154

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-7. Cell AND4_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
D	A–Z	t_{PHH}	0.125
		t_{PLL}	0.125
	B–Z	t_{PHH}	0.125
		t_{PLL}	0.136
	C–Z	t_{PHH}	0.123
		t_{PLL}	0.145
	D–Z	t_{PHH}	0.118
		t_{PLL}	0.152
E	A–Z	t_{PHH}	0.120
		t_{PLL}	0.121
	B–Z	t_{PHH}	0.121
		t_{PLL}	0.131
	C–Z	t_{PHH}	0.119
		t_{PLL}	0.141
	D–Z	t_{PHH}	0.115
		t_{PLL}	0.148
F	A–Z	t_{PHH}	0.118
		t_{PLL}	0.120
	B–Z	t_{PHH}	0.119
		t_{PLL}	0.130
	C–Z	t_{PHH}	0.117
		t_{PLL}	0.139
	D–Z	t_{PHH}	0.113
		t_{PLL}	0.147
H	A–Z	t_{PHH}	0.114
		t_{PLL}	0.117
	B–Z	t_{PHH}	0.115
		t_{PLL}	0.128
	C–Z	t_{PHH}	0.113
		t_{PLL}	0.137
	D–Z	t_{PHH}	0.110
		t_{PLL}	0.144

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-7. Cell AND4_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
I	A–Z	t_{PHH}	0.145
		t_{PLL}	0.138
	B–Z	t_{PHH}	0.144
		t_{PLL}	0.147
	C–Z	t_{PHH}	0.141
		t_{PLL}	0.154
	D–Z	t_{PHH}	0.139
		t_{PLL}	0.162
J	A–Z	t_{PHH}	0.138
		t_{PLL}	0.142
	B–Z	t_{PHH}	0.138
		t_{PLL}	0.151
	C–Z	t_{PHH}	0.134
		t_{PLL}	0.159
	D–Z	t_{PHH}	0.133
		t_{PLL}	0.168
K	A–Z	t_{PHH}	0.139
		t_{PLL}	0.136
	B–Z	t_{PHH}	0.139
		t_{PLL}	0.145
	C–Z	t_{PHH}	0.136
		t_{PLL}	0.153
	D–Z	t_{PHH}	0.135
		t_{PLL}	0.161

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.3.4 Cell Specifications

Table 2-8. Cell AND4_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level								
	B	C	D	E	F	H	I	J	K
A	3.3	3.7	4.1	4.7	5.9	7.3	7.9	9.2	11.2
B	3.2	3.5	3.9	4.5	5.5	6.8	7.6	8.9	10.6
C	3.3	3.6	4.0	4.6	5.6	6.9	7.0	8.3	10.1
D	2.8	3.1	3.5	4.1	5.2	6.6	7.6	8.9	10.8
Z	61.6	115.5	173.5	233.6	374.5	499.9	745.9	995.2	1279.3

Table 2-9. Cell AND4_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
B	4.48	6.72
C		
D		
E		
F	5.04	
H		
I	8.96	
J		
K		

2.4 INVERT_{PL} Cell

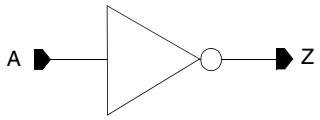
2.4.1 Function

Inverter

2.4.2 Description

This cell is a combinational gate inverter. The Boolean expression for this cell is $Z = \overline{A}$.

Figure 2-4. Cell INVERT_{PL} Symbols



2.4.3 Propagation Delay Table

Table 2-10. Cell INVERT_{PL} Propagation Delays (Page 1 of 2)

Path (Input to Output)	Performance Level	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A–Z	A	t_{PLH}	0.099
		t_{PHL}	0.035
	B	t_{PLH}	0.089
		t_{PHL}	0.037
	C	t_{PLH}	0.062
		t_{PHL}	0.035
	D	t_{PLH}	0.053
		t_{PHL}	0.030
	E	t_{PLH}	0.049
		t_{PHL}	0.026
	F	t_{PLH}	0.051
		t_{PHL}	0.007
	H	t_{PLH}	0.044
		t_{PHL}	0.012
	I	t_{PLH}	0.039
		t_{PHL}	0.016
	J	t_{PLH}	0.038
		t_{PHL}	0.017

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-10. Cell INVERT_{PL} Propagation Delays (Page 2 of 2)

Path (Input to Output)	Performance Level	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A–Z	K	t_{PLH}	0.038
		t_{PHL}	0.015
	L	t_{PLH}	0.038
		t_{PHL}	0.014
	M	t_{PLH}	0.035
		t_{PHL}	0.017
	N	t_{PLH}	0.034
		t_{PHL}	0.018
	O	t_{PLH}	0.034
		t_{PHL}	0.018
	U	t_{PLH}	0.033
		t_{PHL}	0.018

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.4.4 Cell Specifications

Table 2-11. Cell INVERT_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level														
	A	B	C	D	E	F	H	I	J	K	L	M	N	O	U
A	2.1	2.2	3.4	4.6	6.0	12.4	14.4	17.4	25.5	31.3	35.3	52.1	65.8	79.5	167.6
Z	40.1	48.4	98.5	148.9	201.8	337.2	448.1	595.8	859.6	1045.0	1183.4	1779.2	2322.4	2747.6	5834.8

Table 2-12. Cell INVERT_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
A	1.68	6.72
B		
C		
D		
E		
F		
H		
I		
J	2.80	
K		
L		
M	4.48	
N	5.60	
O	7.28	
U	14.56	

2.5 INVERTBAL_{PL} Cell

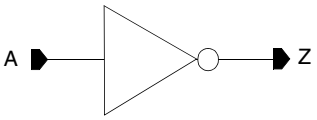
2.5.1 Function

Balanced inverter

2.5.2 Description

This cell is a combinational gate, balanced inverter. The Boolean expression for this cell is $Z = \overline{A}$.

Figure 2-5. Cell INVERTBAL_{PL} Symbols



2.5.3 Propagation Delay Table

Table 2-13. Cell INVERTBAL_{PL} Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A–Z	E	t_{PLH}	0.038
		t_{PHL}	0.027
	H	t_{PLH}	0.034
		t_{PHL}	0.025
	J	t_{PLH}	0.032
		t_{PHL}	0.023
	L	t_{PLH}	0.032
		t_{PHL}	0.022

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.5.4 Cell Specifications

Table 2-14. Cell INVERTBAL_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level			
	E	H	J	L
A	10.3	15.7	31.6	47.2
Z	355.8	568.5	1128.6	1687.7

Table 2-15. Cell INVERTBAL_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
E	1.68	6.72
H		
J	3.36	
L	5.04	

2.6 NAND2_{PL} Cell

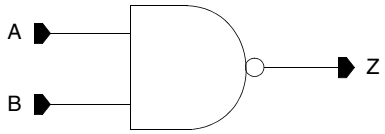
2.6.1 Function

Two-way NAND

2.6.2 Description

This cell is a combinational gate, two-way NAND. The Boolean expression for this cell is $Z = \overline{A \times B}$.

Figure 2-6. Cell NAND2_{PL} Symbols



2.6.3 Propagation Delay Table

Table 2-16. Cell NAND2_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A	A–Z	t_{PLH}	0.089
		t_{PHL}	0.060
	B–Z	t_{PLH}	0.098
		t_{PHL}	0.052
B	A–Z	t_{PLH}	0.085
		t_{PHL}	0.052
	B–Z	t_{PLH}	0.095
		t_{PHL}	0.045
C	A–Z	t_{PLH}	0.064
		t_{PHL}	0.037
	B–Z	t_{PLH}	0.076
		t_{PHL}	0.034
D	A–Z	t_{PLH}	0.057
		t_{PHL}	0.032
	B–Z	t_{PLH}	0.070
		t_{PHL}	0.030

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-16. Cell NAND2_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	A–Z	t_{PLH}	0.054
		t_{PHL}	0.029
	B–Z	t_{PLH}	0.068
		t_{PHL}	0.028
F	A–Z	t_{PLH}	0.054
		t_{PHL}	0.021
	B–Z	t_{PLH}	0.070
		t_{PHL}	0.022
H	A–Z	t_{PLH}	0.052
		t_{PHL}	0.020
	B–Z	t_{PLH}	0.069
		t_{PHL}	0.020
I	A–Z	t_{PLH}	0.054
		t_{PHL}	0.017
	B–Z	t_{PLH}	0.072
		t_{PHL}	0.019
J	A–Z	t_{PLH}	0.056
		t_{PHL}	0.024
	B–Z	t_{PLH}	0.056
		t_{PHL}	0.024
K	A–Z	t_{PLH}	0.053
		t_{PHL}	0.025
	B–Z	t_{PLH}	0.055
		t_{PHL}	0.025
L	A–Z	t_{PLH}	0.052
		t_{PHL}	0.026
	B–Z	t_{PLH}	0.052
		t_{PHL}	0.026
M	A–Z	t_{PLH}	0.055
		t_{PHL}	0.023
	B–Z	t_{PLH}	0.055
		t_{PHL}	0.023

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.6.4 Cell Specifications

Table 2-17. Cell NAND2_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level											
	A	B	C	D	E	F	H	I	J	K	L	M
A	2.4	2.6	4.7	6.6	8.5	12.7	24.8	26.2	30.7	39.8	48.9	61.8
B	2.5	2.7	4.4	6.3	8.2	12.9	24.7	26.0	30.4	39.7	48.9	61.4
Z	48.9	54.9	116.3	180.3	239.2	332.1	649.5	661.0	878.6	1165.9	1461.9	1754.9

Table 2-18. Cell NAND2_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
A	2.24	6.72
B		
C		
D		
E		
F		
H	4.48	
I		
J		
K	6.16	
L	6.72	
M	8.96	

2.7 NAND2BAL_{PL} Cell

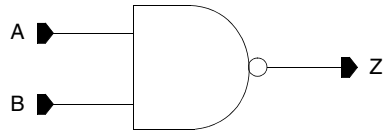
2.7.1 Function

Balanced two-way NAND

2.7.2 Description

This cell is a combinational gate, balanced two-way NAND. The Boolean expression for this cell is $Z = \overline{A \times B}$. The rising and falling delays are balanced; the A to Z delay is equal to the B to Z delay.

Figure 2-7. Cell NAND2BAL_{PL} Symbols



2.7.3 Propagation Delay Table

Table 2-19. Cell NAND2BAL_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	A–Z	t_{PLH}	0.052
		t_{PHL}	0.039
	B–Z	t_{PLH}	0.052
		t_{PHL}	0.040
H	A–Z	t_{PLH}	0.049
		t_{PHL}	0.036
	B–Z	t_{PLH}	0.048
		t_{PHL}	0.036
J	A–Z	t_{PLH}	0.048
		t_{PHL}	0.035
	B–Z	t_{PLH}	0.047
		t_{PHL}	0.035
L	A–Z	t_{PLH}	0.048
		t_{PHL}	0.034
	B–Z	t_{PLH}	0.047
		t_{PHL}	0.034

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.7.4 Cell Specifications

Table 2-20. Cell NAND2BAL_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level			
	E	H	J	L
A	11.1	17.1	34.4	51.7
B	11.0	16.9	34.3	51.0
Z	315.4	528.0	1047.8	1568.2

Table 2-21. Cell NAND2BAL_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
E	2.80	6.72
H		
J	5.60	
L	8.40	

2.8 NAND3_{PL} Cell

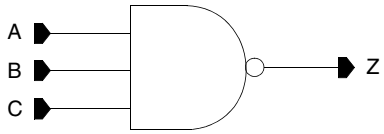
2.8.1 Function

Three-way NAND

2.8.2 Description

This cell is a combinational gate, three-way NAND. The Boolean expression for this cell is $Z = \overline{A \times B \times C}$.

Figure 2-8. Cell NAND3_{PL} Symbols



2.8.3 Propagation Delay Table

Table 2-22. Cell NAND3_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A	A–Z	t_{PLH}	0.108
		t_{PHL}	0.080
	B–Z	t_{PLH}	0.118
		t_{PHL}	0.077
	C–Z	t_{PLH}	0.125
		t_{PHL}	0.068
B	A–Z	t_{PLH}	0.091
		t_{PHL}	0.058
	B–Z	t_{PLH}	0.103
		t_{PHL}	0.058
	C–Z	t_{PLH}	0.114
		t_{PHL}	0.052
C	A–Z	t_{PLH}	0.066
		t_{PHL}	0.050
	B–Z	t_{PLH}	0.079
		t_{PHL}	0.050
	C–Z	t_{PLH}	0.088
		t_{PHL}	0.046

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-22. Cell NAND3_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
D	A–Z	t_{PLH}	0.067
		t_{PHL}	0.040
	B–Z	t_{PLH}	0.082
		t_{PHL}	0.041
	C–Z	t_{PLH}	0.093
		t_{PHL}	0.040
E	A–Z	t_{PLH}	0.063
		t_{PHL}	0.036
	B–Z	t_{PLH}	0.079
		t_{PHL}	0.038
	C–Z	t_{PLH}	0.090
		t_{PHL}	0.037
F	A–Z	t_{PLH}	0.061
		t_{PHL}	0.038
	B–Z	t_{PLH}	0.075
		t_{PHL}	0.038
	C–Z	t_{PLH}	0.087
		t_{PHL}	0.038
H	A–Z	t_{PLH}	0.059
		t_{PHL}	0.036
	B–Z	t_{PLH}	0.074
		t_{PHL}	0.036
	C–Z	t_{PLH}	0.086
		t_{PHL}	0.036
I	A–Z	t_{PLH}	0.062
		t_{PHL}	0.030
	B–Z	t_{PLH}	0.079
		t_{PHL}	0.033
	C–Z	t_{PLH}	0.092
		t_{PHL}	0.033

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-22. Cell NAND3_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
J	A–Z	t_{PLH}	0.059
		t_{PHL}	0.031
	B–Z	t_{PLH}	0.076
		t_{PHL}	0.034
	C–Z	t_{PLH}	0.089
		t_{PHL}	0.034
K	A–Z	t_{PLH}	0.059
		t_{PHL}	0.034
	B–Z	t_{PLH}	0.074
		t_{PHL}	0.036
	C–Z	t_{PLH}	0.086
		t_{PHL}	0.035

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.8.4 Cell Specifications

Table 2-23. Cell NAND3_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level									
	A	B	C	D	E	F	H	I	J	K
A	2.1	3.2	5.3	7.6	10.2	16.0	20.2	33.0	41.5	50.8
B	2.3	3.1	5.3	8.0	10.7	15.7	19.8	32.0	41.3	49.5
C	2.4	3.1	5.2	7.8	10.3	15.5	19.4	31.8	41.0	49.8
Z	37.4	58.8	139.9	181.6	253.5	384.7	503.1	739.4	996.9	1241.9

Table 2-24. Cell NAND3_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
A	3.36	6.72
B		
C		
D		
E		
F	5.60	
H		
I	8.40	
J	9.52	
K	11.76	

2.9 NAND4_{PL} Cell

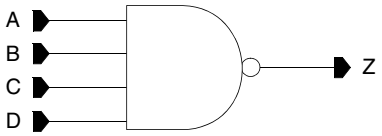
2.9.1 Function

Four-way NAND

2.9.2 Description

This cell is a combinational gate, four-way NAND. The Boolean expression for this cell is $Z = \overline{A \times B \times C \times D}$.

Figure 2-9. Cell NAND4_{PL} Symbols



2.9.3 Propagation Delay Table

Table 2-25. Cell NAND4_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A	A–Z	t_{PLH}	0.099
		t_{PHL}	0.066
	B–Z	t_{PLH}	0.113
		t_{PHL}	0.068
	C–Z	t_{PLH}	0.124
		t_{PHL}	0.068
	D–Z	t_{PLH}	0.133
		t_{PHL}	0.066
B	A–Z	t_{PLH}	0.083
		t_{PHL}	0.053
	B–Z	t_{PLH}	0.099
		t_{PHL}	0.056
	C–Z	t_{PLH}	0.111
		t_{PHL}	0.057
	D–Z	t_{PLH}	0.121
		t_{PHL}	0.057

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-25. Cell NAND4_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	A–Z	t_{PLH}	0.078
		t_{PHL}	0.044
	B–Z	t_{PLH}	0.095
		t_{PHL}	0.048
	C–Z	t_{PLH}	0.109
		t_{PHL}	0.050
	D–Z	t_{PLH}	0.122
		t_{PHL}	0.052
D	A–Z	t_{PLH}	0.075
		t_{PHL}	0.041
	B–Z	t_{PLH}	0.094
		t_{PHL}	0.045
	C–Z	t_{PLH}	0.107
		t_{PHL}	0.048
	D–Z	t_{PLH}	0.121
		t_{PHL}	0.050
E	A–Z	t_{PLH}	0.070
		t_{PHL}	0.046
	B–Z	t_{PLH}	0.086
		t_{PHL}	0.050
	C–Z	t_{PLH}	0.100
		t_{PHL}	0.054
	D–Z	t_{PLH}	0.110
		t_{PHL}	0.053
F	A–Z	t_{PLH}	0.066
		t_{PHL}	0.043
	B–Z	t_{PLH}	0.082
		t_{PHL}	0.047
	C–Z	t_{PLH}	0.097
		t_{PHL}	0.051
	D–Z	t_{PLH}	0.106
		t_{PHL}	0.051

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.9.4 Cell Specifications

Table 2-26. Cell NAND4_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level					
	A	B	C	D	E	F
A	3.6	5.0	9.6	11.6	13.9	19.6
B	3.4	4.8	9.2	11.1	13.5	19.1
C	3.3	4.8	8.6	10.6	13.4	18.9
D	3.3	4.6	9.2	11.1	13.4	19.0
Z	56.9	95.4	174.5	218.2	296.1	448.3

Table 2-27. Cell NAND4_{PL} Area

<table>
<tr><th rowspan="2">Performance Level</th><th colspan="2">Cell Dimensions (μm)</th></tr>
<tr><th>Width</th><th>Length</th></tr>
<tr><td>A</td><td rowspan="2">3.36</td><td rowspan="6">6.72</td></tr>
<tr><td>B</td></tr>
<tr><td>C</td><td rowspan="2">5.60</td></tr>
<tr><td>D</td></tr>
<tr><td>E</td><td rowspan="2">7.84</td></tr>
<tr><td>F</td></tr>
</table>

2.10 NOR2_{PL} Cell

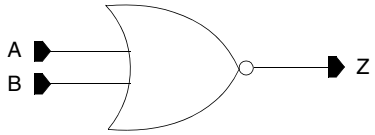
2.10.1 Function

Two-way NOR

2.10.2 Description

This cell is a combinational gate, two-way NOR. The Boolean expression for this cell is $Z = \overline{A + B}$.

Figure 2-10. Cell NOR2_{PL} Symbols



2.10.3 Propagation Delay Table

Table 2-28. Cell NOR2_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A	A–Z	t_{PLH}	0.121
		t_{PHL}	0.039
	B–Z	t_{PLH}	0.112
		t_{PHL}	0.045
B	A–Z	t_{PLH}	0.082
		t_{PHL}	0.049
	B–Z	t_{PLH}	0.078
		t_{PHL}	0.061
C	A–Z	t_{PLH}	0.062
		t_{PHL}	0.043
	B–Z	t_{PLH}	0.061
		t_{PHL}	0.060
D	A–Z	t_{PLH}	0.053
		t_{PHL}	0.038
	B–Z	t_{PLH}	0.054
		t_{PHL}	0.056

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-28. Cell NOR2_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	A–Z	t_{PLH}	0.050
		t_{PHL}	0.037
	B–Z	t_{PLH}	0.051
		t_{PHL}	0.055
F	A–Z	t_{PLH}	0.050
		t_{PHL}	0.035
	B–Z	t_{PLH}	0.051
		t_{PHL}	0.053
H	A–Z	t_{PLH}	0.048
		t_{PHL}	0.034
	B–Z	t_{PLH}	0.049
		t_{PHL}	0.053
I	A–Z	t_{PLH}	0.044
		t_{PHL}	0.032
	B–Z	t_{PLH}	0.047
		t_{PHL}	0.051
J	A–Z	t_{PLH}	0.045
		t_{PHL}	0.037
	B–Z	t_{PLH}	0.045
		t_{PHL}	0.046

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.10.4 Cell Specifications

Table 2-29. Cell NOR2_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level								
	A	B	C	D	E	F	H	I	J
A	2.5	3.5	5.7	8.5	11.1	16.8	21.1	29.1	43.7
B	2.7	3.5	5.7	8.7	11.0	16.9	21.1	28.9	43.7
Z	27.0	53.3	110.2	168.4	229.8	331.9	434.0	617.6	941.5

Table 2-30. Cell NOR2_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
A	2.24	6.72
B		
C		
D		
E		
F	3.92	
H		
I	4.48	
J	6.72	

2.11 NOR3_{PL} Cell

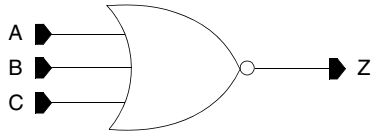
2.11.1 Function

Three-way NOR

2.11.2 Description

This cell is a combinational gate, three-way NOR. The Boolean expression for this cell is $Z = \overline{A + B + C}$.

Figure 2-11. Cell NOR3_{PL} Symbols



2.11.3 Propagation Delay Table

Table 2-31. Cell NOR3_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A	A–Z	t_{PLH}	0.099
		t_{PHL}	0.059
	B–Z	t_{PLH}	0.103
		t_{PHL}	0.076
	C–Z	t_{PLH}	0.105
		t_{PHL}	0.082
B	A–Z	t_{PLH}	0.084
		t_{PHL}	0.053
	B–Z	t_{PLH}	0.091
		t_{PHL}	0.072
	C–Z	t_{PLH}	0.094
		t_{PHL}	0.080
C	A–Z	t_{PLH}	0.067
		t_{PHL}	0.060
	B–Z	t_{PLH}	0.077
		t_{PHL}	0.080
	C–Z	t_{PLH}	0.082
		t_{PHL}	0.092

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-31. Cell NOR3_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
D	A–Z	t_{PLH}	0.062
		t_{PHL}	0.053
	B–Z	t_{PLH}	0.072
		t_{PHL}	0.074
	C–Z	t_{PLH}	0.078
		t_{PHL}	0.085
E	A–Z	t_{PLH}	0.060
		t_{PHL}	0.048
	B–Z	t_{PLH}	0.069
		t_{PHL}	0.067
	C–Z	t_{PLH}	0.075
		t_{PHL}	0.081
F	A–Z	t_{PLH}	0.055
		t_{PHL}	0.044
	B–Z	t_{PLH}	0.065
		t_{PHL}	0.064
	C–Z	t_{PLH}	0.071
		t_{PHL}	0.077

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.11.4 Cell Specifications

Table 2-32. Cell NOR3_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level					
	A	B	C	D	E	F
A	3.9	5.3	9.9	13.6	18.2	28.3
B	3.8	5.1	9.3	12.9	17.3	27.2
C	3.6	4.9	9.5	13.1	17.8	28.4
Z	42.6	63.5	129.9	190.5	249.9	410.4

Table 2-33. Cell NOR3_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
A	2.80	6.72
B		
C	4.48	
D		
E	5.60	
F	6.16	

2.12 NOR4_{PL} Cell

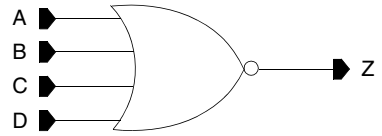
2.12.1 Function

Four-way NOR

2.12.2 Description

This cell is a combinational gate, four-way NOR. The Boolean expression for this cell is $Z = \overline{A + B + C + D}$.

Figure 2-12. Cell NOR4_{PL} Symbols



2.12.3 Propagation Delay Table

Table 2-34. Cell NOR4_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A	A–Z	t_{PLH}	0.099
		t_{PHL}	0.067
	B–Z	t_{PLH}	0.112
		t_{PHL}	0.091
	C–Z	t_{PLH}	0.126
		t_{PHL}	0.102
	D–Z	t_{PLH}	0.131
		t_{PHL}	0.103
B	A–Z	t_{PLH}	0.080
		t_{PHL}	0.062
	B–Z	t_{PLH}	0.095
		t_{PHL}	0.086
	C–Z	t_{PLH}	0.110
		t_{PHL}	0.099
	D–Z	t_{PLH}	0.117
		t_{PHL}	0.103

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-34. Cell NOR4_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	A–Z	t_{PLH}	0.072
		t_{PHL}	0.058
	B–Z	t_{PLH}	0.087
		t_{PHL}	0.080
	C–Z	t_{PLH}	0.102
		t_{PHL}	0.093
	D–Z	t_{PLH}	0.113
		t_{PHL}	0.102
D	A–Z	t_{PLH}	0.065
		t_{PHL}	0.055
	B–Z	t_{PLH}	0.081
		t_{PHL}	0.079
	C–Z	t_{PLH}	0.096
		t_{PHL}	0.092
	D–Z	t_{PLH}	0.106
		t_{PHL}	0.096

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.12.4 Cell Specifications

Table 2-35. Cell NOR4_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level			
	A	B	C	D
A	4.2	6.4	14.1	28.6
B	4.7	6.8	13.6	27.2
C	4.6	6.7	13.2	26.9
D	4.2	6.4	13.6	26.7
Z	40.1	69.7	148.6	298.5

Table 2-36. Cell NOR4_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
A	2.80	6.72
B		
C	5.60	
D	9.52	

2.13 OR2_{PL} Cell

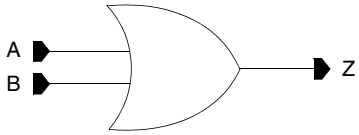
2.13.1 Function

Two-way OR

2.13.2 Description

This cell is a combinational gate, two-way OR. The Boolean expression for this cell is $Z = A + B$.

Figure 2-13. Cell OR2_{PL} Symbols



2.13.3 Propagation Delay Table

Table 2-37. Cell OR2_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A–Z	t_{PHH}	0.095
		t_{PLL}	0.148
	B–Z	t_{PHH}	0.102
		t_{PLL}	0.139
C	A–Z	t_{PHH}	0.091
		t_{PLL}	0.134
	B–Z	t_{PHH}	0.101
		t_{PLL}	0.127
D	A–Z	t_{PHH}	0.096
		t_{PLL}	0.136
	B–Z	t_{PHH}	0.107
		t_{PLL}	0.128
E	A–Z	t_{PHH}	0.092
		t_{PLL}	0.129
	B–Z	t_{PHH}	0.103
		t_{PLL}	0.122

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-37. Cell OR2_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
F	A–Z	t_{PHH}	0.090
		t_{PLL}	0.127
	B–Z	t_{PHH}	0.101
		t_{PLL}	0.120
H	A–Z	t_{PHH}	0.090
		t_{PLL}	0.135
	B–Z	t_{PHH}	0.098
		t_{PLL}	0.126
I	A–Z	t_{PHH}	0.087
		t_{PLL}	0.124
	B–Z	t_{PHH}	0.099
		t_{PLL}	0.117
J	A–Z	t_{PHH}	0.088
		t_{PLL}	0.131
	B–Z	t_{PHH}	0.099
		t_{PLL}	0.123
K	A–Z	t_{PHH}	0.099
		t_{PLL}	0.135
	B–Z	t_{PHH}	0.111
		t_{PLL}	0.128

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.13.4 Cell Specifications

Table 2-38. Cell OR2_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level								
	B	C	D	E	F	H	I	J	K
A	2.7	3.4	3.5	4.2	5.2	6.0	8.3	10.9	12.2
B	2.7	3.2	3.3	4.0	5.0	5.7	8.0	10.9	12.2
Z	52.1	107.2	168.4	231.9	356.3	477.2	711.2	979.7	1394.6

Table 2-39. Cell OR2_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
B	3.36	6.72
C		
D		
E		
F		
H		
I		
J	4.48	
K		

2.14 OR3_{PL} Cell

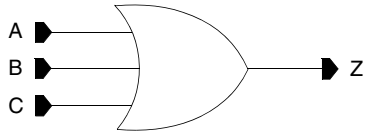
2.14.1 Function

Three-way OR

2.14.2 Description

This cell is a combinational gate, three-way OR. The Boolean expression for this cell is $Z = A + B + C$.

Figure 2-14. Cell OR3_{PL} Symbols



2.14.3 Propagation Delay Table

Table 2-40. Cell OR3_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A–Z	t_{PHH}	0.106
		t_{PLL}	0.154
	B–Z	t_{PHH}	0.117
		t_{PLL}	0.156
	C–Z	t_{PHH}	0.123
		t_{PLL}	0.157
C	A–Z	t_{PHH}	0.102
		t_{PLL}	0.152
	B–Z	t_{PHH}	0.114
		t_{PLL}	0.154
	C–Z	t_{PHH}	0.122
		t_{PLL}	0.155
D	A–Z	t_{PHH}	0.111
		t_{PLL}	0.144
	B–Z	t_{PHH}	0.124
		t_{PLL}	0.148
	C–Z	t_{PHH}	0.133
		t_{PLL}	0.150

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-40. Cell OR3_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	A–Z	t_{PHH}	0.110
		t_{PLL}	0.143
	B–Z	t_{PHH}	0.123
		t_{PLL}	0.147
	C–Z	t_{PHH}	0.132
		t_{PLL}	0.149
F	A–Z	t_{PHH}	0.109
		t_{PLL}	0.138
	B–Z	t_{PHH}	0.125
		t_{PLL}	0.144
	C–Z	t_{PHH}	0.134
		t_{PLL}	0.145
H	A–Z	t_{PHH}	0.103
		t_{PLL}	0.135
	B–Z	t_{PHH}	0.119
		t_{PLL}	0.141
	C–Z	t_{PHH}	0.128
		t_{PLL}	0.142
I	A–Z	t_{PHH}	0.118
		t_{PLL}	0.150
	B–Z	t_{PHH}	0.132
		t_{PLL}	0.155
	C–Z	t_{PHH}	0.147
		t_{PLL}	0.157
J	A–Z	t_{PHH}	0.112
		t_{PLL}	0.147
	B–Z	t_{PHH}	0.127
		t_{PLL}	0.152
	C–Z	t_{PHH}	0.140
		t_{PLL}	0.154

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-40. Cell OR3_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
K	A–Z	t_{PHH}	0.116
		t_{PLL}	0.151
	B–Z	t_{PHH}	0.131
		t_{PLL}	0.158
	C–Z	t_{PHH}	0.143
		t_{PLL}	0.159

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.14.4 Cell Specifications

Table 2-41. Cell OR3_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level								
	B	C	D	E	F	H	I	J	K
A	3.4	3.6	4.0	4.4	6.0	7.5	9.2	11.6	14.2
B	3.4	3.6	4.0	4.4	5.8	7.2	8.4	10.8	13.4
C	3.2	3.5	3.8	4.3	5.5	6.9	8.6	11.0	13.7
Z	57.2	109.2	165.2	221.3	359.5	475.5	710.3	947.8	1405.9

Table 2-42. Cell OR3_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
B	4.48	6.72
C		
D		
E		
F		
H		
I	7.28	
J		
K		

2.15 OR4_{PL} Cell

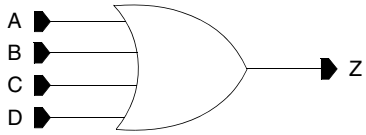
2.15.1 Function

Four-way OR

2.15.2 Description

This cell is a combinational gate, four-way OR. The Boolean expression for this cell is $Z = A + B + C + D$.

Figure 2-15. Cell OR4_{PL} Symbols



2.15.3 Propagation Delay Table

Table 2-43. Cell OR4_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A–Z	t_{PHH}	0.108
		t_{PLL}	0.146
	B–Z	t_{PHH}	0.125
		t_{PLL}	0.159
	C–Z	t_{PHH}	0.135
		t_{PLL}	0.171
	D–Z	t_{PHH}	0.136
		t_{PLL}	0.176
C	A–Z	t_{PHH}	0.107
		t_{PLL}	0.132
	B–Z	t_{PHH}	0.128
		t_{PLL}	0.148
	C–Z	t_{PHH}	0.140
		t_{PLL}	0.161
	D–Z	t_{PHH}	0.143
		t_{PLL}	0.166

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-43. Cell OR4_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
D	A–Z	t_{PHH}	0.106
		t_{PLL}	0.129
	B–Z	t_{PHH}	0.127
		t_{PLL}	0.145
	C–Z	t_{PHH}	0.140
		t_{PLL}	0.158
	D–Z	t_{PHH}	0.144
		t_{PLL}	0.163
E	A–Z	t_{PHH}	0.106
		t_{PLL}	0.128
	B–Z	t_{PHH}	0.127
		t_{PLL}	0.144
	C–Z	t_{PHH}	0.140
		t_{PLL}	0.157
	D–Z	t_{PHH}	0.145
		t_{PLL}	0.163
F	A–Z	t_{PHH}	0.081
		t_{PLL}	0.118
	B–Z	t_{PHH}	0.092
		t_{PLL}	0.112
	C–Z	t_{PHH}	0.091
		t_{PLL}	0.124
	D–Z	t_{PHH}	0.101
		t_{PLL}	0.117
H	A–Z	t_{PHH}	0.085
		t_{PLL}	0.129
	B–Z	t_{PHH}	0.095
		t_{PLL}	0.123
	C–Z	t_{PHH}	0.093
		t_{PLL}	0.134
	D–Z	t_{PHH}	0.103
		t_{PLL}	0.127

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-43. Cell OR4_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
I	A–Z	t_{PHH}	0.107
		t_{PLL}	0.146
	B–Z	t_{PHH}	0.117
		t_{PLL}	0.138
	C–Z	t_{PHH}	0.117
		t_{PLL}	0.150
	D–Z	t_{PHH}	0.126
		t_{PLL}	0.142
J	A–Z	t_{PHH}	0.111
		t_{PLL}	0.155
	B–Z	t_{PHH}	0.121
		t_{PLL}	0.147
	C–Z	t_{PHH}	0.120
		t_{PLL}	0.159
	D–Z	t_{PHH}	0.130
		t_{PLL}	0.151
K	A–Z	t_{PHH}	0.120
		t_{PLL}	0.161
	B–Z	t_{PHH}	0.131
		t_{PLL}	0.153
	C–Z	t_{PHH}	0.129
		t_{PLL}	0.166
	D–Z	t_{PHH}	0.139
		t_{PLL}	0.158

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.15.4 Cell Specifications

Table 2-44. Cell OR4_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level								
	B	C	D	E	F	H	I	J	K
A	4.6	5.5	6.3	7.0	8.3	8.2	8.6	10.7	11.2
B	4.5	5.4	6.0	6.7	7.9	7.9	8.3	10.9	11.4
C	4.5	5.4	6.0	6.6	8.3	8.2	8.6	10.7	11.2
D	3.9	4.8	5.6	6.2	7.9	7.9	8.3	11.0	11.5
Z	56.9	116.0	175.1	239.9	382.9	530.7	779.8	1132.8	1431.9

Table 2-45. Cell OR4_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
B	4.48	6.72
C		
D		
E		
F	5.60	
H		
I	7.84	
J	11.20	
K		

2.16 XOR2_{PL} Cell

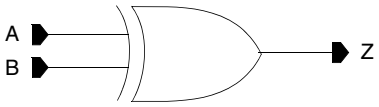
2.16.1 Function

Two-way XOR

2.16.2 Description

This cell is a combinational gate, two-way XOR. The Boolean expression for this cell is $Z = A \oplus B$.

Figure 2-16. Cell XOR2_{PL} Symbols



2.16.3 Propagation Delay Table

Table 2-46. Cell XOR2_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A	A–Z	t_{PHH}	0.112
		t_{PLL}	0.125
		t_{PLH}	0.108
		t_{PHL}	0.082
	B–Z	t_{PHH}	0.098
		t_{PLL}	0.123
		t_{PLH}	0.129
		t_{PHL}	0.046
B	A–Z	t_{PHH}	0.108
		t_{PLL}	0.119
		t_{PLH}	0.100
		t_{PHL}	0.083
	B–Z	t_{PHH}	0.096
		t_{PLL}	0.117
		t_{PLH}	0.120
		t_{PHL}	0.046

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-46. Cell XOR2_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	A–Z	t_{PHH}	0.093
		t_{PLL}	0.102
		t_{PLH}	0.085
		t_{PHL}	0.073
	B–Z	t_{PHH}	0.085
		t_{PLL}	0.101
		t_{PLH}	0.102
		t_{PHL}	0.039
D	A–Z	t_{PHH}	0.123
		t_{PLL}	0.138
		t_{PLH}	0.154
		t_{PHL}	0.141
	B–Z	t_{PHH}	0.127
		t_{PLL}	0.104
		t_{PLH}	0.150
		t_{PHL}	0.148
E	A–Z	t_{PHH}	0.118
		t_{PLL}	0.135
		t_{PLH}	0.148
		t_{PHL}	0.138
	B–Z	t_{PHH}	0.122
		t_{PLL}	0.102
		t_{PLH}	0.144
		t_{PHL}	0.144
F	A–Z	t_{PHH}	0.113
		t_{PLL}	0.130
		t_{PLH}	0.140
		t_{PHL}	0.132
	B–Z	t_{PHH}	0.117
		t_{PLL}	0.098
		t_{PLH}	0.135
		t_{PHL}	0.138

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-46. Cell XOR2_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
H	A–Z	t_{PHH}	0.120
		t_{PLL}	0.129
		t_{PLH}	0.142
		t_{PHL}	0.135
	B–Z	t_{PHH}	0.126
		t_{PLL}	0.098
		t_{PLH}	0.136
		t_{PHL}	0.141
I	A–Z	t_{PHH}	0.132
		t_{PLL}	0.142
		t_{PLH}	0.155
		t_{PHL}	0.151
	B–Z	t_{PHH}	0.140
		t_{PLL}	0.110
		t_{PLH}	0.146
		t_{PHL}	0.158
J	A–Z	t_{PHH}	0.149
		t_{PLL}	0.161
		t_{PLH}	0.173
		t_{PHL}	0.176
	B–Z	t_{PHH}	0.158
		t_{PLL}	0.128
		t_{PLH}	0.159
		t_{PHL}	0.181

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.16.4 Cell Specifications

Table 2-47. Cell XOR2_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level								
	A	B	C	D	E	F	H	I	J
A	4.2	4.7	7.8	4.7	5.3	6.9	7.4	7.4	7.3
B	5.3	5.8	9.5	6.9	7.8	10.1	10.9	10.9	10.9
Z	59.4	72.7	144.8	163.4	224.6	355.6	444.6	708.3	1017.7

Table 2-48. Cell XOR2_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
A	3.92	6.72
B		
C		
D	5.60	
E		
F		
H		
I		
J	7.28	

2.17 XOR3_{PL} Cell

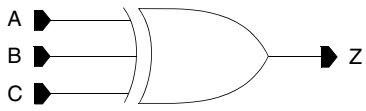
2.17.1 Function

Three-way XOR

2.17.2 Description

This cell is a combinational gate, three-way XOR. The Boolean expression for this cell is $Z = A \oplus B \oplus C$.

Figure 2-17. Cell XOR3_{PL} Symbols



2.17.3 Propagation Delay Table

Table 2-49. Cell XOR3_{PL} Propagation Delays (Page 1 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A–Z	t_{PHH}	0.182
		t_{PLL}	0.184
		t_{PLH}	0.188
		t_{PHL}	0.151
	B–Z	t_{PHH}	0.198
		t_{PLL}	0.213
		t_{PLH}	0.198
		t_{PHL}	0.184
	C–Z	t_{PHH}	0.096
		t_{PLL}	0.120
		t_{PLH}	0.124
		t_{PHL}	0.126
C	A–Z	t_{PHH}	0.177
		t_{PLL}	0.183
		t_{PLH}	0.182
		t_{PHL}	0.151

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-49. Cell XOR3_{PL} Propagation Delays (Page 2 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	B–Z	t_{PHH}	0.192
		t_{PLL}	0.212
		t_{PLH}	0.192
		t_{PHL}	0.183
	C–Z	t_{PHH}	0.095
		t_{PLL}	0.120
		t_{PLH}	0.119
		t_{PHL}	0.128
D	A–Z	t_{PHH}	0.175
		t_{PLL}	0.183
		t_{PLH}	0.181
		t_{PHL}	0.148
	B–Z	t_{PHH}	0.192
		t_{PLL}	0.213
		t_{PLH}	0.193
		t_{PHL}	0.184
	C–Z	t_{PHH}	0.092
		t_{PLL}	0.118
		t_{PLH}	0.117
		t_{PHL}	0.127
E	A–Z	t_{PHH}	0.179
		t_{PLL}	0.186
		t_{PLH}	0.186
		t_{PHL}	0.148
	B–Z	t_{PHH}	0.192
		t_{PLL}	0.213
		t_{PLH}	0.194
		t_{PHL}	0.176
	C–Z	t_{PHH}	0.103
		t_{PLL}	0.121
		t_{PLH}	0.122
		t_{PHL}	0.131

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-49. Cell XOR3_{PL} Propagation Delays (Page 3 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
F	A–Z	t_{PHH}	0.179
		t_{PLL}	0.194
		t_{PLH}	0.183
		t_{PHL}	0.156
	B–Z	t_{PHH}	0.201
		t_{PLL}	0.216
		t_{PLH}	0.201
		t_{PHL}	0.189
	C–Z	t_{PHH}	0.108
		t_{PLL}	0.116
		t_{PLH}	0.121
		t_{PHL}	0.124
H	A–Z	t_{PHH}	0.183
		t_{PLL}	0.201
		t_{PLH}	0.188
		t_{PHL}	0.166
	B–Z	t_{PHH}	0.208
		t_{PLL}	0.221
		t_{PLH}	0.207
		t_{PHL}	0.199
	C–Z	t_{PHH}	0.115
		t_{PLL}	0.126
		t_{PLH}	0.125
		t_{PHL}	0.135
I	A–Z	t_{PHH}	0.201
		t_{PLL}	0.221
		t_{PLH}	0.207
		t_{PHL}	0.182
	B–Z	t_{PHH}	0.222
		t_{PLL}	0.244
		t_{PLH}	0.224
		t_{PHL}	0.220

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-49. Cell XOR3_{PL} Propagation Delays (Page 4 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
I	C–Z	t_{PHH}	0.133
		t_{PLL}	0.138
		t_{PLH}	0.138
		t_{PHL}	0.151

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.17.4 Cell Specifications

Table 2-50. Cell XOR3_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level						
	B	C	D	E	F	H	I
A	11.3	11.3	11.7	11.7	13.1	13.1	13.1
B	8.0	8.0	8.0	8.9	8.9	8.9	8.9
C	8.5	8.6	9.0	9.0	11.6	11.6	12.7
Z	64.9	121.5	172.9	238.6	385.3	512.7	761.3

Table 2-51. Cell XOR3_{PL} Area

Performance Level	Cell Dimensions (µm)	
	Width	Length
B	9.52	6.72
C		
D		
E		
F		
H		
I	10.64	

2.18 XNOR2_{PL} Cell

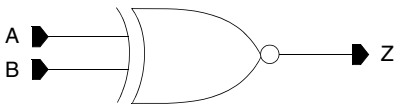
2.18.1 Function

Two-way XNOR

2.18.2 Description

This cell is a combinational gate, two-way XNOR. The Boolean expression for this cell is $Z = \overline{A \oplus B}$.

Figure 2-18. Cell XNOR2_{PL} Symbols



2.18.3 Propagation Delay Table

Table 2-52. Cell XNOR2_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A	A–Z	t_{PLH}	0.105
		t_{PHL}	0.086
		t_{PHH}	0.114
		t_{PLL}	0.122
	B–Z	t_{PLH}	0.073
		t_{PHL}	0.095
		t_{PHH}	0.122
		t_{PLL}	0.116
B	A–Z	t_{PLH}	0.098
		t_{PHL}	0.085
		t_{PHH}	0.109
		t_{PLL}	0.116
	B–Z	t_{PLH}	0.067
		t_{PHL}	0.093
		t_{PHH}	0.115
		t_{PLL}	0.111

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-52. Cell XNOR2_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	A–Z	t_{PLH}	0.083
		t_{PHL}	0.077
		t_{PHH}	0.094
		t_{PLL}	0.100
	B–Z	t_{PLH}	0.055
		t_{PHL}	0.083
		t_{PHH}	0.098
		t_{PLL}	0.097
D	A–Z	t_{PLH}	0.144
		t_{PHL}	0.130
		t_{PHH}	0.110
		t_{PLL}	0.134
	B–Z	t_{PLH}	0.142
		t_{PHL}	0.118
		t_{PHH}	0.074
		t_{PLL}	0.153
E	A–Z	t_{PLH}	0.151
		t_{PHL}	0.136
		t_{PHH}	0.114
		t_{PLL}	0.140
	B–Z	t_{PLH}	0.149
		t_{PHL}	0.123
		t_{PHH}	0.078
		t_{PLL}	0.161
F	A–Z	t_{PLH}	0.142
		t_{PHL}	0.131
		t_{PHH}	0.110
		t_{PLL}	0.133
	B–Z	t_{PLH}	0.140
		t_{PHL}	0.118
		t_{PHH}	0.075
		t_{PLL}	0.153

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-52. Cell XNOR2_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
H	A–Z	t_{PLH}	0.144
		t_{PHL}	0.133
		t_{PHH}	0.120
		t_{PLL}	0.127
	B–Z	t_{PLH}	0.142
		t_{PHL}	0.120
		t_{PHH}	0.082
		t_{PLL}	0.145
I	A–Z	t_{PLH}	0.157
		t_{PHL}	0.146
		t_{PHH}	0.133
		t_{PLL}	0.138
	B–Z	t_{PLH}	0.154
		t_{PHL}	0.129
		t_{PHH}	0.094
		t_{PLL}	0.160
J	A–Z	t_{PLH}	0.175
		t_{PHL}	0.169
		t_{PHH}	0.150
		t_{PLL}	0.157
	B–Z	t_{PLH}	0.173
		t_{PHL}	0.145
		t_{PHH}	0.112
		t_{PLL}	0.183

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.18.4 Cell Specifications

Table 2-53. Cell XNOR2_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level								
	A	B	C	D	E	F	H	I	J
A	4.1	4.6	7.7	5.9	5.2	6.8	7.7	7.7	7.6
B	6.1	6.9	11.7	7.7	6.7	8.7	9.6	9.6	9.5
Z	59.0	72.9	145.8	233.8	224.3	350.6	439.3	706.3	1011.9

Table 2-54. Cell XNOR2_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
A	3.92	6.72
B		
C		
D	5.04	
E		
F		
H		
I	5.60	
J	6.72	

2.19 XNOR3_{PL} Cell

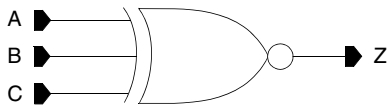
2.19.1 Function

Three-way XNOR

2.19.2 Description

This cell is a combinational gate, three-way XNOR. The Boolean expression for this cell is $Z = \overline{A \oplus B \oplus C}$.

Figure 2-19. Cell XNOR3_{PL} Symbols



2.19.3 Propagation Delay Table

Table 2-55. Cell XNOR3_{PL} Propagation Delays (Page 1 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A–Z	t_{PLH}	0.175
		t_{PHL}	0.172
		t_{PHH}	0.148
		t_{PLL}	0.176
	B–Z	t_{PLH}	0.204
		t_{PHL}	0.186
		t_{PHH}	0.175
		t_{PLL}	0.185
	C–Z	t_{PLH}	0.130
		t_{PHL}	0.116
		t_{PHH}	0.089
		t_{PLL}	0.122
C	A–Z	t_{PLH}	0.168
		t_{PHL}	0.172
		t_{PHH}	0.142
		t_{PLL}	0.176

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-55. Cell XNOR3_{PL} Propagation Delays (Page 2 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	B–Z	t_{PLH}	0.198
		t_{PHL}	0.185
		t_{PHH}	0.168
		t_{PLL}	0.185
	C–Z	t_{PLH}	0.124
		t_{PHL}	0.117
		t_{PHH}	0.088
		t_{PLL}	0.122
D	A–Z	t_{PLH}	0.165
		t_{PHL}	0.167
		t_{PHH}	0.137
		t_{PLL}	0.170
	B–Z	t_{PLH}	0.196
		t_{PHL}	0.182
		t_{PHH}	0.167
		t_{PLL}	0.182
	C–Z	t_{PLH}	0.123
		t_{PHL}	0.116
		t_{PHH}	0.085
		t_{PLL}	0.120
E	A–Z	t_{PLH}	0.172
		t_{PHL}	0.166
		t_{PHH}	0.142
		t_{PLL}	0.172
	B–Z	t_{PLH}	0.200
		t_{PHL}	0.177
		t_{PHH}	0.162
		t_{PLL}	0.177
	C–Z	t_{PLH}	0.129
		t_{PHL}	0.120
		t_{PHH}	0.095
		t_{PLL}	0.123

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-55. Cell XNOR3_{PL} Propagation Delays (Page 3 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
F	A–Z	t_{PLH}	0.179
		t_{PHL}	0.157
		t_{PHH}	0.153
		t_{PLL}	0.164
	B–Z	t_{PLH}	0.204
		t_{PHL}	0.181
		t_{PHH}	0.177
		t_{PLL}	0.179
	C–Z	t_{PLH}	0.129
		t_{PHL}	0.119
		t_{PHH}	0.099
		t_{PLL}	0.116
H	A–Z	t_{PLH}	0.180
		t_{PHL}	0.169
		t_{PHH}	0.159
		t_{PLL}	0.176
	B–Z	t_{PLH}	0.202
		t_{PHL}	0.195
		t_{PHH}	0.184
		t_{PLL}	0.191
	C–Z	t_{PLH}	0.133
		t_{PHL}	0.129
		t_{PHH}	0.105
		t_{PLL}	0.126
I	A–Z	t_{PLH}	0.198
		t_{PHL}	0.186
		t_{PHH}	0.177
		t_{PLL}	0.193
	B–Z	t_{PLH}	0.223
		t_{PHL}	0.211
		t_{PHH}	0.204
		t_{PLL}	0.209

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 2-55. Cell XNOR3_{PL} Propagation Delays (Page 4 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
I	C–Z	t_{PLH}	0.155
		t_{PHL}	0.141
		t_{PHH}	0.118
		t_{PLL}	0.140

1. Minimum input transition and minimum output load. See .lib timing files for more information.

2.19.4 Cell Specifications

Table 2-56. Cell XNOR3_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level						
	B	C	D	E	F	H	I
A	11.3	11.3	11.7	11.7	13.1	13.0	13.1
B	8.0	8.0	8.0	8.9	8.8	8.8	8.8
C	8.0	8.0	8.3	8.3	10.8	10.8	11.9
Z	64.6	120.8	172.0	239.0	387.6	512.7	764.0

Table 2-57. Cell XNOR3_{PL} Area

Performance Level	Cell Dimensions (µm)	
	Width	Length
B	9.52	6.72
C		
D		
E		
F		
H		
I	10.64	

3. Standard Cell Complex Logic

3.1 AO21_{PL} Cell

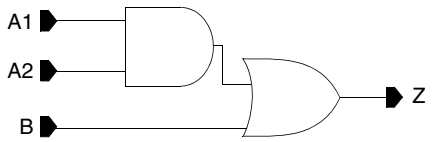
3.1.1 Function

2 × 1 AND OR

3.1.2 Description

This cell is a combinational gate, 2 × 1 AND OR. The Boolean expression for this cell is $Z = (A1 \times A2) + B$.

Figure 3-1. Cell AO21_{PL} Symbols



3.1.3 Propagation Delay Table

Table 3-1. Cell AO21_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A1–Z	t_{PHH}	0.125
		t_{PLL}	0.141
	A2–Z	t_{PHH}	0.116
		t_{PLL}	0.151
	B–Z	t_{PHH}	0.126
		t_{PLL}	0.100
C	A1–Z	t_{PHH}	0.124
		t_{PLL}	0.130
	A2–Z	t_{PHH}	0.112
		t_{PLL}	0.138
	B–Z	t_{PHH}	0.130
		t_{PLL}	0.093

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-1. Cell AO21_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
D	A1–Z	t_{PHH}	0.113
		t_{PLL}	0.119
	A2–Z	t_{PHH}	0.103
		t_{PLL}	0.128
	B–Z	t_{PHH}	0.150
		t_{PLL}	0.084
E	A1–Z	t_{PHH}	0.107
		t_{PLL}	0.115
	A2–Z	t_{PHH}	0.097
		t_{PLL}	0.124
	B–Z	t_{PHH}	0.156
		t_{PLL}	0.080
F	A1–Z	t_{PHH}	0.098
		t_{PLL}	0.110
	A2–Z	t_{PHH}	0.090
		t_{PLL}	0.120
	B–Z	t_{PHH}	0.151
		t_{PLL}	0.075
H	A1–Z	t_{PHH}	0.102
		t_{PLL}	0.122
	A2–Z	t_{PHH}	0.094
		t_{PLL}	0.133
	B–Z	t_{PHH}	0.149
		t_{PLL}	0.080
I	A1–Z	t_{PHH}	0.103
		t_{PLL}	0.131
	A2–Z	t_{PHH}	0.095
		t_{PLL}	0.142
	B–Z	t_{PHH}	0.148
		t_{PLL}	0.085

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-1. Cell AO21_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
J	A1–Z	t_{PHH}	0.115
		t_{PLL}	0.127
	A2–Z	t_{PHH}	0.106
		t_{PLL}	0.137
	B–Z	t_{PHH}	0.174
		t_{PLL}	0.117
K	A1–Z	t_{PHH}	0.120
		t_{PLL}	0.122
	A2–Z	t_{PHH}	0.110
		t_{PLL}	0.131
	B–Z	t_{PHH}	0.184
		t_{PLL}	0.114

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.1.4 Cell Specifications

Table 3-2. Cell AO21_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level								
	B	C	D	E	F	H	I	J	K
A1	3.0	3.5	4.6	5.6	7.6	7.5	8.5	12.3	16.1
A2	2.7	3.2	4.4	5.3	7.2	7.2	8.1	11.6	15.3
B	4.6	5.6	7.1	8.4	11.4	11.0	12.5	10.6	13.9
Z	56.6	113.7	174.9	235.6	356.0	474.9	708.3	942.6	1374.2

Table 3-3. Cell AO21_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
B	3.92	6.72
C		
D		
E		
F		
H		
I		
J	6.16	
K		

3.2 AO22_{PL} Cell

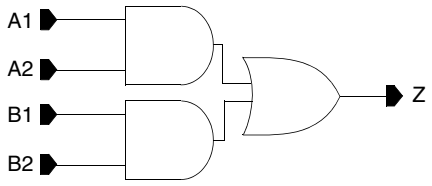
3.2.1 Function

2 × 2 AND OR

3.2.2 Description

This cell is a combinational gate, 2 × 2 AND OR. The Boolean expression for this cell is $Z = (A1 \times A2) + (B1 \times B2)$.

Figure 3-2. Cell AO22_{PL} Symbols



3.2.3 Propagation Delay Table

Table 3-4. Cell AO22_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A1–Z	t_{PHH}	0.108
		t_{PLL}	0.114
	A2–Z	t_{PHH}	0.101
		t_{PLL}	0.125
	B1–Z	t_{PHH}	0.137
		t_{PLL}	0.128
	B2–Z	t_{PHH}	0.128
		t_{PLL}	0.139
C	A1–Z	t_{PHH}	0.088
		t_{PLL}	0.093
	A2–Z	t_{PHH}	0.083
		t_{PLL}	0.104
	B1–Z	t_{PHH}	0.124
		t_{PLL}	0.111

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-4. Cell AO22_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	B2–Z	t_{PHH}	0.116
		t_{PLL}	0.120
D	A1–Z	t_{PHH}	0.083
		t_{PLL}	0.092
	A2–Z	t_{PHH}	0.078
		t_{PLL}	0.103
	B1–Z	t_{PHH}	0.117
		t_{PLL}	0.108
	B2–Z	t_{PHH}	0.110
		t_{PLL}	0.118
E	A1–Z	t_{PHH}	0.082
		t_{PLL}	0.092
	A2–Z	t_{PHH}	0.077
		t_{PLL}	0.103
	B1–Z	t_{PHH}	0.115
		t_{PLL}	0.108
	B2–Z	t_{PHH}	0.107
		t_{PLL}	0.118
F	A1–Z	t_{PHH}	0.091
		t_{PLL}	0.104
	A2–Z	t_{PHH}	0.084
		t_{PLL}	0.115
	B1–Z	t_{PHH}	0.117
		t_{PLL}	0.115
	B2–Z	t_{PHH}	0.109
		t_{PLL}	0.126
H	A1–Z	t_{PHH}	0.096
		t_{PLL}	0.105
	A2–Z	t_{PHH}	0.088
		t_{PLL}	0.114
	B1–Z	t_{PHH}	0.125
		t_{PLL}	0.117
	B2–Z	t_{PHH}	0.116
		t_{PLL}	0.126

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-4. Cell AO22_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
I	A1–Z	t_{PHH}	0.093
		t_{PLL}	0.110
	A2–Z	t_{PHH}	0.087
		t_{PLL}	0.120
	B1–Z	t_{PHH}	0.118
		t_{PLL}	0.119
	B2–Z	t_{PHH}	0.109
		t_{PLL}	0.129
J	A1–Z	t_{PHH}	0.098
		t_{PLL}	0.105
	A2–Z	t_{PHH}	0.091
		t_{PLL}	0.114
	B1–Z	t_{PHH}	0.127
		t_{PLL}	0.116
	B2–Z	t_{PHH}	0.118
		t_{PLL}	0.124
K	A1–Z	t_{PHH}	0.103
		t_{PLL}	0.115
	A2–Z	t_{PHH}	0.096
		t_{PLL}	0.124
	B1–Z	t_{PHH}	0.131
		t_{PLL}	0.125
	B2–Z	t_{PHH}	0.122
		t_{PLL}	0.132

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.2.4 Cell Specifications

Table 3-5. Cell AO22_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level								
	B	C	D	E	F	H	I	J	K
A1	4.5	8.4	9.1	9.5	8.8	9.6	15.2	18.0	17.9
A2	3.9	7.8	8.6	8.9	8.1	9.0	14.9	17.6	17.6
B1	4.3	7.9	8.6	9.0	8.3	9.1	14.7	17.3	17.3
B2	4.1	7.6	8.3	8.6	8.1	8.9	14.3	16.9	17.0
Z	54.5	114.1	177.7	236.9	392.1	553.4	780.5	1058.9	1407.4

Table 3-6. Cell AO22_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
B	4.48	6.72
C		
D		
E		
F		
H		
I	8.40	
J		
K		

3.3 AO33_{PL} Cell

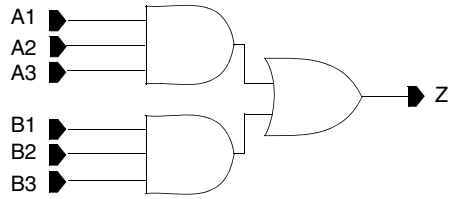
3.3.1 Function

3 × 3 AND OR

3.3.2 Description

This cell is a combinational gate, 3 × 3 AND OR. The Boolean expression for this cell is $Z = (A1 \times A2 \times A3) + (B1 \times B2 \times B3)$.

Figure 3-3. Cell AO33_{PL} Symbols



3.3.3 Propagation Delay Table

Table 3-7. Cell AO33_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	A1–Z	t_{PHH}	0.157
		t_{PLL}	0.169
	A2–Z	t_{PHH}	0.152
		t_{PLL}	0.176
	A3–Z	t_{PHH}	0.142
		t_{PLL}	0.184
	B1–Z	t_{PHH}	0.171
		t_{PLL}	0.171
	B2–Z	t_{PHH}	0.167
		t_{PLL}	0.179
	B3–Z	t_{PHH}	0.156
		t_{PLL}	0.187

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-7. Cell AO33_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	A1–Z	t_{PHH}	0.165
		t_{PLL}	0.164
	A2–Z	t_{PHH}	0.159
		t_{PLL}	0.170
	A3–Z	t_{PHH}	0.150
		t_{PLL}	0.177
	B1–Z	t_{PHH}	0.179
		t_{PLL}	0.167
	B2–Z	t_{PHH}	0.175
		t_{PLL}	0.175
	B3–Z	t_{PHH}	0.163
		t_{PLL}	0.182
H	A1–Z	t_{PHH}	0.143
		t_{PLL}	0.147
	A2–Z	t_{PHH}	0.138
		t_{PLL}	0.156
	A3–Z	t_{PHH}	0.131
		t_{PLL}	0.163
	B1–Z	t_{PHH}	0.154
		t_{PLL}	0.151
	B2–Z	t_{PHH}	0.149
		t_{PLL}	0.160
	B3–Z	t_{PHH}	0.140
		t_{PLL}	0.168

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.3.4 Cell Specifications

Table 3-8. Cell AO33_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level		
	C	E	H
A1	2.7	3.0	4.8
A2	2.3	2.7	4.5
A3	2.4	2.8	4.5
B1	2.6	3.0	4.7
B2	2.3	2.7	4.6
B3	2.4	2.8	4.5
Z	111.7	239.8	497.2

Table 3-9. Cell AO33_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
C	8.96	6.72
E		
H		

3.4 AO44_{PL} Cell

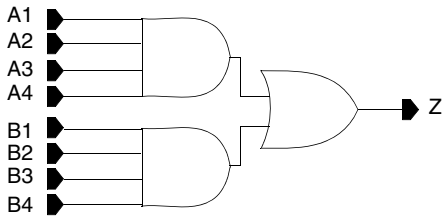
3.4.1 Function

4 × 4 AND OR

3.4.2 Description

This cell is a combinational gate, 4 × 4 AND OR. The Boolean expression for this cell is $Z = (A1 \times A2 \times A3 \times A4) + (B1 \times B2 \times B3 \times B4)$.

Figure 3-4. Cell AO44_{PL} Symbols



3.4.3 Propagation Delay Table

Table 3-10. Cell AO44_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	A1–Z	t_{PHH}	0.194
		t_{PLL}	0.181
	A2–Z	t_{PHH}	0.194
		t_{PLL}	0.190
	A3–Z	t_{PHH}	0.190
		t_{PLL}	0.197
	A4–Z	t_{PHH}	0.184
		t_{PLL}	0.204
	B1–Z	t_{PHH}	0.212
		t_{PLL}	0.184
	B2–Z	t_{PHH}	0.211
		t_{PLL}	0.192
	B3–Z	t_{PHH}	0.207
		t_{PLL}	0.199

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-10. Cell AO44_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	B4–Z	t_{PHH}	0.201
		t_{PLL}	0.207
E	A1–Z	t_{PHH}	0.197
		t_{PLL}	0.189
	A2–Z	t_{PHH}	0.196
		t_{PLL}	0.197
	A3–Z	t_{PHH}	0.193
		t_{PLL}	0.205
	A4–Z	t_{PHH}	0.187
		t_{PLL}	0.213
	B1–Z	t_{PHH}	0.213
		t_{PLL}	0.194
	B2–Z	t_{PHH}	0.213
		t_{PLL}	0.203
	B3–Z	t_{PHH}	0.209
		t_{PLL}	0.210
	B4–Z	t_{PHH}	0.204
		t_{PLL}	0.218
H	A1–Z	t_{PHH}	0.162
		t_{PLL}	0.168
	A2–Z	t_{PHH}	0.162
		t_{PLL}	0.178
	A3–Z	t_{PHH}	0.159
		t_{PLL}	0.187
	A4–Z	t_{PHH}	0.156
		t_{PLL}	0.195
	B1–Z	t_{PHH}	0.175
		t_{PLL}	0.172
	B2–Z	t_{PHH}	0.175
		t_{PLL}	0.182
	B3–Z	t_{PHH}	0.172
		t_{PLL}	0.190
	B4–Z	t_{PHH}	0.168
		t_{PLL}	0.199

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.4.4 Cell Specifications

Table 3-11. Cell AO44_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level		
	C	E	H
A1	2.6	2.8	4.3
A2	2.6	2.8	4.3
A3	2.5	2.8	4.2
A4	2.4	2.7	4.1
B1	2.6	2.8	4.3
B2	2.6	2.8	4.3
B3	2.5	2.7	4.2
B4	2.4	2.6	4.1
Z	115.3	255.2	521.2

Table 3-12. Cell AO44_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
C	9.52	6.72
E		
H		

3.5 AO222_{PL} Cell

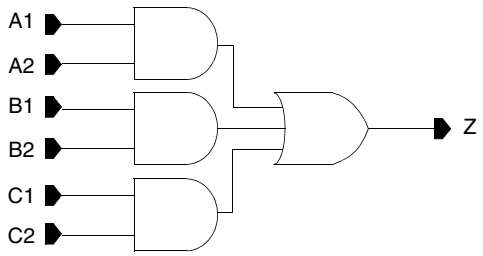
3.5.1 Function

2 × 2 × 2 AND OR

3.5.2 Description

This cell is a combinational gate, 2 × 2 × 2 AND OR. The Boolean expression for this cell is $Z = (A1 \times A2) + (B1 \times B2) + (C1 \times C2)$.

Figure 3-5. Cell AO222_{PL} Symbols



3.5.3 Propagation Delay Table

Table 3-13. Cell AO222_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A1–Z	t_{PHH}	0.121
		t_{PLL}	0.132
	A2–Z	t_{PHH}	0.112
		t_{PLL}	0.142
	B1–Z	t_{PHH}	0.112
		t_{PLL}	0.110
	B2–Z	t_{PHH}	0.106
		t_{PLL}	0.122
	C1–Z	t_{PHH}	0.146
		t_{PLL}	0.128
	C2–Z	t_{PHH}	0.138
		t_{PLL}	0.137

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-13. Cell AO222_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	A1–Z	t_{PHH}	0.115
		t_{PLL}	0.126
	A2–Z	t_{PHH}	0.104
		t_{PLL}	0.135
	B1–Z	t_{PHH}	0.093
		t_{PLL}	0.099
	B2–Z	t_{PHH}	0.089
		t_{PLL}	0.111
	C1–Z	t_{PHH}	0.125
		t_{PLL}	0.115
	C2–Z	t_{PHH}	0.118
		t_{PLL}	0.125
D	A1–Z	t_{PHH}	0.113
		t_{PLL}	0.121
	A2–Z	t_{PHH}	0.103
		t_{PLL}	0.130
	B1–Z	t_{PHH}	0.093
		t_{PLL}	0.100
	B2–Z	t_{PHH}	0.089
		t_{PLL}	0.112
	C1–Z	t_{PHH}	0.125
		t_{PLL}	0.115
	C2–Z	t_{PHH}	0.117
		t_{PLL}	0.125
E	A1–Z	t_{PHH}	0.122
		t_{PLL}	0.130
	A2–Z	t_{PHH}	0.111
		t_{PLL}	0.138
	B1–Z	t_{PHH}	0.097
		t_{PLL}	0.100
	B2–Z	t_{PHH}	0.092
		t_{PLL}	0.111

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-13. Cell AO222_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	C1–Z	t_{PHH}	0.129
		t_{PLL}	0.115
	C2–Z	t_{PHH}	0.121
		t_{PLL}	0.124
F	A1–Z	t_{PHH}	0.163
		t_{PLL}	0.156
	A2–Z	t_{PHH}	0.150
		t_{PLL}	0.162
	B1–Z	t_{PHH}	0.100
		t_{PLL}	0.104
	B2–Z	t_{PHH}	0.093
		t_{PLL}	0.114
	C1–Z	t_{PHH}	0.131
		t_{PLL}	0.117
	C2–Z	t_{PHH}	0.122
		t_{PLL}	0.126
H	A1–Z	t_{PHH}	0.174
		t_{PLL}	0.168
	A2–Z	t_{PHH}	0.161
		t_{PLL}	0.174
	B1–Z	t_{PHH}	0.104
		t_{PLL}	0.110
	B2–Z	t_{PHH}	0.097
		t_{PLL}	0.120
	C1–Z	t_{PHH}	0.134
		t_{PLL}	0.122
	C2–Z	t_{PHH}	0.125
		t_{PLL}	0.131

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.5.4 Cell Specifications

Table 3-14. Cell AO222_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level					
	B	C	D	E	F	H
A1	2.9	3.4	3.5	3.5	3.8	3.8
A2	2.7	3.2	3.7	3.7	3.5	3.5
B1	6.0	8.9	9.1	9.3	9.5	9.5
B2	5.8	8.6	8.8	9.0	9.2	9.2
C1	5.8	8.6	8.8	9.3	9.2	9.2
C2	5.8	8.4	8.6	8.8	9.1	9.1
Z	58.5	121.6	188.2	252.6	376.9	471.3

Table 3-15. Cell AO222_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
B	6.72	6.72
C		
D		
E		
F	7.28	
H		

3.6 AO2222_{PL} Cell

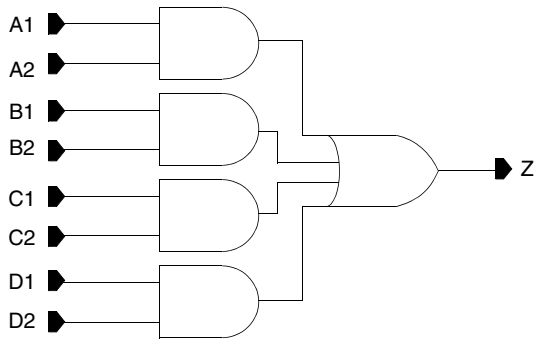
3.6.1 Function

2 × 2 × 2 × 2 AND OR

3.6.2 Description

This cell is a combinational gate, 2 × 2 × 2 × 2 AND OR. The Boolean expression for this cell is $Z = (A1 \times A2) + (B1 \times B2) + (C1 \times C2) + (D1 \times D2)$.

Figure 3-6. Cell AO2222_{PL} Symbols



3.6.3 Propagation Delay Table

Table 3-16. Cell AO2222_{PL} Propagation Delays (Page 1 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A1–Z	t_{PHH}	0.110
		t_{PLL}	0.114
	A2–Z	t_{PHH}	0.105
		t_{PLL}	0.125
	B1–Z	t_{PHH}	0.144
		t_{PLL}	0.131
	B2–Z	t_{PHH}	0.136
		t_{PLL}	0.140
	C1–Z	t_{PHH}	0.104
		t_{PLL}	0.114
	C2–Z	t_{PHH}	0.098
		t_{PLL}	0.125

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-16. Cell AO2222_{PL} Propagation Delays (Page 2 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	D1–Z	t_{PHH}	0.137
		t_{PLL}	0.132
	D2–Z	t_{PHH}	0.128
		t_{PLL}	0.141
C	A1–Z	t_{PHH}	0.091
		t_{PLL}	0.101
	A2–Z	t_{PHH}	0.087
		t_{PLL}	0.113
	B1–Z	t_{PHH}	0.122
		t_{PLL}	0.115
	B2–Z	t_{PHH}	0.115
		t_{PLL}	0.126
	C1–Z	t_{PHH}	0.084
		t_{PLL}	0.100
	C2–Z	t_{PHH}	0.080
		t_{PLL}	0.112
	D1–Z	t_{PHH}	0.115
		t_{PLL}	0.115
	D2–Z	t_{PHH}	0.108
		t_{PLL}	0.125
D	A1–Z	t_{PHH}	0.093
		t_{PLL}	0.101
	A2–Z	t_{PHH}	0.088
		t_{PLL}	0.112
	B1–Z	t_{PHH}	0.123
		t_{PLL}	0.115
	B2–Z	t_{PHH}	0.116
		t_{PLL}	0.125
	C1–Z	t_{PHH}	0.085
		t_{PLL}	0.099
	C2–Z	t_{PHH}	0.081
		t_{PLL}	0.111

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-16. Cell AO2222_{PL} Propagation Delays (Page 3 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
D	D1–Z	t_{PHH}	0.116
		t_{PLL}	0.113
	D2–Z	t_{PHH}	0.108
		t_{PLL}	0.124
E	A1–Z	t_{PHH}	0.096
		t_{PLL}	0.101
	A2–Z	t_{PHH}	0.091
		t_{PLL}	0.112
	B1–Z	t_{PHH}	0.127
		t_{PLL}	0.115
	B2–Z	t_{PHH}	0.119
		t_{PLL}	0.125
	C1–Z	t_{PHH}	0.088
		t_{PLL}	0.099
	C2–Z	t_{PHH}	0.083
		t_{PLL}	0.110
	D1–Z	t_{PHH}	0.119
		t_{PLL}	0.113
	D2–Z	t_{PHH}	0.112
		t_{PLL}	0.123
F	A1–Z	t_{PHH}	0.099
		t_{PLL}	0.105
	A2–Z	t_{PHH}	0.092
		t_{PLL}	0.115
	B1–Z	t_{PHH}	0.129
		t_{PLL}	0.118
	B2–Z	t_{PHH}	0.120
		t_{PLL}	0.126
	C1–Z	t_{PHH}	0.110
		t_{PLL}	0.109
	C2–Z	t_{PHH}	0.103
		t_{PLL}	0.119

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-16. Cell AO2222_{PL} Propagation Delays (Page 4 of 4)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
F	D1–Z	t_{PHH}	0.140
		t_{PLL}	0.122
	D2–Z	t_{PHH}	0.132
		t_{PLL}	0.130
H	A1–Z	t_{PHH}	0.103
		t_{PLL}	0.112
	A2–Z	t_{PHH}	0.096
		t_{PLL}	0.121
	B1–Z	t_{PHH}	0.132
		t_{PLL}	0.124
	B2–Z	t_{PHH}	0.123
		t_{PLL}	0.133
	C1–Z	t_{PHH}	0.113
		t_{PLL}	0.116
	C2–Z	t_{PHH}	0.106
		t_{PLL}	0.125
	D1–Z	t_{PHH}	0.143
		t_{PLL}	0.128
	D2–Z	t_{PHH}	0.134
		t_{PLL}	0.136

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.6.4 Cell Specifications

Table 3-17. Cell AO2222_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level					
	B	C	D	E	F	H
A1	6.0	9.0	9.1	9.2	9.3	9.2
A2	5.7	8.7	8.8	8.9	9.0	8.9
B1	5.7	8.7	8.8	9.2	9.3	9.3
B2	5.9	8.8	8.9	8.9	8.9	8.9
C1	5.9	9.0	9.1	9.2	9.2	9.2
C2	5.7	8.7	8.8	8.9	9.0	9.0
D1	5.7	8.8	8.8	9.2	9.3	9.2
D2	5.8	8.6	8.7	8.8	8.9	8.9
Z	58.6	121.6	183.7	253.0	380.0	493.4

Table 3-18. Cell AO2222_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
B	7.84	6.72
C		
D		
E		
F	8.96	
H		

3.7 AOI21_{PL} Cell

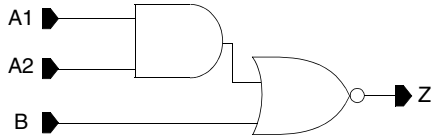
3.7.1 Function

2 × 1 AND OR inverter

3.7.2 Description

This cell is a combinational gate, 2 × 1 AND OR inverter. The Boolean expression for this cell is $Z = \overline{(A1 \times A2) + B}$.

Figure 3-7. Cell AOI21_{PL} Symbols



3.7.3 Propagation Delay Table

Table 3-19. Cell AOI21_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A	A1–Z	t_{PLH}	0.114
		t_{PHL}	0.068
	A2–Z	t_{PLH}	0.123
		t_{PHL}	0.058
	B–Z	t_{PLH}	0.072
		t_{PHL}	0.070
B	A1–Z	t_{PLH}	0.081
		t_{PHL}	0.068
	A2–Z	t_{PLH}	0.090
		t_{PHL}	0.059
	B–Z	t_{PLH}	0.053
		t_{PHL}	0.096

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-19. Cell AOI21_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	A1–Z	t_{PLH}	0.066
		t_{PHL}	0.054
	A2–Z	t_{PLH}	0.077
		t_{PHL}	0.048
	B–Z	t_{PLH}	0.044
		t_{PHL}	0.102
D	A1–Z	t_{PLH}	0.068
		t_{PHL}	0.043
	A2–Z	t_{PLH}	0.081
		t_{PHL}	0.040
	B–Z	t_{PLH}	0.069
		t_{PHL}	0.074
E	A1–Z	t_{PLH}	0.066
		t_{PHL}	0.040
	A2–Z	t_{PLH}	0.080
		t_{PHL}	0.037
	B–Z	t_{PLH}	0.067
		t_{PHL}	0.069
F	A1–Z	t_{PLH}	0.063
		t_{PHL}	0.039
	A2–Z	t_{PLH}	0.077
		t_{PHL}	0.037
	B–Z	t_{PLH}	0.064
		t_{PHL}	0.069
H	A1–Z	t_{PLH}	0.065
		t_{PHL}	0.038
	A2–Z	t_{PLH}	0.079
		t_{PHL}	0.036
	B–Z	t_{PLH}	0.065
		t_{PHL}	0.063

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.7.4 Cell Specifications

Table 3-20. Cell AOI21_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level						
	A	B	C	D	E	F	H
A1	2.8	4.1	7.2	11.8	15.1	24.3	34.2
A2	2.6	3.8	6.9	11.3	14.8	24.0	34.6
B	4.5	6.5	11.2	11.2	14.2	20.6	30.8
Z	31.9	61.9	128.3	191.8	251.4	417.4	580.3

Table 3-21. Cell AOI21_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
A	2.80	6.72
B		
C		
D	3.92	
E		
F	6.16	
H	8.96	

3.8 AOI22_{PL} Cell

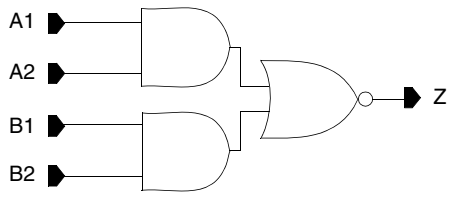
3.8.1 Function

2 × 2 AND OR inverter

3.8.2 Description

This cell is a combinational gate, 2 × 2 AND OR inverter. The Boolean expression for this cell is $Z = \overline{(A1 \times A2) + (B1 \times B2)}$.

Figure 3-8. Cell AOI22_{PL} Symbols



3.8.3 Propagation Delay Table

Table 3-22. Cell AOI22_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A	A1–Z	t_{PLH}	0.100
		t_{PHL}	0.076
	A2–Z	t_{PLH}	0.108
		t_{PHL}	0.066
	B1–Z	t_{PLH}	0.114
		t_{PHL}	0.104
	B2–Z	t_{PLH}	0.122
		t_{PHL}	0.092
B	A1–Z	t_{PLH}	0.075
		t_{PHL}	0.057
	A2–Z	t_{PLH}	0.085
		t_{PHL}	0.050
	B1–Z	t_{PLH}	0.089
		t_{PHL}	0.087
	B2–Z	t_{PLH}	0.099
		t_{PHL}	0.077

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-22. Cell AOI22_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	A1–Z	t_{PLH}	0.062
		t_{PHL}	0.045
	A2–Z	t_{PLH}	0.074
		t_{PHL}	0.041
	B1–Z	t_{PLH}	0.076
		t_{PHL}	0.075
	B2–Z	t_{PLH}	0.086
		t_{PHL}	0.068
D	A1–Z	t_{PLH}	0.062
		t_{PHL}	0.049
	A2–Z	t_{PLH}	0.073
		t_{PHL}	0.044
	B1–Z	t_{PLH}	0.076
		t_{PHL}	0.081
	B2–Z	t_{PLH}	0.085
		t_{PHL}	0.073
E	A1–Z	t_{PLH}	0.059
		t_{PHL}	0.046
	A2–Z	t_{PLH}	0.070
		t_{PHL}	0.042
	B1–Z	t_{PLH}	0.073
		t_{PHL}	0.079
	B2–Z	t_{PLH}	0.082
		t_{PHL}	0.071
F	A1–Z	t_{PLH}	0.055
		t_{PHL}	0.047
	A2–Z	t_{PLH}	0.066
		t_{PHL}	0.043
	B1–Z	t_{PLH}	0.071
		t_{PHL}	0.081
	B2–Z	t_{PLH}	0.080
		t_{PHL}	0.073

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-22. Cell AOI22_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
H	A1–Z	t_{PLH}	0.054
		t_{PHL}	0.048
	A2–Z	t_{PLH}	0.064
		t_{PHL}	0.043
	B1–Z	t_{PLH}	0.070
		t_{PHL}	0.084
	B2–Z	t_{PLH}	0.078
		t_{PHL}	0.076

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.8.4 Cell Specifications

Table 3-23. Cell AOI22_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level						
	A	B	C	D	E	F	H
A1	3.0	4.7	8.4	12.4	16.4	23.7	31.5
A2	2.6	4.4	8.0	12.6	16.4	23.9	31.7
B1	3.1	4.8	8.2	12.2	16.2	23.7	30.9
B2	3.2	4.7	8.2	12.2	16.1	23.6	31.0
Z	46.1	90.4	181.1	277.9	380.2	554.4	735.4

Table 3-24. Cell AOI22_{PL} Area

Performance Level	Cell Dimensions (µm)	
	Width	Length
A	3.36	6.72
B		
C		
D	6.16	
E		
F	8.96	
H	11.20	

3.9 AOI33_{PL} Cell

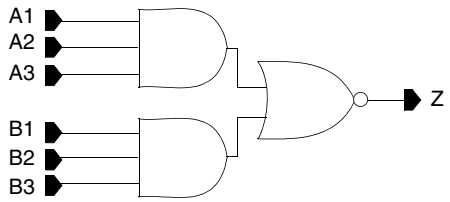
3.9.1 Function

3 × 3 AND OR inverter

3.9.2 Description

This cell is a combinational gate, 3 × 3 AND OR inverter. The Boolean expression for this cell is $Z = \overline{(A1 \times A2 \times A3) + (B1 \times B2 \times B3)}$.

Figure 3-9. Cell AOI33_{PL} Symbols



3.9.3 Propagation Delay Table

Table 3-25. Cell AOI33_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	A1–Z	t_{PLH}	0.212
		t_{PHL}	0.190
	A2–Z	t_{PLH}	0.220
		t_{PHL}	0.185
	A3–Z	t_{PLH}	0.229
		t_{PHL}	0.176
	B1–Z	t_{PLH}	0.231
		t_{PHL}	0.199
	B2–Z	t_{PLH}	0.239
		t_{PHL}	0.194
	B3–Z	t_{PLH}	0.248
		t_{PHL}	0.184

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-25. Cell AOI33_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	A1–Z	t_{PLH}	0.193
		t_{PHL}	0.184
	A2–Z	t_{PLH}	0.201
		t_{PHL}	0.179
	A3–Z	t_{PLH}	0.210
		t_{PHL}	0.171
	B1–Z	t_{PLH}	0.207
		t_{PHL}	0.190
	B2–Z	t_{PLH}	0.214
		t_{PHL}	0.186
	B3–Z	t_{PLH}	0.223
		t_{PHL}	0.176
H	A1–Z	t_{PLH}	0.163
		t_{PHL}	0.160
	A2–Z	t_{PLH}	0.173
		t_{PHL}	0.158
	A3–Z	t_{PLH}	0.183
		t_{PHL}	0.152
	B1–Z	t_{PLH}	0.169
		t_{PHL}	0.159
	B2–Z	t_{PLH}	0.180
		t_{PHL}	0.156
	B3–Z	t_{PLH}	0.189
		t_{PHL}	0.150

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.9.4 Cell Specifications

Table 3-26. Cell AOI33_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level		
	C	E	H
A1	2.7	3.1	4.8
A2	2.6	3.0	4.7
A3	2.4	2.8	4.5
B1	2.7	3.0	4.8
B2	2.5	2.9	4.6
B3	2.4	2.8	4.4
Z	116.5	245.7	450.2

Table 3-27. Cell AOI33_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
C	9.52	6.72
E		
H		

3.10 AOI44_{PL} Cell

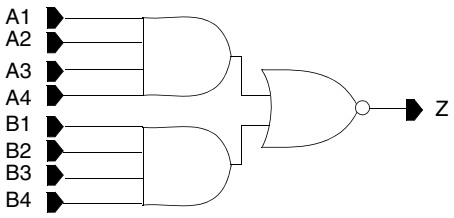
3.10.1 Function

4 × 4 AND OR inverter

3.10.2 Description

This cell is a combinational gate, 4 × 4 AND OR inverter. The Boolean expression for this cell is $Z = \overline{(A1 \times A2 \times A3 \times A4) + (B1 \times B2 \times B3 \times B4)}$.

Figure 3-10. Cell AOI44_{PL} Symbols



3.10.3 Propagation Delay Table

Table 3-28. Cell AOI44_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	A1–Z	t_{PLH}	0.212
		t_{PHL}	0.200
	A2–Z	t_{PLH}	0.222
		t_{PHL}	0.200
	A3–Z	t_{PLH}	0.231
		t_{PHL}	0.198
	A4–Z	t_{PLH}	0.239
		t_{PHL}	0.193
	B1–Z	t_{PLH}	0.221
		t_{PHL}	0.224
	B2–Z	t_{PLH}	0.231
		t_{PHL}	0.223
	B3–Z	t_{PLH}	0.240
		t_{PHL}	0.221
	B4–Z	t_{PLH}	0.249
		t_{PHL}	0.217

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-28. Cell AOI44_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	A1–Z	t_{PLH}	0.206
		t_{PHL}	0.191
	A2–Z	t_{PLH}	0.217
		t_{PHL}	0.192
	A3–Z	t_{PLH}	0.227
		t_{PHL}	0.190
	A4–Z	t_{PLH}	0.235
		t_{PHL}	0.186
	B1–Z	t_{PLH}	0.212
		t_{PHL}	0.208
	B2–Z	t_{PLH}	0.223
		t_{PHL}	0.209
	B3–Z	t_{PLH}	0.232
		t_{PHL}	0.207
	B4–Z	t_{PLH}	0.242
		t_{PHL}	0.204
H	A1–Z	t_{PLH}	0.176
		t_{PHL}	0.166
	A2–Z	t_{PLH}	0.189
		t_{PHL}	0.168
	A3–Z	t_{PLH}	0.200
		t_{PHL}	0.168
	A4–Z	t_{PLH}	0.210
		t_{PHL}	0.166
	B1–Z	t_{PLH}	0.181
		t_{PHL}	0.180
	B2–Z	t_{PLH}	0.194
		t_{PHL}	0.183
	B3–Z	t_{PLH}	0.205
		t_{PHL}	0.183
	B4–Z	t_{PLH}	0.215
		t_{PHL}	0.181

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.10.4 Cell Specifications

Table 3-29. Cell AOI44_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level		
	C	E	H
A1	2.6	2.9	4.6
A2	2.5	2.7	4.3
A3	2.4	2.7	4.2
A4	2.2	2.5	4.1
B1	2.6	2.8	4.5
B2	2.4	2.7	4.3
B3	2.3	2.6	4.1
B4	2.3	2.6	4.1
Z	121.1	245.3	469.1

Table 3-30. Cell AOI44_{PL} Area

Performance Level	Cell Dimensions (µm)	
	Width	Length
C	10.64	6.72
E		
H		

3.11 AOI222_{PL} Cell

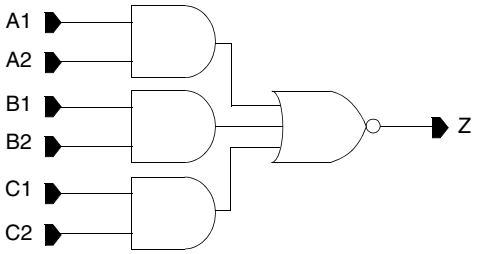
3.11.1 Function

2 × 2 × 2 AND OR inverter

3.11.2 Description

This cell is a combinational gate, 2 × 2 × 2 AND OR inverter. The Boolean expression for this cell is $Z = \overline{(A1 \times A2) + (B1 \times B2) + (C1 \times C2)}$.

Figure 3-11. Cell AOI222_{PL} Symbols



3.11.3 Propagation Delay Table

Table 3-31. Cell AOI222_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
F	A1–Z	t_{PLH}	0.138
		t_{PHL}	0.179
	A2–Z	t_{PLH}	0.144
		t_{PHL}	0.167
	B1–Z	t_{PLH}	0.140
		t_{PHL}	0.163
	B2–Z	t_{PLH}	0.148
		t_{PHL}	0.155
	C1–Z	t_{PLH}	0.159
		t_{PHL}	0.210
	C2–Z	t_{PLH}	0.166
		t_{PHL}	0.201

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-31. Cell AOI222_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
H	A1–Z	t_{PLH}	0.139
		t_{PHL}	0.168
	A2–Z	t_{PLH}	0.147
		t_{PHL}	0.157
	B1–Z	t_{PLH}	0.135
		t_{PHL}	0.156
	B2–Z	t_{PLH}	0.145
		t_{PHL}	0.151
	C1–Z	t_{PLH}	0.150
		t_{PHL}	0.190
	C2–Z	t_{PLH}	0.159
		t_{PHL}	0.182
I	A1–Z	t_{PLH}	0.145
		t_{PHL}	0.159
	A2–Z	t_{PLH}	0.153
		t_{PHL}	0.150
	B1–Z	t_{PLH}	0.141
		t_{PHL}	0.152
	B2–Z	t_{PLH}	0.152
		t_{PHL}	0.147
	C1–Z	t_{PLH}	0.156
		t_{PHL}	0.184
	C2–Z	t_{PLH}	0.166
		t_{PHL}	0.176

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.11.4 Cell Specifications

Table 3-32. Cell AOI222_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level		
	F	H	I
A1	4.8	4.7	5.1
A2	4.3	4.3	4.6
B1	8.3	9.1	9.2
B2	8.0	8.7	8.8
C1	7.9	8.8	8.9
C2	8.2	8.9	9.0
Z	389.7	502.7	716.2

Table 3-33. Cell AOI222_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
F	7.84	6.72
H		
I		

3.12 AOI2222_{PL} Cell

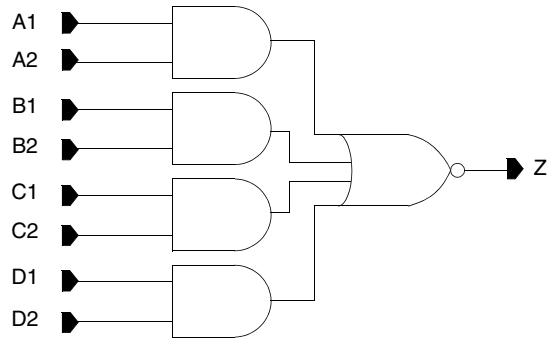
3.12.1 Function

2 × 2 × 2 × 2 AND OR inverter

3.12.2 Description

This cell is a combinational gate, 2 × 2 × 2 × 2 AND OR inverter. The Boolean expression for this cell is $Z = \overline{(A1 \times A2) + (B1 \times B2) + (C1 \times C2) + (D1 \times D2)}$.

Figure 3-12. Cell AOI2222_{PL} Symbols



3.12.3 Propagation Delay Table

Table 3-34. Cell AOI2222_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
F	A1–Z	t_{PLH}	0.140
		t_{PHL}	0.165
	A2–Z	t_{PLH}	0.148
		t_{PHL}	0.157
	B1–Z	t_{PLH}	0.160
		t_{PHL}	0.212
	B2–Z	t_{PLH}	0.166
		t_{PHL}	0.202
	C1–Z	t_{PLH}	0.136
		t_{PHL}	0.153
	C2–Z	t_{PLH}	0.144
		t_{PHL}	0.145

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-34. Cell AOI2222_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
F	D1–Z	t_{PLH}	0.158
		t_{PHL}	0.200
	D2–Z	t_{PLH}	0.164
		t_{PHL}	0.191
H	A1–Z	t_{PLH}	0.135
		t_{PHL}	0.158
	A2–Z	t_{PLH}	0.146
		t_{PHL}	0.153
	B1–Z	t_{PLH}	0.151
		t_{PHL}	0.191
	B2–Z	t_{PLH}	0.160
		t_{PHL}	0.183
	C1–Z	t_{PLH}	0.131
		t_{PHL}	0.143
	C2–Z	t_{PLH}	0.142
		t_{PHL}	0.138
	D1–Z	t_{PLH}	0.148
		t_{PHL}	0.177
	D2–Z	t_{PLH}	0.157
		t_{PHL}	0.169
I	A1–Z	t_{PLH}	0.142
		t_{PHL}	0.153
	A2–Z	t_{PLH}	0.152
		t_{PHL}	0.148
	B1–Z	t_{PLH}	0.157
		t_{PHL}	0.185
	B2–Z	t_{PLH}	0.166
		t_{PHL}	0.177
	C1–Z	t_{PLH}	0.138
		t_{PHL}	0.140
	C2–Z	t_{PLH}	0.149
		t_{PHL}	0.136

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-34. Cell AOI2222_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
I	D1–Z	t_{PLH}	0.155
		t_{PHL}	0.173
	D2–Z	t_{PLH}	0.165
		t_{PHL}	0.165

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.12.4 Cell Specifications

Table 3-35. Cell AOI2222_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level		
	F	H	I
A1	8.2	9.0	9.2
A2	8.0	8.8	8.9
B1	7.9	8.8	8.9
B2	8.1	8.9	9.0
C1	8.2	9.0	9.2
C2	8.0	8.8	8.9
D1	7.9	8.8	8.9
D2	7.9	8.7	8.8
Z	389.2	501.2	715.7

Table 3-36. Cell AOI2222_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
F	8.96	6.72
H		
I		

3.13 OA21_{PL} Cell

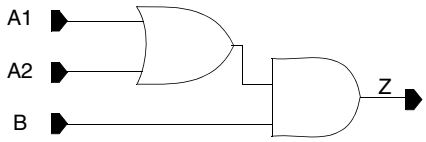
3.13.1 Function

2 × 1 OR AND

3.13.2 Description

This cell is a combinational gate, 2 × 1 OR AND. The Boolean expression for this cell is $Z = (A1 + A2) \times B$.

Figure 3-13. Cell OA21_{PL} Symbols



3.13.3 Propagation Delay Table

Table 3-37. Cell OA21_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A1–Z	t_{PHH}	0.118
		t_{PLL}	0.155
	A2–Z	t_{PHH}	0.128
		t_{PLL}	0.147
	B–Z	t_{PHH}	0.112
		t_{PLL}	0.132
C	A1–Z	t_{PHH}	0.114
		t_{PLL}	0.157
	A2–Z	t_{PHH}	0.124
		t_{PLL}	0.148
	B–Z	t_{PHH}	0.105
		t_{PLL}	0.142
D	A1–Z	t_{PHH}	0.125
		t_{PLL}	0.148
	A2–Z	t_{PHH}	0.137
		t_{PLL}	0.140
	B–Z	t_{PHH}	0.114
		t_{PLL}	0.152

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-37. Cell OA21_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	A1–Z	t_{PHH}	0.135
		t_{PLL}	0.145
	A2–Z	t_{PHH}	0.148
		t_{PLL}	0.137
	B–Z	t_{PHH}	0.122
		t_{PLL}	0.164
F	A1–Z	t_{PHH}	0.128
		t_{PLL}	0.139
	A2–Z	t_{PHH}	0.142
		t_{PLL}	0.132
	B–Z	t_{PHH}	0.115
		t_{PLL}	0.157
H	A1–Z	t_{PHH}	0.120
		t_{PLL}	0.135
	A2–Z	t_{PHH}	0.135
		t_{PLL}	0.128
	B–Z	t_{PHH}	0.107
		t_{PLL}	0.156
I	A1–Z	t_{PHH}	0.115
		t_{PLL}	0.131
	A2–Z	t_{PHH}	0.130
		t_{PLL}	0.124
	B–Z	t_{PHH}	0.103
		t_{PLL}	0.152
J	A1–Z	t_{PHH}	0.110
		t_{PLL}	0.132
	A2–Z	t_{PHH}	0.124
		t_{PLL}	0.125
	B–Z	t_{PHH}	0.101
		t_{PLL}	0.157

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-37. Cell OA21_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
K	A1–Z	t_{PHH}	0.108
		t_{PLL}	0.129
	A2–Z	t_{PHH}	0.122
		t_{PLL}	0.123
	B–Z	t_{PHH}	0.100
		t_{PLL}	0.155

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.13.4 Cell Specifications

Table 3-38. Cell OA21_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level								
	B	C	D	E	F	H	I	J	K
A1	2.9	3.0	3.3	3.6	4.8	6.1	7.8	12.3	15.8
A2	2.7	2.8	3.1	3.4	4.4	5.7	7.3	12.3	15.6
B	3.9	3.9	3.9	4.0	5.0	6.2	7.6	8.9	11.0
Z	54.9	111.4	176.2	245.2	385.8	521.4	704.5	1043.2	1394.0

Table 3-39. Cell OA21_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
B	3.92	6.72
C		
D		
E		
F		
H		
I		
J	8.40	
K		

3.14 OA22_{PL} Cell

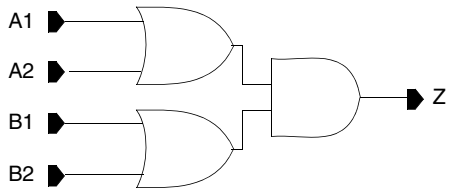
3.14.1 Function

2 × 2 OR AND

3.14.2 Description

This cell is a combinational gate, 2 × 2 OR AND. The Boolean expression for this cell is $Z = (A1 + A2) \times (B1 + B2)$.

Figure 3-14. Cell OA22_{PL} Symbols



3.14.3 Propagation Delay Table

Table 3-40. Cell OA22_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A1–Z	t_{PHH}	0.128
		t_{PLL}	0.133
	A2–Z	t_{PHH}	0.144
		t_{PLL}	0.129
	B1–Z	t_{PHH}	0.133
		t_{PLL}	0.162
	B2–Z	t_{PHH}	0.145
		t_{PLL}	0.152
C	A1–Z	t_{PHH}	0.114
		t_{PLL}	0.132
	A2–Z	t_{PHH}	0.129
		t_{PLL}	0.127
	B1–Z	t_{PHH}	0.116
		t_{PLL}	0.158
	B2–Z	t_{PHH}	0.129
		t_{PLL}	0.149

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-40. Cell OA22_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
D	A1–Z	t_{PHH}	0.110
		t_{PLL}	0.127
	A2–Z	t_{PHH}	0.124
		t_{PLL}	0.122
	B1–Z	t_{PHH}	0.111
		t_{PLL}	0.151
	B2–Z	t_{PHH}	0.123
		t_{PLL}	0.142
E	A1–Z	t_{PHH}	0.106
		t_{PLL}	0.126
	A2–Z	t_{PHH}	0.120
		t_{PLL}	0.120
	B1–Z	t_{PHH}	0.106
		t_{PLL}	0.148
	B2–Z	t_{PHH}	0.118
		t_{PLL}	0.140
F	A1–Z	t_{PHH}	0.101
		t_{PLL}	0.123
	A2–Z	t_{PHH}	0.114
		t_{PLL}	0.117
	B1–Z	t_{PHH}	0.100
		t_{PLL}	0.143
	B2–Z	t_{PHH}	0.111
		t_{PLL}	0.135
H	A1–Z	t_{PHH}	0.096
		t_{PLL}	0.119
	A2–Z	t_{PHH}	0.109
		t_{PLL}	0.113
	B1–Z	t_{PHH}	0.095
		t_{PLL}	0.139
	B2–Z	t_{PHH}	0.106
		t_{PLL}	0.131

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-40. Cell OA22_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
I	A1–Z	t_{PHH}	0.107
		t_{PLL}	0.133
	A2–Z	t_{PHH}	0.119
		t_{PLL}	0.126
	B1–Z	t_{PHH}	0.105
		t_{PLL}	0.152
	B2–Z	t_{PHH}	0.116
		t_{PLL}	0.143
J	A1–Z	t_{PHH}	0.105
		t_{PLL}	0.129
	A2–Z	t_{PHH}	0.119
		t_{PLL}	0.122
	B1–Z	t_{PHH}	0.104
		t_{PLL}	0.149
	B2–Z	t_{PHH}	0.116
		t_{PLL}	0.140
K	A1–Z	t_{PHH}	0.108
		t_{PLL}	0.132
	A2–Z	t_{PHH}	0.121
		t_{PLL}	0.125
	B1–Z	t_{PHH}	0.106
		t_{PLL}	0.151
	B2–Z	t_{PHH}	0.118
		t_{PLL}	0.144

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.14.4 Cell Specifications

Table 3-41. Cell OA22_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level								
	B	C	D	E	F	H	I	J	K
A1	3.2	3.6	4.2	4.8	6.5	8.4	8.4	13.4	16.4
A2	3.5	3.9	4.4	5.0	6.3	8.1	8.1	13.2	16.1
B1	3.6	4.1	4.6	5.2	6.8	8.7	8.7	13.1	16.0
B2	3.1	3.5	4.0	4.5	6.0	7.7	7.7	12.8	15.6
Z	59.1	110.9	167.5	226.4	364.2	485.7	706.2	978.4	1392.0

Table 3-42. Cell OA22_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
B	4.48	6.72
C		
D		
E		
F		
H		
I		
J	10.08	
K		

3.15 OA222_{PL} Cell

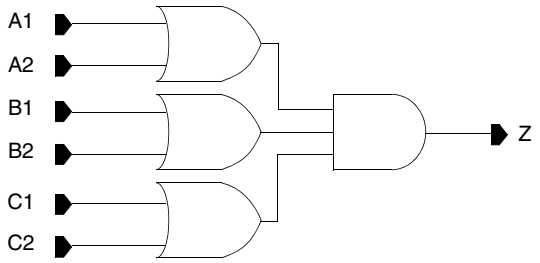
3.15.1 Function

2 × 2 × 2 OR AND

3.15.2 Description

This cell is a combinational gate, 2 × 2 × 2 OR AND. The Boolean expression for this cell is $Z = (A1 + A2) \times (B1 + B2) \times (C1 + C2)$.

Figure 3-15. Cell OA222_{PL} Symbols



3.15.3 Propagation Delay Table

Table 3-43. Cell OA222_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A1–Z	t_{PHH}	0.106
		t_{PLL}	0.175
	A2–Z	t_{PHH}	0.113
		t_{PLL}	0.166
	B1–Z	t_{PHH}	0.132
		t_{PLL}	0.180
	B2–Z	t_{PHH}	0.144
		t_{PLL}	0.173
	C1–Z	t_{PHH}	0.139
		t_{PLL}	0.218
	C2–Z	t_{PHH}	0.146
		t_{PLL}	0.206

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-43. Cell OA222_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	A1–Z	t_{PHH}	0.115
		t_{PLL}	0.178
	A2–Z	t_{PHH}	0.122
		t_{PLL}	0.169
	B1–Z	t_{PHH}	0.141
		t_{PLL}	0.176
	B2–Z	t_{PHH}	0.154
		t_{PLL}	0.170
	C1–Z	t_{PHH}	0.144
		t_{PLL}	0.204
	C2–Z	t_{PHH}	0.153
		t_{PLL}	0.194
D	A1–Z	t_{PHH}	0.119
		t_{PLL}	0.156
	A2–Z	t_{PHH}	0.130
		t_{PLL}	0.149
	B1–Z	t_{PHH}	0.150
		t_{PLL}	0.154
	B2–Z	t_{PHH}	0.167
		t_{PLL}	0.148
	C1–Z	t_{PHH}	0.150
		t_{PLL}	0.173
	C2–Z	t_{PHH}	0.162
		t_{PLL}	0.164
E	A1–Z	t_{PHH}	0.115
		t_{PLL}	0.153
	A2–Z	t_{PHH}	0.127
		t_{PLL}	0.147
	B1–Z	t_{PHH}	0.144
		t_{PLL}	0.151
	B2–Z	t_{PHH}	0.159
		t_{PLL}	0.144

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-43. Cell OA222_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	C1–Z	t_{PHH}	0.142
		t_{PLL}	0.167
	C2–Z	t_{PHH}	0.154
		t_{PLL}	0.159
F	A1–Z	t_{PHH}	0.108
		t_{PLL}	0.147
	A2–Z	t_{PHH}	0.119
		t_{PLL}	0.141
	B1–Z	t_{PHH}	0.131
		t_{PLL}	0.144
	B2–Z	t_{PHH}	0.147
		t_{PLL}	0.138
	C1–Z	t_{PHH}	0.128
		t_{PLL}	0.160
	C2–Z	t_{PHH}	0.141
		t_{PLL}	0.152

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.15.4 Cell Specifications

Table 3-44. Cell OA222_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level				
	B	C	D	E	F
A1	2.9	3.3	4.8	5.8	7.5
A2	2.7	3.0	4.5	5.4	7.1
B1	2.9	3.3	4.9	5.9	7.6
B2	3.0	3.3	4.7	5.6	7.2
C1	3.4	3.7	5.2	6.2	7.9
C2	2.7	3.0	4.4	5.4	6.9
Z	61.7	129.9	209.9	277.2	363.5

Table 3-45. Cell OA222_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
B	7.84	6.72
C		
D	8.40	
E		
F		

3.16 OA2222_{PL} Cell

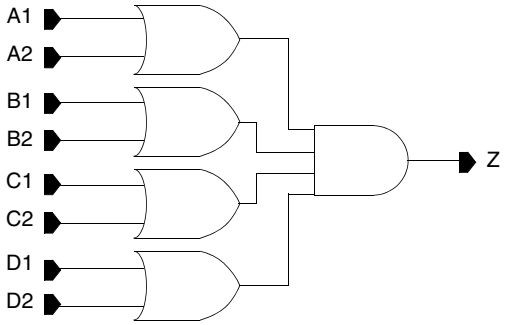
3.16.1 Function

2 × 2 × 2 × 2 OR AND

3.16.2 Description

This cell is a combinational gate, 2 × 2 × 2 × 2 OR AND. The Boolean expression for this cell is $Z = (A1 + A2) \times (B1 + B2) \times (C1 + C2) \times (D1 + D2)$.

Figure 3-16. Cell OA2222_{PL} Symbols



3.16.3 Propagation Delay Table

Table 3-46. Cell OA2222_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A1–Z	t_{PHH}	0.136
		t_{PLL}	0.184
	A2–Z	t_{PHH}	0.147
		t_{PLL}	0.178
	B1–Z	t_{PHH}	0.143
		t_{PLL}	0.222
	B2–Z	t_{PHH}	0.150
		t_{PLL}	0.211
	C1–Z	t_{PHH}	0.132
		t_{PLL}	0.180
	C2–Z	t_{PHH}	0.144
		t_{PLL}	0.173
	D1–Z	t_{PHH}	0.139
		t_{PLL}	0.218
	D2–Z	t_{PHH}	0.146
		t_{PLL}	0.206
C	A1–Z	t_{PHH}	0.147
		t_{PLL}	0.184
	A2–Z	t_{PHH}	0.160
		t_{PLL}	0.178
	B1–Z	t_{PHH}	0.150
		t_{PLL}	0.213
	B2–Z	t_{PHH}	0.159
		t_{PLL}	0.203
	C1–Z	t_{PHH}	0.141
		t_{PLL}	0.176
	C2–Z	t_{PHH}	0.154
		t_{PLL}	0.170
	D1–Z	t_{PHH}	0.144
		t_{PLL}	0.204
	D2–Z	t_{PHH}	0.153
		t_{PLL}	0.194

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-46. Cell OA2222_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
D	A1–Z	t_{PHH}	0.152
		t_{PLL}	0.160
	A2–Z	t_{PHH}	0.168
		t_{PLL}	0.155
	B1–Z	t_{PHH}	0.151
		t_{PLL}	0.180
	B2–Z	t_{PHH}	0.166
		t_{PLL}	0.172
	C1–Z	t_{PHH}	0.149
		t_{PLL}	0.154
	C2–Z	t_{PHH}	0.166
		t_{PLL}	0.148
	D1–Z	t_{PHH}	0.149
		t_{PLL}	0.172
	D2–Z	t_{PHH}	0.161
		t_{PLL}	0.164
E	A1–Z	t_{PHH}	0.147
		t_{PLL}	0.157
	A2–Z	t_{PHH}	0.162
		t_{PLL}	0.152
	B1–Z	t_{PHH}	0.144
		t_{PLL}	0.175
	B2–Z	t_{PHH}	0.159
		t_{PLL}	0.167
	C1–Z	t_{PHH}	0.143
		t_{PLL}	0.150
	C2–Z	t_{PHH}	0.159
		t_{PLL}	0.144
	D1–Z	t_{PHH}	0.141
		t_{PLL}	0.167
	D2–Z	t_{PHH}	0.153
		t_{PLL}	0.159

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-46. Cell OA2222_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
F	A1–Z	t_{PHH}	0.137
		t_{PLL}	0.151
	A2–Z	t_{PHH}	0.151
		t_{PLL}	0.145
	B1–Z	t_{PHH}	0.134
		t_{PLL}	0.168
	B2–Z	t_{PHH}	0.147
		t_{PLL}	0.160
	C1–Z	t_{PHH}	0.131
		t_{PLL}	0.144
	C2–Z	t_{PHH}	0.146
		t_{PLL}	0.137
	D1–Z	t_{PHH}	0.128
		t_{PLL}	0.160
	D2–Z	t_{PHH}	0.141
		t_{PLL}	0.152

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.16.4 Cell Specifications

Table 3-47. Cell OA2222_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level				
	B	C	D	E	F
A1	2.9	3.3	4.9	5.9	7.6
A2	3.0	3.3	4.7	5.6	7.2
B1	3.4	3.7	5.3	6.2	7.9
B2	2.7	3.0	4.4	5.4	7.0
C1	2.9	3.3	4.9	5.9	7.6
C2	3.0	3.3	4.7	5.6	7.2
D1	3.3	3.7	5.2	6.2	7.9
D2	2.7	3.0	4.5	5.4	6.9
Z	61.6	130.3	210.3	277.7	363.5

Table 3-48. Cell OA2222_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
B	9.52	6.72
C		
D		
E		
F		

3.17 OAI21_{PL} Cell

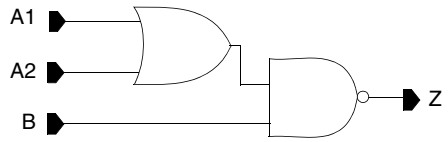
3.17.1 Function

2 × 1 OR AND inverter

3.17.2 Description

This cell is a combinational gate, 2 × 1 OR AND inverter. The Boolean expression for this cell is $Z = \overline{(A1 + A2) \times B}$.

Figure 3-17. Cell OAI21_{PL} Symbols



3.17.3 Propagation Delay Table

Table 3-49. Cell OAI21_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A	A1–Z	t_{PLH}	0.108
		t_{PHL}	0.067
	A2–Z	t_{PLH}	0.101
		t_{PHL}	0.078
	B–Z	t_{PLH}	0.105
		t_{PHL}	0.057
B	A1–Z	t_{PLH}	0.086
		t_{PHL}	0.054
	A2–Z	t_{PLH}	0.081
		t_{PHL}	0.067
	B–Z	t_{PLH}	0.089
		t_{PHL}	0.046

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-49. Cell OAI21_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	A1–Z	t_{PLH}	0.072
		t_{PHL}	0.042
	A2–Z	t_{PLH}	0.069
		t_{PHL}	0.056
	B–Z	t_{PLH}	0.080
		t_{PHL}	0.036
D	A1–Z	t_{PLH}	0.071
		t_{PHL}	0.041
	A2–Z	t_{PLH}	0.068
		t_{PHL}	0.059
	B–Z	t_{PLH}	0.085
		t_{PHL}	0.040
E	A1–Z	t_{PLH}	0.065
		t_{PHL}	0.039
	A2–Z	t_{PLH}	0.063
		t_{PHL}	0.053
	B–Z	t_{PLH}	0.090
		t_{PHL}	0.035
F	A1–Z	t_{PLH}	0.061
		t_{PHL}	0.041
	A2–Z	t_{PLH}	0.060
		t_{PHL}	0.057
	B–Z	t_{PLH}	0.074
		t_{PHL}	0.036
H	A1–Z	t_{PLH}	0.063
		t_{PHL}	0.053
	A2–Z	t_{PLH}	0.065
		t_{PHL}	0.038
	B–Z	t_{PLH}	0.076
		t_{PHL}	0.054

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.17.4 Cell Specifications

Table 3-50. Cell OAI21_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level						
	A	B	C	D	E	F	H
A1	3.0	4.2	7.1	11.3	15.3	21.1	28.1
A2	3.0	4.1	6.9	10.5	14.8	21.0	28.7
B	3.8	5.1	8.2	7.7	10.8	16.8	22.7
Z	34.1	60.9	118.7	181.7	265.3	390.9	488.1

Table 3-51. Cell OAI21_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
A	2.80	6.72
B		
C		
D	3.92	
E		
F	5.60	
H	7.28	

3.18 OAI22_{PL} Cell

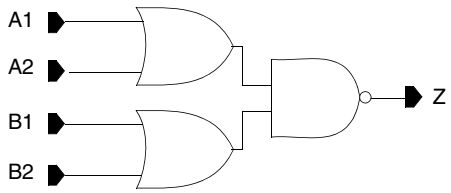
3.18.1 Function

2 × 2 OR AND inverter

3.18.2 Description

This cell is a combinational gate, 2 × 2 OR AND inverter. The Boolean expression for this cell is $Z = \overline{(A1 + A2) \times (B1 + B2)}$.

Figure 3-18. Cell OAI22_{PL} Symbols



3.18.3 Propagation Delay Table

Table 3-52. Cell OAI22_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A	A1–Z	t_{PLH}	0.095
		t_{PHL}	0.074
	A2–Z	t_{PLH}	0.091
		t_{PHL}	0.089
	B1–Z	t_{PLH}	0.120
		t_{PHL}	0.078
	B2–Z	t_{PLH}	0.110
		t_{PHL}	0.089
B	A1–Z	t_{PLH}	0.077
		t_{PHL}	0.060
	A2–Z	t_{PLH}	0.075
		t_{PHL}	0.076
	B1–Z	t_{PLH}	0.099
		t_{PHL}	0.061
	B2–Z	t_{PLH}	0.092
		t_{PHL}	0.074

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-52. Cell OAI22_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	A1–Z	t_{PLH}	0.069
		t_{PHL}	0.054
	A2–Z	t_{PLH}	0.068
		t_{PHL}	0.071
	B1–Z	t_{PLH}	0.089
		t_{PHL}	0.054
	B2–Z	t_{PLH}	0.084
		t_{PHL}	0.070
D	A1–Z	t_{PLH}	0.067
		t_{PHL}	0.052
	A2–Z	t_{PLH}	0.066
		t_{PHL}	0.068
	B1–Z	t_{PLH}	0.087
		t_{PHL}	0.054
	B2–Z	t_{PLH}	0.083
		t_{PHL}	0.067
E	A1–Z	t_{PLH}	0.065
		t_{PHL}	0.049
	A2–Z	t_{PLH}	0.064
		t_{PHL}	0.065
	B1–Z	t_{PLH}	0.085
		t_{PHL}	0.050
	B2–Z	t_{PLH}	0.081
		t_{PHL}	0.064
F	A1–Z	t_{PLH}	0.062
		t_{PHL}	0.047
	A2–Z	t_{PLH}	0.061
		t_{PHL}	0.063
	B1–Z	t_{PLH}	0.083
		t_{PHL}	0.048
	B2–Z	t_{PLH}	0.079
		t_{PHL}	0.063

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.18.4 Cell Specifications

Table 3-53. Cell OAI22_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level					
	A	B	C	D	E	F
A1	3.4	4.9	9.0	13.7	17.6	30.4
A2	3.5	4.8	9.3	13.9	17.6	30.4
B1	3.8	5.3	8.8	13.8	17.5	29.6
B2	3.2	4.6	9.0	13.7	17.4	29.7
Z	45.2	80.5	160.5	237.3	313.4	551.3

Table 3-54. Cell OAI22_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
A	3.92	6.72
B		
C	5.04	
D	7.28	
E		
F	10.08	

3.19 OAI222_{PL} Cell

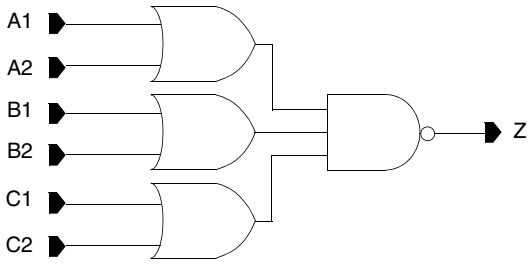
3.19.1 Function

2 × 2 × 2 OR AND inverter

3.19.2 Description

This cell is a combinational gate, 2 × 2 × 2 OR AND inverter. The Boolean expression for this cell is $Z = \overline{(A1 + A2) \times (B1 + B2) \times (C1 + C2)}$.

Figure 3-19. Cell OAI222_{PL} Symbols



3.19.3 Propagation Delay Table

Table 3-55. Cell OAI222_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	A1–Z	t_{PLH}	0.213
		t_{PHL}	0.147
	A2–Z	t_{PLH}	0.204
		t_{PHL}	0.150
	B1–Z	t_{PLH}	0.248
		t_{PHL}	0.175
	B2–Z	t_{PLH}	0.241
		t_{PHL}	0.184
	C1–Z	t_{PLH}	0.290
		t_{PHL}	0.180
	C2–Z	t_{PLH}	0.279
		t_{PHL}	0.184

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-55. Cell OAI222_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
H	A1–Z	t_{PLH}	0.190
		t_{PHL}	0.130
	A2–Z	t_{PLH}	0.182
		t_{PHL}	0.136
	B1–Z	t_{PLH}	0.217
		t_{PHL}	0.153
	B2–Z	t_{PLH}	0.209
		t_{PHL}	0.162
	C1–Z	t_{PLH}	0.249
		t_{PHL}	0.156
	C2–Z	t_{PLH}	0.240
		t_{PHL}	0.161

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.19.4 Cell Specifications

Table 3-56. Cell OAI222_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level	
	E	H
A1	3.0	4.6
A2	2.8	4.3
B1	3.2	5.0
B2	3.2	4.9
C1	3.5	5.2
C2	2.9	4.5
Z	236.5	467.1

Table 3-57. Cell OAI222_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
E	8.96	6.72
H		

3.20 OAI2222_{PL} Cell

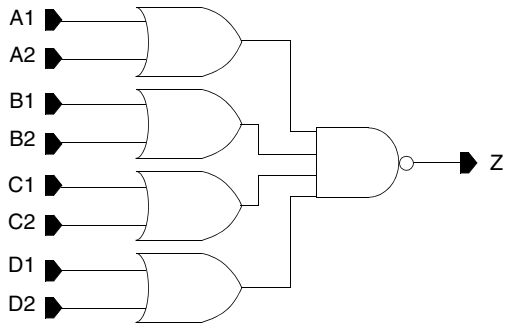
3.20.1 Function

2 × 2 × 2 × 2 OR AND inverter

3.20.2 Description

This cell is a combinational gate, 2 × 2 × 2 × 2 OR AND inverter. The Boolean expression for this cell is $Z = \overline{(A1 + A2) \times (B1 + B2) \times (C1 + C2) \times (D1 + D2)}$.

Figure 3-20. Cell OAI2222_{PL} Symbols



3.20.3 Propagation Delay Table

Table 3-58. Cell OAI2222_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	A1–Z	t_{PLH}	0.227
		t_{PHL}	0.162
	A2–Z	t_{PLH}	0.220
		t_{PHL}	0.171
	B1–Z	t_{PLH}	0.270
		t_{PHL}	0.170
	B2–Z	t_{PLH}	0.258
		t_{PHL}	0.172
	C1–Z	t_{PLH}	0.249
		t_{PHL}	0.177
	C2–Z	t_{PLH}	0.242
		t_{PHL}	0.185

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 3-58. Cell OAI2222_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	D1–Z	t_{PLH}	0.290
		t_{PHL}	0.182
	D2–Z	t_{PLH}	0.280
		t_{PHL}	0.186
H	A1–Z	t_{PLH}	0.202
		t_{PHL}	0.141
	A2–Z	t_{PLH}	0.194
		t_{PHL}	0.150
	B1–Z	t_{PLH}	0.235
		t_{PHL}	0.145
	B2–Z	t_{PLH}	0.225
		t_{PHL}	0.150
	C1–Z	t_{PLH}	0.217
		t_{PHL}	0.155
	C2–Z	t_{PLH}	0.209
		t_{PHL}	0.163
	D1–Z	t_{PLH}	0.250
		t_{PHL}	0.157
	D2–Z	t_{PLH}	0.240
		t_{PHL}	0.162

1. Minimum input transition and minimum output load. See .lib timing files for more information.

3.20.4 Cell Specifications

Table 3-59. Cell OAI2222_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level	
	E	H
A1	3.1	4.9
A2	3.2	4.9
B1	3.6	5.3
B2	2.9	4.5
C1	3.1	4.9
C2	3.2	4.9
D1	3.5	5.2
D2	2.9	4.5
Z	236.4	469.1

Table 3-60. Cell OAI2222_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
E	10.64	10.64
H		

4. Standard Cell Unique Logic

4.1 ADDF_{PL} Cell

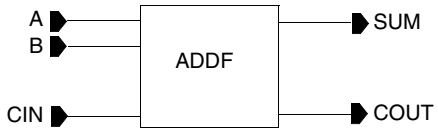
4.1.1 Function

Full adder

4.1.2 Description

This cell is a full, three-bit adder with sum (SUM) and carry (COUT) as outputs.

Figure 4-1. Cell ADDF_{PL} Symbols



4.1.3 Truth Table

Table 4-1. Cell ADDF_{PL} Truth Table

Inputs			Outputs	
A	B	CIN	COUT	SUM
0	0	0	0	0
0	1	0	0	1
1	0	0	0	1
1	1	0	1	0
0	0	1	0	1
0	1	1	1	0
1	0	1	1	0
1	1	1	1	1

4.1.4 Propagation Delay Table

Table 4-2. Cell ADDF_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A–COUT	t_{PHH}	0.186
		t_{PLL}	0.230
	B–COUT	t_{PHH}	0.219
		t_{PLL}	0.188
	CIN–COUT	t_{PHH}	0.118
		t_{PLL}	0.118
	A–SUM	t_{PHH}	0.211
		t_{PLL}	0.196
		t_{PLH}	0.221
		t_{PHL}	0.175
	B–SUM	t_{PHH}	0.254
		t_{PLL}	0.222
		t_{PLH}	0.236
		t_{PHL}	0.207
	CIN–SUM	t_{PHH}	0.090
		t_{PLL}	0.125
		t_{PLH}	0.141
		t_{PHL}	0.145
C	A–COUT	t_{PHH}	0.179
		t_{PLL}	0.225
	B–COUT	t_{PHH}	0.217
		t_{PLL}	0.200
	CIN–COUT	t_{PHH}	0.112
		t_{PLL}	0.118
	A–SUM	t_{PHH}	0.205
		t_{PLL}	0.192
		t_{PLH}	0.216
		t_{PHL}	0.169
	B–SUM	t_{PHH}	0.254
		t_{PLL}	0.218
		t_{PLH}	0.235
		t_{PHL}	0.206

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 4-2. Cell ADDF_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	CIN–SUM	t_{PHH}	0.090
		t_{PLL}	0.123
		t_{PLH}	0.140
		t_{PHL}	0.143
D	A–COUT	t_{PHH}	0.186
		t_{PLL}	0.221
	B–COUT	t_{PHH}	0.226
		t_{PLL}	0.208
	CIN–COUT	t_{PHH}	0.116
		t_{PLL}	0.120
	A–SUM	t_{PHH}	0.194
		t_{PLL}	0.193
		t_{PLH}	0.204
		t_{PHL}	0.169
	B–SUM	t_{PHH}	0.245
		t_{PLL}	0.220
		t_{PLH}	0.225
		t_{PHL}	0.209
	CIN–SUM	t_{PHH}	0.089
		t_{PLL}	0.121
		t_{PLH}	0.138
		t_{PHL}	0.142
E	A–COUT	t_{PHH}	0.192
		t_{PLL}	0.224
	B–COUT	t_{PHH}	0.232
		t_{PLL}	0.212
	CIN–COUT	t_{PHH}	0.120
		t_{PLL}	0.122
	A–SUM	t_{PHH}	0.201
		t_{PLL}	0.198
		t_{PLH}	0.212
		t_{PHL}	0.175

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 4-2. Cell ADDF_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	B–SUM	t_{PHH}	0.256
		t_{PLL}	0.226
		t_{PLH}	0.235
		t_{PHL}	0.215
	CIN–SUM	t_{PHH}	0.100
		t_{PLL}	0.125
		t_{PLH}	0.147
		t_{PHL}	0.147
F	A–COUT	t_{PHH}	0.224
		t_{PLL}	0.231
	B–COUT	t_{PHH}	0.270
		t_{PLL}	0.229
	CIN–COUT	t_{PHH}	0.150
		t_{PLL}	0.132
	A–SUM	t_{PHH}	0.203
		t_{PLL}	0.226
		t_{PLH}	0.217
		t_{PHL}	0.199
	B–SUM	t_{PHH}	0.274
		t_{PLL}	0.257
		t_{PLH}	0.251
		t_{PHL}	0.245
	CIN–SUM	t_{PHH}	0.107
		t_{PLL}	0.147
		t_{PLH}	0.160
		t_{PHL}	0.170

1. Minimum input transition and minimum output load. See .lib timing files for more information.

4.1.5 Cell Specifications

Table 4-3. Cell ADDF_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level				
	B	C	D	E	F
A	11.5	11.9	12.2	12.2	13.6
B	8.1	8.1	8.0	8.0	8.4
CIN	10.6	10.7	10.8	10.9	11.6
SUM	67.4	123.7	182.0	246.5	482.7
COUT	67.0	127.0	186.6	252.4	647.6

Table 4-4. Cell ADDF_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
B	13.44	6.72
C		
D		
E		
F	14.00	

4.2 BUFFER_{PL} Cell

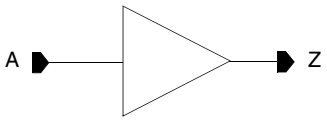
4.2.1 Function

Buffer

4.2.2 Description

This cell is a buffer combinational gate. The Boolean expression for this cell is $Z = A$.

Figure 4-2. Cell BUFFER_{PL} Symbols



4.2.3 Propagation Delay Table

Table 4-5. Cell BUFFER_{PL} Propagation Delays (Page 1 of 2)

Path (Input to Output)	Performance Level	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A–Z	C	t_{PHH}	0.087
		t_{PLL}	0.107
	D	t_{PHH}	0.081
		t_{PLL}	0.103
	E	t_{PHH}	0.084
		t_{PLL}	0.102
	F	t_{PHH}	0.087
		t_{PLL}	0.107
	H	t_{PHH}	0.075
		t_{PLL}	0.109
	I	t_{PHH}	0.081
		t_{PLL}	0.119
	J	t_{PHH}	0.085
		t_{PLL}	0.123
	K	t_{PHH}	0.092
		t_{PLL}	0.115
	L	t_{PHH}	0.075
		t_{PLL}	0.092

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 4-5. Cell BUFFER_{PL} Propagation Delays (Page 2 of 2)

Path (Input to Output)	Performance Level	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A–Z	M	t_{PHH}	0.079
		t_{PLL}	0.100
	N	t_{PHH}	0.106
		t_{PLL}	0.121
	O	t_{PHH}	0.104
		t_{PLL}	0.120

1. Minimum input transition and minimum output load. See .lib timing files for more information.

4.2.4 Cell Specifications

Table 4-6. Cell BUFFER_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level											
	C	D	E	F	H	I	J	K	L	M	N	O
A	3.1	3.6	3.9	4.3	5.6	6.1	7.3	8.6	17.1	17.9	14.8	17.4
Z	107.4	167.0	225.1	342.4	452.2	710.0	895.4	1149.0	1460.2	1835.6	2359.6	2822.0

Table 4-7. Cell BUFFER_{PL} Area

Performance Level	Cell Dimensions (µm)	
	Width	Length
C	2.80	6.72
D		
E		
F		
H		
I		
J	3.92	
K		
L		
M	6.16	
N	7.28	
O		

4.3 CLK_{PL} Cell

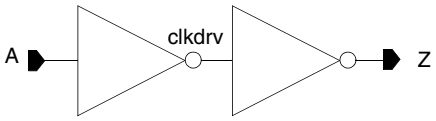
4.3.1 Function

Clock driver

4.3.2 Description

This cell is a clock driver combinational gate. The Boolean expression for this cell is $Z = A$.

Figure 4-3. Cell CLK_{PL} Symbols



4.3.3 Truth Table

Table 4-8. Cell CLK_{PL} Truth Table

Input	Output
A	Z
1	0
0	1

4.3.4 Propagation Delay Table

Table 4-9. Cell CLK_{PL} Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A1–Z	I	t_{PHH}	0.119
		t_{PLL}	0.107
	K	t_{PHH}	0.134
		t_{PLL}	0.120
	M	t_{PHH}	0.124
		t_{PLL}	0.114
	O	t_{PHH}	0.128
		t_{PLL}	0.116
	Q	t_{PHH}	0.128
		t_{PLL}	0.119

1. Minimum input transition and minimum output load. See .lib timing files for more information.

4.3.5 Cell Specifications

Table 4-10. Cell CLK_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level				
	I	K	M	O	Q
A	10.1	13.2	24.3	32.8	46.4
Z	1161.7	2119.3	3524.2	4912.3	6931.8

Table 4-11. Cell CLK_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
I	3.92	6.72
K	5.04	
M	8.96	
O	13.44	
Q	17.36	

4.4 CLKI_{PL} Cell

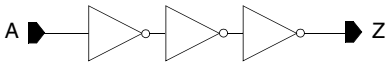
4.4.1 Function

Inverting clock driver

4.4.2 Description

This cell is an inverting clock driver combinational gate. The Boolean expression for this cell is $Z = \overline{A}$.

Figure 4-4. Cell CLKI_{PL} Symbols



4.4.3 Truth Table

Table 4-12. Cell CLKI_{PL} Truth Table

Input	Output
A	Z
1	0
0	1

4.4.4 Propagation Delay Table

Table 4-13. Cell CLKI_{PL} Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A1–Z	I	t_{PLH}	0.165
		t_{PHL}	0.178
	K	t_{PLH}	0.177
		t_{PHL}	0.186
	M	t_{PLH}	0.180
		t_{PHL}	0.184
	O	t_{PLH}	0.179
		t_{PHL}	0.180
	Q	t_{PLH}	0.202
		t_{PHL}	0.189

1. Minimum input transition and minimum output load. See .lib timing files for more information.

4.4.5 Cell Specifications

Table 4-14. Cell CLKI_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level				
	I	K	M	O	Q
A	5.7	6.4	8.3	12.2	14.0
Z	1089.0	1997.6	2995.2	4896.9	6935.2

Table 4-15. Cell CLKI_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
I	5.60	6.72
K	6.72	
M	10.08	
O	14.00	
Q	19.04	

4.5 COMP2_{PL} Cell

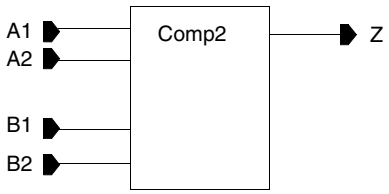
4.5.1 Function

Two-bit comparator

4.5.2 Description

This cell is a two-bit comparator combinational gate. The output of the two-bit comparator is ‘1’ when the A1/B1 and the A2/B2 pairs are the same. The A1/B1 pair does not need to have the same value as the A2/B2 pair.

Figure 4-5. Cell COMP2_{PL} Symbols



4.5.3 Truth Table

Table 4-16. Cell COMP2_{PL} Truth Table

Inputs				Output
A1	A2	B1	B2	Z
0	–	1	–	0
1	–	0	–	0
–	0	–	1	0
–	1	–	0	0
0	0	0	0	1
0	1	0	1	1
1	0	1	0	1
1	1	1	1	1

4.5.4 Propagation Delay Table

Table 4-17. Cell COMP2_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	A1–Z	t_{PLH}	0.197
		t_{PHL}	0.180
		t_{PHH}	0.142
		t_{PLL}	0.188
	A2–Z	t_{PLH}	0.214
		t_{PHL}	0.203
		t_{PHH}	0.157
		t_{PLL}	0.210
	B1–Z	t_{PLH}	0.195
		t_{PHL}	0.158
		t_{PHH}	0.106
		t_{PLL}	0.217
	B2–Z	t_{PLH}	0.212
		t_{PHL}	0.178
		t_{PHH}	0.122
		t_{PLL}	0.241
C	A1–Z	t_{PLH}	0.176
		t_{PHL}	0.171
		t_{PHH}	0.126
		t_{PLL}	0.179
	A2–Z	t_{PLH}	0.191
		t_{PHL}	0.191
		t_{PHH}	0.139
		t_{PLL}	0.199
	B1–Z	t_{PLH}	0.174
		t_{PHL}	0.150
		t_{PHH}	0.092
		t_{PLL}	0.208
	B2–Z	t_{PLH}	0.189
		t_{PHL}	0.168
		t_{PHH}	0.106
		t_{PLL}	0.228

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 4-17. Cell COMP2_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
D	A1–Z	t_{PLH}	0.167
		t_{PHL}	0.165
		t_{PHH}	0.119
		t_{PLL}	0.175
	A2–Z	t_{PLH}	0.180
		t_{PHL}	0.183
		t_{PHH}	0.131
		t_{PLL}	0.193
	B1–Z	t_{PLH}	0.164
		t_{PHL}	0.145
		t_{PHH}	0.086
		t_{PLL}	0.204
	B2–Z	t_{PLH}	0.178
		t_{PHL}	0.161
		t_{PHH}	0.099
		t_{PLL}	0.222
E	A1–Z	t_{PLH}	0.160
		t_{PHL}	0.159
		t_{PHH}	0.115
		t_{PLL}	0.169
	A2–Z	t_{PLH}	0.173
		t_{PHL}	0.174
		t_{PHH}	0.126
		t_{PLL}	0.185
	B1–Z	t_{PLH}	0.157
		t_{PHL}	0.139
		t_{PHH}	0.083
		t_{PLL}	0.197
	B2–Z	t_{PLH}	0.170
		t_{PHL}	0.154
		t_{PHH}	0.095
		t_{PLL}	0.213

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 4-17. Cell COMP2_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
F	A1–Z	t_{PLH}	0.171
		t_{PHL}	0.176
		t_{PHH}	0.128
		t_{PLL}	0.179
	A2–Z	t_{PLH}	0.183
		t_{PHL}	0.191
		t_{PHH}	0.138
		t_{PLL}	0.194
	B1–Z	t_{PLH}	0.168
		t_{PHL}	0.149
		t_{PHH}	0.096
		t_{PLL}	0.214
	B2–Z	t_{PLH}	0.180
		t_{PHL}	0.163
		t_{PHH}	0.108
		t_{PLL}	0.229

1. Minimum input transition and minimum output load. See .lib timing files for more information.

4.5.5 Cell Specifications

Table 4-18. Cell COMP2_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level				
	B	C	D	E	F
A1	3.3	4.0	4.9	5.8	5.8
A2	3.3	4.0	4.8	5.8	5.8
B1	4.6	5.5	6.5	7.7	7.8
B2	4.6	5.5	6.6	7.8	7.8
Z	64.0	122.3	187.4	247.5	360.2

Table 4-19. Cell COMP2_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
B	10.08	6.72
C		
D		
E		
F	11.20	

4.6 DELAY4_{PL} Cell

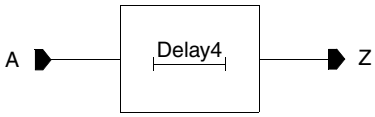
4.6.1 Function

Delay line

4.6.2 Description

This cell is a delay line combinational gate. The Boolean expression for this cell is $Z = A$.

Figure 4-6. Cell DELAY4_{PL} Symbols



4.6.3 Propagation Delay Table

Table 4-20. Cell DELAY4_{PL} Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A–Z	C	t_{PHH}	0.259
		t_{PLL}	0.239
	F	t_{PHH}	0.214
		t_{PLL}	0.198
	J	t_{PHH}	0.182
		t_{PLL}	0.178

1. Minimum input transition and minimum output load. See .lib timing files for more information.

4.6.4 Cell Specifications

Table 4-21. Cell DELAY4_{PL} Capacitance

	Capacitance (fF) by Performance Level		
Input / Output Pins	C	F	J
A	5.7	5.7	5.7
Z	617.4	593.0	567.2

Table 4-22. Cell DELAY4_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
C	5.60	6.72
F		
J		

4.7 DELAY6_{PL} Cell

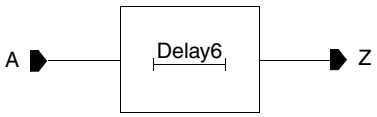
4.7.1 Function

Delay line

4.7.2 Description

This cell is a delay line combinational gate. The Boolean expression for this cell is $Z = A$.

Figure 4-7. Cell DELAY6_{PL} Symbols



4.7.3 Propagation Delay Table

Table 4-23. Cell DELAY6_{PL} Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
A–Z	A	t_{PHH}	1.633
		t_{PLL}	1.635
	B	t_{PHH}	1.028
		t_{PLL}	1.036
	C	t_{PHH}	0.509
		t_{PLL}	0.486
	F	t_{PHH}	0.419
		t_{PLL}	0.399
	J	t_{PHH}	0.347
		t_{PLL}	0.338
	M	t_{PHH}	0.252
		t_{PLL}	0.244

1. Minimum input transition and minimum output load. See .lib timing files for more information.

4.7.4 Cell Specifications

Table 4-24. Cell DELAY6_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level					
	A	B	C	F	J	M
A	4.0	5.5	5.7	5.7	5.7	5.7
Z	672.3	597.6	603.5	594.2	592.7	581.0

Table 4-25. Cell DELAY6_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
A	8.40	6.72
B		
C		
F		
J		
M		

4.8 MUX21_{PL} Cell

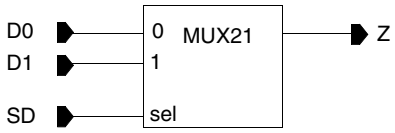
4.8.1 Function

2:1 Multiplexer

4.8.2 Description

This cell is a 2:1 multiplexer combinational gate. The cell selects data from D0 or D1 based on the value of the SD input pin.

Figure 4-8. Cell MUX21_{PL} Symbols



4.8.3 Truth Table

Table 4-26. Cell MUX21_{PL} Truth Table

Inputs			Output
D0	D1	SD	Z
0	–	0	0
1	–	0	1
–	0	1	0
–	1	1	1

4.8.4 Propagation Delay Table

Table 4-27. Cell MUX21_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	D0–Z	t_{PHH}	0.086
		t_{PLL}	0.132
	D1–Z	t_{PHH}	0.085
		t_{PLL}	0.134
	SD–Z	t_{PHH}	0.075
		t_{PLL}	0.120
		t_{PLH}	0.172
		t_{PHL}	0.165

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 4-27. Cell MUX21_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
D	D0–Z	t_{PHH}	0.085
		t_{PLL}	0.132
	D1–Z	t_{PHH}	0.085
		t_{PLL}	0.133
	SD–Z	t_{PHH}	0.075
		t_{PLL}	0.120
		t_{PLH}	0.171
		t_{PHL}	0.164
E	D0–Z	t_{PHH}	0.087
		t_{PLL}	0.132
	D1–Z	t_{PHH}	0.086
		t_{PLL}	0.133
	SD–Z	t_{PHH}	0.077
		t_{PLL}	0.122
		t_{PLH}	0.173
		t_{PHL}	0.165
F	D0–Z	t_{PHH}	0.095
		t_{PLL}	0.135
	D1–Z	t_{PHH}	0.094
		t_{PLL}	0.136
	SD–Z	t_{PHH}	0.086
		t_{PLL}	0.127
		t_{PLH}	0.182
		t_{PHL}	0.170
H	D0–Z	t_{PHH}	0.094
		t_{PLL}	0.134
	D1–Z	t_{PHH}	0.093
		t_{PLL}	0.135
	SD–Z	t_{PHH}	0.087
		t_{PLL}	0.126
		t_{PLH}	0.178
		t_{PHL}	0.179

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 4-27. Cell MUX21_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
I	D0–Z	t_{PHH}	0.103
		t_{PLL}	0.135
	D1–Z	t_{PHH}	0.102
		t_{PLL}	0.136
	SD–Z	t_{PHH}	0.095
		t_{PLL}	0.128
		t_{PLH}	0.172
		t_{PHL}	0.171

1. Minimum input transition and minimum output load. See .lib timing files for more information.

4.8.5 Cell Specifications

Table 4-28. Cell MUX21_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level					
	C	D	E	F	H	I
D0	6.0	6.0	6.2	6.5	7.7	8.8
D1	6.3	6.3	6.4	6.8	7.8	8.8
SD	8.1	8.1	8.2	8.5	9.6	11.1
Z	116.0	165.0	226.4	360.0	460.3	715.4

Table 4-29. Cell MUX21_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
C	5.04	6.72
D		
E		
F		
H		
I		

4.9 MUX21BAL_{PL} Cell

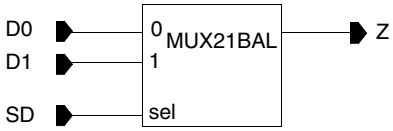
4.9.1 Function

Balanced 2:1 multiplexer

4.9.2 Description

This cell selects data from D0 or D1 based on the value of the SD input. The delay of D0 to Z equals the delay of D1 to Z. The rising data delay equals the falling data delay. The rising select delay equals the falling select delay.

Figure 4-9. Cell MUX21BAL_{PL} Symbols



4.9.3 Truth Table

Table 4-30. Cell MUX21BAL_{PL} Truth Table

Inputs			Output
D0	D1	SD	Z
0	–	0	0
1	–	0	1
–	0	1	0
–	1	1	1

4.9.4 Propagation Delay Table

Table 4-31. Cell MUX21BAL_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
H	D0–Z	t_{PHH}	0.130
		t_{PLL}	0.132
	D1–Z	t_{PHH}	0.130
		t_{PLL}	0.133
	SD–Z	t_{PHH}	0.188
		t_{PLL}	0.194
		t_{PLH}	0.200
		t_{PHL}	0.191
J	D0–Z	t_{PHH}	0.160
		t_{PLL}	0.161
	D1–Z	t_{PHH}	0.162
		t_{PLL}	0.163
	SD–Z	t_{PHH}	0.225
		t_{PLL}	0.221
		t_{PLH}	0.227
		t_{PHL}	0.222
L	D0–Z	t_{PHH}	0.188
		t_{PLL}	0.189
	D1–Z	t_{PHH}	0.192
		t_{PLL}	0.192
	SD–Z	t_{PHH}	0.255
		t_{PLL}	0.246
		t_{PLH}	0.255
		t_{PHL}	0.247

1. Minimum input transition and minimum output load. See .lib timing files for more information.

4.9.5 Cell Specifications

Table 4-32. Cell MUX21BAL_{PL} Capacitance (Page 1 of 2)

	Capacitance (fF) by Performance Level		
Input / Output Pins	H	J	L
D0	8.4	8.6	8.7

Table 4-32. Cell MUX21BAL_{PL} Capacitance (Page 2 of 2)

Input / Output Pins	Capacitance (fF) by Performance Level		
	H	J	L
D1	9.1	9.3	9.3
SD	18.5	18.3	18.3
Z	703.0	1390.6	2025.8

Table 4-33. Cell MUX21BAL_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
H	8.96	6.72
J	10.64	
L	12.32	

4.10 MUX21I_{PL} Cell

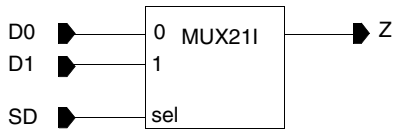
4.10.1 Function

2:1 Multiplexer with inverted output

4.10.2 Description

This cell is a 2:1 multiplexer with inverted output combinational gate. This cell selects data from D0 or D1 based on the value of the SD input pin.

Figure 4-10. Cell MUX21I_{PL} Symbols



4.10.3 Truth Table

Table 4-34. Cell MUX21I_{PL} Truth Table

Inputs			Output
D0	D1	SD	Z
0	–	0	0
1	–	0	1
–	0	1	0
–	1	1	1

4.10.4 Propagation Delay Table

Table 4-35. Cell MUX21I_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
B	D0–Z	t_{PLH}	0.091
		t_{PHL}	0.047
	D1–Z	t_{PLH}	0.093
		t_{PHL}	0.047
	SD–Z	t_{PLH}	0.078
		t_{PHL}	0.035
		t_{PHH}	0.103
		t_{PLL}	0.137

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 4-35. Cell MUX21I_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
C	D0–Z	t_{PLH}	0.081
		t_{PHL}	0.054
	D1–Z	t_{PLH}	0.082
		t_{PHL}	0.055
	SD–Z	t_{PLH}	0.068
		t_{PHL}	0.040
		t_{PHH}	0.087
		t_{PLL}	0.133
D	D0–Z	t_{PLH}	0.075
		t_{PHL}	0.054
	D1–Z	t_{PLH}	0.076
		t_{PHL}	0.055
	SD–Z	t_{PLH}	0.062
		t_{PHL}	0.040
		t_{PHH}	0.094
		t_{PLL}	0.127
E	D0–Z	t_{PLH}	0.078
		t_{PHL}	0.060
	D1–Z	t_{PLH}	0.082
		t_{PHL}	0.058
	SD–Z	t_{PLH}	0.065
		t_{PHL}	0.042
		t_{PHH}	0.123
		t_{PLL}	0.162
F	D0–Z	t_{PLH}	0.161
		t_{PHL}	0.135
	D1–Z	t_{PLH}	0.161
		t_{PHL}	0.134
	SD–Z	t_{PLH}	0.149
		t_{PHL}	0.123
		t_{PHH}	0.162
		t_{PLL}	0.208

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 4-35. Cell MUX21I_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
H	D0–Z	t_{PLH}	0.156
		t_{PHL}	0.138
	D1–Z	t_{PLH}	0.156
		t_{PHL}	0.138
	SD–Z	t_{PLH}	0.145
		t_{PHL}	0.128
		t_{PHH}	0.156
		t_{PLL}	0.210
I	D0–Z	t_{PLH}	0.157
		t_{PHL}	0.149
	D1–Z	t_{PLH}	0.157
		t_{PHL}	0.149
	SD–Z	t_{PLH}	0.146
		t_{PHL}	0.140
		t_{PHH}	0.157
		t_{PLL}	0.221

1. Minimum input transition and minimum output load. See .lib timing files for more information.

4.10.5 Cell Specifications

Table 4-36. Cell MUX21I_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level						
	B	C	D	E	F	H	I
D0	5.7	6.6	8.3	16.6	6.9	7.0	7.0
D1	6.0	6.9	8.7	16.0	7.0	7.0	7.0
SD	8.6	10.1	12.1	17.8	10.0	10.0	10.1
Z	81.9	107.2	148.4	287.2	343.8	450.9	712.3

Table 4-37. Cell MUX21I_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
B	3.92	6.72
C		
D		
E	8.40	
F	6.72	
H		
I		

4.11 MUX41_{PL} Cell

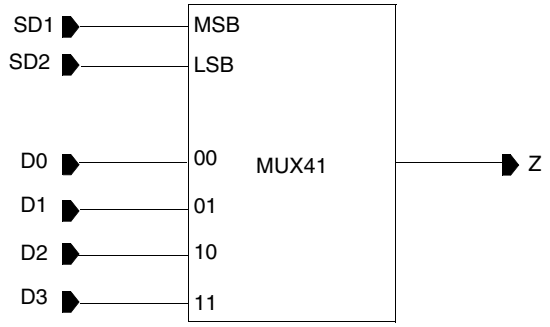
4.11.1 Function

4:1 Multiplexer

4.11.2 Description

This cell is a 4:1 multiplexer combinational gate. This cell selects data from D0, D1, D2, or D3 based on the values of the SD1 and SD2 input pins.

Figure 4-11. Cell MUX41_{PL} Symbols



4.11.3 Truth Table

Table 4-38. Cell MUX41_{PL} Truth Table

Inputs		Outputs
SD1	SD2	Z
0	0	
0	1	
1	0	
1	1	

4.11.4 Propagation Delay Table

Table 4-39. Cell MUX41_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
D	D0–Z	t_{PHH}	0.131
		t_{PLL}	0.160
	D1–Z	t_{PHH}	0.120
		t_{PLL}	0.158
	D2–Z	t_{PHH}	0.137
		t_{PLL}	0.168
	D3–Z	t_{PHH}	0.124
		t_{PLL}	0.165
	SD1–Z	t_{PHH}	0.107
		t_{PLL}	0.144
		t_{PLH}	0.156
		t_{PHL}	0.140
	SD2–Z	t_{PHH}	0.119
		t_{PLL}	0.194
		t_{PLH}	0.211
		t_{PHL}	0.170
F	D0–Z	t_{PHH}	0.139
		t_{PLL}	0.160
	D1–Z	t_{PHH}	0.139
		t_{PLL}	0.164
	D2–Z	t_{PHH}	0.142
		t_{PLL}	0.166
	D3–Z	t_{PHH}	0.141
		t_{PLL}	0.170
	SD1–Z	t_{PHH}	0.117
		t_{PLL}	0.150
		t_{PLH}	0.160
		t_{PHL}	0.142
	SD2–Z	t_{PHH}	0.138
		t_{PLL}	0.195
		t_{PLH}	0.218
		t_{PHL}	0.177

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 4-39. Cell MUX41_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
J	D0–Z	t_{PHH}	0.176
		t_{PLL}	0.204
	D1–Z	t_{PHH}	0.177
		t_{PLL}	0.207
	D2–Z	t_{PHH}	0.177
		t_{PLL}	0.207
	D3–Z	t_{PHH}	0.177
		t_{PLL}	0.210
	SD1–Z	t_{PHH}	0.122
		t_{PLL}	0.152
		t_{PLH}	0.169
		t_{PHL}	0.143
	SD2–Z	t_{PHH}	0.163
		t_{PLL}	0.204
		t_{PLH}	0.223
		t_{PHL}	0.175

1. Minimum input transition and minimum output load. See .lib timing files for more information.

4.11.5 Cell Specifications

Table 4-40. Cell MUX41_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level		
	D	F	J
D0	7.5	7.8	7.7
D1	7.8	8.0	8.1
D2	7.7	7.9	7.8
D3	7.9	8.1	8.1
SD1	5.9	6.8	13.3
SD2	10.1	11.2	20.3
Z	166.8	385.5	925.1

Table 4-41. Cell MUX41_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
D	12.32	6.72
F		
J	13.44	

4.12 TERM_{PL} Cell

4.12.1 Function

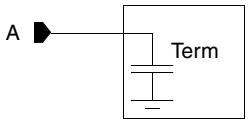
Net terminator

4.12.2 Description

This cell is a net terminator combinational gate. The net terminator is used to add capacitive load to a net. The additional load will modify the rise and fall time of the net.

Capacitive loads vary by performance level, as shown in *Table 4-42*.

Figure 4-12. Cell TERM_{PL} Symbols



4.12.3 Cell Specifications

Table 4-42. Cell TERM_{PL} Capacitance

Input Pin	Capacitance (fF) by Performance Level			
	A	B	C	D
A	5.90	9.10	14.10	18.29

Table 4-43. Cell TERM_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
A	1.68	6.72
B		
C		
D		

5. Standard Cell Sequential Logic

5.1 DFF_{PL} Cell

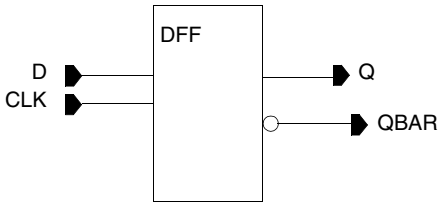
5.1.1 Function

DFF, Q, and QBAR outputs

5.1.2 Description

This cell is a positive edge-triggered D flip-flop with true and complement outputs.

Figure 5-1. Cell DFF_{PL} Symbols



5.1.3 DFF Truth Table

Table 5-1. Cell DFF_{PL} Truth Table

Inputs		Outputs	
CLK	D	Q	QBAR
(01)	0	0	1
(01)	1	1	0
(1x)	x	–	–
(x0)	x	–	–

5.1.4 Delay Tables

Table 5-2. Cell DFF_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	CLK–Q	t_{PHH}	0.226
		t_{PHL}	0.160
	CLK–QBAR	t_{PHH}	0.106
		t_{PHL}	0.164

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-2. Cell DFF_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
H	CLK–Q	t_{PHH}	0.261
		t_{PHL}	0.196
	CLK–QBAR	t_{PHH}	0.124
		t_{PHL}	0.168
K	CLK–Q	t_{PHH}	0.264
		t_{PHL}	0.188
	CLK–QBAR	t_{PHH}	0.274
		t_{PHL}	0.345

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-3. Cell DFF_{PL} Latch Setup and Hold Delays

Data / Clock	Condition[1]	Constraint (ps) by Performance Level		
		E	H	K
D 01 / CLK	Setup	31	35	26
	Hold	9	14	2
D 10 / CLK	Setup	182	183	179
	Hold	-149	-147	-151

1. Setup and hold are calculated using nominal case conditions (1.8 V, 25°C; clock and data slew rate = 200 ps).

5.1.5 Cell Specifications

Table 5-4. Cell DFF_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level		
	E	H	K
CLK	11.1	11.0	11.0
D	4.6	4.8	4.7
Q	236.9	463.9	1159.8
QBAR	248.0	517.3	1184.6

Table 5-5. Cell DFF_{PL} Area

Performance Level	Cell Dimensions (µm)	
	Width	Length
E	7.84	6.72
H	8.96	
K	12.32	

5.2 DFFR_{PL} Cell

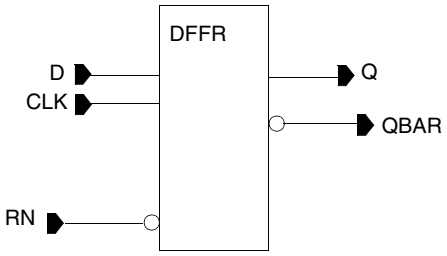
5.2.1 Function

DFF, Q, and QBAR outputs, -asynchronous reset

5.2.2 Description

This cell is a positive edge-triggered D flip-flop with asynchronous inputs and a reset function. If RN = 0, the Q output is forced to ‘0’ (reset) and the QBAR output is forced to ‘1’.

Figure 5-2. Cell DFFR_{PL} Symbols



5.2.3 DFF Truth Table

Table 5-6. Cell DFFR_{PL} Truth Table

Inputs			Outputs	
CLK	D	RN	Q	QBAR
x	x	0	0	1
(01)	1	1	1	0
(1x)	x	1	–	–
(x0)	x	1	–	–
(01)	0	x	0	1

5.2.4 Delay Tables

Table 5-7. Cell DFFR_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	RN–Q	t_{PLL}	0.238
	CLK–Q	t_{PHH}	0.289
		t_{PHL}	0.181
	RN–QBAR	t_{PLH}	0.184
	CLK–QBAR	t_{PHH}	0.120
		t_{PHL}	0.187
H	RN–Q	t_{PLL}	0.266
	CLK–Q	t_{PHH}	0.344
		t_{PHL}	0.220
	RN–QBAR	t_{PLH}	0.195
	CLK–QBAR	t_{PHH}	0.140
		t_{PHL}	0.198
K	RN–Q	t_{PLL}	0.283
	CLK–Q	t_{PHH}	0.332
		t_{PHL}	0.216
	RN–QBAR	t_{PLH}	0.373
	CLK–QBAR	t_{PHH}	0.306
		t_{PHL}	0.419

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-8. Cell DFFR_{PL} Latch Setup and Hold Delays

Data / Clock	Condition[1]	Constraint (ps) by Performance Level		
		E	H	K
D 01 / CLK	Setup	103	122	58
	Hold	4	9	-2
D 10 / CLK	Setup	184	185	183
	Hold	-148	-145	-151

1. Setup and hold are calculated using nominal case conditions (1.8 V, 25°C; clock and data slew rate = 200 ps).

5.2.5 Cell Specifications

Table 5-9. Cell DFFR_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level		
	E	H	K
CLK	12.3	12.2	12.2
D	4.8	4.7	4.7
Q	236.1	488.6	1265.3
QBAR	261.6	516.3	1181.7
RN	7.6	7.7	7.6

Table 5-10. Cell DFFR_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
E	9.52	6.72
H	10.64	
K	14.00	

5.3 DFFS_{PL} Cell

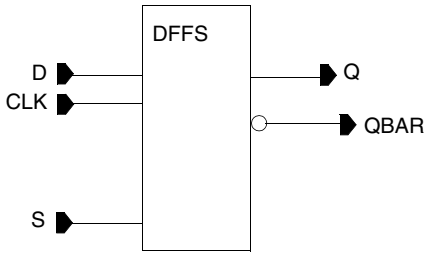
5.3.1 Function

DFF, Q, and QBAR outputs, asynchronous set

5.3.2 Description

This cell is a positive edge-triggered D flip-flop with asynchronous inputs and a set function. If S = 1, the Q output is forced to ‘1’ (set) and the QBAR output is forced to ‘0’.

Figure 5-3. Cell DFFS_{PL} Symbols



5.3.3 DFF Truth Table

Table 5-11. Cell DFFS_{PL} Truth Table

Inputs			Outputs	
CLK	D	S	Q	QBAR
(01)	0	0	0	1
(01)	1	x	1	0
(1x)	x	0	–	–
(x0)	x	0	–	–
x	x	1	0	1

5.3.4 Delay Tables

Table 5-12. Cell DFFS_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 5.0 V T_j 25°C
E	S–Q	t_{PHH}	0.229
	CLK–Q	t_{PHH}	0.277
		t_{PHL}	0.183
	S–QBAR	t_{PHL}	0.167
	CLK–QBAR	t_{PHH}	0.125
		t_{PHL}	0.196
H	S–Q	t_{PHH}	0.272
	CLK–Q	t_{PHH}	0.331
		t_{PHL}	0.226
	S–QBAR	t_{PHL}	0.176
	CLK–QBAR	t_{PHH}	0.147
		t_{PHL}	0.193
K	S–Q	t_{PHH}	0.276
	CLK–Q	t_{PHH}	0.319
		t_{PHL}	0.216
	S–QBAR	t_{PHL}	0.359
	CLK–QBAR	t_{PHH}	0.304
		t_{PHL}	0.404

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-13. Cell DFFS_{PL} Latch Setup and Hold Delays

Data / Clock	Condition[1]	Constraint (ps) by Performance Level		
		E	H	K
D 01 / CLK	Setup	55	89	45
	Hold	4	8	-2
D 10 / CLK	Setup	189	188	185
	Hold	-158	-15	-157

1. Setup and hold are calculated using nominal case conditions (1.8 V, 25°C; clock and data slew rate = 200 ps).

5.3.5 Cell Specifications

Table 5-14. Cell DFFS_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level		
	E	H	K
CLK	11.5	11.8	11.7
D	4.8	4.8	4.8
Q	235.9	489.5	1265.2
QBAR	244.9	545.1	1181.3
S	7.7	7.5	7.5

Table 5-15. Cell DFFS_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
E	10.08	6.72
H	11.20	
K	14.56	

5.4 DFFSR_{PL} Cell

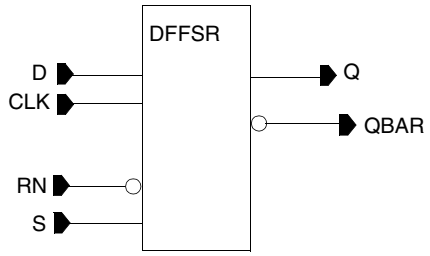
5.4.1 Function

DFF, Q, and QBAR outputs, asynchronous set, -asynchronous reset

5.4.2 Description

This cell is a positive edge-triggered D flip-flop with asynchronous inputs, and set and reset functions. S and RN are the set and reset inputs, respectively. If S = 1, the Q output is forced to ‘1’ (set). If RN = 0, the Q output is forced to ‘0’ (reset). The set function is dominant.

Figure 5-4. Cell DFFSR_{PL} Symbols



5.4.3 DFF Truth Table

Table 5-16. Cell DFFSR_{PL} Truth Table

Inputs				Outputs	
CLK	D	RN	S	Q	QBAR
x	x	0	0	0	1
(1x)	x	1	0	–	–
(x0)	x	1	0	–	–
(01)	0	x	0	0	1
x	x	x	1	1	0
(01)	1	1	x	1	0

5.4.4 Delay Tables

Table 5-17. Cell DFFSR_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	RN–Q	t_{PLL}	0.256
	S–Q	t_{PHH}	0.275
	CLK–Q	t_{PHH}	0.260
		t_{PHL}	0.163
	RN–QBAR	t_{PLH}	0.223
	S–QBAR	t_{PHL}	0.197
	CLK–QBAR	t_{PHH}	0.126
		t_{PHL}	0.173
H	RN–Q	t_{PLL}	0.303
	S–Q	t_{PHH}	0.312
	CLK–Q	t_{PHH}	0.298
		t_{PHL}	0.221
	RN–QBAR	t_{PLH}	0.222
	S–QBAR	t_{PHL}	0.218
	CLK–QBAR	t_{PHH}	0.136
		t_{PHL}	0.189
K	RN–Q	t_{PLL}	0.329
	S–Q	t_{PHH}	0.327
	CLK–Q	t_{PHH}	0.315
		t_{PHL}	0.229
	RN–QBAR	t_{PLH}	0.422
	S–QBAR	t_{PHL}	0.410
	CLK–QBAR	t_{PHH}	0.322
		t_{PHL}	0.400

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-18. Cell DFFSR_{PL} Latch Setup and Hold Delays

Data / Clock	Condition[1]	Constraint (ps) by Performance Level		
		E	H	K
D 01 / CLK	Setup	5	68	42
	Hold	6	14	2
D 10 / CLK	Setup	196	199	196
	Hold	-162	-153	-163

1. Setup and hold are calculated using nominal case conditions (1.8 V, 25°C; clock and data slew rate = 200 ps).

5.4.5 Cell Specifications

Table 5-19. Cell DFFSR_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level		
	E	H	K
CLK	11.6	11.6	11.6
D	5.2	5.2	5.2
Q	128.3	475.1	1275.6
QBAR	128.9	516.5	1169.1
RN	5.3	5.4	5.4
S	5.2	5.3	5.3

Table 5-20. Cell DFFSR_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
E	12.32	6.72
H	13.44	
K	16.79	

5.5 LATSR_{PL} Cell

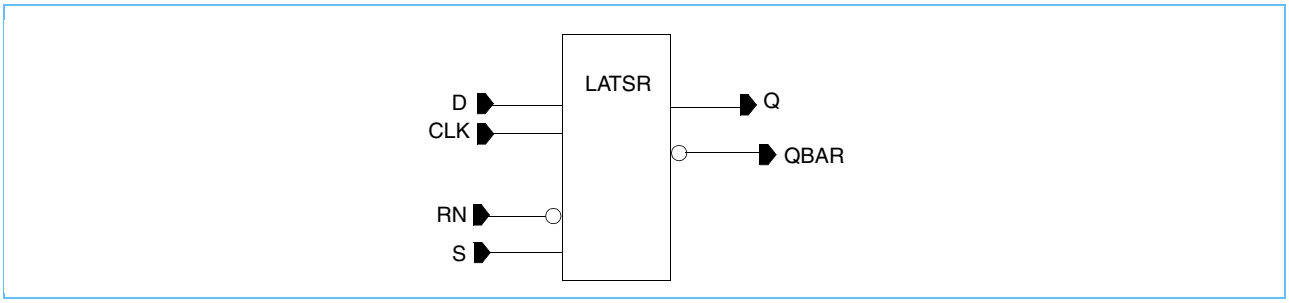
5.5.1 Function

Latch with Q and QBAR outputs, asynchronous set, and -asynchronous reset

5.5.2 Description

This is a polarity-hold latch with asynchronous set and reset functions. S and RN are the set and reset inputs respectively. If S = 1, the Q output is forced to a ‘1’ (set). If RN = 0, the Q output is forced to a ‘0’ (reset). The set function is dominant.

Figure 5-5. Cell LATSR_{PL} Symbols



5.5.3 DFF Truth Table

Table 5-21. Cell LATSR_{PL} Truth Table

Inputs				Outputs	
CLK	D	RN	S	Q	QBAR
x	x	0	0	0	1
0	x	1	0	–	–
1	0	x	0	0	1
x	x	x	1	1	0
1	1	1	x	1	0

5.5.4 Delay Tables

Table 5-22. Cell LATSR_{PL} Propagation Delays (Page 1 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	CLK–Q	t_{PHH}	0.145
		t_{PHL}	0.162
	D–Q	t_{PHH}	0.198
		t_{PLL}	0.212
	RN–Q	t_{PLL}	0.340
	S–Q	t_{PHH}	0.184
	CLK–QBAR	t_{PHH}	0.280
		t_{PHL}	0.225
	D–QBAR	t_{PLH}	0.332
		t_{PHL}	0.278
	RN–QBAR	t_{PLH}	0.491
	S–QBAR	t_{PHL}	0.260
H	CLK–Q	t_{PHH}	0.173
		t_{PHL}	0.175
	D–Q	t_{PHH}	0.224
		t_{PLL}	0.230
	RN–Q	t_{PLL}	0.385
	S–Q	t_{PHH}	0.204
	CLK–QBAR	t_{PHH}	0.362
		t_{PHL}	0.290
	D–QBAR	t_{PLH}	0.418
		t_{PHL}	0.342
	RN–QBAR	t_{PLH}	0.628
	S–QBAR	t_{PHL}	0.313
K	CLK–Q	t_{PHH}	0.291
		t_{PHL}	0.339
	D–Q	t_{PHH}	0.346
		t_{PLL}	0.389
	RN–Q	t_{PLL}	0.552
	S–Q	t_{PHH}	0.320
	CLK–QBAR	t_{PHH}	0.249
		t_{PHL}	0.223

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-22. Cell LATSR_{PL} Propagation Delays (Page 2 of 2)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
K	D–QBAR	t_{PLH}	0.300
		t_{PHL}	0.277
	RN–QBAR	t_{PLH}	0.453
	S–QBAR	t_{PHL}	0.252

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-23. Cell LATSR_{PL} Latch Setup and Hold Delays

Data / Clock	Condition[1]	Constraint (ps) by Performance Level		
		E	H	K
D 01 / CLK	Setup	239	274	245
	Hold	-227	-270	-238
D 10 / CLK	Setup	225	281	224
	Hold	-217	-278	-222

1. Setup and hold are calculated using nominal case conditions (1.8 V, 25°C; clock and data slew rate = 200 ps).

5.5.5 Cell Specifications

Table 5-24. Cell LATSR_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level		
	E	H	K
CLK	5.8	5.8	5.8
D	7.7	7.6	7.6
Q	262.0	565.0	922.2
QBAR	239.5	498.0	971.2
RN	5.6	5.6	5.6
S	10.4	10.3	10.4

Table 5-25. Cell LATSR_{PL} Area

Performance Level	Cell Dimensions (µm)	
	Width	Length
E	7.84	6.72
H	8.96	
K	12.88	

5.6 SDFF_{PL} Cell

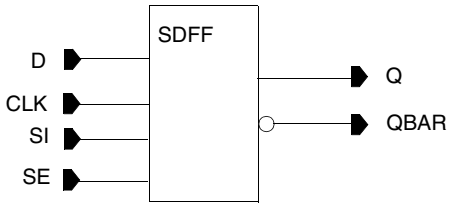
5.6.1 Function

Scannable DFF, Q, and QBAR outputs

5.6.2 Description

This cell is a positive edge-triggered scannable D flip-flop with true and complement outputs. When the scan enable pin is high, the latch is in scan mode. Setting the scan enable pin low enables the latch for normal operation.

Figure 5-6. Cell SDFF_{PL} Symbols



5.6.3 DFF Truth Table

Table 5-26. Cell SDFF_{PL} Truth Table

Inputs				Outputs	
CLK	D	SE	SI	Q	QBAR
(01)	0	x	0	0	1
(01)	x	1	0	0	1
(01)	1	x	1	1	0
(01)	x	1	1	1	0
(01)	0	0	x	0	1
(01)	1	0	x	1	0
(1x)	x	x	x	–	–
(x0)	x	x	x	–	–

5.6.4 Delay Tables

Table 5-27. Cell SDFF_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	CLK–Q	t_{PHH}	0.226
		t_{PHL}	0.160
	CLK–QBAR	t_{PHH}	0.106
		t_{PHL}	0.165
H	CLK–Q	t_{PHH}	0.261
		t_{PHL}	0.197
	CLK–QBAR	t_{PHH}	0.125
		t_{PHL}	0.169
K	CLK–Q	t_{PHH}	0.264
		t_{PHL}	0.188
	CLK–QBAR	t_{PHH}	0.274
		t_{PHL}	0.345

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-28. Cell SDFF_{PL} Latch Setup and Hold Delays

Data / Clock	Condition[1]	Constraint (ps) by Performance Level		
		E	H	K
D 01 / CLK	Setup	57	62	47
	Hold	-15	-9	-19
D 10 / CLK	Setup	208	210	201
	Hold	-178	-176	-177

1. Setup and hold are calculated using nominal case conditions (1.8 V, 25°C; clock and data slew rate = 200 ps).

5.6.5 Cell Specifications

Table 5-29. Cell SDFF_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level		
	E	H	K
CLK	11.1	11.0	10.9
D	11.0	11.2	10.8
Q	236.7	462.2	1157.9
QBAR	247.7	516.5	1182.3
SE	6.8	6.8	7.4
SI	9.6	9.7	9.0

Table 5-30. Cell SDFF_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
E	11.20	6.72
H	12.32	
K	15.68	

5.7 SDFFR_{PL} Cell

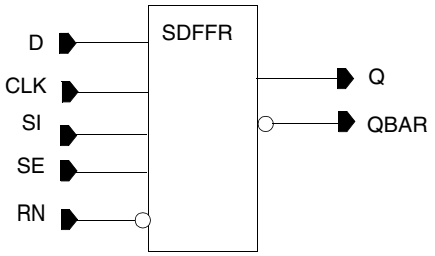
5.7.1 Function

Scannable DFF, Q, and QBAR outputs, -asynchronous reset

5.7.2 Description

This cell is a positive edge-triggered scannable D flip-flop with asynchronous inputs and a reset function. If RN = 0, the Q output is forced to ‘0’ (reset) and the QBAR output is forced to ‘1’.

Figure 5-7. Cell SDFFR_{PL} Symbols



5.7.3 DFF Truth Table

Table 5-31. Cell SDFFR_{PL} Truth Table

Inputs					Outputs	
CLK	D	RN	SE	SI	Q	QBAR
x	x	0	x	x	0	1
(01)	1	1	x	1	1	0
(01)	x	1	1	1	1	0
(01)	1	1	0	x	1	0
(1x)	x	1	x	x	–	–
(x0)	x	1	x	x	–	–
(01)	0	x	x	0	0	1
(01)	x	x	1	0	0	1
(01)	0	x	0	x	0	1

5.7.4 Delay Tables

Table 5-32. Cell SDFFR_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	RN–Q	t_{PLL}	0.238
	CLK–Q	t_{PHH}	0.289
		t_{PHL}	0.182
	RN–QBAR	t_{PLH}	0.184
	CLK–QBAR	t_{PHH}	0.121
		t_{PHL}	0.188
H	RN–Q	t_{PLL}	0.266
	CLK–Q	t_{PHH}	0.344
		t_{PHL}	0.221
	RN–QBAR	t_{PLH}	0.195
	CLK–QBAR	t_{PHH}	0.141
		t_{PHL}	0.198
K	RN–Q	t_{PLL}	0.284
	CLK–Q	t_{PHH}	0.333
		t_{PHL}	0.217
	RN–QBAR	t_{PLH}	0.373
	CLK–QBAR	t_{PHH}	0.306
		t_{PHL}	0.419

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-33. Cell SDFFR_{PL} Latch Setup and Hold Delays

Data / Clock	Condition[1]	Constraint (ps) by Performance Level		
		E	H	K
D 01 / CLK	Setup	122	15	81
	Hold	-17	-11	-25
D 10 / CLK	Setup	204	206	207
	Hold	-172	-168	-175

1. Setup and hold are calculated using nominal case conditions (1.8 V, 25°C; clock and data slew rate = 200 ps).

5.7.5 Cell Specifications

Table 5-34. Cell SDFFR_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level		
	E	H	K
CLK	12.2	12.2	12.2
D	10.8	10.8	10.8
Q	236.1	483.3	1271.0
QBAR	261.2	515.5	1179.0
RN	7.6	7.7	7.6
SE	7.5	7.5	7.5
SI	9.0	9.0	9.0

Table 5-35. Cell SDFFR_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
E	12.88	6.72
H	14.00	
K	17.36	

5.8 SDFFS_{PL} Cell

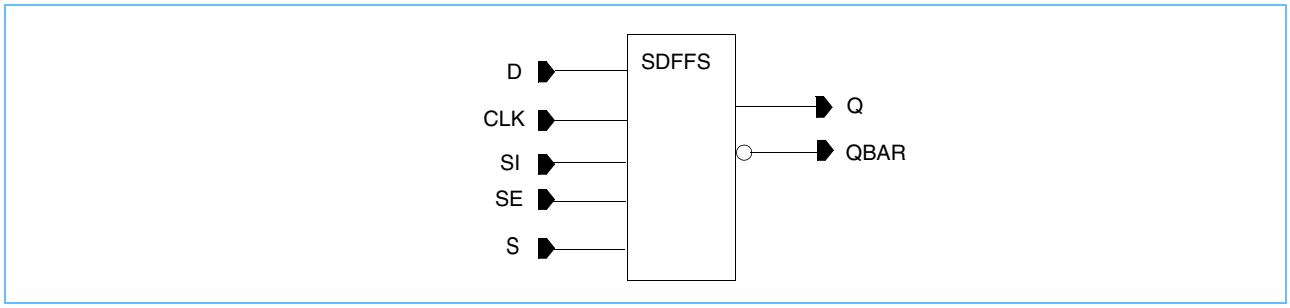
5.8.1 Function

Scannable DFF, Q, and QBAR outputs, asynchronous set

5.8.2 Description

This cell is a positive edge-triggered scannable D flip-flop with asynchronous inputs and a set function. If S = 1, the Q output is forced to '1' (set) and the QBAR output is forced to '0'.

Figure 5-8. Cell SDFFS_{PL} Symbols



5.8.3 DFF Truth Table

Table 5-36. Cell SDFFS_{PL} Truth Table

Inputs					Outputs	
CLK	D	S	SE	SI	Q	QBAR
(01)	0	0	x	0	0	1
(01)	x	0	1	0	0	1
(01)	0	0	0	x	0	1
(01)	1	x	x	1	1	0
(01)	x	x	1	1	1	0
(01)	1	x	0	x	1	0
(1x)	x	0	x	x	–	–
(x0)	x	0	x	x	–	–
x	x	1	x	x	1	0

5.8.4 Delay Tables

Table 5-37. Cell SDFFS_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	S–Q	t_{PHH}	0.229
	CLK–Q	t_{PHH}	0.278
		t_{PHL}	0.183
	S–QBAR	t_{PHL}	0.167
	CLK–QBAR	t_{PHH}	0.125
		t_{PHL}	0.197
H	S–Q	t_{PHH}	0.272
	CLK–Q	t_{PHH}	0.331
		t_{PHL}	0.226
	S–QBAR	t_{PHL}	0.177
	CLK–QBAR	t_{PHH}	0.147
		t_{PHL}	0.193
K	S–Q	t_{PHH}	0.276
	CLK–Q	t_{PHH}	0.319
		t_{PHL}	0.216
	S–QBAR	t_{PHL}	0.360
	CLK–QBAR	t_{PHH}	0.304
		t_{PHL}	0.404

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-38. Cell SDFFS_{PL} Latch Setup and Hold Delays

Data / Clock	Condition[1]	Constraint (ps) by Performance Level		
		E	H	K
D 01 / CLK	Setup	80	111	69
	Hold	-18	-14	-25
D 10 / CLK	Setup	212	210	206
	Hold	-185	-177	-183

1. Setup and hold are calculated using nominal case conditions (1.8 V, 25°C; clock and data slew rate = 200 ps).

5.8.5 Cell Specifications

Table 5-39. Cell SDFFS_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level		
	E	H	K
CLK	11.5	11.8	11.7
D	11.1	10.8	10.8
Q	235.8	489.0	1261.7
QBAR	244.9	545.1	1179.5
S	7.7	7.5	7.5
SE	6.9	7.5	7.5
SI	9.6	9.0	9.0

Table 5-40. Cell SDFFS_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
E	13.44	6.72
H	14.56	
K	17.92	

5.9 SDFFSR_{PL} Cell

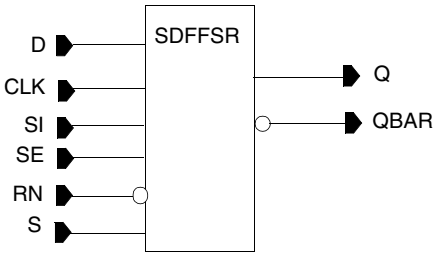
5.9.1 Function

Scannable DFF, Q, and QBAR outputs, asynchronous set, -asynchronous reset

5.9.2 Description

This cell is a positive edge-triggered scannable D flip-flop with asynchronous inputs, and set and reset functions. S and RN are the set and reset inputs, respectively. If S = 1, the Q output is forced to ‘1’ (set). If RN = 0, the Q output is forced to ‘0’ (reset). The set function is dominant.

Figure 5-9. Cell SDFFSR_{PL} Symbols



5.9.3 DFF Truth Table

Table 5-41. Cell SDFFSR_{PL} Truth Table

Inputs						Outputs	
CLK	D	RN	S	SE	SI	Q	QBAR
x	x	0	0	x	x	0	1
(1x)	x	1	0	x	x	–	–
(x0)	x	1	0	x	x	–	–
(01)	0	x	0	x	0	0	1
(01)	x	x	0	1	0	0	1
(01)	0	x	0	0	x	0	1
x	x	x	1	x	x	1	0
(01)	1	1	x	x	1	1	0
(01)	x	1	x	1	1	1	0
(01)	1	1	x	0	x	1	0

5.9.4 Delay Tables

Table 5-42. Cell SDFFSR_{PL} Propagation Delays

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	RN–Q	t_{PLL}	0.256
	S–Q	t_{PHH}	0.276
	CLK–Q	t_{PHH}	0.261
		t_{PHL}	0.163
	RN–QBAR	t_{PLH}	0.223
	S–QBAR	t_{PHL}	0.197
	CLK–QBAR	t_{PHH}	0.126
		t_{PHL}	0.174
H	RN–Q	t_{PLL}	0.303
	S–Q	t_{PHH}	0.312
	CLK–Q	t_{PHH}	0.297
		t_{PHL}	0.220
	RN–QBAR	t_{PLH}	0.223
	S–QBAR	t_{PHL}	0.218
	CLK–QBAR	t_{PHH}	0.136
		t_{PHL}	0.188
K	RN–Q	t_{PLL}	0.329
	S–Q	t_{PHH}	0.327
	CLK–Q	t_{PHH}	0.315
		t_{PHL}	0.229
	RN–QBAR	t_{PLH}	0.423
	S–QBAR	t_{PHL}	0.410
	CLK–QBAR	t_{PHH}	0.322
		t_{PHL}	0.399

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-43. Cell SDFFSR_{PL} Latch Setup and Hold Delays

Data / Clock	Condition[1]	Constraint (ps) by Performance Level		
		E	H	K
D 01 / CLK	Setup	73	91	65
	Hold	-15	-8	-18
D 10 / CLK	Setup	220	218	216
	Hold	-184	-18	-186

1. Setup and hold are calculated using nominal case conditions (1.8 V, 25°C; clock and data slew rate = 200 ps).

5.9.5 Cell Specifications

Table 5-44. Cell SDFFSR_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level		
	E	H	K
CLK	11.6	11.6	11.6
D	10.8	10.8	10.8
Q	128.2	474.6	1273.4
QBAR	128.8	515.8	1171.3
RN	5.4	5.4	5.4
S	5.2	5.3	5.3
SE	7.5	7.5	7.5
SI	9.0	9.0	9.0

Table 5-45. Cell SDFFSR_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
E	15.68	6.72
H	16.80	
K	20.16	

5.10 SLATSR_{PL} Cell

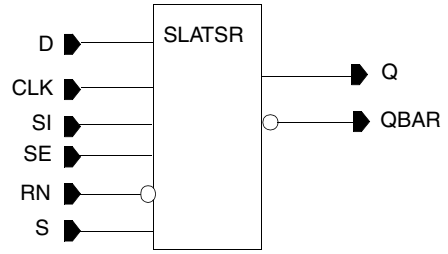
5.10.1 Function

Scannable latch with Q and QBAR outputs, asynchronous set, -asynchronous reset

5.10.2 Description

This cell is a scannable polarity-hold latch with asynchronous set and reset functions. S and RN are the set and reset inputs, respectively. The scan enable pin selects data or scan input. If S = 1, the Q output is forced to ‘1’ (set). If RN = 0, the Q output is forced to ‘0’ (reset). The set function is dominant.

Figure 5-10. Cell SLATSR_{PL} Symbols



5.10.3 DFF Truth Table

Table 5-46. Cell SLATSR_{PL} Truth Table

Inputs						Outputs	
CLK	D	RN	S	SE	SI	Q	QBAR
x	x	0	0	x	x	0	1
0	x	1	0	x	x	–	–
1	0	x	0	x	0	0	1
1	x	x	0	1	0	0	1
1	0	x	0	0	x	0	1
x	x	x	1	x	x	1	0
1	1	1	x	x	1	1	0
1	x	1	x	1	1	1	0
1	1	1	x	0	x	1	0

5.10.4 Delay Tables

Table 5-47. Cell SLATSR_{PL} Propagation Delays (Page 1 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
E	CLK–Q	t_{PHH}	0.145
		t_{PHL}	0.162
	D–Q	t_{PHH}	0.236
		t_{PLL}	0.244
	RN–Q	t_{PLL}	0.341
	S–Q	t_{PHH}	0.184
	SE–Q	t_{PHH}	0.390
		t_{PLL}	0.304
		t_{PLH}	0.262
		t_{PHL}	0.311
	SI–Q	t_{PHH}	0.332
		t_{PLL}	0.300
	CLK–QBAR	t_{PHH}	0.281
		t_{PHL}	0.225
	D–QBAR	t_{PLH}	0.364
		t_{PHL}	0.316
	RN–QBAR	t_{PLH}	0.493
	S–QBAR	t_{PHL}	0.260
	SE–QBAR	t_{PLH}	0.424
		t_{PHL}	0.471
		t_{PHH}	0.432
		t_{PLL}	0.342
	SI–QBAR	t_{PLH}	0.420
		t_{PHL}	0.412
H	CLK–Q	t_{PHH}	0.172
		t_{PHL}	0.175
	D–Q	t_{PHH}	0.261
		t_{PLL}	0.262

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-47. Cell SLATSR_{PL} Propagation Delays (Page 2 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
H	RN–Q	t_{PLL}	0.386
	S–Q	t_{PHH}	0.205
	SE–Q	t_{PHH}	0.418
		t_{PLL}	0.322
		t_{PLH}	0.288
		t_{PHL}	0.329
	SI–Q	t_{PHH}	0.360
		t_{PLL}	0.318
	CLK–QBAR	t_{PHH}	0.362
		t_{PHL}	0.290
	D–QBAR	t_{PLH}	0.450
		t_{PHL}	0.380
	RN–QBAR	t_{PLH}	0.631
	S–QBAR	t_{PHL}	0.314
	SE–QBAR	t_{PLH}	0.510
		t_{PHL}	0.536
		t_{PHH}	0.518
		t_{PLL}	0.407
	SI–QBAR	t_{PLH}	0.506
		t_{PHL}	0.478
K	CLK–Q	t_{PHH}	0.291
		t_{PHL}	0.339
	D–Q	t_{PHH}	0.384
		t_{PLL}	0.422
	RN–Q	t_{PLL}	0.553
	S–Q	t_{PHH}	0.321
	SE–Q	t_{PHH}	0.538
		t_{PLL}	0.481
		t_{PLH}	0.410
		t_{PHL}	0.488
	SI–Q	t_{PHH}	0.481
		t_{PLL}	0.477
	CLK–QBAR	t_{PHH}	0.249
		t_{PHL}	0.223

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-47. Cell SLATSR_{PL} Propagation Delays (Page 3 of 3)

Performance Level	Path (Input to Output)	Parameter	Nominal Process (ns)[1] V_{DD} 1.8 V T_j 25°C
K	D–QBAR	t_{PLH}	0.332
		t_{PHL}	0.315
	RN–QBAR	t_{PLH}	0.455
	S–QBAR	t_{PHL}	0.253
	SE–QBAR	t_{PLH}	0.391
		t_{PHL}	0.470
		t_{PHH}	0.399
		t_{PLL}	0.341
	SI–QBAR	t_{PLH}	0.387
		t_{PHL}	0.412

1. Minimum input transition and minimum output load. See .lib timing files for more information.

Table 5-48. Cell SLATSR_{PL} Latch Setup and Hold Delays

Data / Clock	Condition[1]	Constraint (ps) by Performance Level		
		E	H	K
D 01 / CLK	Setup	276	313	281
	Hold	-265	-310	-274
D 10 / CLK	Setup	259	316	258
	Hold	-253	-314	-257

1. Setup and hold are calculated using nominal case conditions (1.8 V, 25°C; clock and data slew rate = 200 ps).

5.10.5 Cell Specifications

Table 5-49. Cell SLATSR_{PL} Capacitance

Input / Output Pins	Capacitance (fF) by Performance Level		
	E	H	K
CLK	5.8	5.8	5.8
D	13.6	13.6	13.6
Q	261.7	564.1	917.1
QBAR	240.9	495.5	969.2
RN	5.7	5.6	5.6
S	10.5	10.3	10.4
SE	6.1	6.1	6.1
SI	11.2	11.2	11.1

Table 5-50. Cell SLATSR_{PL} Area

Performance Level	Cell Dimensions (μm)	
	Width	Length
E	11.20	6.72
H	12.32	
K	16.24	

6. Physical Design Cells

6.1 DECAP_{PL} Cell

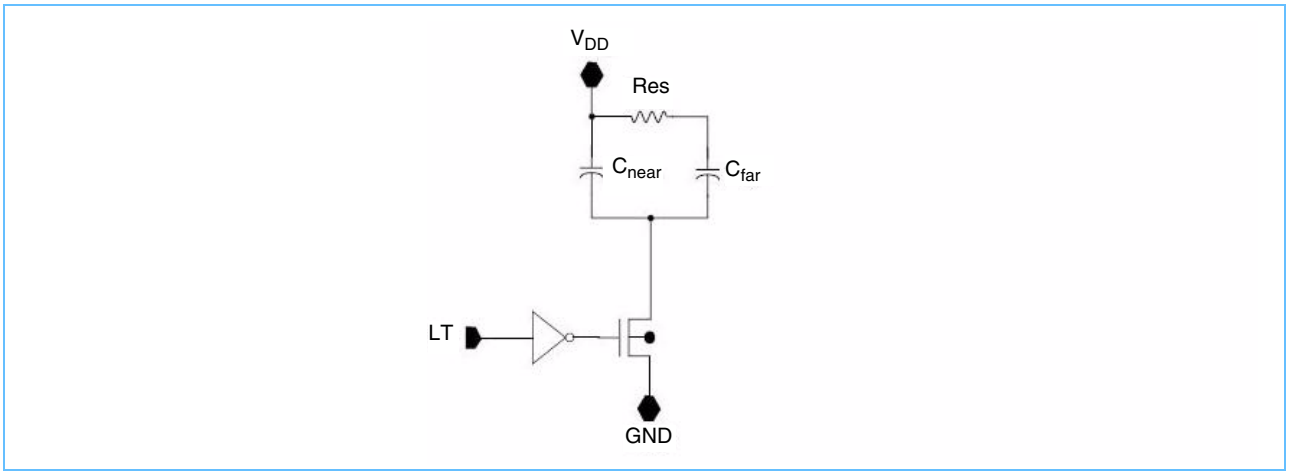
6.1.1 Function

V_{DD}-to-GND decoupling capacitor

6.1.2 Description

This cell is an NFET in n-well capacitor that can be placed on a chip to provide local noise decoupling from V_{DD} to GND. It should be uniformly distributed about the chip but placed near switching circuits. The LT pin is used at test to eliminate potential leakage current. The slew of the LT pin is noncritical. The DECAP cell is modeled as a pi network, where C_{near} is defined as the capacitance closest to the switching event. Be aware that these cells have high a polysilicon density that can cause checking concerns at the chip level. Blocks of DECAP cells should not exceed 3 mm^2 because they could affect the lithography of neighboring devices.

Figure 6-1. Cell DECAP_{PL} Symbols



6.1.3 Truth Table

Table 6-1. Cell DECAP_{PL} Truth Table

Input	
LT	Mode
0	Decoupling, normal mode
1	Leakage test, decoupling off

6.2 FILL{1,2} Cell

6.2.1 Function

One- and two-cell postfill cells

6.2.2 Description

One- and two-cell postfill cells are used during the physical design process. After design placement is completed, there are gaps left in unused areas of the layout. These gaps must be filled to provide n-well and power bus continuity. The available filler cells come in various sizes to fit different gaps. A typical physical design postfill strategy is to fill the largest gaps first with the largest filler cells, then repeat the process with subsequently smaller filler cells. By the time the process is repeated with the one-cell filler cell, all unused gaps in the layout are filled.

There are no active devices in FILL1 or FILL2. See *Section 6.4 GAUNUSEDxxx Cell* on page 232 for larger filler cells.

6.2.3 Cell Specifications

Table 6-2. Cell FILL{1,2} Area

Cell	Cell Dimensions (μm)	
	Width	Length
FILL1	0.56	6.72
FILL2	1.12	

6.3 FGTIE_{PL} Cell

6.3.1 Function

Floating gate tie-off

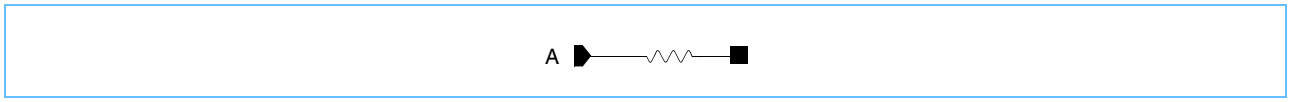
6.3.2 Description

This cell is used during physical design to correct antenna violations. Antenna violations can occur when large amounts of metal wiring are tied to polysilicon gates without being tied to diffusion for a specified length. During manufacturing, charge can build up on the metal and be discharged to the floating gate and damage the thin oxide under the gate.

Most physical design tools correct antenna violations in one of two ways. One way is to alter the wiring levels used in order to prevent large sections of M1 from being tied directly to a gate. The other way is to insert a diode near the gate to dissipate the charge into the substrate. This cell can be used to accomplish the latter. The input is essentially tied to a floating diffusion, which forms a diode with the substrate.

Physical design software typically inserts this cell automatically when necessary. However, these cells can also be manually placed in close proximity to cells with antenna violations.

Figure 6-2. Cell FGTIE_{PL} Symbols



6.3.3 Cell Specifications

Table 6-3. Cell FGTIE_{PL} Capacitance

	Capacitance (fF) by Performance Level
Input Pin	A
A	0

Table 6-4. Cell FGTIE_{PL} Area

	Cell Dimensions (μm)	
Performance Level	Width	Length
A	1.68	6.72

6.4 GAUNUSEDxxx Cell

6.4.1 Function

Gate array postfill cells

6.4.2 Description

Gate array post-fill cells are used during the postfill physical design process. After design placement is completed, there are gaps left in unused areas of the layout. These gaps must be filled to provide n-well and power bus continuity. Available filler cells come in various sizes to fit different gaps. A typical physical design post-fill strategy is to fill the largest gaps first with the largest filler cells, then repeat the process with subsequently smaller filler cells. By the time the process is repeated with the one-cell filler cell, all unused gaps in the layout are filled.

The GAUNUSED cells contain gate array background shapes, including spare transistors. A supported engineering change order physical design methodology replaces these spare cells with gate array cells, requiring only a back-end of the line mask change. See *Section 6.2 FILL{1,2} Cell* for smaller fill cells.

6.4.3 Cell Specifications

Table 6-5. Cell GAUNUSEDxxx Area

Cell	Cell Dimensions (μm)	
	Width	Length
GAUNUSED003	1.68	6.72
GAUNUSED006	3.36	
GAUNUSED012	6.72	
GAUNUSED024	13.44	
GAUNUSED048	26.88	
GAUNUSED096	53.76	