AN10439

Wafer level chip size package

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Document information

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Abstract	This application note provides guidelines for the use of Wafer Level Chip Scale Packages (WLCSP) using ball drop bumps with bump pitches of 500 μm and 400 μm.

Revision history

Rev	Date	Description
v.04	20140825	revision
v.03	20071017	internal release; adapted to NXP house style
v.02	20060713	internal release; minor changes
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1. Introduction

This application note provides the guidelines for the use of Wafer Level Chip Size Packages (WLCSP) using ball drop bumps with bump pitches of 500 μm and 400 μm.

2. Package description

Wafer level chip scale packages offer the smallest package size possible. The package size is equal to the die size. The solder-bumps provide the interconnection to the outside world. Three constructions can be distinguished: direct bumping, repassivation and redistribution (see Figure 1).

- Repassivation: the Input/Outputs (IO)s on the die are designed in such a way that they are already at the bump position. A repassivation layer is added to provide improved board level reliability behavior. It also decouples the Under Bump Metallization (UBM) and bump from the die passivation to avoid cracking of the die passivation during temperature cycling. A UBM is added to provide adhesion, act as a barrier layer and ensure solder wetting.
- Redistribution: the IOs on the die are relocated to the correct bump locations with a redistribution layer, consisting of either Cu or Al. Two repassivation layers are used. In general, a redistribution construction offers a better board level reliability behavior than a repassivation construction.
- Direct bumping: the UBM is deposited directly on the wafer passivation without a compliant layer in between. Because of the strong interaction between the front-end process, the bumping process and the bump design, this construction has limited use.

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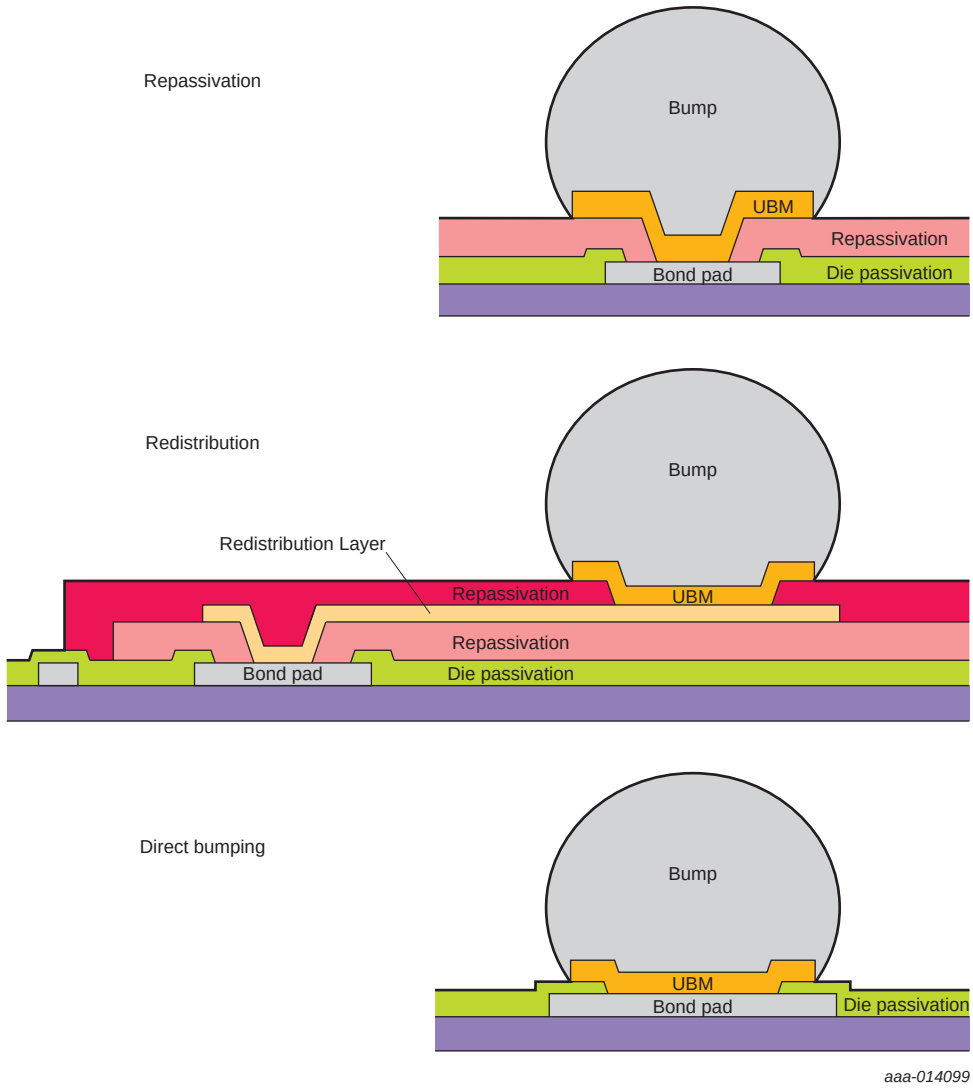

Fig 1. Bumping constructions

Ball drop does bump placement. For a 0.5 mm pitch, 300 μm preformed balls are used and for 0.4 mm pitch, 250 μm balls are used. Table 1 gives an overview of possible WLCSP dimensions. Optional Back Side Coating (BSC) is used which reduces back side chipping, increases laser marking visibility and provides some protection for backside mechanical impacts.

Table 1. WLCSP dimensions for preformed solder balls

Bump pitch	**500 μm**	**400 μm**
Solder bump diameter	320 μm ± 30 μm	260 μm ± 30 μm
Solder bump composition	SAC105Ni	SAC105Ni
Solder bump height	230 μm ± 30 μm	200 μm ± 30 μm
Si thickness	300 μm ± 25 μm	300 μm ± 25 μm
BSC thickness	40 μm ± 4 μm	40 μm ± 4 μm

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3. Board design and considerations

A proper Printed-Circuit Board (PCB) design ensures a good electrical reliability performance when using a WLCSP. This design concerns not only the footprint design but also the location of the WLCSP product on the board.

3.1 Footprint layout

Figure 2 shows the 2 types of commonly used solder pads: Solder Mask Defined (SMD) pads and copper (Cu) defined pads, also known as Non-Solder Mask Defined (NSMD) pads. There is high preference for NSMD compared to SMD due to the improved solder joint reliability.

The recommended PCB solder pad dimensions are listed in Table 2.

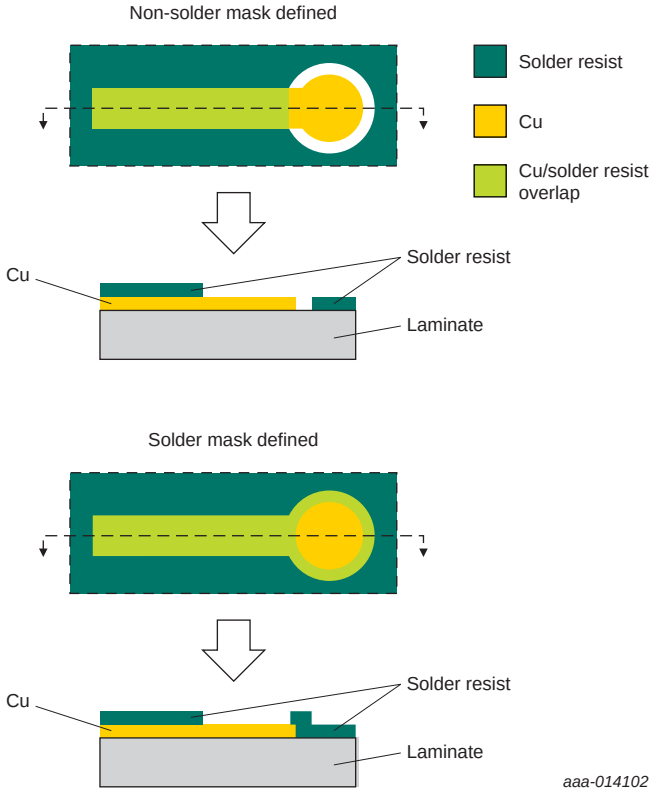

Fig 2. Recommended WLCSP solder pads

Table 2. PCB solder pad dimensions

Bump pitch	500 µm	400 µm
Cu pad shape	circular	circular
Cu solder pad	0.280 mm ± 0.025 mm	0.240 mm ± 0.020 mm
Solder resist	0.380 mm ± 0.025 mm	0.320 mm ± 0.020 mm

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It is recommended that the whole internal area of the pad is flat. The use of via's under the bumps should be avoided wherever possible as non-flat surfaces can create voids in the solder joint and affect the reliability. If via-in-pad structure (micro-via) is employed, filled micro vias are preferred. The maximum track width should not exceed $^2/_3$ of the pad diameter.

The connection of single pads directly to large areas of solid metal (e.g. ground planes), should be avoided because of potential unbalanced thermal profile.

3.2 PCB surface finish

On the board Cu-pad finishes such as Cu-OSP (Organic Surface Preservatives (OSP)) and Ni-Au (Electroplated Nickel, Immersion Gold (ENIG)) are used during internal qualification. These finishes ensure a good reliability of the WLCSP product.

3.3 Clearances/Location

For a typical advanced electronic equipment board, clearance around the maximum size of the component should be taken into account. This clearance is to accommodate for the pick and placement accuracy of the WLCSP component as well that of the surrounding components. When underfill is applied, room should be available for dispensing. Like all the other surface-mounted components, the placing of WLCSP products near mounting holes, connectors, clamps etc. is not recommended. It is not recommended due to the increased amount of bending stress on the bumps. There is also a chance of hitting the product during assembly or during use of the end product. Usually during PCB assembly multiple PCBs are part of a larger panel. The separation of this panel in single PCBs can result in mechanical stress to components that are mounted near the separation lanes. The amount of clearance from the separation lane depends on the separation process.

4. Assembly process

4.1 Stencil printing of solder paste

Table 3 gives an overview of the recommended stencil dimensions for WLCSPs with ball drop bumps at 500 μm and 400 μm pitch.

Table 3. Recommended stencil dimensions

Bump pitch	Stencil thickness	Stencil opening shape	Stencil opening
500 μm	100 μm	circular	300 μm
	150 μm	circular	340 μm
400 μm	100 μm	circular	275 μm

An electroformed or lasercut stencil can be used. For the 150 μm stencil, it is advised to use an electroformed stencil. For 0.5 mm pitch preformed bumps, two options are included. The version with the thicker stencil has improved solder fatigue durability for the larger components used on the same PCB. Before using the stencil, the dimensional accuracy should be checked.

Guideline for stencil opening dimensions:

- Top (print) side: design value +0/−20 μm

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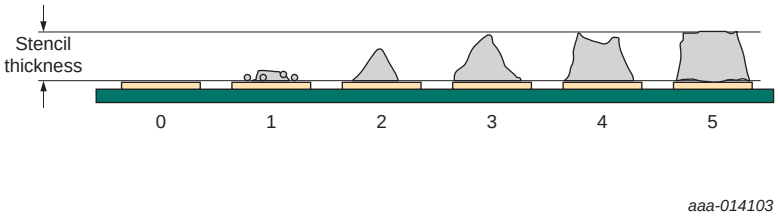
- PCB side: design value +/–12 μm

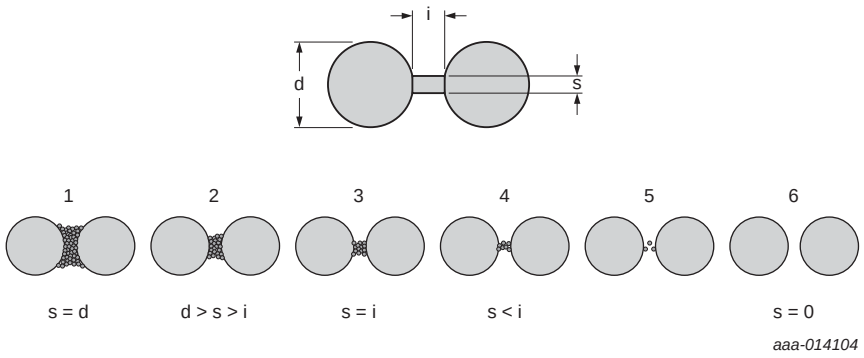
Use a lead-free (Pb-free) SnAgCu (SAC) solder paste. For SAC solder, the melting process difference between the bumps and the solder paste is similar. It results in an optimal solder joint with good mixing of the solder from the paste and the solder ball. Use solder particles type 3, type 4 or type 5, for best print definition. Storage and use conditions as specified by the solder paste supplier should be followed. A solder ball test can be used to verify the reflow properties of the solder paste (IPC-TM-650, Solder Ball Test, see Ref. 1). Before applying the paste on the stencil, it should be allowed to reach room temperature and be thoroughly mixed.

Adjust print speed and pressure so that the stencil is wiped clean of paste and the solder paste rolls nicely in front of the squeegee. If needed, the bottom side of the stencil can be cleaned regularly to avoid smearing. Criteria for print definition and smearing are given in Figure 3 and Figure 4. The print result depends on the rheology of the solder paste, the dimensions of the stencil opening, the print parameters, and the solder land definition on the PCB. A larger aperture gives a better definition but worse smearing.



(0) No solder paste
(1) Irregular shape (few balls)
(2) Pyramid, lower than stencil thickness
(3) Pyramid, height equal to stencil thickness
(4) Beginning flat-top with “dog ears”
(5) Flat-top side
3, 4 and 5 are acceptable rankings

Fig 3. Ranking for definition of solder paste deposits



5 and 6 are acceptable rankings

Fig 4. Ranking for smearing of solder-paste deposits

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4.2 Component placement

Component placement force should be such that it is high enough so that the component sticks to the solder paste during further processing. The solder-paste smearing, ball deformation and die-crack define the maximum limit. Use the minimum required placement force, typically in the order of 10 g/bump. Ideally, after placement, there should still be a layer of solder-particles beneath a bump. SMD solder-lands are more prone to solder-paste smearing after component placement, especially for a 150 μm thick stencil.

Maximum advised component displacement is 30 % of metal pad diameter. For a 150 μm thick stencil, it is less because of higher risk for smearing. As an alignment method, use local fiducials and a vision system that uses the bumps for alignment instead of the component outline.

4.3 Reflow

A general reflow profile consists of 4 steps, see Figure 5:

1. Heating zone, fast heating to reach a certain minimum temperature across the whole board
2. Equalization zone, to equalize the temperatures across the board up to a certain temperature range to avoid large temperature differences in the reflow zone. It depends on the component mix.
3. Reflow zone, zone in which the actual soldering is done
4. Cooling zone, ramp down zone

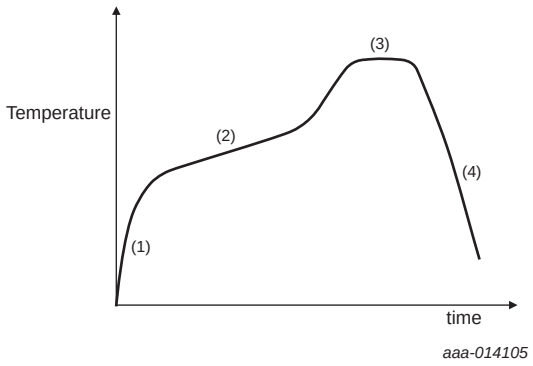

Fig 5. Zones in reflow profile

Follow the recommendations of the solder paste supplier on the optimum shape of the reflow curve, taking into account the mix of components on the board. At the same time, the profile should not be more stringent than the JEDEC profile requirements for MSL assessment, see Ref. 2. For good wetting, typical minimum temperature in the peak zone is 235 °C for SAC solder.

Proper board support during all steps of the reflow profile is essential to avoid board sagging resulting in stress on the soldered joints.

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4.4 Underfilling

Underfill improves the board level reliability behavior. However, it might influence electrical performance of the product. A careful assessment is advised. The type to be used depends on the application. Follow the advice from the underfill supplier. When selecting an underfill, consider the flowing behavior. The adhesion to the particular solder mask used on the PCB and the die surface, voiding behavior, and the potential impact on (biased) humidity reliability performance. Ultimately board level reliability results determine which the best underfill to use is. The underfill storage and use conditions as defined by the supplier should be followed.

For underfill curing, follow the recommendations of the underfill vendor.

The underfill should fill the complete gap between the WLCSP and the board. No underfill is allowed on the top of the die. An occasional void is allowed but it should not contact a bump.

5. Rework process

For rework, use a BGA rework system. Manual handling of WLCSPs should be reduced to the absolute minimum. In case it is necessary, a vacuum pick-up tool should be used. WLCSP removal, damages the solder bumps and therefore removed WLCSPs cannot be reused. Rework consists of the following steps: device removal, site preparation, application of solder paste to the site, device placement and device attachment. To find more information on board cleaning and site preparation, take notice of the ‘Repair’ section in the general application note AN10365. See Ref. 3.

6. Returning WLCSPs to NXP

Return the whole assembly to NXP in case WLCSPs are sent back for analysis purposes. Removing the WLCSPs from the PCB damages the solder balls and most probably also the part. In case the whole assembly cannot be sent to NXP, cut out a part around the device as large as possible by sawing. During sawing, the PCB-clamps should not be placed on top of the WLCSP. Too tight clamping should be avoided, because it can cause the PCB to warp and damage the device.

If the WLCSP must be removed from the PCB, follow the rework guidelines for device removal.

Packing for shipment of devices on PCBs is between two ElectroStatic Discharge (ESD) hard foam materials and tape along all edges. Demounted WLCSPs are best packed in gel pack. Both WLCSPs on PCB and demounted WLCSPs should be packed in ESD-bags and preferably in dry pack for shipping.

7. Reliability

NXP has done extensive testing of WLCSP packages to provide the optimum manufacturing conditions for assembly and to ensure the necessary quality and reliability over the life time of the product in consumer equipment.

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During the qualification, reliability tests are performed on wafer level, standalone device level and on board level to ensure the quality level. Product-related reliability data are included in the product qualification report.

The board level reliability tests are done to ensure the solder joint reliability. These tests are performed on daisy chain components (similar to related products) and electrical resistance is continuously monitored during the test. The board design and the assembly are in accordance with sections 3 and 4 (board design and assembly).

- A board level temperature cycling test is performed according to JEDEC condition G (−40 °C and 125 °C), soak mode 2 and a low ramp rate (lower than 20 °C/min for any portion of the cycle). See Ref. 4.
- Board level drop tests are performed using a 1.0 mm board and the following test conditions: Peak acceleration: 1500 g ± 10 %, Pulse duration: 1 ms ± 10 %.

The board-level reliability test-results are provided per product due to specific dependence on dimensions such as array size and pitch.

8. Moisture sensitivity level

The default Moisture Sensitivity Level (MSL) for WLCSPs is 1.

9. Storage conditions

The label on the packing specifies the shelf life and floor life conditions.

After expiration date or in case the humidity indicator shows > 10 %, solderability should be checked. See Ref. 6: JESD22-B102E, surface mount process simulation test. Baking is not allowed for WLCSPs.

10. References

[1] IPC-TM-650, Solder Ball Test

[2] JSTD020D, Moisture Reflow Sensitivity Classification for Nonhermetic Solid-State Surface Mount Devices

[3] AN10365, Surface Mount Reflow Soldering, Application Note

[4] JESD22-A104, Temperature Cycling

[5] JSTD033, Standard for Handling, Packing, Shipping and use of Moisture/Reflow Sensitive Surface Mount Devices

[6] JESD22-B102, Surface Mount Process Simulation Test

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