Document ID: SS-TEST-PLAN-001

Document Title: Test & Evaluation Master Plan (TEMP)

Version: 1.0

Status: Released

Date: 12 August 2025

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1. Introduction

1.1 Purpose

The purpose of this Test & Evaluation Master Plan (TEMP) is to provide the master framework for all test and evaluation (T&E) activities conducted at Synthetic Systems. This plan ensures that all products are rigorously verified against their design specifications and validated against their operational requirements. It establishes a consistent and repeatable methodology for planning, executing, and reporting on test activities, underpinning the company's commitment to quality and engineering excellence.

1.2 Scope

This TEMP applies to all T&E activities across the entire product lifecycle, as defined in the *SS-ENG-PLAN-001 Engineering Management Plan*. It governs the testing of all hardware, software, and integrated systems developed by Synthetic Systems, including the Hydra-C4 Comms Module, Trident-S Antenna Array, and Aegis-Link Control Software. All personnel involved in T&E activities, including engineers, technicians, and quality assurance staff, must adhere to the principles and processes outlined herein.

1.3 Policy Statement

Synthetic Systems is committed to a T&E strategy that provides objective, quantifiable evidence of product performance and quality. Our approach is to "test early and test often," integrating T&E as a continuous activity throughout the development lifecycle. All testing shall be conducted against approved, configuration-controlled documentation and shall be traceable to system requirements. We will maintain a robust defect management process to ensure issues are identified, tracked, and resolved in a timely manner, delivering reliable and fit-for-purpose systems to our

customers.

2. References

This TEMP is a subordinate document to the following corporate plans and policies:

- **SS-ENG-PLAN-001:** Engineering Management Plan
- **SS-QM-PLAN-001:** Quality Management Plan

The processes defined herein are aligned with and support the following related documents:

- **SS-CM-PLAN-001:** Configuration Management Plan
- **SS-RM-PROC-001:** Risk Management Process

3. T&E Governance and Roles

- **Test & Evaluation Lead:** The owner of this TEMP. The T&E Lead is responsible for the overall T&E strategy, resource planning, and ensuring that T&E activities are conducted in accordance with this plan.
- **Test Engineer:** Responsible for developing detailed, product-specific test plans and procedures, executing tests, and producing formal test reports.
- **Chief Engineer:** The final technical authority for T&E activities, responsible for approving the overall T&E strategy for a project and providing guidance on complex technical issues.
- **Quality Department:** Responsible for providing independent oversight of T&E activities. As per the *SS-QM-PLAN-001*, the Quality department is responsible for the final approval of all formal test procedures to ensure compliance with quality standards and traceability to requirements.

4. T&E in the Engineering Lifecycle

T&E is an integral part of the engineering lifecycle defined in *SS-ENG-PLAN-001*. The formal T&E phase is preceded by the Test Readiness Review (TRR), which ensures the system, test environment, and documentation are ready for formal verification and validation. This TEMP provides the overarching framework, which is then detailed in product-specific (L3) test documentation.

5. Levels of Testing

Our T&E strategy employs a progressive, multi-level approach to build confidence in the system from the component level up to the final integrated product.

5.1 Component Level Testing

This is the lowest level of testing, focused on individual hardware components or

software units.

- **Software Unit Testing:** Testing of individual software functions or methods, typically performed by the developer.
- **Hardware Component Testing:** Electrical and functional testing of individual printed circuit boards (PCBs) or other hardware components before they are integrated.

5.2 Integration Level Testing

This level focuses on verifying the interaction and interoperability between integrated components.

- **Software Integration Testing:** Testing the interfaces and interactions between different software modules.
- **Hardware/Software Integration Testing:** Verifying the interaction between software running on the target hardware.
- **System Integration Testing (SIT):** A formal testing stage where the complete system (e.g., Hydra-C4, Trident-S, and Aegis-Link) is integrated and tested as a whole for the first time. The primary purpose of SIT is to identify and resolve issues at the interfaces between major subsystems. SIT is typically conducted in the engineering lab environment.

5.3 System Level Testing

This level of testing validates the functionality and performance of the fully integrated system against its requirements.

- **Factory Acceptance Testing (FAT):** A formal and comprehensive test campaign conducted at Synthetic Systems' facilities. The purpose of FAT is to provide a final verification of the system against the complete set of system requirements before it is shipped to a customer. FAT is typically witnessed by the customer and is a major contractual milestone.
- **Hardware Acceptance Test Procedures:** This term refers to the specific L3 documents (e.g., *SS-HYD-TEST-001*) that contain the detailed, step-by-step instructions for conducting the FAT on a specific hardware product. These procedures form the basis of the formal acceptance process.

5.4 Specialised Testing

Depending on project requirements, specialised testing may be required.

- **Environmental Stress Screening (ESS):** As detailed in *SS-TRI-TEST-001*, this involves subjecting hardware to thermal cycling and vibration to precipitate latent defects.

- **Security Testing:** Assessing the system's resilience against cyber threats, aligned with *SS-SEC-POL-001*.
- **Independent Verification & Validation (IV&V):** As detailed in *SS-AEG-TEST-001*, this involves using a third party to provide an independent assessment of the software's correctness.

6. Test Documentation

A formal hierarchy of documentation shall be used for all T&E activities.

- **Test & Evaluation Master Plan (TEMP):** This document (SS-TEST-PLAN-001).
- **Product Test Plan:** A product-specific (L3) document that details the scope, approach, resources, and schedule of all testing activities for a particular product (e.g., *SS-xxx-TEST-001*).
- **Test Case Specification (TCS):** A document that specifies the detailed test cases for a feature or requirement. Each test case must trace to a specific system requirement.
- **Test Procedure:** A document providing step-by-step instructions for executing a set of test cases. **All formal test procedures must be approved by the responsible Test Engineer and the Quality department prior to execution.**
- **Test Report:** A document that summarises the results of a test execution, providing a record of the outcome of each test case and detailing any defects found.

7. Defect Management

The systematic management of defects is critical to product quality. All defects, anomalies, and unexpected test results shall be formally documented and tracked.

7.1 Defect Management Lifecycle

1. **Identification:** A potential defect is observed during testing.
2. **Logging:** A formal Defect Report (DR) is created in the central Defect Tracking System. The DR must include a clear title, a detailed description of the issue, steps to reproduce it, the expected vs. actual results, and any relevant logs or screenshots.
3. **Triage:** The DR is reviewed by a board (typically including the PEM, Chief Engineer, and T&E Lead) to confirm its validity, assign a priority and severity, and assign it to the appropriate engineering team for investigation.
4. **Resolution:** The assigned engineer investigates the defect and implements a fix. The resolution is documented in the DR.
5. **Verification:** The Test Engineer re-runs the relevant test case(s) on a new build containing the fix to verify that the defect has been resolved and has not

introduced any regressions.
6. **Closure:** Once the fix is verified, the DR is formally closed.

7.2 Relationship to other Processes

- **Non-Conformance Reports (NCR):** For defects that escape to a later lifecycle phase or are found in delivered products, a formal NCR must be raised in accordance with the *SS-QM-PLAN-001*. The NCR process will be used to manage the disposition of the non-conforming item.
- **Engineering Change Proposals (ECP):** If the resolution for a defect requires a change to a formal baseline (e.g., a hardware design), an ECP must be submitted to the Configuration Control Board (CCB) as per the *SS-CM-PLAN-001*.

8. Document Control

This TEMP is a controlled document. The official version is maintained by the Engineering Directorate. Any printed copies are considered uncontrolled. The Test & Evaluation Lead is responsible for the biennial review and maintenance of this plan.