1. Why can’t you use both pins PA0 and PC0 for external interrupts at the same time?
They are both connected to the same MUX connecting to the EXTI0 Register.

2. What software priority level gives the highest priority? What level gives the lowest?
Level 0 gives the highest priority.
Level 3 is the lowest priority.

3. How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt (including non-implemented bits)? Which bits in the group are implemented?
Including non-implemented bits, it has 8-bits reserved for each interrupt region. The uppermost two bits in each region are implemented in our board.

4. What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer? Make sure to include a screenshot in the post-lab submission.
93.82 Microseconds

5. Why do you need to clear status flag bits in peripherals when servicing their interrupts?

The interrupt will not know that it has finished running unless you signal to it that it is finished, so we need to set the clear status flag in the interrupt handler to let the peripherals interrupts know that they have been serviced.