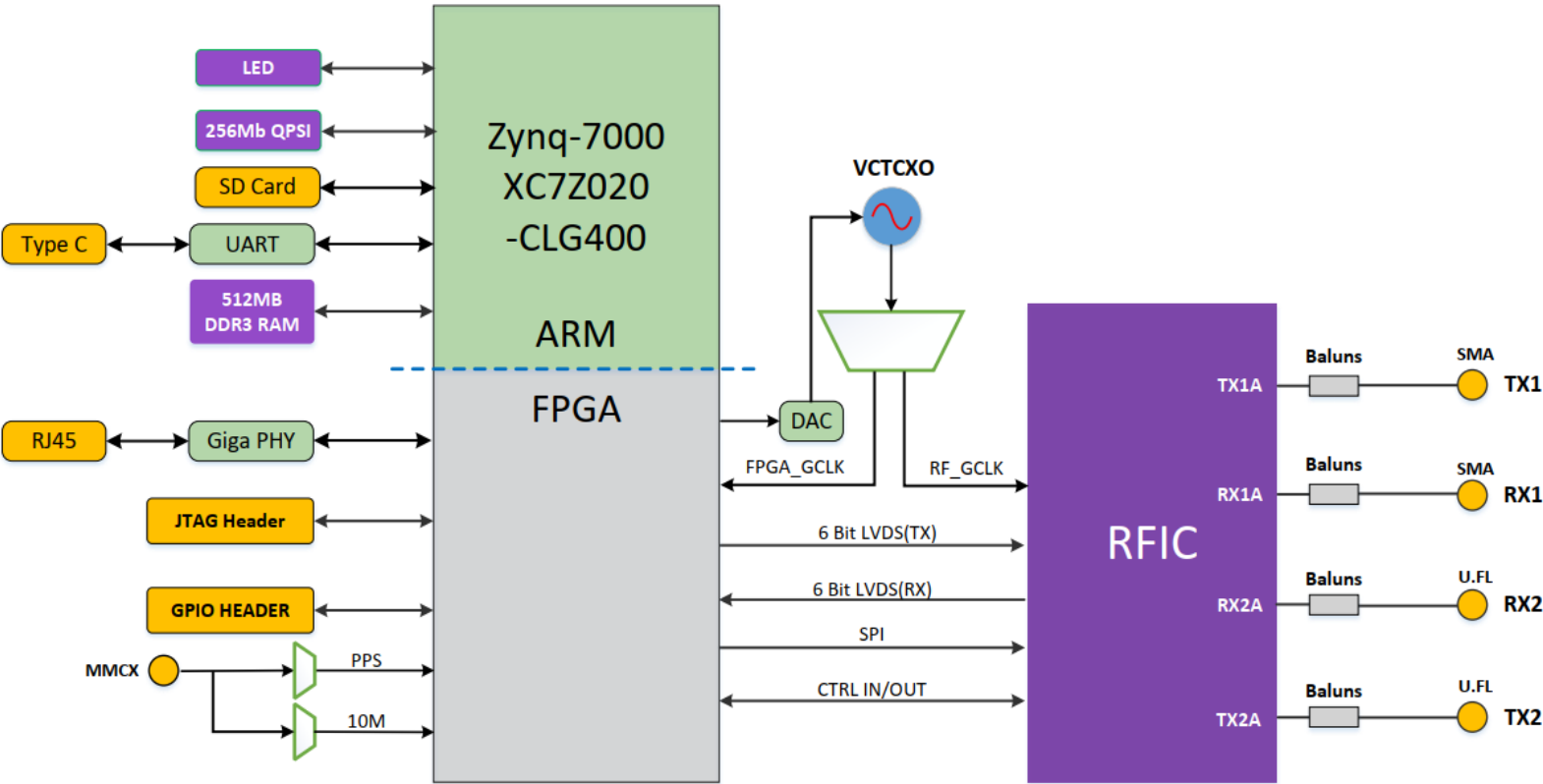


Note:  
MicroPhase board HW FULL schematics are not available. MicroPhase has an open source code but not an open hardware schematics. Nonetheless, DEVELOPMENT schematics are available here .  
This schematic will give you information about HW configuration, FPGA pin connection

| REV | DATE      | PAGES | DESCRIPTION     |
|-----|-----------|-------|-----------------|
| 1.0 | 15/7/2022 | All   | Rev 1.0 Release |
|     |           |       |                 |
|     |           |       |                 |
|     |           |       |                 |
|     |           |       |                 |
|     |           |       |                 |
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|     |           |       |                 |
|     |           |       |                 |

# ANTSDR E200 Block Diagram



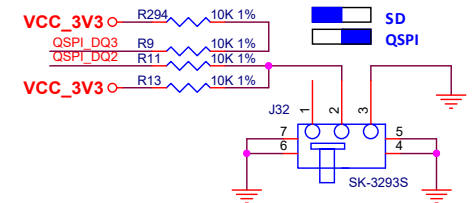
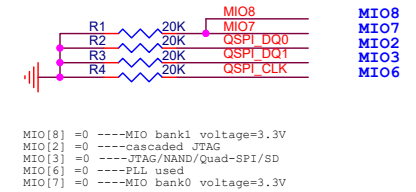
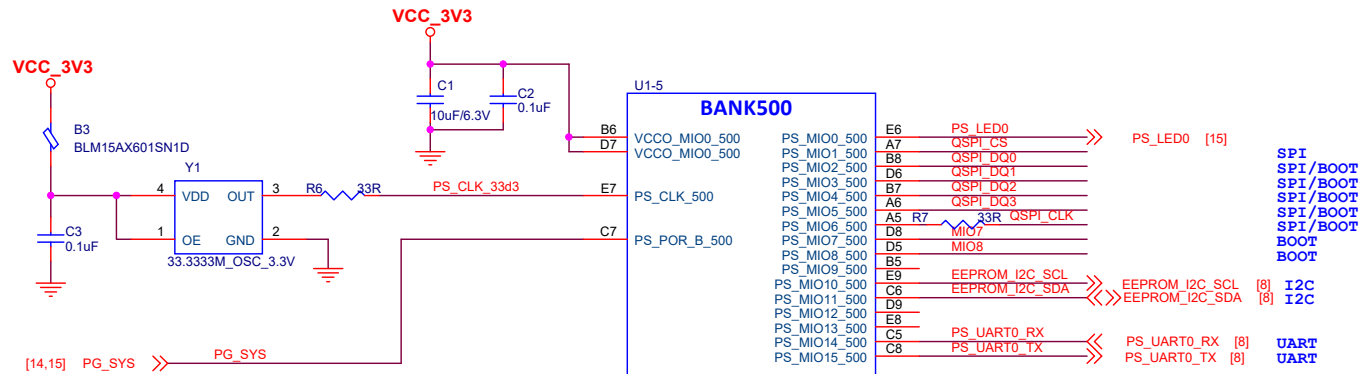
| PAGE | DESCRIPTION                                   |
|------|---|
| 1    | Title, Notes, Block Diagram, Revision History |
| 2    | PS BANK500&501                                |
| 3    | PS BANK502                                    |
| 4    | PL BANK0&13                                   |
| 5    | PL BANK34&35                                  |
| 6    | ZYNQ Power                                    |
| 7    | DDR3 RAM                                      |
| 8    | URAT EEPROM JTAG                              |
| 9    | PL ETH  |
| 10   | SD  |
| 11   | AD9363  |
| 12   | RF TX1/RX1                                    |
| 13   | CLOCK GPIO                                    |
| 14   | Power   |
| 15   | Power   |
| 16   |   |
| 17   |   |
| 18   |   |
| 19   |   |
| 20   |   |
| 21   |   |
| 22   |   |
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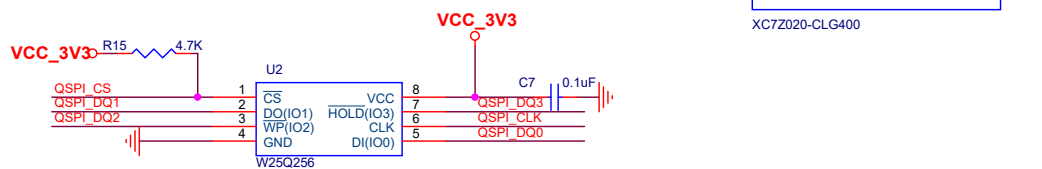
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|  |               |
|--|---------------|
| MicroPhase MicroPhase Inc. www.microphase.cn |               |
| Title ANT E200                               |               |
| Size B                                       | Rev 1.0       |
| Block Diagram                                |               |
| Date: Monday, October 17, 2022               | Sheet 1 of 15 |

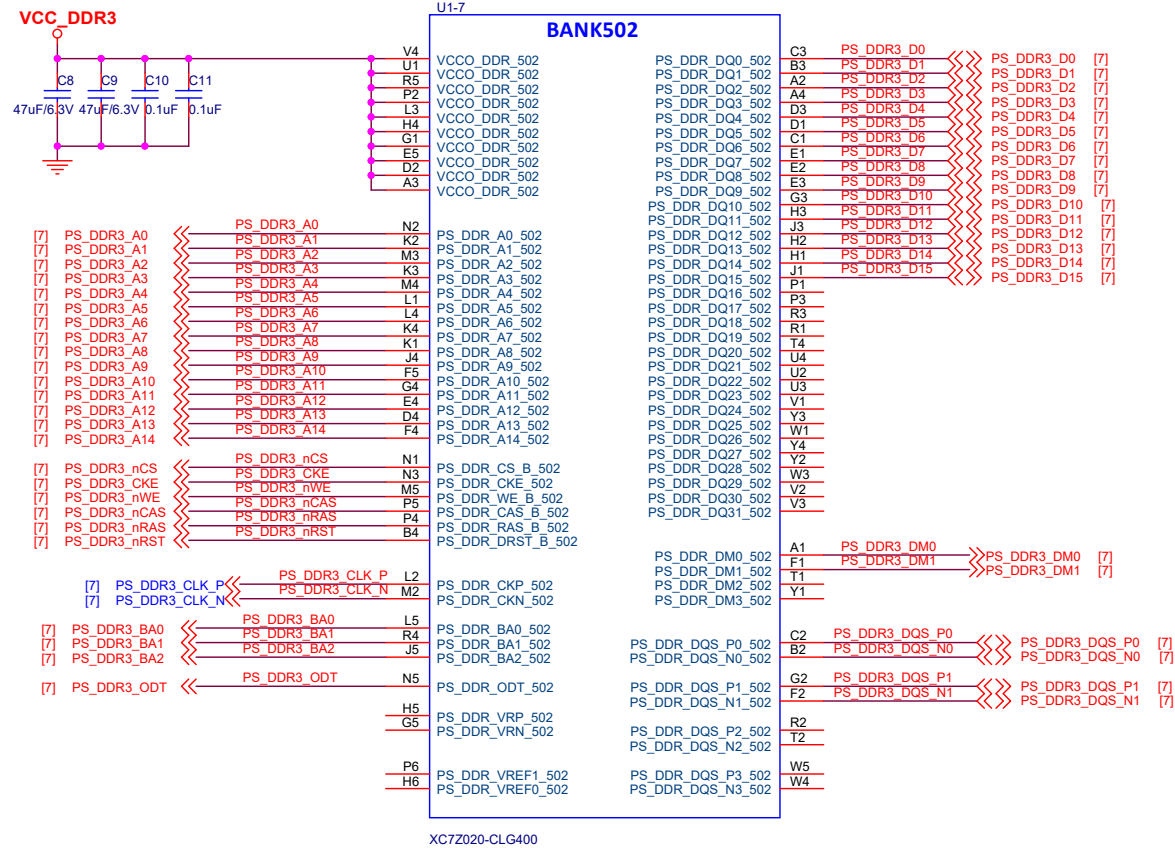
# PS B500 B501



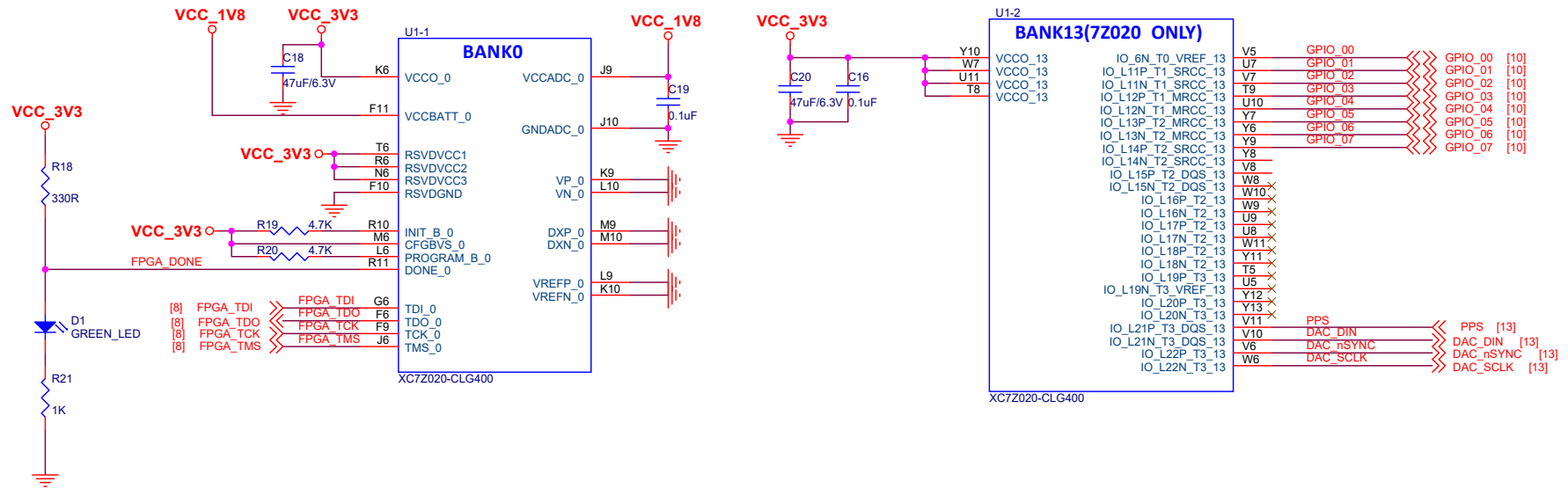
| Boot Mode | MIO[5]<br>(QSPI_DQ3) | MIO[4]<br>(QSPI_DQ2) |
|-----------|----------------------|----------------------|
| JTAG      | 0                    | 0                    |
| NAND      | 0                    | 1                    |
| QSPI      | 1                    | 0                    |
| SD Card   | 1                    | 1                    |



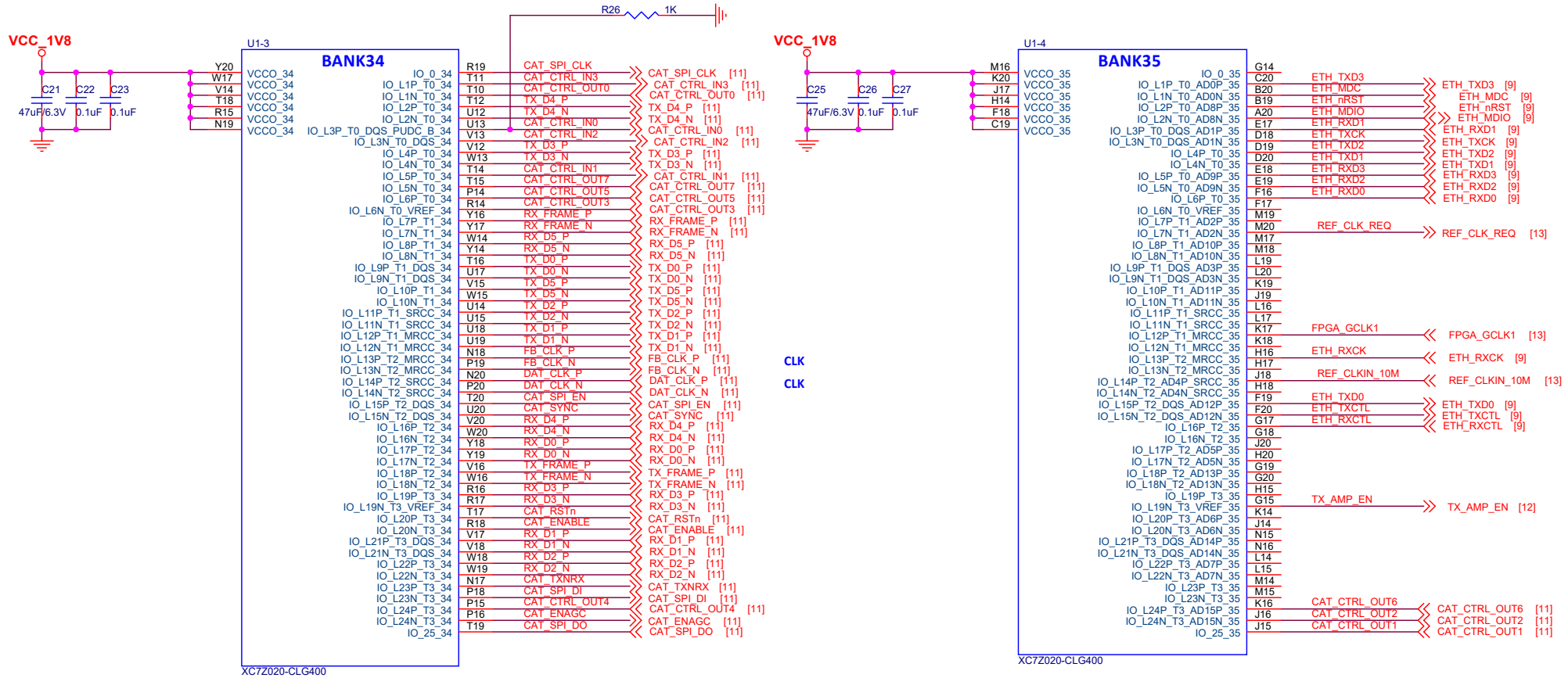
# PS B502



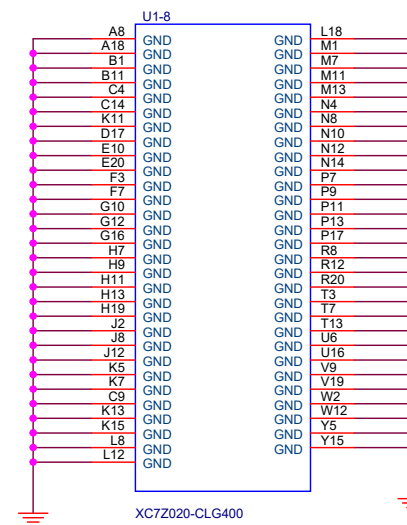
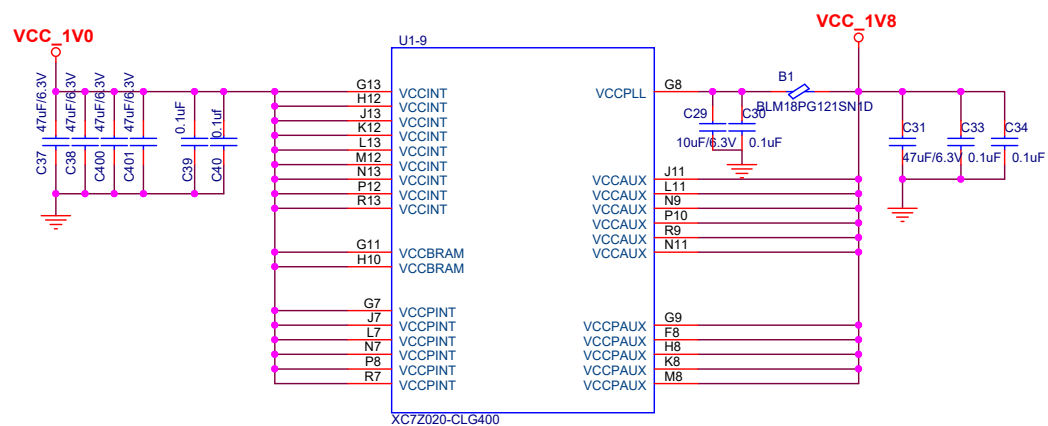
# PL B0 B13



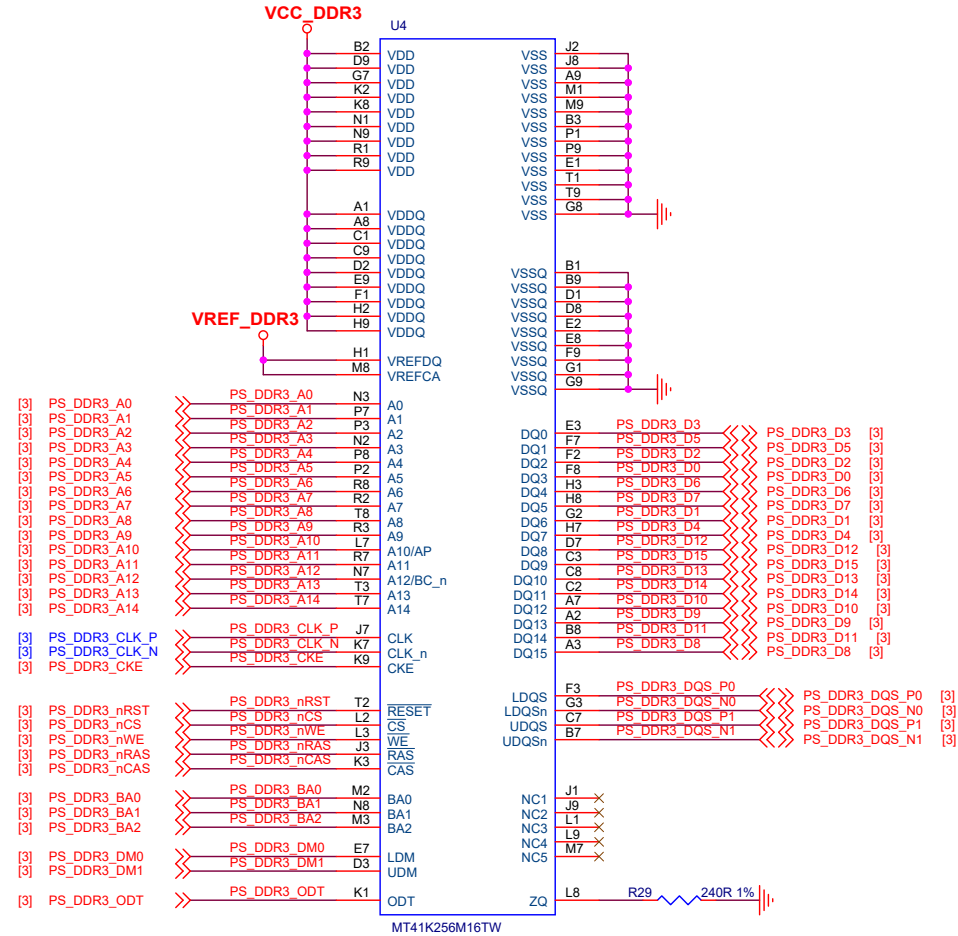
# PL B34 35



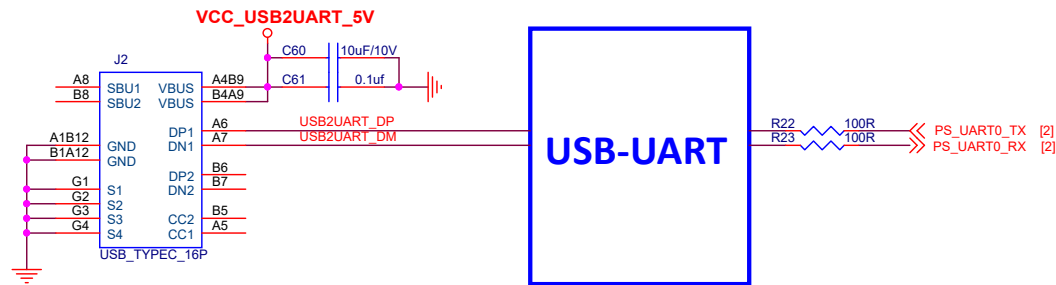
# ZYNQ POWER



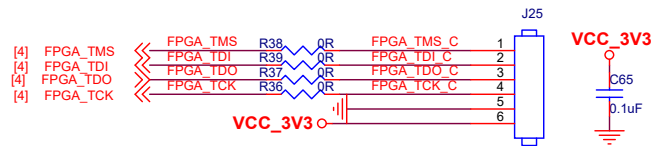
# DDR3



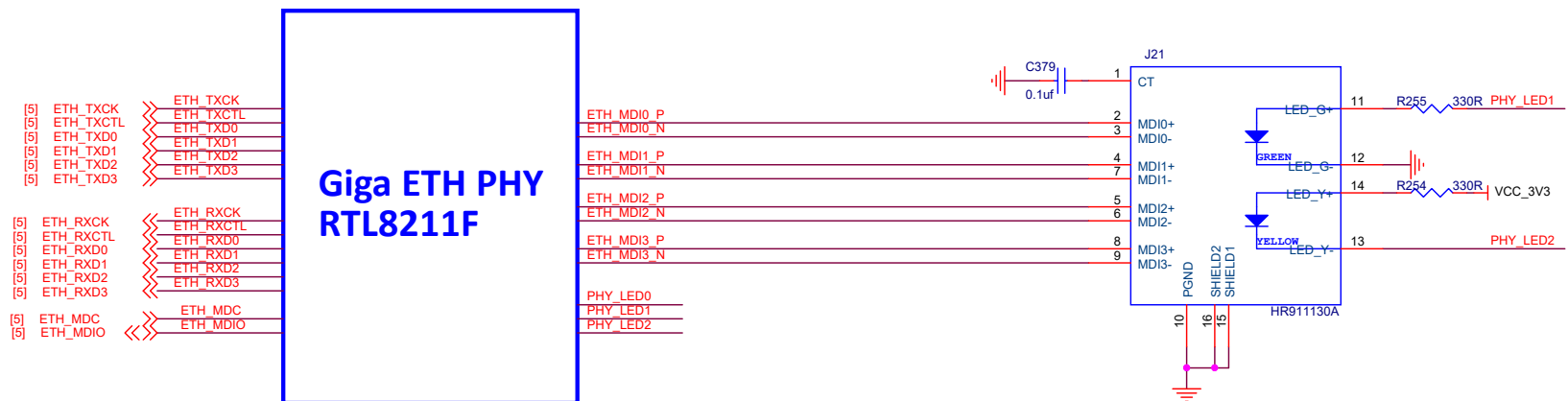
# USB-UART



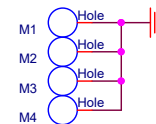
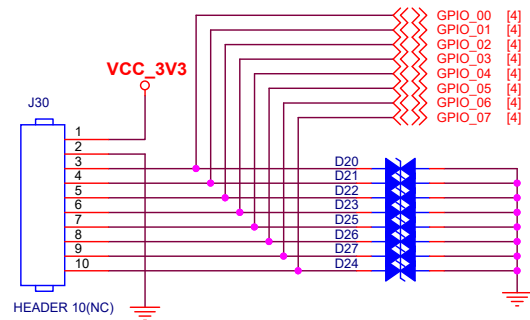
# JTAG





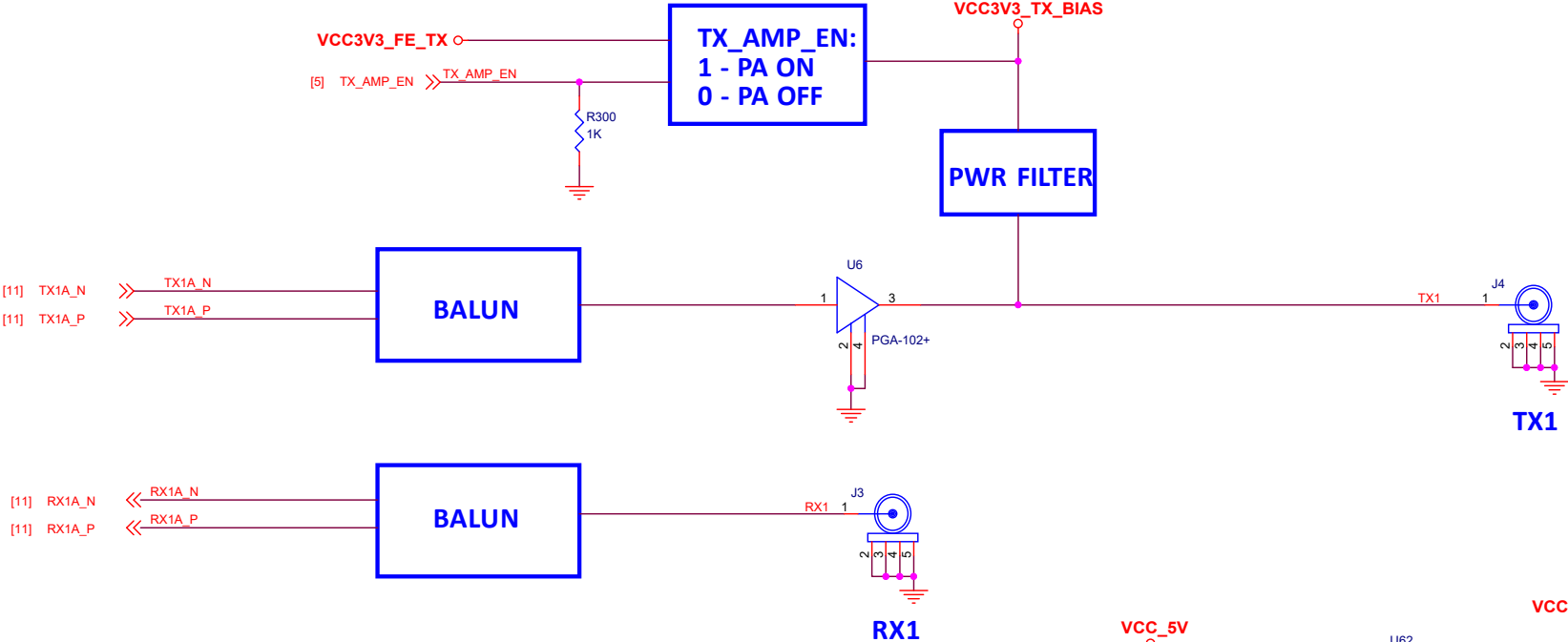


# GPIO

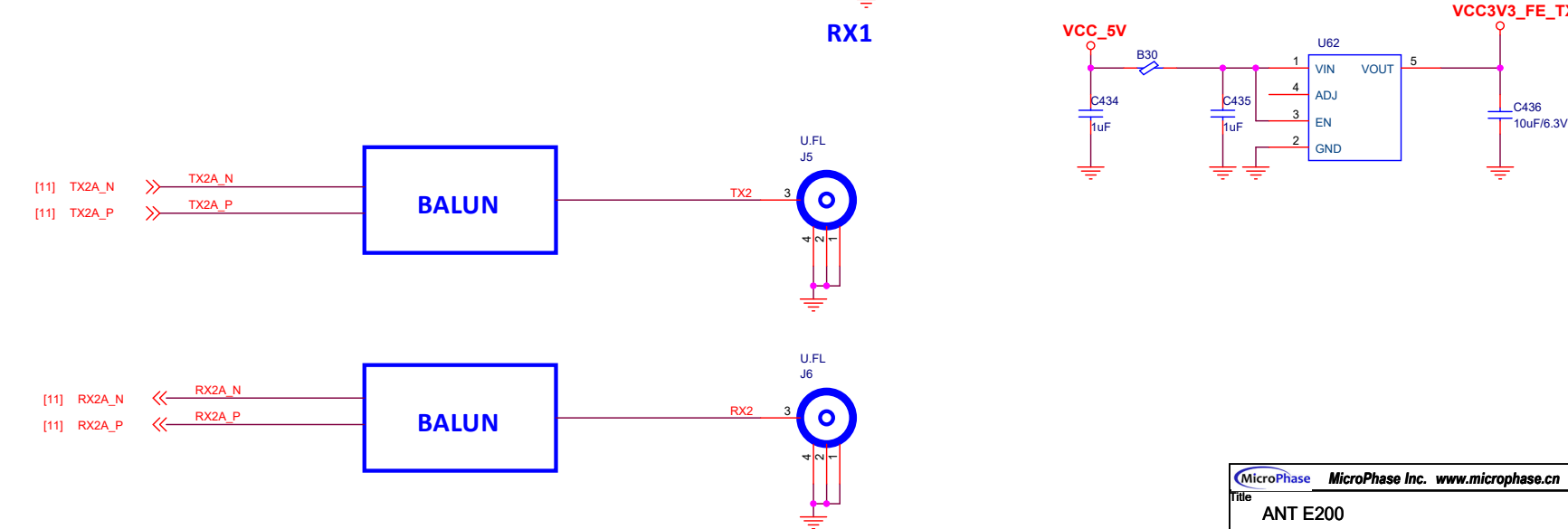




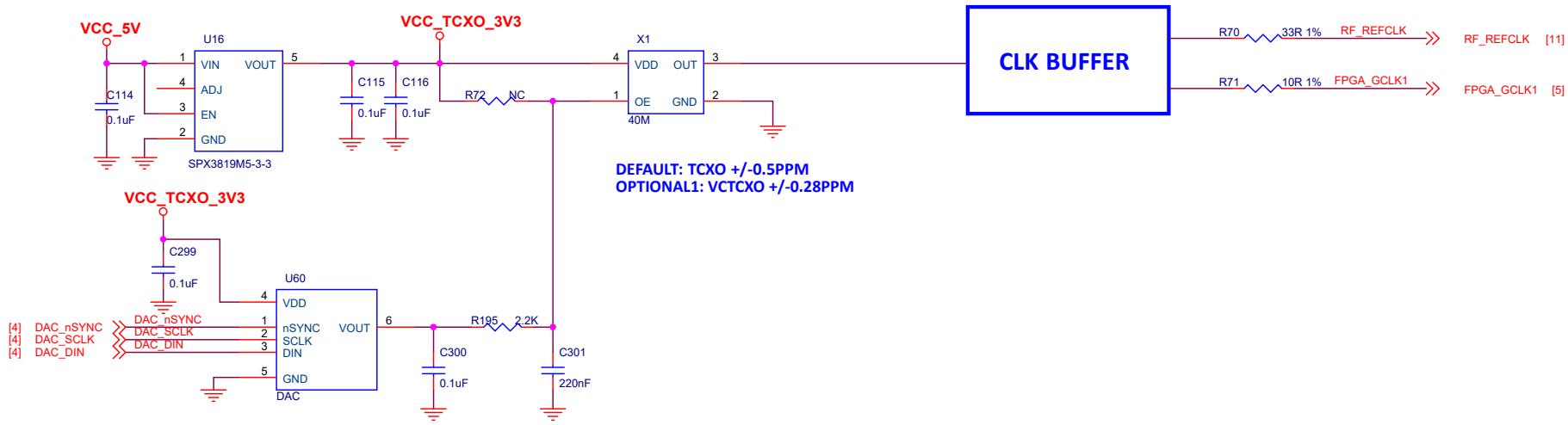
RF\_CH1



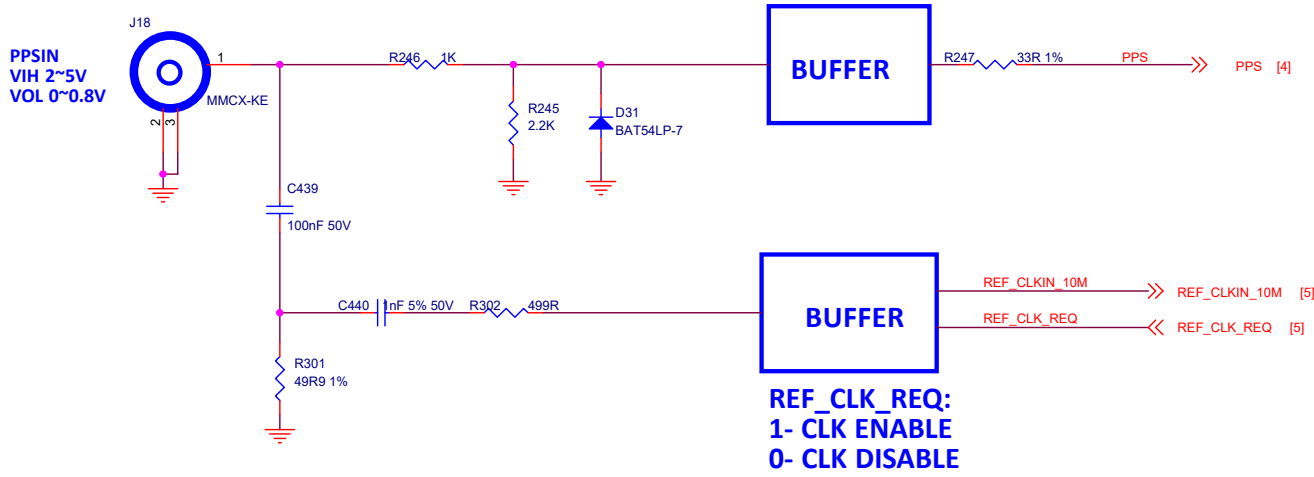
RF\_CH2

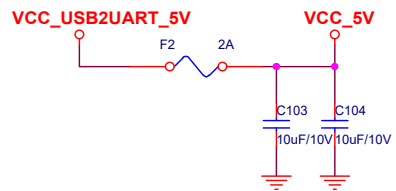


# CLOCK



# PPS/10M





Power System

# LED

