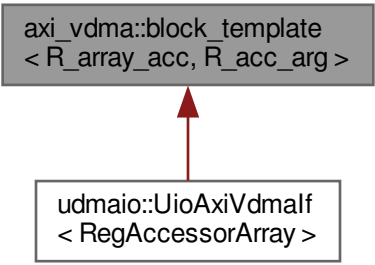


```
axi_vdma::block_template  
< R_array_acc, R_acc_arg >
```



```
graph BT; A["udmaio::UioAxiVdmalf< RegAccessorArray >"] --> B["axi_vdma::block_template< R_array_acc, R_acc_arg >"]
```

```
udmaio::UioAxiVdmalf  
< RegAccessorArray >
```