Arm® Arm926EJ-S™ Processor-Based MPU, 800 MHz, MIPI DSI® or CSI-2, LVDS, RGB, 2D Graphics, Gigabit Ethernet with TSN, CAN-FD, Octal/Quad SPI, Crypto, PUF

SAM9X7 Series Fine Pitch Package Devices

Introduction

The SAM9X7 Series microprocessors are high-performance and cost-optimized Arm926EJ-S CPU-based embedded microprocessors (MPU), running up to 800 MHz. The devices integrate powerful peripherals for connectivity and user interface applications, including MIPI DSI, LVDS, RGB and 2D graphics, MIPI-CSI-2, Gigabit Ethernet with TSN and CAN-FD. Advanced security functions are offered, such as tamper detection, secure boot, secure key storage, TRNG, PUF as well as high-performance crypto accelerators for AES and SHA. The SAM9X7 Series is supported by Microchip MPLAB®-X development tools, Harmony, Linux® distributions and the Ensemble Graphics Toolkit.

Reference Documents

The SAM9X7 Series Fine Pitch Package devices conform functionally to the SAM9X7 Series device data sheet referenced below, except for the differences described in this product brief and for the anomalies described in the SAM9X7 Series Silicon Errata and Data Sheet Clarifications document referenced below.

Type	Title	Literature No.	Available
Data sheet	SAM9X7 Series	DS60001813	www.microchip.com
Errata sheet(1)	SAM9X7 Series Silicon Errata and Data Sheet Clarification	DS80001082	www.microchip.com

Note:

1. The SAM9X7 Series errata sheet applies even though it does not refer explicitly to SAM9X7 Series Fine Pitch Package devices.

Features

- CPU Running up to 800 MHz
  - Arm926EJ-S Arm Thumb® processor
  - 32-Kbyte data cache, 32-Kbyte instruction cache, Memory Management Unit (MMU)
- Memories
  - One 176-Kbyte internal ROM
    - 80-Kbyte internal ROM embedding a secure bootloader program supporting boot on NAND Flash, SD Card, SPI or QSPI Flash; bootloader features selectable by OTP bits
    - 96-Kbyte ROM for NAND Flash BCH ECC table
  - One 64-Kbyte internal SRAM (SRAM0), single cycle access at system speed
  - DDR3(L)/DDR2 controller running at up to 266 MHz
  - External Bus Interface (EBI) supporting:
    - 16-bit 8/4-bank DDR3(L)/DDR2
    - 16-bit static memories
    - 8-bit NAND Flash with up to 24-bit programmable multi-bit error correcting code
  - One 10-Kbyte OTP memory for secure key storage with Emulation mode (OTP bits are emulated by a 4-Kbyte SRAM (SRAM1))

- System Running up to 266 MHz
  - Power-on reset cells, reset controller, shutdown controller, periodic interval timer, watchdog timer running on internal slow RC oscillator (32 kHz typical) and real-time clock running on slow crystal oscillator (32.768 kHz)
  - Two internal trimmed RC oscillators with typical values: 32 kHz (slow) and 12 MHz (fast)
  - Two crystal oscillators: 32.768 kHz (slow) and 20 to 50 MHz (fast)
  - One PLL for the system and one PLL optimized for USB high-speed operation (480 MHz)
    - One PLL for audio operations, with dedicated output clock
    - One PLL in LVDS I/F (LVDS usage only)
    - One PLL in MIPI DPHY (MIPI DSI usage only)
  - One dual-port 16-channel DMA controller
  - Advanced interrupt controller and debug unit
  - JTAG port with disable bit in OTP memory
  - Two programmable clock output signals
- Low-Power Modes
  - Backup mode with RTC, eight 32-bit general purpose backup registers, and shutdown controller to control the external power supply
  - Clock generator and power management controller
  - Software-programmable ultra-low power modes: Very slow clock operating mode (ULP0), and no-clock operating mode (ULP1) with fast wake-up capabilities
  - Software programmable power optimization capabilities
- Peripherals
  - LCD controller with overlay, alpha-blending, rotation, scaling and color conversion; display size up to 1024x768 (XGA) with overlay (application-dependent); still images up to 1280x720 (720p)
  - RGB, LVDS, MIPI DSI interfaces (see Configuration Summary)
  - 2D graphics controller supporting fill BLT, copy BLT, transparent BLT, blend/alpha BLT, ROP4 BLT (raster operations) and command ring buffer
  - Image sensor controller with ITU-R BT; 601/656/1120 video interface support up to 5 Mpixels; support of raw Bayer 12, YCbCr, monochrome and JPEG compressed sensors up to 12 bits
    - MIPI CSI2 I/F support
    - 12-bit parallel I/F support
  - One high-speed USB device, three high-speed USB hosts with dedicated on-chip transceivers
  - One 10/100/1000 Mbps Ethernet Mac controller, with IEEE®-1588 and TSN support, RGMII and RMII support
  - Two 4-bit secure digital multimedia card controllers
  - Two CAN FD controllers with timestamping
  - One Quad/Octal SPI controller
  - Two 3-channel 32-bit timers/counters
  - Two high-resolution (64-bit) periodic interval timers
  - One synchronous serial controller
  - One inter-IC sound multi-channel controller with TDM support
  - One audio class D controller with single-ended or bridge-tied load connection to power stage
  - One 4-channel 16-bit PWM controller

  - Thirteen FLEXCOMs (USART, SPI and TWI/I2C)
  - One 8-channel, 12-bit, analog-to-digital converter with 4/5 wires resistive touchscreen support
- Hardware Cryptography
  - SHA (SHA1, SHA224, SHA256, SHA384, SHA512) and HMAC compliant with FIPS PUB 180
  - AES: 256-, 192-, 128-bit key algorithms compliant with FIPS PUB 197
  - AES/SHA tight coupling for IPsec hardware acceleration
  - TDES: 2-key or 3-key algorithms compliant with FIPS PUB 46
  - True random number generator compliant with NIST Special Publication 800-22 Test Suite and FIPS PUBs 140-2 and 140-3
  - Key bus providing private key transfers between AES, TDES, TRNG, OTPC
  - Physical Unclonable Function (PUF) including NIST SP 800-90B (DRNG) and embedding four Kbytes of SRAM (PUFSRAM)
- I/O Ports
  - Four parallel input/output controllers
  - Up to 106 programmable I/O lines multiplexed with up to four peripheral I/Os
  - Input change interrupt capability on each I/O line, optional Schmitt trigger input
  - Individually programmable open-drain, pull-up and pull-down resistors, synchronous output
  - General-purpose analog and digital inputs tolerant to positive and negative current injection
- Design for low ElectroMagnetic Interference (EMI)
  - Slewrate-controlled I/Os
  - DDR PHY with impedance-calibrated drivers
  - Spread spectrum PLLs
- Operating Conditions
  - Junction temperature (T_J) range: -40°C to +125°C
  - SAM9X7x-V devices ambient temperature (T_A) range: -40°C to +105°C
- Package
  - 9x9 mm^2, 0.5-mm pitch, 256-ball BGA

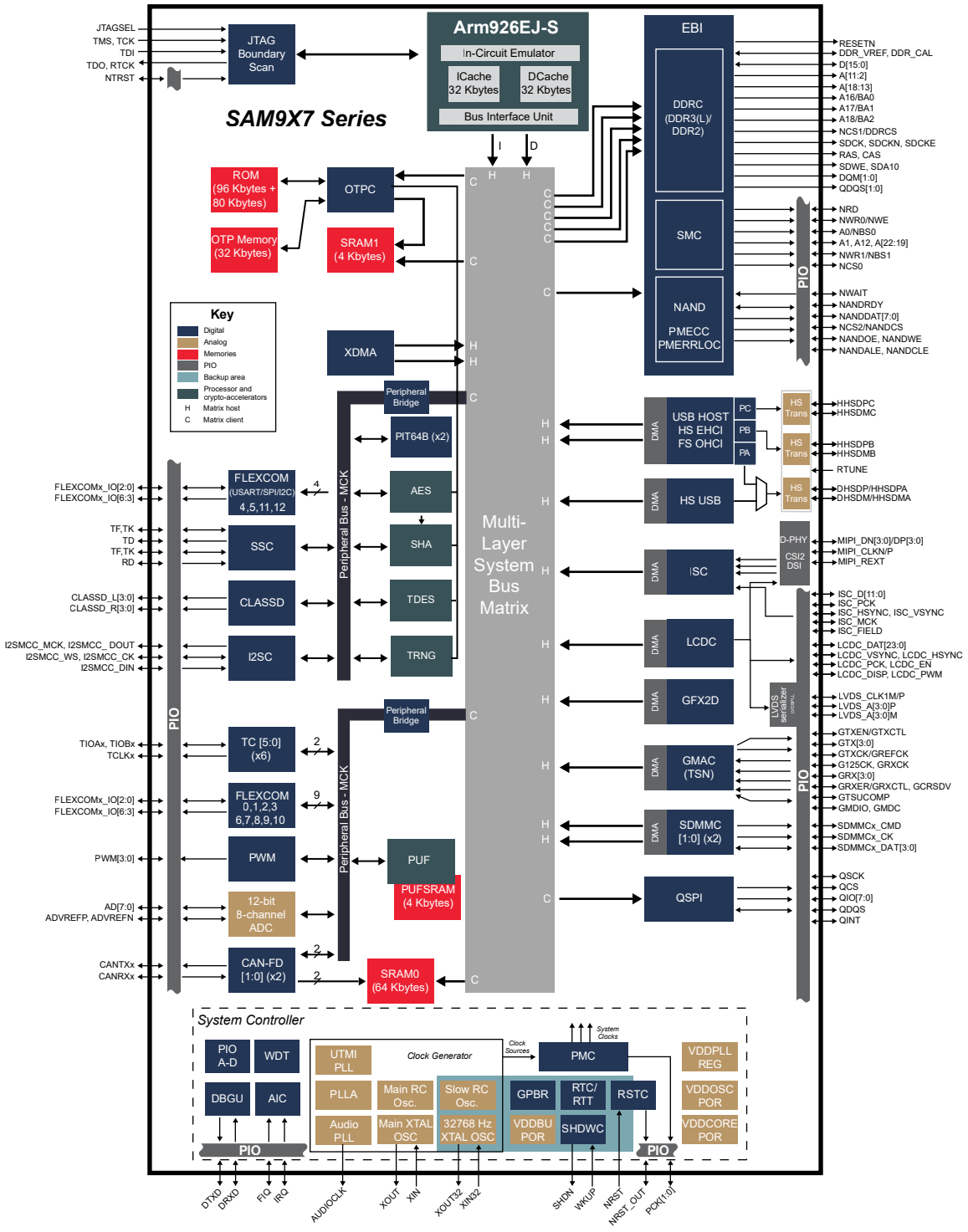
1. Configuration Summary

Table 1-1. Configuration Summary

Feature	SAM9X70	SAM9X72	SAM9X75
Package	9x9 mm^2, 0.5-mm pitch, 256-ball BGA		
Core	Arm926EJ-S @ 800 MHz		
SMC	Up to 16 bits		
MIPI DPHY	No		Bidirectional, 4 lanes
PIOs	106		
SRAM0/SRAM1	64/4 Kbytes		
Quad/Octal SPI	1		
LCD, GFX2D	No	LVDS, parallel port	LVDS, MIPI DSI, parallel port
Camera Interface (ISC)	Parallel port		MIPI CSI2, parallel port
GMAC	10/100/1000 Mbps with IEEE-1588 and TSN support		
CAN-FD	No	2	
USB	3 (3 hosts or 2 hosts/1 device)		
UART/SPI/I2C	13		
SDIO/SD/MMC	2		
I2SMCC/SSC/CLASSD	1/1/1		
ADC Inputs	8 (8 channels)		
64-bit/32-bit Timer Counter Channels	2/6		
PWM	4 (PWMC)		
Cryptography	AES/TDES/SHA/TRNG		

2. Block Diagram

Figure 2-1. SAM9X7 Series Block Diagram



3. Signal Description

The following table provides details on signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Comments	Active Level
Clocks, Oscillators and PLLs				
XIN	Main Crystal Oscillator Input	Input	–	–
XOUT	Main Crystal Oscillator Output	Output	–	–
XIN32	32.768 kHz Crystal Oscillator Input	Input	–	–
XOUT32	32.768 kHz Crystal Oscillator Output	Output	–	–
RTUNE	USB External Tune Resistor	Analog	–	–
PCK[1:0]	Programmable Clock Output	Output	–	–
AUDIOCLK	Audio Programmable Clock Output	Output	–	–
Shutdown, Wake-Up Logic				
SHDN	Shutdown Control	Output	–	–
WKUP0	Wake-Up Input	Input	–	–
ICE and JTAG				
TCK	Test Clock	Input	–	–
TDI	Test Data In	Input	–	–
TDO	Test Data Out	Output	–	–
TMS	Test Mode Select	Input	–	–
JTAGSEL	JTAG Selection	Input	–	–
RTCK	Return Test Clock	Output	–	–
Reset/Test				
NRST	External Reset Input	Input	–	Low
NRST_OUT	Reset Controller Output	Output	–	Low
TST	Test Mode Select	Input	–	–
NTRST	Test Reset Signal	Input	–	–
Debug Unit - DBGU				
DRXD	Debug Receive Data	Input	–	–
DTXD	Debug Transmit Data	Output	–	–
Advanced Interrupt Controller - AIC				
IRQ	External Interrupt Input	Input	–	–
FIQ	Fast Interrupt Input	Input	–	–
PIO Controller - PIOA - PIOB - PIOC - PIOD				
PA[31:0]	Parallel IO Controller A	I/O	–	–
PB[26:0]	Parallel IO Controller B	I/O	–	–
PC[31:0]	Parallel IO Controller C	I/O	–	–
PD[14:0]	Parallel IO Controller D	I/O	–	–
External Bus Interface - EBI				
A[22:0]	Address Bus	Output	–	–
NWAIT/NANDRDY	External Wait Signal/NAND Flash R/B Signal	Input	–	Low
Static Memory Controller - SMC				
NCS[2:0]	Chip Select Lines	Output	–	Low
NWR[1:0]	Write Signal	Output	–	Low
NRD	Read Signal	Output	–	Low

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Signal Name	Function	Type	Comments	Active Level
NWE	Write Enable	Output	–	Low
NBS[1:0]	Byte Mask Signal	Output	–	Low
NAND Flash Controller				
NANDDAT[7:0]	NAND Flash I/O	I/O	–	–
NANDCS	NAND Flash Chip Select	Output	–	Low
NANDOE	NAND Flash Output Enable	Output	–	Low
NANDWE	NAND Flash Write Enable	Output	–	Low
NANDALE	NAND Address Latch Enable	Output	–	Low
NANDCLE	NAND Command Latch Enable	Output	–	Low
DDR2/DDR3(L) Controller				
SDCK	DRAM Clock	Output	–	–
SDCKN	DRAM Clock Bar	Output	–	–
SDCKE	DRAM Clock Enable	Output	–	High
DDRCS	DRAM Chip Select	Output	–	Low
BA[2:0]	Bank Select	Output	–	Low
SDWE	DRAM Write Enable	Output	–	Low
DDR_VREF	I/O Reference Voltage	I/O	–	–
DDR_CAL	Calibration Input	I/O	–	–
RAS - CAS	Row and Column Signal	Output	–	Low
A[22:0]	Address Bus	Output	–	–
SDA10	SDRAM Address 10 Line	Output	–	–
D[15:0]	Data Bus	I/O	–	–
DQS[1:0]	Positive Data Strobe	I/O	–	–
DQSN[1:0]	Negative Data Strobe (DDR2/3(L)-SDRAM only)	I/O	–	–
DQM[1:0]	Write Data Mask	Output	–	–
RESETN	DDR3-SDRAM Reset	Output	–	–
Secure Data Memory Card - SDMMCx [1:0]				
SDMMCx_CMD	SD Card/eMMC™ Command Line	I/O	–	–
SDMMCx_CK	SD Card/eMMC Clock Signal	Output	–	–
SDMMCx_DAT[3:0]	SD Card/eMMC Data Lines	I/O	–	–
Flexible Serial Communication Controller - FLEXCOMx [12:0]				
FLEXCOMx_IO0	Transmit Data (TXD/MOSI/TWD)	I/O	–	–
FLEXCOMx_IO1	Receive Data (RXD/MISO/TWCK)	I/O	–	–
FLEXCOMx_IO2	Serial Clock (SCK/SPCK)	I/O	–	–
FLEXCOMx_IO3	Clear To Send/Peripheral Chip Select	I/O	–	–
FLEXCOMx_IO4	Request To Send/Peripheral Chip Select	Output	–	–
FLEXCOMx_IO5	Peripheral Chip Select	Output	–	–
FLEXCOMx_IO6	Peripheral Chip Select	Output	–	–
FLEXCOMx_IO7	LON Collision	Input	–	–
Synchronous Serial Controller - SSC				
TD	Transmit Data	Output	–	–
RD	Receive Data	Input	–	–
TK	Transmit Clock	I/O	–	–
RK	Receive Clock	I/O	–	–
TF	Transmit Frame Synchronization	I/O	–	–

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Signal Name	Function	Type	Comments	Active Level
RF	Receive Frame Synchronization	I/O	–	–
Timer/Counter - TCx [5:0]				
TCLK[2:0]	External Clock Input	Input	–	–
TIOA[2:0]	I/O Line A	I/O	–	–
TIOB[2:0]	I/O Line B	I/O	–	–
Pulse Width Modulation Controller - PWMC				
PWM[3:0]	Pulse Width Modulation Output	Output	–	–
USB Host High Speed Port - UHPHS				
HHSDMA	USB Host Port A High Speed Data -	Analog	–	–
HHSDPA	USB Host Port A High Speed Data +	Analog	–	–
HHSDMB	USB Host Port B High Speed Data -	Analog	–	–
HHSDPB	USB Host Port B High Speed Data +	Analog	RTUNE	–
HHSDMC	USB Host Port C High Speed Data -	Analog	–	–
HHSDPC	USB Host Port C High Speed Data +	Analog	–	–
USB Device High Speed Port - UDPHS				
DHSDM	USB Device High Speed Data -	Analog	–	–
DHSDP	USB Device High Speed Data +	Analog	–	–
Gigabit Ethernet 10/100/1000 with IEEE-1588 and TSN (RGMII/RMII only) - GMAC				
GTXCK/GREFCK	Transmit Clock or Reference Clock	I/O	–	–
G125CK	125 MHz Reference Clock	Input	–	–
GRXCK	Receive Clock	Input	–	–
GTXEN/GTXCTL	Transmit Enable or Transmit Control	Output	–	–
GTX[3:0]	Transmit Data	Output	–	–
GCRSDV/GRXCTL	Receive Data Valid or Receive Control	Input	–	–
GRX[3:0]	Receive Data	Input	–	–
GRXER	Receive Error	Input	–	–
GMDC	Management Data Clock	Output	–	–
GMDIO	Management Data Input/Output	I/O	–	–
GTSUCOMP	TSU Timer Comparison Valid	Output	–	–
Analog-to-Digital Converter - ADC				
AD[7:0]	8 Analog Inputs	Input	–	–
ADTRG	ADC Trigger	Input	–	–
ADVREFN	ADC Negative Reference Voltage	Analog Input	–	–
ADVREFP	ADC Positive Reference Voltage	Analog Input	–	–
CAN Controller - CANx [1:0]				
CANRXx	CAN Receive	Input	–	–
CANTXx	CAN Transmit	Output	–	–
Class D Controller - CLASSD				
CLASSD_L0	Class D Controller Left Output 0	Output	–	–
CLASSD_L1	Class D Controller Left Output 1	Output	–	–
CLASSD_L2	Class D Controller Left Output 2	Output	–	–
CLASSD_L3	Class D Controller Left Output 3	Output	–	–
CLASSD_R0	Class D Controller Right Output 0	Output	–	–
CLASSD_R1	Class D Controller Right Output 1	Output	–	–

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Signal Name	Function	Type	Comments	Active Level
CLASSD_R2	Class D Controller Right Output 2	Output	–	–
CLASSD_R3	Class D Controller Right Output 3	Output	–	–
Quad/Octal I/O SPI - QSPI				
QSCK	Quad IO SPI Serial Clock	Output	–	–
QCS	Quad IO SPI Chip Select	Output	–	–
QIO[7:0]	IO SPI I/O 0 to 7	I/O	–	–
QDQS	Octal IO Data Strobe	I/O	–	–
QINT	Interrupt	Input	–	–
Inter IC Sound Multi Channel Controller - I2SMCC				
I2SMCC_MCK	Main System Bus Clock	Output	–	–
I2SMCC_CK	Serial Clock	I/O	–	–
I2SMCC_WS	I2S Word Select	I/O	–	–
I2SMCC_DIN	Serial Data Input	Input	–	–
I2SMCC_DOUT	Serial Data Output	Output	–	–
MIPI DPHY				
MIPI_DP[3:0] MIPI_DN[3:0]	MIPI DPHY Differential Output Data Lane [3:0]	I/O	–	–
MIPI_CLKP MIPI_CLKN	MIPI DPHY Differential Output Clock Lane	I/O	–	–
MIPI_REXT	Calibration Reference Resistor (4.02 KΩ E96)	I/O	–	–
Low Voltage Differential Signaling Controller (LVDS)				
LVDS_A[3:0]P LVDS_A[3:0]M	Differential LVDS Data Line Transceiver Output [3:0]	Output	–	–
LVDS_CLK1M LVDS_CLK1P	Differential LVDS Clock Line Transceiver Output	Output	–	–
Image Sensor Controller (ISC)				
ISC_MCK	Main System Bus Clock to Sensor	Output	–	–
ISC_PCK	Pixel Clock from Sensor	Input	–	–
ISC_D[11:0]	Data	Input	–	–
ISC_HSYNC	Horizontal Synchronization	Input	–	–
ISC_VSYNC	Vertical Synchronization	Input	–	–
ISC_FIELD	Field to Interface Video Streams	Input	–	–
LCD Controller (LCDC)				
LCDC_DAT[23:0]	Data Bus	Output	–	–
LCDC_PCK	Pixel Clock	Output	–	–
LCDC_HSYNC	Horizontal Synchronization	Output	–	–
LCDC_VSYNC	Vertical Synchronization	Output	–	–
LCDC_DEN	Data Enable	Output	–	–
LCDC_DISP	Display On/Off	Output	–	–
LCDC_PWM	PWM for Contrast Control	Output	–	–

4. Package and Pinout

4.1 Package

The SAM9X7 Series Fine Pitch Package Devices are available in the following package.

Package Name	Ball Count	Ball Pitch	Package Size
TFBGA256	256	0.5 mm	9x9 mm

For further details, refer to Mechanical Characteristics.

4.2 Pinout

Figure 4-1. SAM9X7 Series Fine Pitch Package Device Pinout

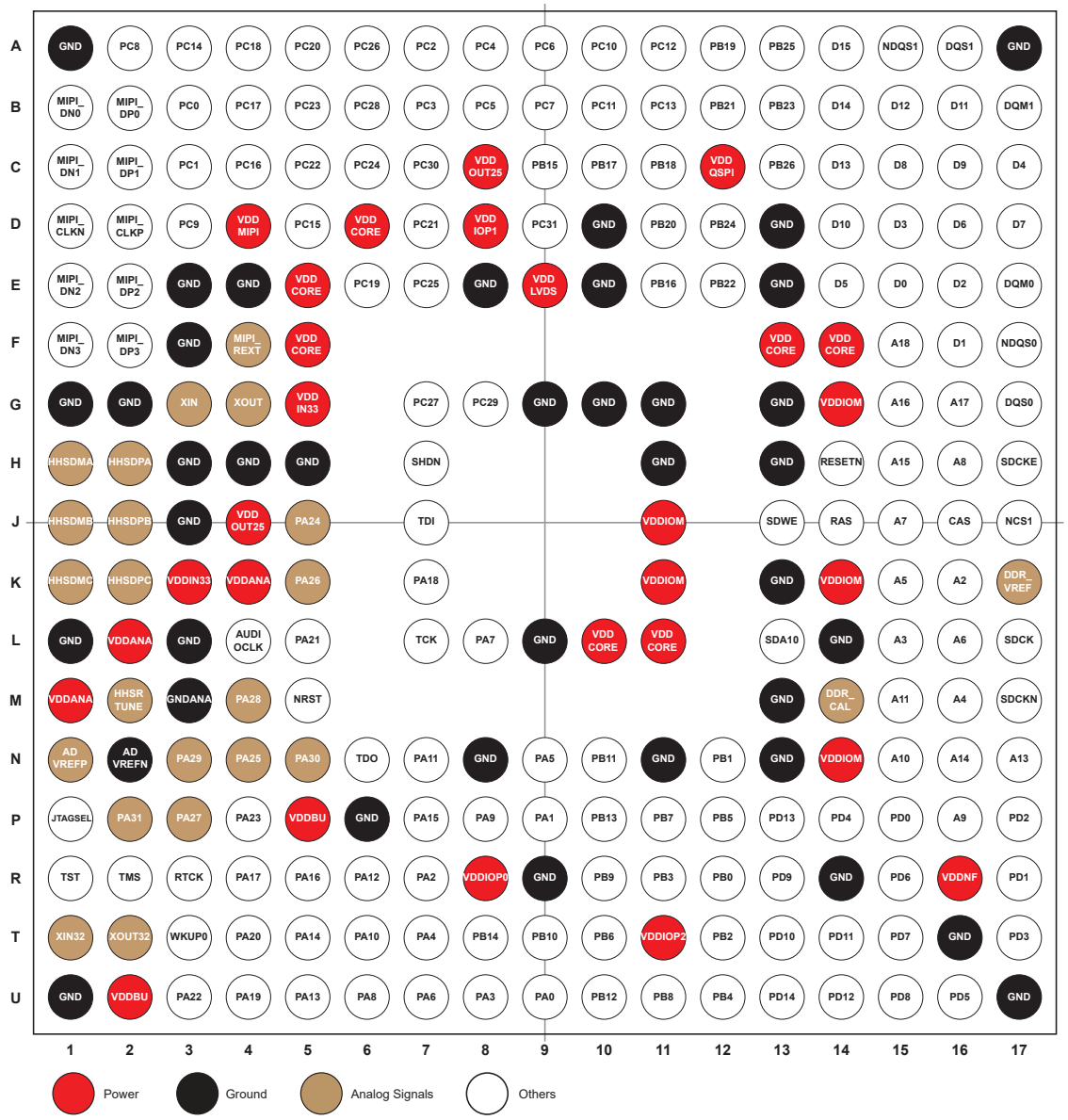

Table 4-1. Pin Description

256-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
U9	VDDIOP0	GPIO	PA0	I/O	–	–	A	SDMMC0_DAT0	I/O	1	PIO, I, PU, ST
P9	VDDIOP0	GPIO	PA1	I/O	–	–	A	SDMMC0_CMD	I/O	1	PIO, I, PU, ST
R7	VDDIOP0	GPIO	PA2	I/O	WKUP1	–	A	SDMMC0_CK	I/O	1	PIO, I, PU, ST
U8	VDDIOP0	GPIO	PA3	I/O	–	–	A	SDMMC0_DAT1	I/O	1	PIO, I, PU, ST
T7	VDDIOP0	GPIO	PA4	I/O	–	–	A	SDMMC0_DAT2	I/O	1	PIO, I, PU, ST
N9	VDDIOP0	GPIO	PA5	I/O	–	–	A	SDMMC0_DAT3	I/O	1	PIO, I, PU, ST
U7	VDDIOP0	GPIO	PA6	I/O	–	–	A	FLEXCOM0_IO4	O	1	PIO, I, PU, ST
							B	SDMMC1_DAT1	I/O	1	
L8	VDDIOP0	GPIO	PA7	I/O	WKUP2	–	A	FLEXCOM0_IO3	I/O	1	PIO, I, PU, ST
							B	SDMMC1_DAT2	I/O	1	
U6	VDDIOP0	GPIO	PA8	I/O	WKUP3	–	A	FLEXCOM0_IO2	I/O	1	PIO, I, PU, ST
							B	SDMMC1_DAT3	I/O	1	
P8	VDDIOP0	GPIO	PA9	I/O	–	–	A	FLEXCOM4_IO1	I/O	1,2	PIO, I, PU, ST
							B	SDMMC1_DAT0	I/O	1	
T6	VDDIOP0	GPIO	PA10	I/O	–	–	A	FLEXCOM4_IO0	I/O	1,2	PIO, I, PU, ST
							B	SDMMC1_CMD	I/O	1	
N7	VDDIOP0	GPIO	PA11	I/O	–	–	A	FLEXCOM4_IO2	I/O	1,2	PIO, I, PU, ST
							B	SDMMC1_CK	I/O	1	
R6	VDDIOP0	GPIO	PA12	I/O	–	–	A	FLEXCOM4_IO3	I/O	1,2	PIO, I, PU, ST
							C	FLEXCOM5_IO4	O	1	
U5	VDDIOP0	GPIO	PA13	I/O	–	–	A	FLEXCOM2_IO0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM4_IO4	O	1	
T5	VDDIOP0	GPIO	PA14	I/O	–	–	A	FLEXCOM2_IO1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO3	I/O	1,2	
							C	FLEXCOM4_IO5	O	1	
P7	VDDIOP0	GPIO	PA15	I/O	–	–	A	TIOA0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO1	I/O	1,2	
							C	CLASSD_R0	O	1	
R5	VDDIOP0	GPIO	PA16	I/O	–	–	A	TIOA1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO0	I/O	1,2	
							C	CLASSD_R1	O	1	
R4	VDDIOP0	GPIO	PA17	I/O	–	–	A	TIOA2	I/O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO2	I/O	1,2	
							C	CLASSD_R2	O	1	

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256-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
K7	VDDIOP0	GPIO	PA18	I/O	–	–	A	TCLK0	I	1	PIO, I, PU, ST
							B	TK	I/O	1	
							C	CLASSD_L0	O	1	
U4	VDDIOP0	GPIO	PA19	I/O	–	–	A	TCLK1	I	1	PIO, I, PU, ST
							B	TF	I/O	1	
							C	CLASSD_L1	O	1	
T4	VDDIOP0	GPIO	PA20	I/O	WKUP4	–	A	TCLK2	I	1	PIO, I, PU, ST
							B	TD	O	1	
							C	CLASSD_L2	O	1	
L5	VDDIOP0	GPIO	PA21	I/O	–	–	A	TIOB0	I/O	1	PIO, I, PU, ST
							B	RD	I	1	
							C	CLASSD_L3	O	1	
U3	VDDIOP0	GPIO	PA22	I/O	–	–	A	TIOB1	I/O	1	PIO, I, PU, ST
							B	RK	I/O	1	
							C	CLASSD_R3	O	1	
P4	VDDIOP0	GPIO	PA23	I/O	–	–	A	TIOB2	I/O	1	PIO, I, PU, ST
							B	RF	I/O	1	
							C	FLEXCOM2_IO7	I	1	
J5	VDDANA	GPIO	PA24	I/O	AD0	–	A	FLEXCOM6_IO0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO6	O	1	
N4	VDDANA	GPIO	PA25	I/O	AD1	–	A	FLEXCOM6_IO1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO5	O	1	
K5	VDDANA	GPIO	PA26	I/O	AD2	–	A	DRXD	I	1	PIO, I, PU, ST
							B	CANRX0	I	1	
P3	VDDANA	GPIO	PA27	I/O	AD3	–	A	DTXD	O	1	PIO, I, PU, ST
							B	CANTX0	O	1	
M4	VDDANA	GPIO	PA28	I/O	AD4	–	A	FLEXCOM1_IO0	I/O	1	PIO, I, PU, ST
							B	CANTX1	O	1	
N3	VDDANA	GPIO	PA29	I/O	AD5	–	A	FLEXCOM1_IO1	I/O	1	PIO, I, PU, ST
							B	CANRX1	I	1	
N5	VDDANA	GPIO	PA30	I/O	AD6	–	A	FLEXCOM0_IO0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO4	O	2	
							C	FLEXCOM4_IO4	O	2	
P2	VDDANA	GPIO	PA31	I/O	AD7	–	A	FLEXCOM0_IO1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM4_IO5	O	2	
							C	GTSUCOMP	O	1	

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256-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
R12	VDDIOP2	GPIO	PB0	I/O	WKUP5	–	A	GRX2	I	1	PIO, I, PU, ST
							B	FLEXCOM2_IO4	O	1	
							C	GRXER	I	1	
N12	VDDIOP2	GPIO	PB1	I/O	–	–	A	GRX3	I	1	PIO, I, PU, ST
							B	FLEXCOM2_IO3	I/O	1	
T12	VDDIOP2	GPIO	PB2	I/O	–	–	A	G125CK	I	1	PIO, I, PU, ST
							B	FLEXCOM2_IO2	I/O	1	
R11	VDDIOP2	GPIO	PB3	I/O	WKUP6	–	A	GCRSDV/GRXCTL	I	1	PIO, I, PU, ST
							B	FLEXCOM4_IO6	O	1	
U12	VDDIOP2	GPIO	PB4	I/O	–	–	A	GTX2	O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO0	I/O	1	
P12	VDDIOP2	GPIO	PB5	I/O	–	–	A	GTX3	O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO1	I/O	1	
T10	VDDIOP2	GPIO	PB6	I/O	–	–	A	GTXCK/GREFCK	I/O	1	PIO, I, PU, ST
							B	FLEXCOM0_IO7	I	1	
P11	VDDIOP2	GPIO	PB7	I/O	–	–	A	GTXEN/GTXCTL	O	1	PIO, I, PU, ST
							C	FLEXCOM6_IO2	I/O	1	
U11	VDDIOP2	GPIO	PB8	I/O	–	–	A	GRXCK	I	1	PIO, I, PU, ST
							C	FLEXCOM6_IO3	I/O	1	
R10	VDDIOP2	GPIO	PB9	I/O	–	–	A	GMDIO	I/O	1	PIO, I, PU, ST
							B	PCK1	O	1	
							C	FLEXCOM6_IO4	O	1	
T9	VDDIOP2	GPIO	PB10	I/O	–	–	A	GMDC	O	1	PIO, I, PU, ST
							B	PCK0	O	1	
							C	FLEXCOM8_IO2	I/O	1	
N10	VDDIOP2	GPIO	PB11	I/O	–	–	A	GRX0	I	1	PIO, I, PU, ST
							B	PWM0	O	2	
							C	FLEXCOM8_IO3	I/O	1	
U10	VDDIOP2	GPIO	PB12	I/O	–	–	A	GRX1	I	1	PIO, I, PU, ST
							B	PWM1	O	2	
							C	FLEXCOM8_IO4	O	1	
P10	VDDIOP2	GPIO	PB13	I/O	–	–	A	GTX0	O	1	PIO, I, PU, ST
						–	B	PWM2	O	2	
T8	VDDIOP2	GPIO	PB14	I/O	–	–	A	GTX1	O	1	PIO, I, PU, ST
							B	PWM3	O	2	

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256-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
C9	VDDQSPI	GPIO	PB15	I/O	–	–	A	QIO5	I/O	1	PIO, I, PU, ST
							B	–	–	–	
							C	FLEXCOM11_IO0	I/O	1	
							D	I2SMCC_WS	I/O	1	
E11	VDDQSPI	GPIO	PB16	I/O	–	–	A	QIO6	I/O	1	PIO, I, PU, ST
							B	–	–	–	
							C	FLEXCOM11_IO1	I/O	1	
							D	I2SMCC_DIN	I	1	
C10	VDDQSPI	GPIO	PB17	I/O	–	–	A	QIO7	I/O	1	PIO, I, PU, ST
							C	FLEXCOM12_IO0	I/O	1	
							D	I2SMCC_DOUT	O	1	
C11	VDDQSPI	GPIO	PB18	I/O	WKUP7	–	A	QDQS	I	1	PIO, I, PU, ST
							B	ADTRG	I	1	
							C	FLEXCOM12_IO1	I/O	1	
							D	IRQ	I	1	
A12	VDDQSPI	GPIO	PB19	I/O	–	–	A	QSCK	O	1	PIO, I, PU, ST
							C	FLEXCOM12_IO2	I/O	1	
D11	VDDQSPI	GPIO	PB20	I/O	–	–	A	QCS	O	1	PIO, I, PU, ST
							C	FLEXCOM12_IO3	I/O	1	
B12	VDDQSPI	GPIO	PB21	I/O	–	–	A	QIO0	I/O	1	PIO, I, PU, ST
							C	FLEXCOM12_IO4	O	1	
E12	VDDQSPI	GPIO	PB22	I/O	–	–	A	QIO1	I/O	1	PIO, I, PU, ST
							C	FLEXCOM9_IO2	I/O	1	
B13	VDDQSPI	GPIO	PB23	I/O	–	–	A	QIO2	I/O	1	PIO, I, PU, ST
							C	FLEXCOM9_IO3	I/O	1	
D12	VDDQSPI	GPIO	PB24	I/O	–	–	A	QIO3	I/O	1	PIO, I, PU, ST
							C	FLEXCOM9_IO4	O	1	
A13	VDDQSPI	GPIO	PB25	I/O	WKUP8	–	A	QINT	I	1	PIO, I, PU, ST
							D	I2SMCC_MCK	O	1	
C13	VDDQSPI	GPIO	PB26	I/O	–	–	A	QIO4	I/O	1	PIO, I, PU, ST
							D	I2SMCC_CK	I/O	1	
B3	VDDIOP1	GPIO	PC0	I/O	–	–	A	LCDC_DAT0	O	1	PIO, I, PU, ST
							B	ISC_D0	I	1	
							C	FLEXCOM7_IO0	I/O	1	
C3	VDDIOP1	GPIO	PC1	I/O	–	–	A	LCDC_DAT1	O	1	PIO, I, PU, ST
							B	ISC_D1	I	1	
							C	FLEXCOM7_IO1	I/O	1	

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256-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
A7	VDDLVDS	GPIO	PC2	I/O	LVDS_A0M	–	A	LCDC_DAT2	O	1	PIO, I, PU, ST
							B	ISC_D2	I	1	
							C	TIOA3	I/O	1	
B7	VDDLVDS	GPIO	PC3	I/O	LVDS_A0P	–	A	LCDC_DAT3	O	1	PIO, I, PU, ST
							B	ISC_D3	I	1	
							C	TIOB3	I/O	1	
A8	VDDLVDS	GPIO	PC4	I/O	LVDS_A1M	–	A	LCDC_DAT4	O	1	PIO, I, PU, ST
							B	ISC_D4	I	1	
							C	TCLK3	I	1	
B8	VDDLVDS	GPIO	PC5	I/O	LVDS_A1P	–	A	LCDC_DAT5	O	1	PIO, I, PU, ST
							B	ISC_D5	I	1	
							C	TIOA4	I/O	1	
A9	VDDLVDS	GPIO	PC6	I/O	LVDS_A2M	–	A	LCDC_DAT6	O	1	PIO, I, PU, ST
							B	ISC_D6	I	1	
							C	TIOB4	I/O	1	
B9	VDDLVDS	GPIO	PC7	I/O	LVDS_A2P	–	A	LCDC_DAT7	O	1	PIO, I, PU, ST
							B	ISC_D7	I	1	
							C	TCLK4	I	1	
A2	VDDIOP1	GPIO	PC8	I/O	–	–	A	LCDC_DAT8	O	1	PIO, I, PU, ST
							B	ISC_D8	I	1	
							C	FLEXCOM9_IO0	I/O	1	
D3	VDDIOP1	GPIO	PC9	I/O	–	–	A	LCDC_DAT9	O	1	PIO, I, PU, ST
							B	ISC_D9	I	1	
							C	FLEXCOM9_IO1	I/O	1	
A10	VDDLVDS	GPIO	PC10	I/O	LVDS_CLK1M	–	A	LCDC_DAT10	O	1	PIO, I, PU, ST
							B	ISC_D10	I	1	
							C	PWM0	O	3	
B10	VDDLVDS	GPIO	PC11	I/O	LVDS_CLK1P	–	A	LCDC_DAT11	O	1	PIO, I, PU, ST
							B	ISC_D11	I	1	
							C	PWM1	O	3	
A11	VDDLVDS	GPIO	PC12	I/O	LVDS_A3M	–	A	LCDC_DAT12	O	1	PIO, I, PU, ST
							B	ISC_PCK	I	1	
							C	TIOA5	I/O	1	
B11	VDDLVDS	GPIO	PC13	I/O	LVDS_A3P	–	A	LCDC_DAT13	O	1	PIO, I, PU, ST
							B	ISC_VSYNC	I	1	
							C	TIOB5	I/O	1	

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256-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
A3	VDDIOP1	GPIO	PC14	I/O	–	–	A	LCDC_DAT14	O	1	PIO, I, PU, ST
							B	ISC_HSYNC	I	1	
							C	TCLK5	I	1	
D5	VDDIOP1	GPIO	PC15	I/O	–	–	A	LCDC_DAT15	O	1	PIO, I, PU, ST
							B	ISC_MCK	O	1	
							C	PCK0	O	2	
C4	VDDIOP1	GPIO	PC16	I/O	–	–	A	LCDC_DAT16	O	1	PIO, I, PU, ST
							B	ISC_FIELD	I	1	
							C	FLEXCOM10_IO0	I/O	1	
B4	VDDIOP1	GPIO	PC17	I/O	–	–	A	LCDC_DAT17	O	1	PIO, I, PU, ST
							B	FLEXCOM1_IO7	I	1	
							C	FLEXCOM10_IO1	I/O	1	
A4	VDDIOP1	GPIO	PC18	I/O	–	–	A	LCDC_DAT18	O	1	PIO, I, PU, ST
							B	FLEXCOM10_IO2	I/O	1	
							C	PWM0	O	1	
E6	VDDIOP1	GPIO	PC19	I/O	–	–	A	LCDC_DAT19	O	1	PIO, I, PU, ST
							B	FLEXCOM10_IO3	I/O	1	
							C	PWM1	O	1	
A5	VDDIOP1	GPIO	PC20	I/O	–	–	A	LCDC_DAT20	O	1	PIO, I, PU, ST
							B	FLEXCOM10_IO4	O	1	
							C	PWM2	O	1	
D7	VDDIOP1	GPIO	PC21	I/O	–	–	A	LCDC_DAT21	O	1	PIO, I, PU, ST
							C	PWM3	O	1	
C5	VDDIOP1	GPIO	PC22	I/O	–	–	A	LCDC_DAT22	O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO0	I/O	1	
B5	VDDIOP1	GPIO	PC23	I/O	WKUP9	–	A	LCDC_DAT23	O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO1	I/O	1	
C6	VDDIOP1	GPIO	PC24	I/O	WKUP10	–	A	LCDC_DISP	O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO4	O	1	
E7	VDDIOP1	GPIO	PC25	I/O	WKUP12	–	A	NTRST	I	1	NRST_OUT, O, PD
							B	FLEXCOM3_IO3	I/O	1	
							C	NRST_OUT	O	1	
A6	VDDIOP1	GPIO	PC26	I/O	WKUP13	–	A	LCDC_PWM	O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO2	I/O	1	
G7	VDDIOP1	GPIO	PC27	I/O	–	–	A	LCDC_VSYNC	O	1	PIO, I, PU, ST
							C	FLEXCOM1_IO4	O	1	

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256-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
B6	VDDIOP1	GPIO	PC28	I/O	–	–	A	LCDC_HSYNC	O	1	PIO, I, PU, ST
							C	FLEXCOM1_IO3	I/O	1	
G8	VDDIOP1	GPIO	PC29	I/O	–	–	A	LCDC_DEN	O	1	PIO, I, PU, ST
							C	FLEXCOM1_IO2	I/O	1	
C7	VDDIOP1	GPIO	PC30	I/O	–	–	A	LCDC_PCK	O	1	PIO, I, PU, ST
							C	FLEXCOM3_IO7	I	1	
D9	VDDIOP1	GPIO	PC31	I/O	WKUP11	–	A	FIQ	I	1	PIO, I, PU, ST
						–	C	PCK1	O	2	
P15	VDDNF	GPIO	PD0	I/O	–	–	A	NANDOE	O	1	PIO, I, PU
							C	FLEXCOM7_IO2	I/O	1	
R17	VDDNF	GPIO	PD1	I/O	–	–	A	NANDWE	O	1	PIO, I, PU
							C	FLEXCOM7_IO3	I/O	1	
P17	VDDNF	GPIO	PD2	I/O	–	–	A	A21/NANDALE	O	1	A21,O, PD
							C	FLEXCOM7_IO4	O	1	
T17	VDDNF	GPIO	PD3	I/O	–	–	A	A22/NANDCLE	O	1	A22,O, PD
							C	FLEXCOM11_IO2	I/O	1	
P14	VDDNF	GPIO	PD4	I/O	–	–	A	NCS2/NANDCS	O	1	PIO, I, PU
							C	FLEXCOM11_IO3	I/O	1	
U16	VDDNF	GPIO	PD5	I/O	–	–	A	–			PIO, I, PU
							B	NCS0	O	1	
							C	FLEXCOM11_IO4	O	1	
R15	VDDNF	GPIO	PD6	I/O	–	–	A	NANDDAT0	I/O	1	PIO, I, PU
							B	A1	O	1	
T15	VDDNF	GPIO	PD7	I/O	–	–	A	NANDDAT1	I/O	1	PIO, I, PU
							B	A12	O	1	
U15	VDDNF	GPIO	PD8	I/O	–	–	A	NANDDAT2	I/O	1	PIO, I, PU
							B	A19	O	1	
R13	VDDNF	GPIO	PD9	I/O	–	–	A	NANDDAT3	I/O	1	PIO, I, PU
							B	A20	O	1	
T13	VDDNF	GPIO	PD10	I/O	–	–	A	NANDDAT4	I/O	1	PIO, I, PU
							B	NRD	O	1	
T14	VDDNF	GPIO	PD11	I/O	–	–	A	NANDDAT5	I/O	1	PIO, I, PU
							B	NWR0/NWE	O	1	
U14	VDDNF	GPIO	PD12	I/O	–	–	A	NANDDAT6	I/O	1	PIO, I, PU
							B	A0/NBS0	O	1	
P13	VDDNF	GPIO	PD13	I/O	–	–	A	NANDDAT7	I/O	1	PIO, I, PU
							B	NWR1/NBS1	O	1	

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256-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
U13	VDDNF	GPIO	PD14	I/O	–	–	A	NWAIT/NANDRDY	I	1	PIO, I, PU
G14	VDDIOM	power	VDDIOM	I	–	–	–	–	–	–	–
J11	VDDIOM	power	VDDIOM	I	–	–	–	–	–	–	–
K11	VDDIOM	power	VDDIOM	I	–	–	–	–	–	–	–
K14	VDDIOM	power	VDDIOM	I	–	–	–	–	–	–	–
D4	VDDMIPI	power	VDDMIPI	I	–	–	–	–	–	–	–
E9	VDDLVDS	power	VDDLVDS	I	–	–	–	–	–	–	–
R16	VDDNF	power	VDDNF	I	–	–	–	–	–	–	–
R8	VDDIOP0	power	VDDIOP0	I	–	–	–	–	–	–	–
D8	VDDIOP1	power	VDDIOP1	I	–	–	–	–	–	–	–
T11	VDDIOP2	power	VDDIOP2	I	–	–	–	–	–	–	–
C12	VDDQSPI	power	VDDQSPI	I	–	–	–	–	–	–	–
U2	VDDBU	power	VDDBU	I	–	–	–	–	–	–	–
P5	VDDBU	power	VDDBU	I	–	–	–	–	–	–	–
K4	VDDANA	power	VDDANA	I	–	–	–	–	–	–	–
M3	GNDANA	ground	GNDANA	I	–	–	–	–	–	–	–
C8	VDDOUT25	power	VDDOUT25	I	–	–	–	–	–	–	–
G5	VDDIN33	power	VDDIN33	I	–	–	–	–	–	–	–
K3	VDDIN33	power	VDDIN33	I	–	–	–	–	–	–	–
D6	VDDCORE	power	VDDCORE	I	–	–	–	–	–	–	–
E5	VDDCORE	power	VDDCORE	I	–	–	–	–	–	–	–
F5	VDDCORE	power	VDDCORE	I	–	–	–	–	–	–	–
F13	VDDCORE	power	VDDCORE	I	–	–	–	–	–	–	–
F14	VDDCORE	power	VDDCORE	I	–	–	–	–	–	–	–
A1	GND	ground	GND	I	–	–	–	–	–	–	–
J3	GND	ground	GND	I	–	–	–	–	–	–	–
D10	GND	ground	GND	I	–	–	–	–	–	–	–
H3	GND	ground	GND	I	–	–	–	–	–	–	–
L1	GND	ground	GND	I	–	–	–	–	–	–	–
H4	GND	ground	GND	I	–	–	–	–	–	–	–
F3	GND	ground	GND	I	–	–	–	–	–	–	–
D13	GND	ground	GND	I	–	–	–	–	–	–	–
E4	GND	ground	GND	I	–	–	–	–	–	–	–
G11	GND	ground	GND	I	–	–	–	–	–	–	–
H5	GND	ground	GND	I	–	–	–	–	–	–	–
G10	GND	ground	GND	I	–	–	–	–	–	–	–
E10	GND	ground	GND	I	–	–	–	–	–	–	–

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256-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
E8	GND	ground	GND	I	–	–	–	–	–	–	–
G13	GND	ground	GND	I	–	–	–	–	–	–	–
H11	GND	ground	GND	I	–	–	–	–	–	–	–
E13	GND	ground	GND	I	–	–	–	–	–	–	–
G2	GND	ground	GND	I	–	–	–	–	–	–	–
G1	GND	ground	GND	I	–	–	–	–	–	–	–
G9	GND	ground	GND	I	–	–	–	–	–	–	–
E3	GND	ground	GND	I	–	–	–	–	–	–	–
H13	GND	ground	GND	I	–	–	–	–	–	–	–
A17	GND	ground	GND	I	–	–	–	–	–	–	–
K13	GND	ground	GND	I	–	–	–	–	–	–	–
E15	VDDIOM	DDRIO	D0	–	–	–	–	–	–	–	O, PD
F16	VDDIOM	DDRIO	D1	–	–	–	–	–	–	–	O, PD
E16	VDDIOM	DDRIO	D2	–	–	–	–	–	–	–	O, PD
D15	VDDIOM	DDRIO	D3	–	–	–	–	–	–	–	O, PD
C17	VDDIOM	DDRIO	D4	–	–	–	–	–	–	–	O, PD
E14	VDDIOM	DDRIO	D5	–	–	–	–	–	–	–	O, PD
D16	VDDIOM	DDRIO	D6	–	–	–	–	–	–	–	O, PD
D17	VDDIOM	DDRIO	D7	–	–	–	–	–	–	–	O, PD
C15	VDDIOM	DDRIO	D8	–	–	–	–	–	–	–	O, PD
C16	VDDIOM	DDRIO	D9	–	–	–	–	–	–	–	O, PD
D14	VDDIOM	DDRIO	D10	–	–	–	–	–	–	–	O, PD
B16	VDDIOM	DDRIO	D11	–	–	–	–	–	–	–	O, PD
B15	VDDIOM	DDRIO	D12	–	–	–	–	–	–	–	O, PD
C14	VDDIOM	DDRIO	D13	–	–	–	–	–	–	–	O, PD
B14	VDDIOM	DDRIO	D14	–	–	–	–	–	–	–	O, PD
A14	VDDIOM	DDRIO	D15	–	–	–	–	–	–	–	O, PD
K16	VDDIOM	DDRIO	A2	–	–	–	–	–	–	–	O, PD
L15	VDDIOM	DDRIO	A3	–	–	–	–	–	–	–	O, PD
M16	VDDIOM	DDRIO	A4	–	–	–	–	–	–	–	O, PD
K15	VDDIOM	DDRIO	A5	–	–	–	–	–	–	–	O, PD
L16	VDDIOM	DDRIO	A6	–	–	–	–	–	–	–	O, PD
J15	VDDIOM	DDRIO	A7	–	–	–	–	–	–	–	O, PD
H16	VDDIOM	DDRIO	A8	–	–	–	–	–	–	–	O, PD
P16	VDDIOM	DDRIO	A9	–	–	–	–	–	–	–	O, PD
N15	VDDIOM	DDRIO	A10	–	–	–	–	–	–	–	O, PD
M15	VDDIOM	DDRIO	A11	–	–	–	–	–	–	–	O, PD

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256-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
N17	VDDIOM	DDRIO	A13	–	–	–	–	–	–	–	O, PD
N16	VDDIOM	DDRIO	A14	–	–	–	–	–	–	–	O, PD
H15	VDDIOM	DDRIO	A15	–	–	–	–	–	–	–	O, PD
G15	VDDIOM	DDRIO	A16	–	BA0	–	–	–	–	–	O, PD
G16	VDDIOM	DDRIO	A17	–	BA1	–	–	–	–	–	O, PD
F15	VDDIOM	DDRIO	A18	–	BA2	–	–	–	–	–	O, PD
J17	VDDIOM	DDRIO	NCS1	–	DDRCS	–	–	–	–	–	O, PU
L17	VDDIOM	DDRIO	SDCK	–	–	–	–	–	–	–	O, PD
M17	VDDIOM	DDRIO	SDCKN	–	–	–	–	–	–	–	O, PU
H17	VDDIOM	DDRIO	SDCKE	–	–	–	–	–	–	–	O, PU
J14	VDDIOM	DDRIO	RAS	–	–	–	–	–	–	–	O, PU
J16	VDDIOM	DDRIO	CAS	–	–	–	–	–	–	–	O, PU
J13	VDDIOM	DDRIO	SDWE	–	–	–	–	–	–	–	O, PU
L13	VDDIOM	DDRIO	SDA10	–	–	–	–	–	–	–	O, PU
E17	VDDIOM	DDRIO	DQM0	–	–	–	–	–	–	–	O, PU
B17	VDDIOM	DDRIO	DQM1	–	–	–	–	–	–	–	O, PU
G17	VDDIOM	DDRIO	DQS0	–	–	–	–	–	–	–	O, PD
F17	VDDIOM	DDRIO	NDQS0	–	–	–	–	–	–	–	O, PU
A16	VDDIOM	DDRIO	DQS1	–	–	–	–	–	–	–	O, PD
A15	VDDIOM	DDRIO	NDQS1	–	–	–	–	–	–	–	O, PU
M14	VDDIOM	analog	DDR_CAL	I	–	–	–	–	–	–	I
K17	VDDIOM	analog	DDR_VREF	I	–	–	–	–	–	–	I
H14	VDDIOM	DDRIO	RESETN	–	–	–	–	–	–	–	O
N1	VDDANA	analog	ADVREFP	–	–	–	–	–	–	–	I
N2	VDDANA	analog	ADVREFN	–	–	–	–	–	–	–	I
M2	VDDIN33	USBHS	HHSRTUNE	–	–	–	–	–	–	–	I
H2	VDDIN33	USBHS	HHSDPA	–	DHSDP	–	–	–	–	–	O, PD
H1	VDDIN33	USBHS	HHSDMA	–	DHSDM	–	–	–	–	–	O, PD
J2	VDDIN33	USBHS	HHSDPB	–	–	–	–	–	–	–	O, PD
J1	VDDIN33	USBHS	HHSDMB	–	–	–	–	–	–	–	O, PD
K2	VDDIN33	USBHS	HHSDPC	–	–	–	–	–	–	–	O, PD
K1	VDDIN33	USBHS	HHSDMC	–	–	–	–	–	–	–	O, PD
T3	VDDBU	GPIO	WKUP0	–	–	–	–	–	–	–	I, ST
H7	VDDBU	GPIO	SHDN	–	–	–	–	–	–	–	O, PD
P1	VDDBU	GPIO	JTAGSEL	–	–	–	–	–	–	–	I, PD
R1	VDDBU	GPIO	TST	–	–	–	–	–	–	–	I, PD, ST
L7	VDDIOP0	GPIO	TCK	–	–	–	–	–	–	–	I, ST

.....continued

256-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
J7	VDDIOP0	GPIO	TDI	–	–	–	–	–	–	–	I, ST
N6	VDDIOP0	GPIO	TDO	–	–	–	–	–	–	–	O
R2	VDDIOP0	GPIO	TMS	–	–	–	–	–	–	–	I, ST
R3	VDDIOP0	GPIO	RTCK	–	–	–	–	–	–	–	O
M5	VDDIOP0	GPIO	NRST	–	–	–	–	–	–	–	I, PU, ST
T1	VDDBU	CLOCK	XIN32	–	–	–	–	–	–	–	I
T2	VDDBU	CLOCK	XOUT32	–	–	–	–	–	–	–	O
G3	VDDIN33	CLOCK	XIN	–	–	–	–	–	–	–	I
G4	VDDIN33	CLOCK	XOUT	–	–	–	–	–	–	–	O
B1	VDDMIPI	analog	MIPI_DN0	I/O	–	–	–	–	–	–	HiZ(1)
B2	VDDMIPI	analog	MIPI_DP0	I/O	–	–	–	–	–	–	HiZ(1)
C1	VDDMIPI	analog	MIPI_DN1	I/O	–	–	–	–	–	–	HiZ(1)
C2	VDDMIPI	analog	MIPI_DP1	I/O	–	–	–	–	–	–	HiZ(1)
E1	VDDMIPI	analog	MIPI_DN2	I/O	–	–	–	–	–	–	HiZ(1)
E2	VDDMIPI	analog	MIPI_DP2	I/O	–	–	–	–	–	–	HiZ(1)
F1	VDDMIPI	analog	MIPI_DN3	I/O	–	–	–	–	–	–	HiZ(1)
F2	VDDMIPI	analog	MIPI_DP3	I/O	–	–	–	–	–	–	HiZ(1)
D1	VDDMIPI	analog	MIPI_CLKN	O	–	–	–	–	–	–	HiZ(1)
D2	VDDMIPI	analog	MIPI_CLKP	O	–	–	–	–	–	–	HiZ(1)
F4	VDDMIPI	analog	MIPI_REXT	I	–	–	–	–	–	–	I(1)
L4	VDDANA	GPIO	AUDIOCLK	–	–	–	–	–	–	–	O
L10	VDDCORE	power	VDDCORE	I	–	–	–	–	–	–	–
L11	VDDCORE	power	VDDCORE	I	–	–	–	–	–	–	–
J4	VDDOUT25	power	VDDOUT25	I	–	–	–	–	–	–	–
L2	VDDANA	power	VDDANA	I	–	–	–	–	–	–	–
M1	VDDANA	power	VDDANA	I	–	–	–	–	–	–	–
N14	VDDIOM	power	VDDIOM	I	–	–	–	–	–	–	–
L3	GND	ground	GND	I	–	–	–	–	–	–	–
L9	GND	ground	GND	I	–	–	–	–	–	–	–
L14	GND	ground	GND	I	–	–	–	–	–	–	–
M13	GND	ground	GND	I	–	–	–	–	–	–	–
N8	GND	ground	GND	I	–	–	–	–	–	–	–
N11	GND	ground	GND	I	–	–	–	–	–	–	–
N13	GND	ground	GND	I	–	–	–	–	–	–	–
P6	GND	ground	GND	I	–	–	–	–	–	–	–
R9	GND	ground	GND	I	–	–	–	–	–	–	–
R14	GND	ground	GND	I	–	–	–	–	–	–	–

.....continued

256-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
T16	GND	ground	GND	I	–	–	–	–	–	–	–
U1	GND	ground	GND	I	–	–	–	–	–	–	–
U17	GND	ground	GND	I	–	–	–	–	–	–	–

Note:

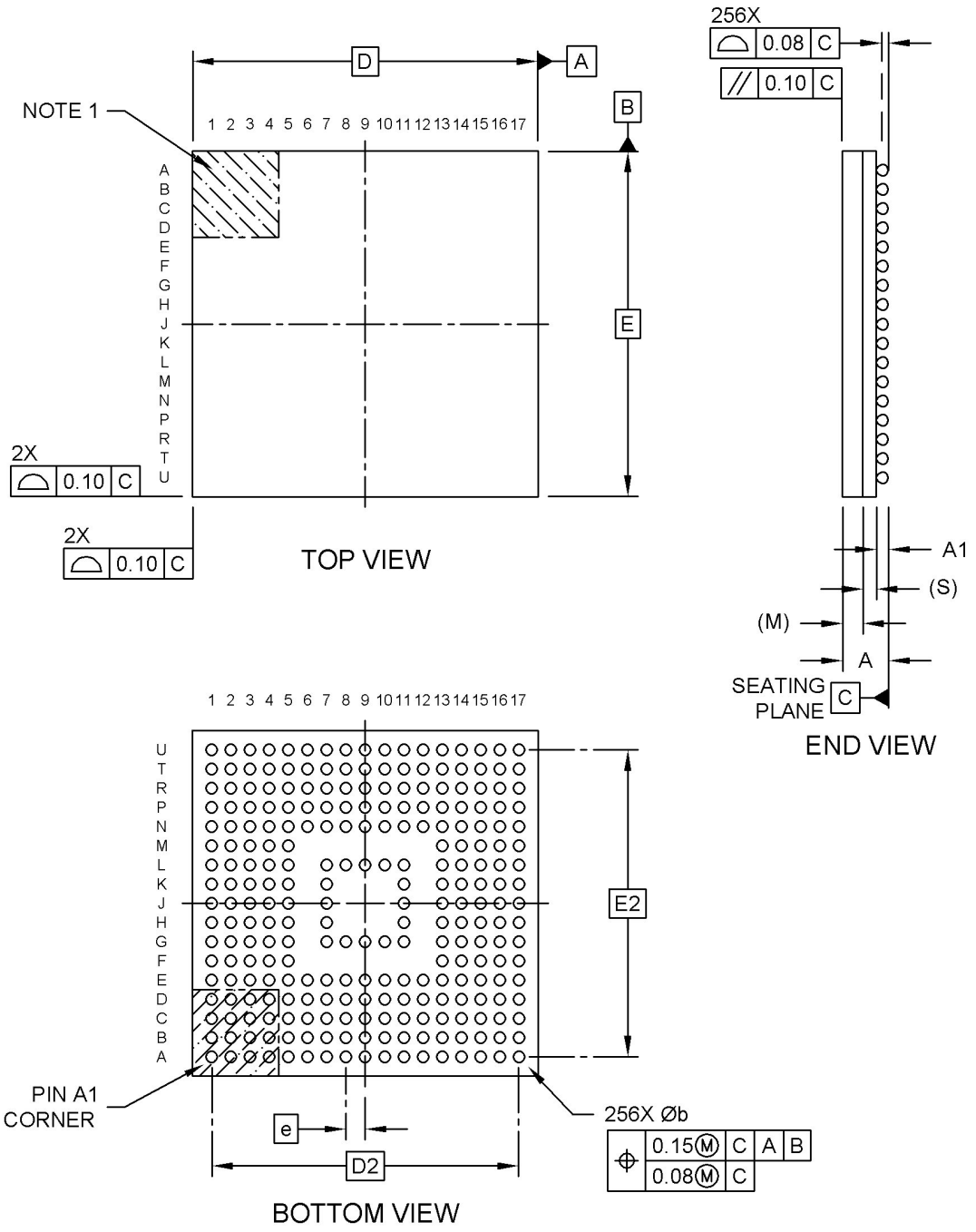
1. On SAM9X70 and SAM9X72: to be tied to GND.

5. Mechanical Characteristics

Figure 5-1. 256-Ball TFBGA Mechanical Characteristics

256-Ball Thin Fine-Pitch Ball Grid Array Package (6GW) - 9x9x1.2 mm Body [TFBGA]

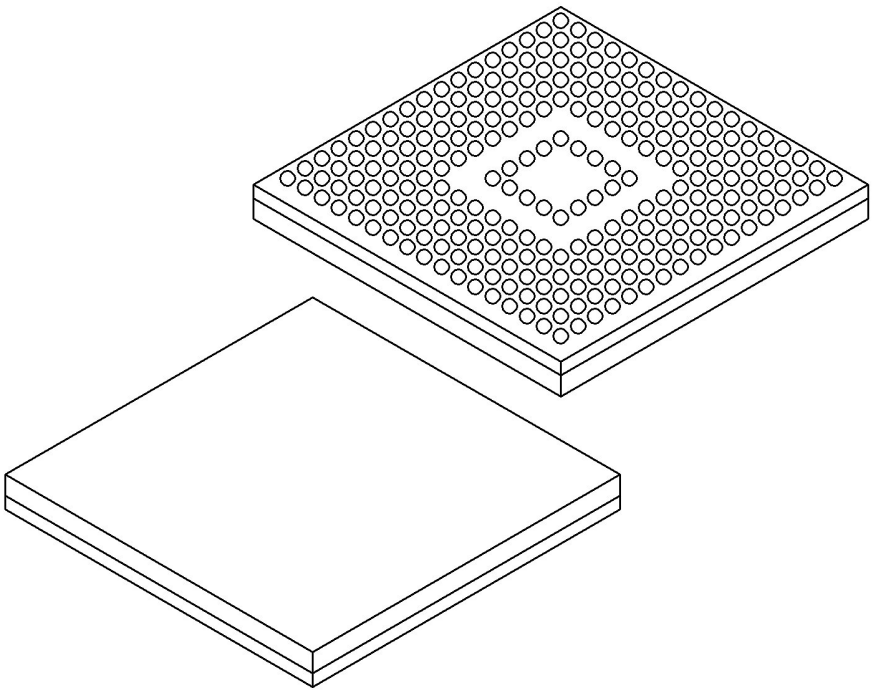
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-622 Rev A Sheet 1 of 2

256-Ball Thin Fine-Pitch Ball Grid Array Package (6GW) - 9x9x1.2 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		256	
Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Ball Height	A1	0.16	0.21	0.26
Mold Thickness	M		0.53 REF	
Substrate Thickness	S		0.35 REF	
Overall Length	D		9.00 BSC	
Ball Array Length	D2		8.00 BSC	
Overall Width	E		9.00 BSC	
Ball Array Width	E2		8.00 BSC	
Ball Diameter	b	0.27	0.32	0.37

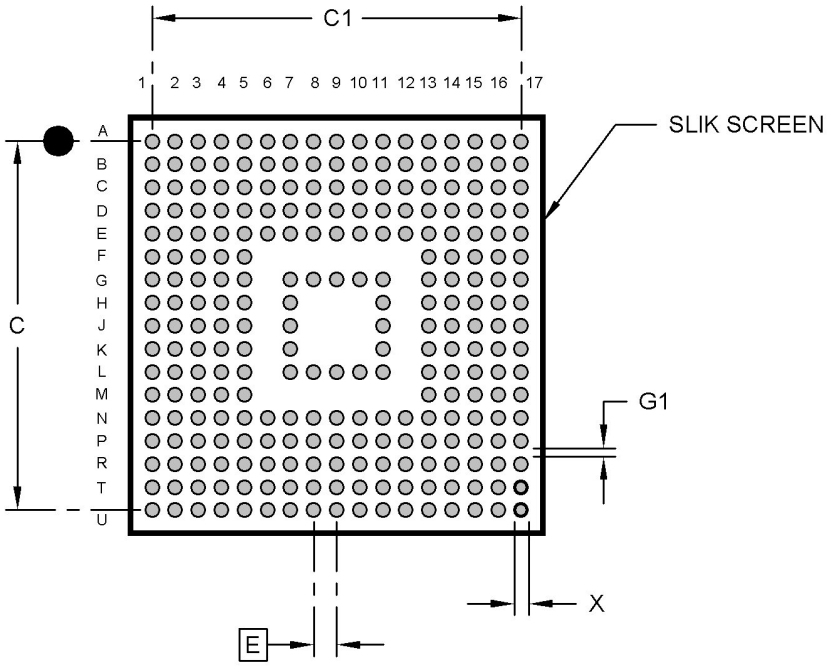
Notes:

1. Pin 1 visual index feature may vary but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-622 Rev A Sheet 2 of 2

256-Ball Thin Fine-Pitch Ball Grid Array Package (6GW) - 9x9x1.2 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Diameter (X256)	X			0.25
Contact Pad to Contact Pad	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2622 Rev A

Table 5-1. 256-ball TFBGA Package Characteristics

Moisture sensitivity level	MSL3

Table 5-2. Device and 256-ball TFBGA Package Weight

182	mg

Table 5-3. 256-ball TFBGA Package Reference

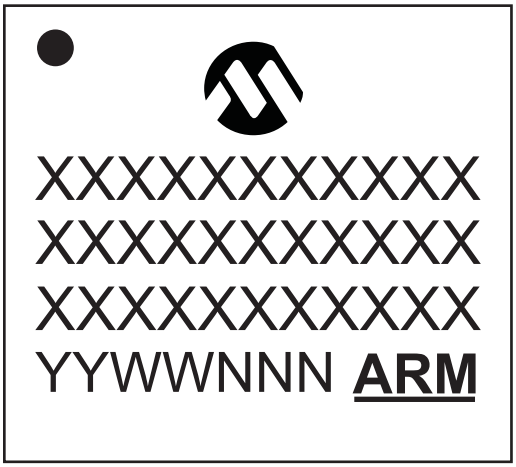
JEDEC drawing reference	N/A
J-STD-609 classification	e8

Table 5-4. 256-ball TFBGA Package Information

Ball land	0.400 mm
Nominal ball diameter	0.320 mm
Solder mask opening	0.275 mm
Solder mask definition	Solder Mask Defined (SMD)
Solder	LF35

6. Marking

Top marking follows the scheme below:



with possible values:

Line	Description	Values
1	Company logo	Microchip logo
2	Company name	Microchip
3	Device name	SAM9X75
4	Temperature code/Packaging code, Jedec symbol	V/6GW e8
5	Lot traceability, Arm logo	YYWWNNN ARM

7. Ordering Information

For details on ordering codes, refer to Product Identification System.

Ordering Code	Package	Ambient Operating Temperature Range
SAM9X70(T)-V/6GW	TFBGA256 9x9 mm, 0.5 mm pitch	-40°C to 105°C
SAM9X72(T)-V/6GW		
SAM9X75(T)-V/6GW		

8. Revision History

8.1 Rev. A - 10/2024

Changes
Preliminary issue

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- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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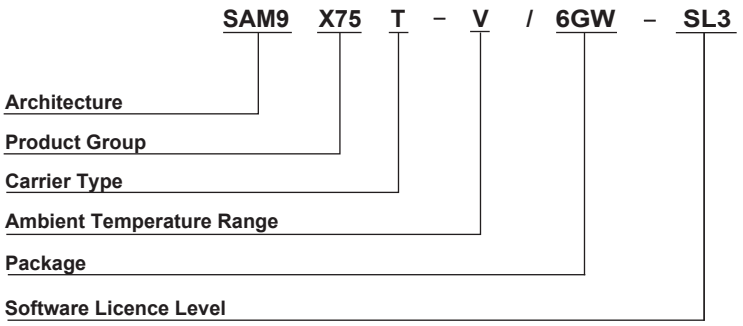
Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Architecture:	SAM9	= Arm926EJ-S Arm Thumb microprocessor
Product Group:	X70	= General purpose microprocessors with variable feature set
	X72	
	X75	
Carrier Type:	Blank	= Standard packaging (tray)
	T	= Tape and reel
Ambient Temperature Range:	V	= –40°C to +105°C
Package:	6GW	= TFBGA256
Software Licence Level:	Blank	= Level 0
	SLn	= Level n

Example:

- SAM9X75T-V/6GW-SL3 = Arm926EJ-S Arm Thumb microprocessor, tape and reel, –40°C to +105°C ambient temperature range, 256-ball TFBGA package, Software Licence Level 3

Notes:

1. The Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.

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