SAM9X75 MPU, up to 2-Gbit DDR3L SDRAM, up to 4-Gbit NAND Flash, Gigabit Ethernet PHY, Power Management IC, 64-Mbit Serial Quad I/O Flash

SAM9X75 SOM Series

Introduction

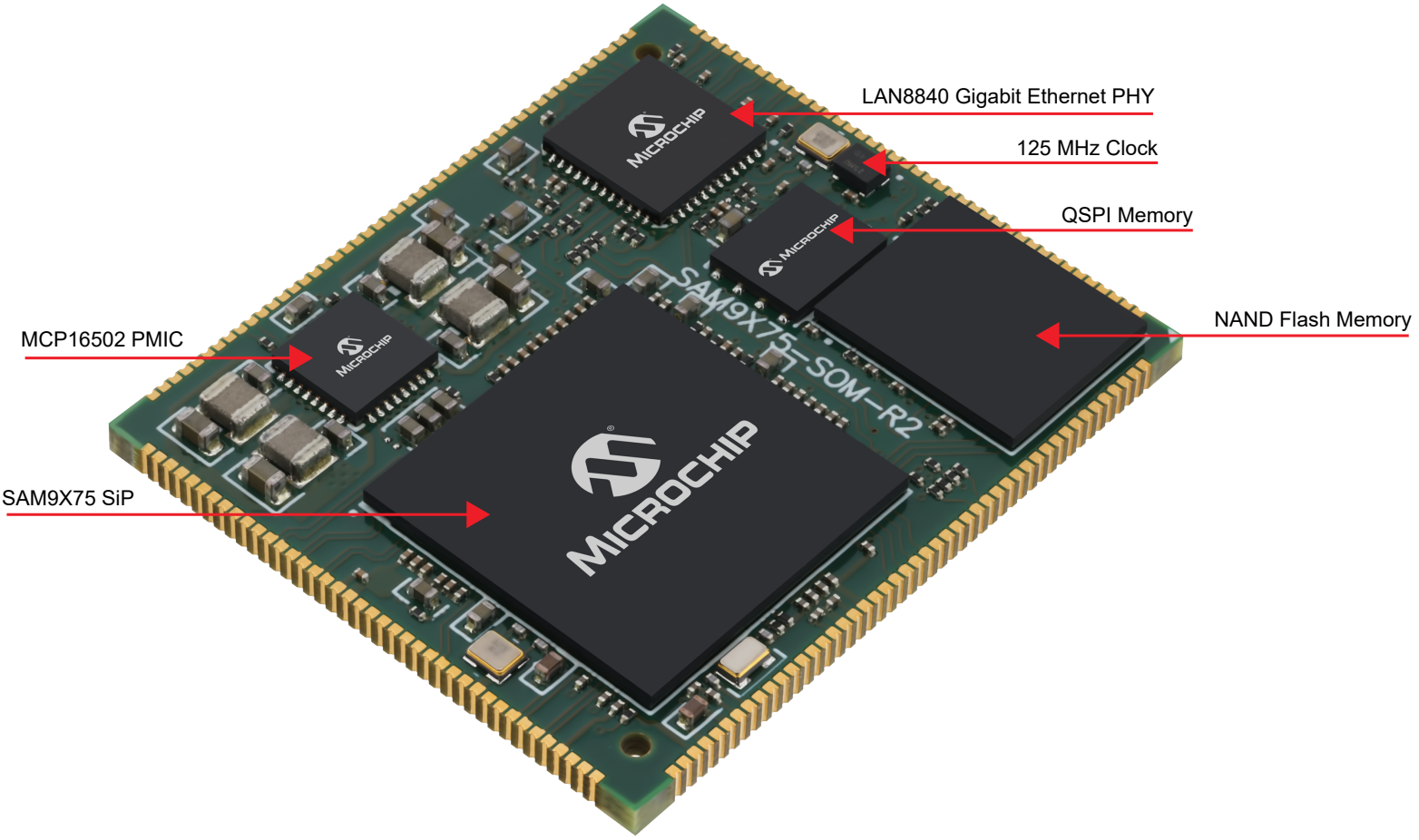
The Microchip SAM9X75 System-On-Module Series is a small single-sided SOM series based on a System-in-Package (SiP) ARM926EJ-S Arm® Thumb® CPU-based embedded microprocessor running up to 800 MHz.

The SAM9X75 SOM Series is built on a common set of proven Microchip components to reduce time to market by simplifying hardware design and software development.

The SOM embeds a SAM9X75 SiP microprocessor with a 1-Gbit or 2-Gbit DDR3L SDRAM, a 2-Gbit or 4-Gbit NAND Flash memory, a Gigabit Ethernet PHY, a 64-Mbit serial Quad I/O Flash memory and a dedicated Power Management Unit.

The SAM9X75 SOM Series also limits design rules of the main application board, reducing overall PCB complexity and cost. The SAM9X75 SOM Series is supported by a free Linux® distribution and bare metal C examples.

Figure 1. SAM9X75 SOM Series Overview



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1. Features

- SAM9X75 System-in-Package including:
  - ARM926EJ-S Arm Thumb processor-based SAM9X75 MPU running up to 800 MHz
  - Up to 2-Gbit DDR3L
- Up to 4-Gbit NAND Flash Memory
- 64-Mbit Serial Quad I/O Flash Memory (SST26VF064BEUIT-104I/MF) with Embedded EUI-48™ and EUI-64™ MAC Addresses
- On-Board Power Management Unit (MCP16502TAB-E/S8B)
- Gigabit Ethernet Transceiver (LAN8840T-V/PSA)
- 24-MHz Crystal Oscillator for microprocessor main clock generation
- 25-MHz Crystal Oscillator and 125-MHz MEMS Oscillator (DSC1501MI2A-125.0000) for Ethernet clock generation
- 32.768-kHz Crystal Oscillator for slow clock generation
- One High-Speed USB Device, three High-Speed USB Hosts with dedicated on-chip transceivers
- Shutdown and Reset Control Pins
- Up to 67 I/Os
- Independent Power Supplies available for SD Cards, RGB LCD, LVDS Display, Camera Sensor and Backup depending on voltage domains
- Operational Conditions:
  - Main operating voltage (5V_MAIN): 3.3V to 5.5V ±5%
  - Module ambient temperature range (T_A) range: –40°C to +85°C
- Package:
  - 35x30 mm 174-pin 0.65 mm Pad Pitch Module, manually solderable for prototyping

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2. Applications

- Industrial Control and Automation
- Smart Appliances
- Human Machine Interfaces (HMI)
- IoT Gateways
- Access Control Panels
- Security and Alarm Systems

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3. Reference Documents

The following reference data sheets are available.

Document Title	Available	Literature No.
SAM9X75 SiP	www.microchip.com	DS60001827
LAN8840	www.microchip.com	DS00004727
DSC150X	www.microchip.com	DS20006516
SST26VF064BEUI	www.microchip.com	DS20006138
MCP16502	www.microchip.com	DS20006275
MX30LF2G28AD-XKI(1)	www.mxic.com.tw	PM2579
MT29F2G08ABAEAH4-IT:G(1)	www.micron.com	–
MX30LF4G28AD-XKI(2)	www.mxic.com.tw	PM2579
MT29F4G08ABAFAH4-IT:F(2)	www.micron.com	–

Notes:

1. 2-Gbit NAND Flash memory
2. 4-Gbit NAND Flash memory

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4. Description

The SAM9X75 SOM Series is a high-performance System-On-Module series based on the ultra-low power ARM926EJ-S CPU-based embedded microprocessor (MPU) SAM9X75. The SAM9X75 SOM Series is certified for industrial operating conditions over the [-40°C to 85°C] industrial ambient temperature range.

The SAM9X75 SOM Series operates at a maximum CPU operating frequency of 800 MHz and a maximum bus speed of 266 MHz and offers the following features:

- DDRx SDRAM memory with one of the following configurations:
  - 1-Gbit DDR3L SDRAM memory size (SAM9X75D1G-I/4TB)
  - 2-Gbit DDR3L SDRAM memory size (SAM9X75D2G-I/4TB)
- 8-bit NAND Flash memory with one of the following configurations:
  - 2-Gbit memory size (MX30LF2G28AD-XKI or MT29F2G08ABAEAH4-IT:G)[(1)]
  - 4-Gbit memory size (MX30LF4G28AD-XKI or MT29F4G08ABAFAH4-IT:F)[(2)]
- 64 Mbits of Serial Quad I/O (SQI) Flash memory with EUI (SST26VF064BEUIT-104I/MF)
- A Gigabit Ethernet transceiver (LAN8840T-V/PSA)

The SAM9X75 SOM Series device is a 35x30 mm 174-pin 0.65 mm Pad Pitch Module.

The device offers an extensive peripheral set, system control and up to 67 I/Os featuring:

- Up to 12 Flexible Serial Communication Controllers (FLEXCOM)
  - Universal Synchronous Asynchronous Receiver Transceiver (USART)
  - Two-Wire Interface (TWI)
  - Serial Peripheral Interface (SPI)
- Up to six 12-bit ADC inputs, with a maximum of 1-Msps conversion rate
- Up to two CAN(FD) interfaces compliant with CAN Protocol version 2.0 Part A, B and ISO 11898-1
- Up to two SDMMC interfaces (MultiMedia Card/e.MMC) compliant with Specification V4.51, SD Memory Card Specification V3.0 and SDIO Specification V3.0
- Up to four PWM interfaces
- Serial interfaces such as SSC and I²S
- 4-lane LVDS or MIPI DSI® interface
- 4-lane CSI-2 camera interface
- Half-bridge class-D stereo

Notes:

1. Only available with 1-Gbit DDR3L SDRAM memory size (SAM9X75D1G-I/4TB).
2. Only available with 2-Gbit DDR3L SDRAM memory size (SAM9X75D2G-I/4TB).

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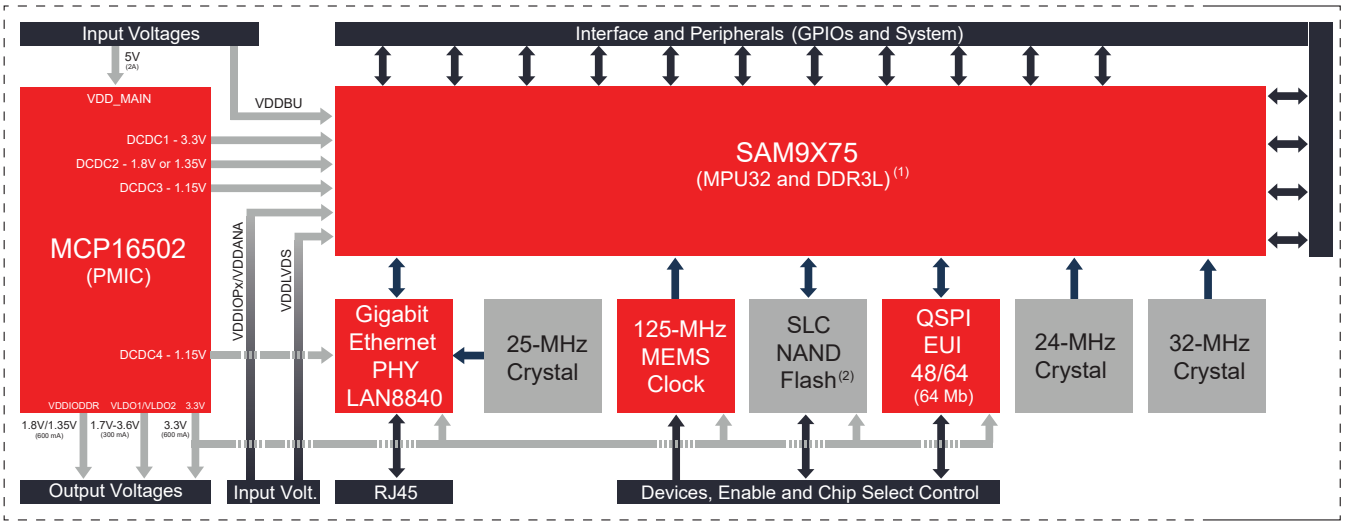
5. Block Diagram

Figure 5-1. SAM9X75 SOM Series Block Diagram



Notes:

1. Several DDRx memory sizes are available depending on the memory configuration.
2. Several NAND Flash memory sizes are available depending on the memory configuration.

For more details, see Ordering Information.

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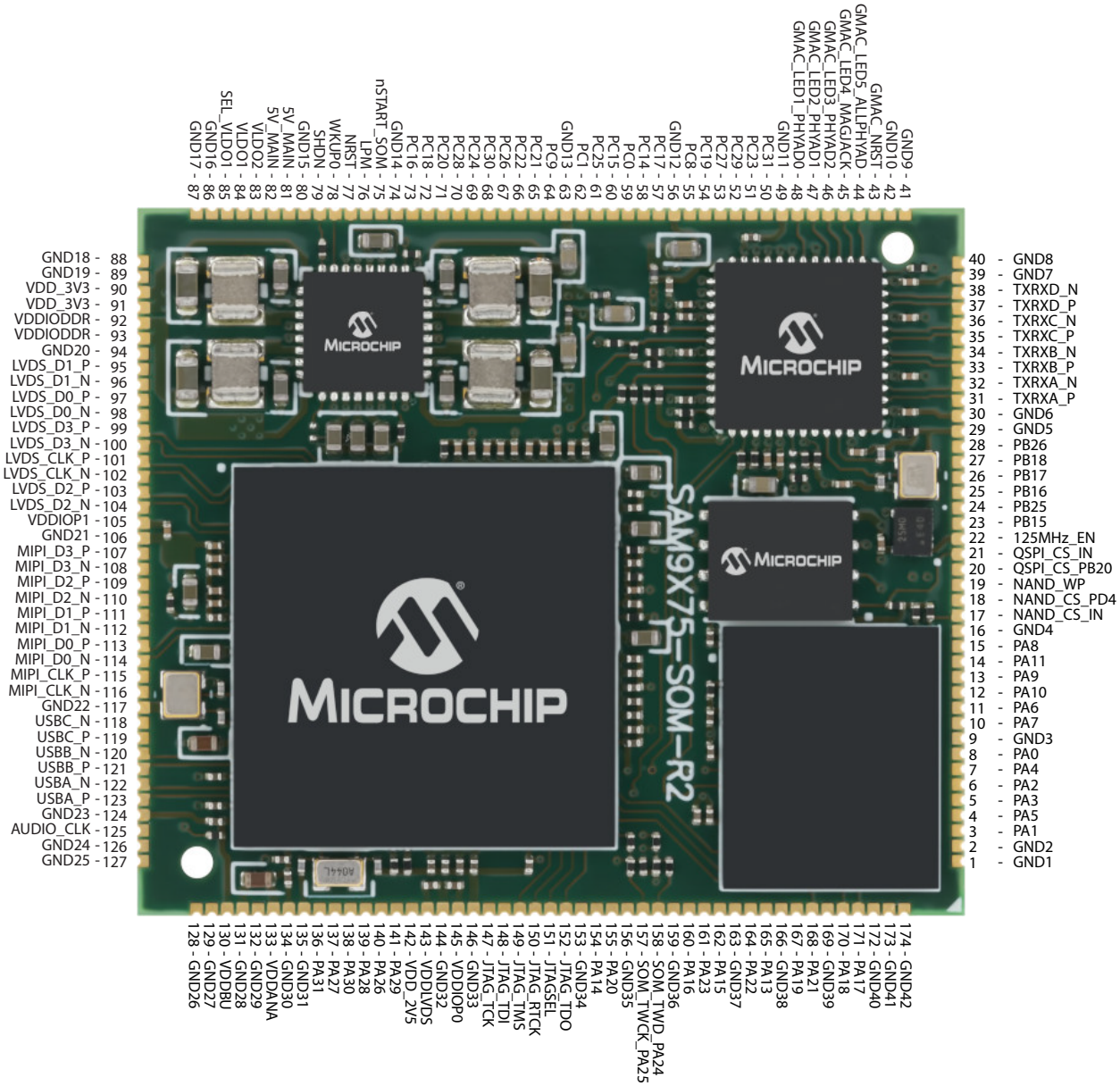
6. Pinout

6.1 Pinout Overview

Figure 6-1. SAM9X75 SOM Series Pin Assignment



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6.2 Pin List

The following tables provide the SAM9X75 SOM Series module pin descriptions.

Important: Compared to the SAM9X75 SiP device, some PIO features are not listed. These features are used internally on the SAM9X75 SOM Series and cannot have other uses.

The device features several PIO controllers that multiplex the I/O lines of the peripheral set. The following PIOx Pin Description tables define how the I/O lines are multiplexed on the different PIO controllers. The "Reset State" column shows whether the PIO line resets in I/O mode or in Peripheral mode. If I/O is shown, the PIO line resets with the characteristics (input, output, pull-up or pull-down) indicated in this same column, so that the device is configured in a known state as soon as the reset is released. As a result, PIO_CFGR.FUNC resets to '0'. If a signal name is shown in the "Reset State" column, the PIO line is assigned to this function and PIO_CFGR.FUNC is not set to '0'. That is the case for pins controlling memories, in particular address lines, which require the pin to be driven as soon as the reset is released.

6.2.1 PIOA Pin List

Table 6-1. PIOA Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State[1]	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
8	VDDIOP0	GPIO	PA0	GPIO	–	A	SDMMC0_DAT0	1	PIO, I, PU, ST	–
3	VDDIOP0	GPIO	PA1	GPIO	–	A	SDMMC0_CMD	1	PIO, I, PU, ST	–
6	VDDIOP0	GPIO	PA2	GPIO	WKUP1	A	SDMMC0_CK	1	PIO, I, PU, ST	–
5	VDDIOP0	GPIO	PA3	GPIO	–	A	SDMMC0_DAT1	1	PIO, I, PU, ST	–
7	VDDIOP0	GPIO	PA4	GPIO	–	A	SDMMC0_DAT2	1	PIO, I, PU, ST	–
4	VDDIOP0	GPIO	PA5	GPIO	–	A	SDMMC0_DAT3	1	PIO, I, PU, ST	–
11	VDDIOP0	GPIO	PA6	GPIO	–	A	FLEXCOM0_IO4	1	PIO, I, PU, ST	–
						B	SDMMC1_DAT1	1		
10	VDDIOP0	GPIO	PA7	GPIO	WKUP2	A	FLEXCOM0_IO3	1	PIO, I, PU, ST	–
						B	SDMMC1_DAT2	1		
15	VDDIOP0	GPIO	PA8	GPIO	WKUP3	A	FLEXCOM0_IO2	1	PIO, I, PU, ST	–
						B	SDMMC1_DAT3	1		
13	VDDIOP0	GPIO	PA9	GPIO	–	A	FLEXCOM4_IO1	1,2	PIO, I, PU, ST	–
						B	SDMMC1_DAT0	1		
12	VDDIOP0	GPIO	PA10	GPIO	–	A	FLEXCOM4_IO0	1,2	PIO, I, PU, ST	–
						B	SDMMC1_CMD	1		
14	VDDIOP0	GPIO	PA11	GPIO	–	A	FLEXCOM4_IO2	1,2	PIO, I, PU, ST	–
						B	SDMMC1_CK	1		
–	VDDIOP0	GPIO	PA12	GPIO	–	–	–	–	PIO, I, PU, ST	Used for PMIC interrupt[2]
165	VDDIOP0	GPIO	PA13	GPIO	–	A	FLEXCOM2_IO0	1	PIO, I, PU, ST	–
						B	FLEXCOM4_IO4	1		
154	VDDIOP0	GPIO	PA14	GPIO	–	A	FLEXCOM2_IO1	1	PIO, I, PU, ST	–
						B	FLEXCOM5_IO3	1,2		
						C	FLEXCOM4_IO5	1		

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Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State[1]	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
162	VDDIOP0	GPIO	PA15	GPIO	–	A	TIOA0	1	PIO, I, PU, ST	–
						B	FLEXCOM5_IO1	1,2		
						C	CLASSD_R0	1		
160	VDDIOP0	GPIO	PA16	GPIO	–	A	TIOA1	1	PIO, I, PU, ST	–
						B	FLEXCOM5_IO0	1,2		
						C	CLASSD_R1	1		
171	VDDIOP0	GPIO	PA17	GPIO	–	A	TIOA2	1	PIO, I, PU, ST	–
						B	FLEXCOM5_IO2	1,2		
						C	CLASSD_R2	1		
170	VDDIOP0	GPIO	PA18	GPIO	–	A	TCLK0	1	PIO, I, PU, ST	–
						B	TK	1		
						C	CLASSD_L0	1		
167	VDDIOP0	GPIO	PA19	GPIO	–	A	TCLK1	1	PIO, I, PU, ST	–
						B	TF	1		
						C	CLASSD_L1	1		
155	VDDIOP0	GPIO	PA20	GPIO	WKUP4	A	TCLK2	1	PIO, I, PU, ST	–
						B	TD	1		
						C	CLASSD_L2	1		
168	VDDIOP0	GPIO	PA21	GPIO	–	A	TIOB0	1	PIO, I, PU, ST	–
						B	RD	1		
						C	CLASSD_L3	1		
164	VDDIOP0	GPIO	PA22	GPIO	–	A	TIOB1	1	PIO, I, PU, ST	–
						B	RK	1		
						C	CLASSD_R3	1		
161	VDDIOP0	GPIO	PA23	GPIO	–	A	TIOB2	1	PIO, I, PU, ST	–
						B	RF	1		
						C	FLEXCOM2_IO7	1		
158	VDDANA	GPIO	PA24	GPIO	–	A	FLEXCOM6_IO0	1	PIO, I, PU, ST	Used for TWI PMIC[2]
157	VDDANA	GPIO	PA25	GPIO	–	A	FLEXCOM6_IO1	1	PIO, I, PU, ST	Used for TWI PMIC[2]
140	VDDANA	GPIO	PA26	GPIO	AD2	A	DRXD	1	PIO, I, PU, ST	–
						B	CANRX0	1		
136	VDDANA	GPIO	PA27	GPIO	AD3	A	DTXD	1	PIO, I, PU, ST	–
						B	CANTX0	1		
139	VDDANA	GPIO	PA28	GPIO	AD4	A	FLEXCOM1_IO0	1	PIO, I, PU, ST	–
						B	CANTX1	1		
141	VDDANA	GPIO	PA29	GPIO	AD5	A	FLEXCOM1_IO1	1	PIO, I, PU, ST	–
						B	CANRX1	1		
138	VDDANA	GPIO	PA30	GPIO	AD6	A	FLEXCOM0_IO0	1	PIO, I, PU, ST	–
						B	FLEXCOM5_IO4	2		
						C	FLEXCOM4_IO4	2		
136	VDDANA	GPIO	PA31	GPIO	AD7	A	FLEXCOM0_IO1	1	PIO, I, PU, ST	[3]
						B	FLEXCOM4_IO5	2		

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Notes:

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger
2. This feature is fixed due to the SAM9X75 SOM Series internal connection.
3. Compared to SAM9X75 SiP, this feature is limited, as it is partly used for other SAM9X75 SOM Series features, for example GMAC or FLEXCOM.

6.2.2 PIOB Pin List

Table 6-2. PIOB Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State[1]	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
–	VDD_3V3	GPIO	PB0	GPIO	–	A	GRX2	1	PIO, I, PU, ST	Used for Gigabit Ethernet[2]
–	VDD_3V3	GPIO	PB1	GPIO	–	A	GRX3	1	PIO, I, PU, ST	Used for Gigabit Ethernet[2]
–	VDD_3V3	GPIO	PB2	GPIO	–	A	G125CK	1	PIO, I, PU, ST	Used for Gigabit Ethernet[2]
–	VDD_3V3	GPIO	PB3	GPIO	–	A	GCRSDV/GRXCTL	1	PIO, I, PU, ST	Used for Gigabit Ethernet[2]
–	VDD_3V3	GPIO	PB4	GPIO	–	A	GTX2	1	PIO, I, PU, ST	Used for Gigabit Ethernet[2]
–	VDD_3V3	GPIO	PB5	GPIO	–	A	GTX3	1	PIO, I, PU, ST	Used for Gigabit Ethernet[2]
–	VDD_3V3	GPIO	PB6	GPIO	–	A	GTXCK/GREFCK	1	PIO, I, PU, ST	Used for Gigabit Ethernet[2]
–	VDD_3V3	GPIO	PB7	GPIO	–	A	GTXEN/GTXCTL	1	PIO, I, PU, ST	Used for Gigabit Ethernet[2]
–	VDD_3V3	GPIO	PB8	GPIO	–	A	GRXCK	1	PIO, I, PU, ST	Used for Gigabit Ethernet[2]
–	VDD_3V3	GPIO	PB9	GPIO	–	A	GMDIO	1	PIO, I, PU, ST	Used for Gigabit Ethernet[2]
–	VDD_3V3	GPIO	PB10	GPIO	–	A	GMDC	1	PIO, I, PU, ST	Used for Gigabit Ethernet[2]
–	VDD_3V3	GPIO	PB11	GPIO	–	A	GRX0	1	PIO, I, PU, ST	Used for Gigabit Ethernet[2]
–	VDD_3V3	GPIO	PB12	GPIO	–	A	GRX1	1	PIO, I, PU, ST	Used for Gigabit Ethernet[2]
–	VDD_3V3	GPIO	PB13	GPIO	–	A	GTX0	1	PIO, I, PU, ST	Used for Gigabit Ethernet[2]
–	VDD_3V3	GPIO	PB14	GPIO	–	A	GTX1	1	PIO, I, PU, ST	Used for Gigabit Ethernet[2]
23	VDD_3V3	GPIO	PB15	GPIO	–	C	FLEXCOM11_IO0	1	PIO, I, PU, ST	[3]
						D	I2SMCC_WS	1		
25	VDD_3V3	GPIO	PB16	GPIO	–	C	FLEXCOM11_IO1	1	PIO, I, PU, ST	[3]
						D	I2SMCC_DIN0	1		
26	VDD_3V3	GPIO	PB17	GPIO	–	C	FLEXCOM12_IO0	1	PIO, I, PU, ST	[3]
						D	I2SMCC_DOUT0	1		
27	VDD_3V3	GPIO	PB18	GPIO	WKUP7	B	ADTRG	1	PIO, I, PU, ST	[3]
						C	FLEXCOM12_IO1	1		
						D	IRQ	1		

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Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State[1]	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
–	VDD_3V3	GPIO	PB19	GPIO	–	A	QSCK	1	PIO, I, PU, ST	Used for QSPI memory[2]
20	VDD_3V3	GPIO	PB20	GPIO	–	A	QCS	1	PIO, I, PU, ST	Used for QSPI memory[2]
–	VDD_3V3	GPIO	PB21	GPIO	–	A	QIO0	1	PIO, I, PU, ST	Used for QSPI memory[2]
–	VDD_3V3	GPIO	PB22	GPIO	–	A	QIO1	1	PIO, I, PU, ST	Used for QSPI memory[2]
–	VDD_3V3	GPIO	PB23	GPIO	–	A	QIO2	1	PIO, I, PU, ST	Used for QSPI memory[2]
–	VDD_3V3	GPIO	PB24	GPIO	–	A	QIO3	1	PIO, I, PU, ST	Used for QSPI memory[2]
24	VDD_3V3	GPIO	PB25	GPIO	WKUP8	D	I2SMCC_MCK	1	PIO, I, PU, ST	[3]
28	VDD_3V3	GPIO	PB26	GPIO	–	D	I2SMCC_CK	1	PIO, I, PU, ST	[3]

Notes:

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger.
2. This feature is fixed due to the SAM9X75 SOM Series internal connection.
3. Compared to SAM9X75 SiP, this feature is limited, as it is partly used for other SAM9X75 SOM Series features, for example GMAC or FLEXCOM.

6.2.3 PIOC Pin List

Table 6-3. PIOC Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State[1]	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
59	VDDIOP1	GPIO	PC0	GPIO	–	A	LCDC_DAT0	1	PIO, I, PU, ST	–
						B	ISC_D0	1		
						C	FLEXCOM7_IO0	1		
62	VDDIOP1	GPIO	PC1	GPIO	–	A	LCDC_DAT1	1	PIO, I, PU, ST	–
						B	ISC_D1	1		
						C	FLEXCOM7_IO1	1		
98	VDDLVDS	GPIO	PC2	GPIO	LVDS_D0_N	A	LCDC_DAT2	1	PIO, I, PU, ST	For LVDS[2]
						B	ISC_D2	1		
						C	TIOA3	1		
97	VDDLVDS	GPIO	PC3	GPIO	LVDS_D0_P	A	LCDC_DAT3	1	PIO, I, PU, ST	For LVDS[2]
						B	ISC_D3	1		
						C	TIOB3	1		
96	VDDLVDS	GPIO	PC4	GPIO	LVDS_D1_N	A	LCDC_DAT4	1	PIO, I, PU, ST	For LVDS[2]
						B	ISC_D4	1		
						C	TCLK3	1		
95	VDDLVDS	GPIO	PC5	GPIO	LVDS_D1_P	A	LCDC_DAT5	1	PIO, I, PU, ST	For LVDS[2]
						B	ISC_D5	1		
						C	TIOA4	1		

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Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State[1]	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
104	VDDLVDS	GPIO	PC6	GPIO	LVDS_D2_N	A	LCDC_DAT6	1	PIO, I, PU, ST	For LVDS[2]
						B	ISC_D6	1		
						C	TIOB4	1		
103	VDDLVDS	GPIO	PC7	GPIO	LVDS_D2_P	A	LCDC_DAT7	1	PIO, I, PU, ST	For LVDS[2]
						B	ISC_D7	1		
						C	TCLK4	1		
55	VDDIOP1	GPIO	PC8	GPIO	–	A	LCDC_DAT8	1	PIO, I, PU, ST	–
						B	ISC_D8	1		
						C	FLEXCOM9_IO0	1		
64	VDDIOP1	GPIO	PC9	GPIO	–	A	LCDC_DAT9	1	PIO, I, PU, ST	–
						B	ISC_D9	1		
						C	FLEXCOM9_IO1	1		
102	VDDLVDS	GPIO	PC10	GPIO	LVDS_CLK_N	A	LCDC_DAT10	1	PIO, I, PU, ST	For LVDS[2]
						B	ISC_D10	1		
						C	PWM0	3		
101	VDDLVDS	GPIO	PC11	GPIO	LVDS_CLK_P	A	LCDC_DAT11	1	PIO, I, PU, ST	For LVDS[2]
						B	ISC_D11	1		
						C	PWM1	3		
100	VDDLVDS	GPIO	PC12	GPIO	LVDS_D3_N	A	LCDC_DAT12	1	PIO, I, PU, ST	For LVDS[2]
						B	ISC_PCK	1		
						C	TIOA5	1		
99	VDDLVDS	GPIO	PC13	GPIO	LVDS_D3_P	A	LCDC_DAT13	1	PIO, I, PU, ST	For LVDS[2]
						B	ISC_VSYNC	1		
						C	TIOB5	1		
58	VDDIOP1	GPIO	PC14	GPIO	–	A	LCDC_DAT14	1	PIO, I, PU, ST	–
						B	ISC_HSYNC	1		
						C	TCLK5	1		
60	VDDIOP1	GPIO	PC15	GPIO	–	A	LCDC_DAT15	1	PIO, I, PU, ST	–
						B	ISC_MCK	1		
						C	PCK0	2		
73	VDDIOP1	GPIO	PC16	GPIO	–	A	LCDC_DAT16	1	PIO, I, PU, ST	–
						B	ISC_FIELD	1		
						C	FLEXCOM10_IO0	1		
57	VDDIOP1	GPIO	PC17	GPIO	–	A	LCDC_DAT17	1	PIO, I, PU, ST	–
						B	FLEXCOM1_IO7	1		
						C	FLEXCOM10_IO1	1		
72	VDDIOP1	GPIO	PC18	GPIO	–	A	LCDC_DAT18	1	PIO, I, PU, ST	–
						B	FLEXCOM10_IO2	1		
						C	PWM0	1		
54	VDDIOP1	GPIO	PC19	GPIO	–	A	LCDC_DAT19	1	PIO, I, PU, ST	–
						B	FLEXCOM10_IO3	1		
						C	PWM1	1		

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Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State[1]	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
71	VDDIOP1	GPIO	PC20	GPIO	–	A	LCDC_DAT20	1	PIO, I, PU, ST	–
						B	FLEXCOM10_IO4	1		
						C	PWM2	1		
65	VDDIOP1	GPIO	PC21	GPIO	–	A	LCDC_DAT21	1	PIO, I, PU, ST	–
						C	PWM3	1		
66	VDDIOP1	GPIO	PC22	GPIO	–	A	LCDC_DAT22	1	PIO, I, PU, ST	–
						B	FLEXCOM3_IO0	1		
51	VDDIOP1	GPIO	PC23	GPIO	WKUP9	A	LCDC_DAT23	1	PIO, I, PU, ST	–
						B	FLEXCOM3_IO1	1		
69	VDDIOP1	GPIO	PC24	GPIO	WKUP10	A	LCDC_DISP	1	PIO, I, PU, ST	–
						B	FLEXCOM3_IO4	1		
61	VDDIOP1	GPIO	PC25	GPIO	WKUP12	A	NTRST	1	NRST_OUT, O, PD	–
						B	FLEXCOM3_IO3	1		
						C	NRST_OUT	1		
67	VDDIOP1	GPIO	PC26	GPIO	WKUP13	A	LCDC_PWM	1	PIO, I, PU, ST	–
						B	FLEXCOM3_IO2	1		
53	VDDIOP1	GPIO	PC27	GPIO	–	A	LCDC_VSYNC	1	PIO, I, PU, ST	–
						C	FLEXCOM1_IO4	1		
70	VDDIOP1	GPIO	PC28	GPIO	–	A	LCDC_HSYNC	1	PIO, I, PU, ST	–
						C	FLEXCOM1_IO3	1		
52	VDDIOP1	GPIO	PC29	GPIO	–	A	LCDC_DEN	1	PIO, I, PU, ST	–
						C	FLEXCOM1_IO2	1		
68	VDDIOP1	GPIO	PC30	GPIO	–	A	LCDC_PCK	1	PIO, I, PU, ST	–
						C	FLEXCOM3_IO7	1		
50	VDDIOP1	GPIO	PC31	GPIO	WKUP11	A	FIQ	1	PIO, I, PU, ST	–
						C	PCK1	2		

Notes:

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger.
2. The design is optimized for this feature.

6.2.4 PIOD Pin List

Table 6-4. PIOD Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State[1]	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
–	VDD_3V3	GPIO	PD0	GPIO	–	A	NANDOE	1	PIO, I, PU	Used for NAND Flash[2]
–	VDD_3V3	GPIO	PD1	GPIO	–	A	NANDWE	1	PIO, I, PU	Used for NAND Flash[2]
–	VDD_3V3	GPIO	PD2	GPIO	–	A	A21/NANDALE	1	A21, O, PD	Used for NAND Flash[2]
–	VDD_3V3	GPIO	PD3	GPIO	–	A	A22/NANDCLE	1	A22, O, PD	Used for NAND Flash[2]
18	VDD_3V3	GPIO	PD4	GPIO	–	A	NCS2/NANDCS	1	PIO, I, PU	Used for NAND Flash[2]
–	VDD_3V3	GPIO	PD5	GPIO	–	–	–	–	PIO, I, PU	Used for Ethernet PHY interrupt[2]
–	VDD_3V3	GPIO	PD6	GPIO	–	A	NANDDAT0	1	PIO, I, PU	Used for NAND Flash[2]

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Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State[1]	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
–	VDD_3V3	GPIO	PD7	GPIO	–	A	NANDDAT1	1	PIO, I, PU	Used for NAND Flash[2]
–	VDD_3V3	GPIO	PD8	GPIO	–	A	NANDDAT2	1	PIO, I, PU	Used for NAND Flash[2]
–	VDD_3V3	GPIO	PD9	GPIO	–	A	NANDDAT3	1	PIO, I, PU	Used for NAND Flash[2]
–	VDD_3V3	GPIO	PD10	GPIO	–	A	NANDDAT4	1	PIO, I, PU	Used for NAND Flash[2]
–	VDD_3V3	GPIO	PD11	GPIO	–	A	NANDDAT5	1	PIO, I, PU	Used for NAND Flash[2]
–	VDD_3V3	ground	PD12	ground	–	A	NANDDAT6	1	PIO, I, PU	Used for NAND Flash[2]
–	VDD_3V3	ground	PD13	ground	–	A	NANDDAT7	1	PIO, I, PU	Used for NAND Flash[2]
–	VDD_3V3	ground	PD14	ground	–	A	NWAIT/ NANDRDY	1	PIO, I, PU	Used for NAND Flash[2]

Notes:

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger.
2. This feature is fixed due to the SAM9X75 SOM Series internal connection.

6.2.5 System Pin List

Table 6-5. System Pin Description

Pin No.	Pin Name	Power Rail	I/O Type	Description
114	MIPI_D0_N	VDD_2V5	DPHYIO	MIPI DPHY negative differential output data lane 0
113	MIPI_D0_P	VDD_2V5	DPHYIO	MIPI DPHY positive differential output data lane 0
112	MIPI_D1_N	VDD_2V5	DPHYIO	MIPI DPHY negative differential output data lane 1
111	MIPI_D1_P	VDD_2V5	DPHYIO	MIPI DPHY positive differential output data lane 1
110	MIPI_D2_N	VDD_2V5	DPHYIO	MIPI DPHY negative differential output data lane 2
109	MIPI_D2_P	VDD_2V5	DPHYIO	MIPI DPHY positive differential output data lane 2
108	MIPI_D3_N	VDD_2V5	DPHYIO	MIPI DPHY negative differential output data lane 3
107	MIPI_D3_P	VDD_2V5	DPHYIO	MIPI DPHY positive differential output data lane 3
116	MIPI_CK_N	VDD_2V5	DPHYIO	MIPI DPHY negative differential output clock lane
115	MIPI_CK_P	VDD_2V5	DPHYIO	MIPI DPHY positive differential output clock lane
123	USBA_P	VDD_3V3	USBHS	USB host port A high-speed data +
122	USBA_N	VDD_3V3	USBHS	USB host port A high-speed data -
121	USBB_P	VDD_3V3	USBHS	USB host port B high-speed data +
120	USBB_N	VDD_3V3	USBHS	USB host port B high-speed data -
119	USBC_P	VDD_3V3	USBHS	USB host port C high-speed data +
118	USBC_N	VDD_3V3	USBHS	USB host port C high-speed data -
125	AUDIO_CLK	VDD_3V3	CLOCK	Audio clock output
78	WKUP0	VDDBU	SYSC	Wake-up input. 100kΩ Internal Pull-Up.
79	SHDN	VDDBU	SYSC	Shutdown control
151	JTAGSEL	VDDBU	SYSC	JTAG selection
147	JTAG_TCK	VDD_3V3	RSTJTAG	Test clock
148	JTAG_TDI	VDD_3V3	RSTJTAG	Test data in
152	JTAG_TDO	VDD_3V3	RSTJTAG	Test data out
149	JTAG_TMS	VDD_3V3	RSTJTAG	Test mode select
150	JTAG_RTCK	VDD_3V3	RSTJTAG	Return test clock
77	nRST	VDD_3V3	RSTJTAG	External nReset input/output. 10kΩ internal pull-up.

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Pin No.	Pin Name	Power Rail	I/O Type	Description
17	NAND_CS_IN	VDD_3V3	GPIO	NAND Flash chip select input. 100kΩ internal pull-up.
19	NAND_WP	VDD_3V3	GPIO	NAND Flash write protect. 100kΩ internal pull-up.
31	TXRXA_P	AVDDL	Analog	Physical receive or transmit signal (+ differential)
32	TXRXA_N	AVDDL	Analog	Physical receive or transmit signal (– differential)
33	TXRXB_P	AVDDL	Analog	Physical receive or transmit signal (+ differential)
34	TXRXB_N	AVDDL	Analog	Physical receive or transmit signal (– differential)
35	TXRXC_P	AVDDL	Analog	Physical receive or transmit signal (+ differential)
36	TXRXC_N	AVDDL	Analog	Physical receive or transmit signal (– differential)
37	TXRXD_P	AVDDL	Analog	Physical receive or transmit signal (+ differential)
38	TXRXD_N	AVDDL	Analog	Physical receive or transmit signal (– differential)
44	GMAC_LED5_ALLPHYAD	VDD_3V3	GPIO	Programmable LED5 output/PHY address strap pin
45	GMAC_LED4_MAGJACK	VDD_3V3	GPIO	Programmable LED4 output/MagJack register settings. 10kΩ internal pull-up.
46	GMAC_LED3_PHYAD2	VDD_3V3	GPIO	Programmable LED3 output/PHYAD2
47	GMAC_LED2_PHYAD1	VDD_3V3	GPIO	Programmable LED2 output/PHYAD1
48	GMAC_LED1_PHYAD0	VDD_3V3	GPIO	Programmable LED1 output/PHYAD0
43	GMAC_NRST	VDD_3V3	GPIO	Gigabit PHY reset line. 10kΩ internal pull-up.
21	QSPI_CS_IN	VDD_3V3	GPIO	NOR Flash chip select input. 10kΩ internal pull-up.
22	125MHz_EN	VDD_3V3	GPIO	125-MHz clock generation enable input (Enable high)

6.2.6 Power Pin List

Table 6-6. Power Pin Description

Pin No.	Pin Name	Power Rail	Type	Description
81	5V_MAIN	5V_MAIN	Input power	5V main input supply
90	VDD_3V3	VDD_3V3	Output power	3.3V I/Os voltage output
91	VDD_3V3	VDD_3V3	Output power	3.3V I/Os voltage output
82	5V_MAIN	5V_MAIN	Input power	5V main input supply
92	VDDIODDR	VDDIODDR	Output power	1.35V/1.8V memory voltage output
93	VDDIODDR	VDDIODDR	Output power	1.35V/1.8V memory voltage output
85	SELVL1	5V_MAIN	Input	VLDO1 Default Output Voltage Selection pin. Three-state input.
84	VLDO1	VOUT1	Output power	VLDO1 output voltage
83	VLDO2	VOUT2	Output power	VLDO2 output voltage
76	LPM	5V_MAIN	Input	Low-Power Mode Input pin. In combination with PWRHLD and HPM, this pin defines the MCP16502 power mode status.
75	nSTART_SOM	5V_MAIN	Input/Pull-up	Start event input. Drives nSTART_SOM to low to initiate a start-up sequence. nSTART_SOM is pulled up internally. A capacitor can be connected to automatically initiate a power-up sequence when the main supply rises.
133	VDDANA	VDDANA	Input power	Analog voltage input
130	VDDBU	VDDBU	Input power	Backup voltage input
145	VDDIOP0	VDDIOP0	Input power	VDDIOP0 voltage input
105	VDDIOP1	VDDIOP1	Input power	VDDIOP1 voltage input
143	VDDLVDS	VDDLVDS	Input power	VDDLVDS voltage input
142	VDD_2V5	VDDOUT25	Output power	2.5V output voltage

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Pin No.	Pin Name	Power Rail	Type	Description
1, 2, 9, 16, 29, 30, 39, 40, 41, 42, 49, 56, 63, 74, 80, 86, 87, 88, 89, 94, 106, 117, 124, 126, 127, 128, 129, 131, 132, 134, 135, 144, 146, 153, 156, 159, 163, 166, 169, 172, 173, 174	GND	GND	Ground	Ground connection

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7. Power Considerations

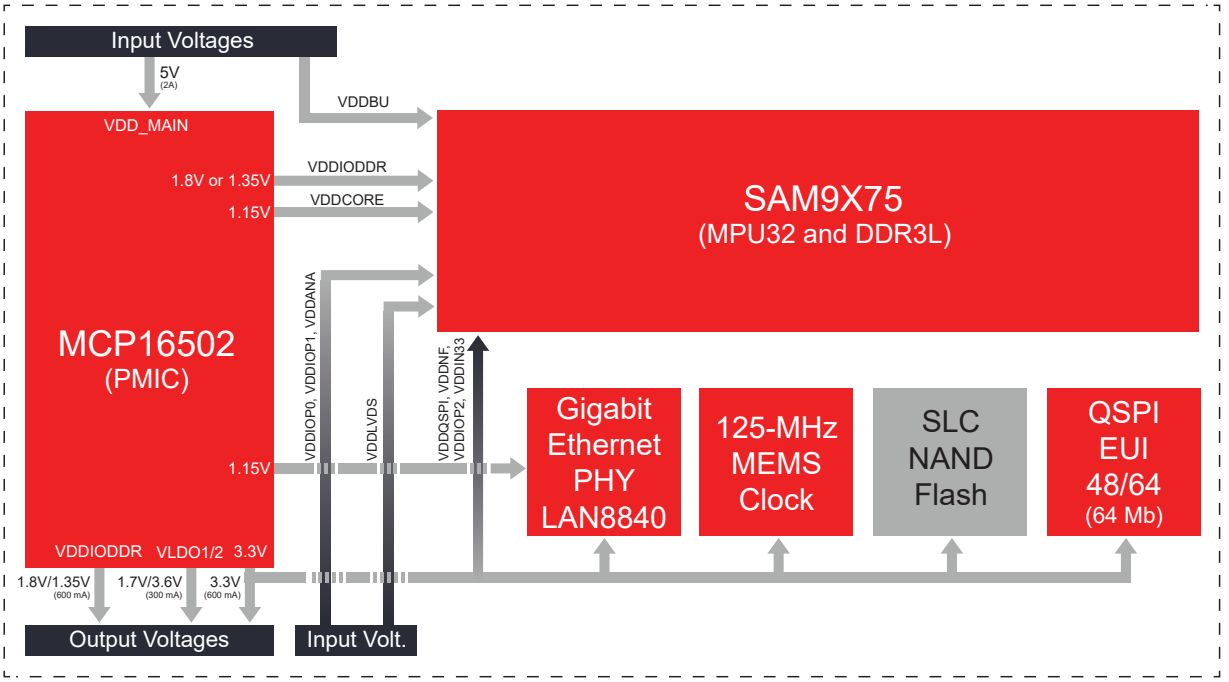
7.1 Power Supplies

Table 7-1. SAM9X75 SOM Series Power Supplies

Pin No.	Name	Power Type	Output Current Capability	Power Domains
130	VDDBU	Input	–	Backup supply input
145, 105	VDDIOP0, VDDIOP1	Input	–	VDDIOPx supplies input
133	VDDANA	Input	–	Analog supply input
90, 91	VDD_3V3	Output	600 mA	I/O supply and customer application output
92, 93	VDDIODDR	Output	600 mA	DDR memory supply and customer application output (1.35V for DDR3L)
81, 82	5V_MAIN	Input	–	System power input
84	VLDO1	Output	300 mA	Adjustable output depending on application settings
83	VLDO2	Output	300 mA	Adjustable output depending on application settings
142	VDDOUT25	Output	N/A	2.5V output for LVDS interface. Do not use for any other purpose.
143	VDDLVDS	Input	–	I/O supply LVDS interface supply input

The Microchip SAM9X75 System-On-Module Series is supplied by a unique input (5V_MAIN) and its internal supplies are delivered by a power management unit (MCP16502), as shown in the following figure.

Figure 7-1. SAM9X75 SOM Series Power Architecture



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7.2 Power-Up/Power-Down Considerations

7.2.1 System Power-Up

At power-up, from a power supply sequencing perspective, the SAM9X75 SOM Series power supplies are categorized into seven independent groups:

- 5V_MAIN (main supply)
- VDDBU (backup group)
- VDD_3V3 (internal periphery group) containing VDDIN33, VDDQSPI, VDDIOP2 and VDDNF inputs
- External VDD_PERIPH (external periphery group) containing VDDANA, VDDIOP0, and VDDIOP1 inputs
- VDDLVDS and VDDMIPI (video group)
- VDDIODDR (memory group)
- VDDCORE (core group)

Figure 7-2 shows the recommended power-up sequence.

Notes:

- VDDBU
  - When supplied from a precharged storage element (battery, supercapacitor or micro-battery), VDDBU is an always-on supply input and is therefore not part of the power supply sequencing.
  - When no storage element is used on VDDBU in the application, VDDBU must be tied to VDD_3V3.
  - When a supercapacitor or a micro-battery is used in the application to power VDDBU in Backup mode, this element must be isolated from VDDBU during its (slow) charge, so that VDDBU closely follows VDD_3V3. In Table 7-2, the parameter t_1 limits the delay to establish VDDBU after VDD_3V3.
- VDDOUT25 is the output of the internal 2.5V regulator, and therefore there is no power supply requirement on this pin.

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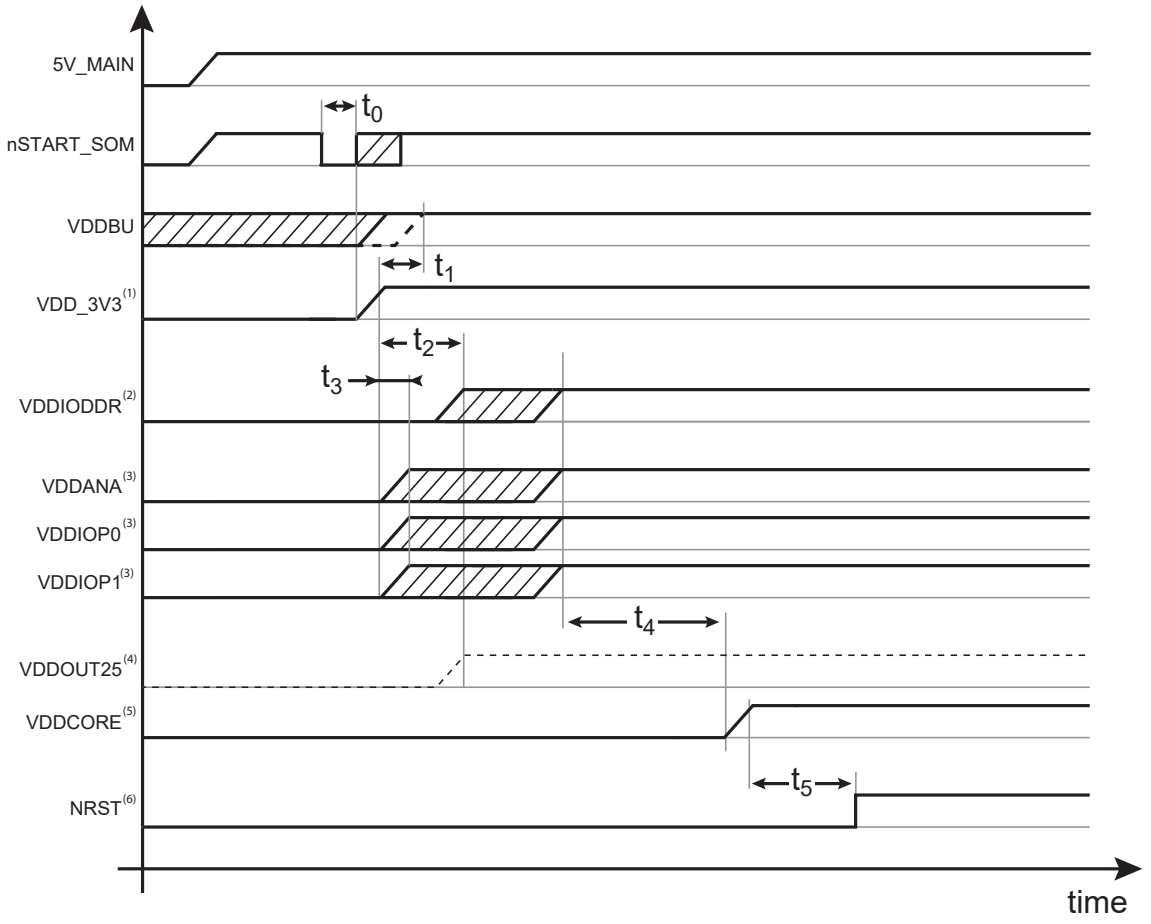
Figure 7-2. Recommended Power-Up Sequence



Notes:

1. VDD_3V3 is generated internally by the MCP16502 PMIC and supplies directly the internal periphery group.
2. VDDIODDR is generated internally by the MCP16502 PMIC and supplies directly the memory group.
3. This group is supplied externally and requires no specific order. Only timing t_3 must be respected.
4. VDDOUT25 is generated internally by the SAM9X75 SiP device and can be used to supply directly the internal video group.
5. VDDCORE is generated internally by the MCP16502 PMIC and supplies directly the core group.
6. The RESET general signal is generated internally by the MCP16502 PMIC and is distributed to the whole system.

Table 7-2. Power-Up Timing Requirements

Symbol	Parameter	Conditions(1)	Min	Typ(2)	Max	Unit
t_0	nSTRT deglitch time	nSTRT pin falling edge	–	0.5	–	ms
t_1	VDDBU delay	Delay from established VDD_3V3 to established VDDBU	–	–	0.2	ms
t_2	VDD_3V3 to memory group delay	Delay from established VDD_3V3 to VDDIODDR supply turn-on	–	8	–	ms

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Symbol	Parameter	Conditions[1]	Min	Typ[2]	Max	Unit
t_3	VDD_3V3 to external periphery group delay[3]	Delay from established VDD_3V3 to external periphery group established supply	0	–	t_2	ms
t_4	Periphery group to VDDCORE delay	Delay from periphery group established supply to VDDCORE supply turn-on	–	4	–	ms
t_5	Reset delay at power-up	From established VDDCORE to NRST high	–	16	–	ms

Notes:

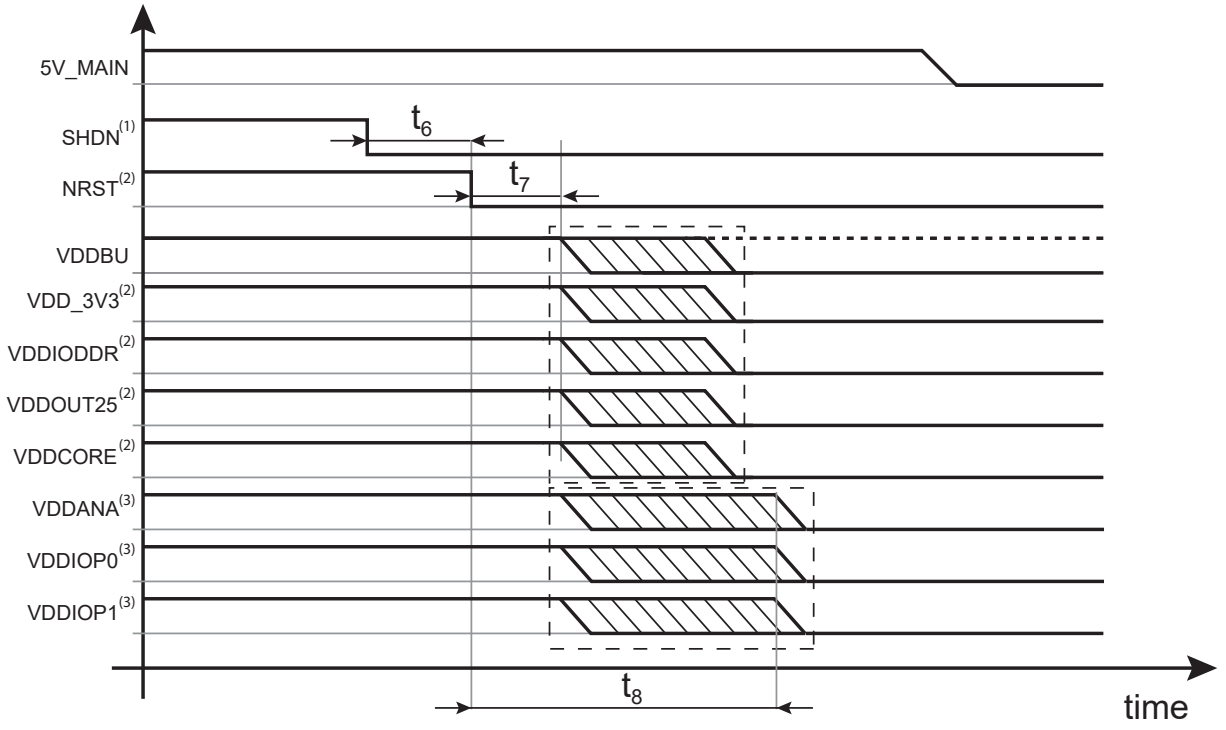
1. The term "established" refers to a power supply having reached 90% of its final value.
2. Typical timing values can be programmed in MCP16502 registers (RSTDLY[2:0]), but they must follow the timing sequence required by the SAM9X75 SiP device.
3. If one of the power inputs of the group is supplied externally, the power must be applied at the same time or after the presence of VDD_3V3 and before the presence of VDDIODDR.

7.2.2 System Power-Down

The following figure shows the SAM9X75 SOM Series power-down sequence that starts by asserting the SHDN line to "0".

Once SHDN and NRST are asserted, the supply inputs can be immediately shut down without any specific timing or order. VDDBU may not be shut down if the application uses a backup storage element on this supply input.

Figure 7-3. Recommended Power-Down Sequence



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Notes:

1. SHDN is generated internally by software request from the SAM9X75 SiP device.
2. All these signals and power rails are controlled internally by the MCP16502 PMIC and are switched off at the same time.
3. This group is supplied externally and requires no specific order. Only timing t_8 must be respected.

Table 7-3. Power-Down Timing Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_6	SHDN to NRST delay at power-down	Delay from asserted SHDN to NRST generation	0	–	10	µs
t_7	NRST delay at power-down	Delay from asserted NRST to first supply turn-off	0	–	10	µs
t_8	External supply delay at power-down	Delay from asserted NRST to external supplies turn-off	t_7	–	1	ms

7.2.3 Particular Considerations

Using the MCP16502, the system can be configured for automatic start-up (see Power Management Unit). Start-up occurs as soon as 5V_MAIN voltage is present, provided that an external capacitor is connected on nSTART_SOM (pin 75).

For this configuration, the external capacitor value must be selected with great care. The recommendations described in the MCP16502 PMIC data sheet under “nSTRT Capacitor for Automatic Turn-On on VIN Ramping” must be followed. For more information, refer to the MCP16502 PMIC data sheet (see Reference Documents).

7.3 Power Management Unit

The Microchip SAM9X75 System-On-Module Series is supplied by an external 5V supply (5V_MAIN) and generates its own internal supplies by interfacing with the Microchip MCP16502 power management unit.

The MCP16502 is a fully-featured Power Management Integrated Circuit (PMIC), cost and size-optimized for Microchip MPU devices such as the SAM9X75 SiP.

The MCP16502 integrates four DC-DC buck regulators used for system supplying and two auxiliary LDOs for customer purpose.

- All buck channels can support loads up to 1A. All bucks are 100% duty cycle capable.
  - The DCDC1 set to 3.3V supplies all pads of the embedded devices. This power rail also offers a 600-mA load to customer applications through VDD_3V3 pins.
  - The DCDC2 set to 1.35V supplies the DDR3L memory. This power rail also offers a 600-mA load to customer applications through VDDIODDR pins.
  - The DCDC3 set to 1.15V supplies the microprocessor core. It is used internally only.
  - The DCDC4 set to 1.15V supplies the Gigabit Ethernet digital core. It is used internally only.
- One 300-mA LDO is provided so that sensitive analog loads can be supported. The LDO output voltage, named VLDO1 (pin 84), is configured by a three-state pin named SEL_VLDO1 (pin 85) at power-up and can deliver 1.8V, 2.5V or 3.3V. Other voltage values can be reached after system initialization by an I²C interface access.

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- One 300-mA LDO is provided so that sensitive analog loads can be supported. The LDO output voltage, named VLDO2 (pin 83), is disabled by default at power-up. Output voltage values are set through an I²C interface access after system initialization.

The default power channel sequencing is built-in as required by the Microchip SAM9X75 MPU device.

Active discharge resistors are provided on each output. All buck channels support safe start-up into pre-biased outputs.

The MCP16502 is available in a 5x5 mm 32-pin VQFN package.

For more information, refer to the MCP16502 PMIC data sheet (see Reference Documents).

The VLDO1 voltage output of the LDO is controlled at boot by configuration of SEL_VLDO1 (pin 85). The default values are selectable among three options corresponding to three different states of the relevant pin: connected to ground (Low), connected to input supply (High) or left unconnected (High-Z). The VLDO1 default voltage can be selected by means of the SEL_VLDO1 pin, as shown in Table 7-4.

Table 7-4. VLDO1 Voltage vs SEL_VLDO1 Pin

SEL_VLDO1 Status	VLDO1 Voltage
Low (grounded)	1.8V
High-Z (not connected)	2.5V
High (up to 5V_MAIN)	3.3V

The LPM pin of the Microchip SAM9X75 System-On-Module Series, combined with the HPM and PWRHLD status pins of the MCP16502 PMIC, defines different power states as illustrated in Table 7-5.

Note: HPM is forced to 0 by hardware, since the High-Performance feature of the MCP16502 PMIC is not supported by the SAM9X75 SiP MPU device. For more information, refer to the MCP16502 data sheet (see Reference Documents).

Table 7-5. MCP16502 Default Power States

PWRHLD	LPM	HPM	Buck1	Buck2	Buck3	Buck4	LDO1	LDO2	nRST	Power State(1)
0	0	0	Off	Off	Off	Off	Off	Off	Low	Off
0	1	0	Off	On(2)	Off	On(2)	Off	Off	Low	Hibernate mode
1	1	0	On(2)	On(2)	On(2)	On(2)	On	Off	HiZ	Low-Power mode
1	0	0	On(3)	On(3)	On(3)	On(3)	On	Off	HiZ	Active mode

Notes:

1. Only allowed modes are listed. If some PWRHLD/LPM/HPM combination is not listed, then such mode is not allowed.
2. In this mode, the DCDC is configured in Automatic Pulse-Frequency Modulation (Auto-PFM) mode.
3. In this mode, the DCDC is configured in Force Pulse-Width Modulation (FPWM) mode.

For more information about the use of the MCP16502 LPM feature, refer to the MCP16502 data sheet (see Reference Documents).

The LPM pin can be managed externally, as shown in the figure below.

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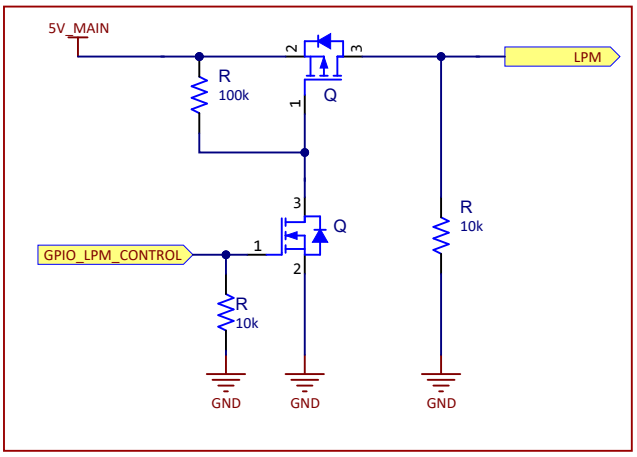
Figure 7-4. LPM Control Schematic Example



7.4 Power Configurations

Three different configurations, depending on customer use, are available.

- Single supply—The SAM9X75 SOM Series can be supplied by only one input supply (for example, a 5V AC/DC wall adapter) and other input supplies can be connected to the internal 3.3V regulator VDD_3V3. All PIO lines are supplied at 3.3V.
- Multiple supplies—The SAM9X75 SOM Series can be supplied by a 5V supply and a backup battery. Some PIO power lines, such as VDDIOPx and VDDANA, are supplied by different LDOs for specific applications.
- Multiple supplies with LVDS—The SAM9X75 SOM Series can be supplied by a 5V supply and a backup battery. Some PIO power lines, such as VDDIOPx and VDDANA, are supplied by different LDOs for specific applications and the VDDLVDS power line is supplied by a VDDOUT25 output supply.

Figure 7-5. SAM9X75 SOM Series Single Supply Connection Example

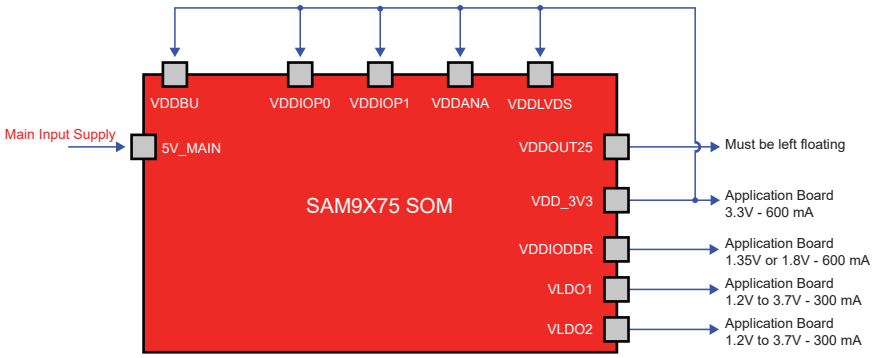


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Figure 7-6. SAM9X75 SOM Series Multiple Supplies Connection Example

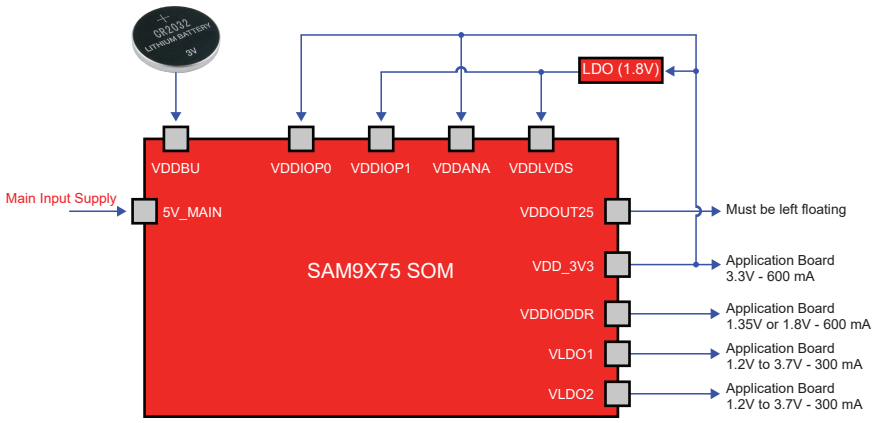
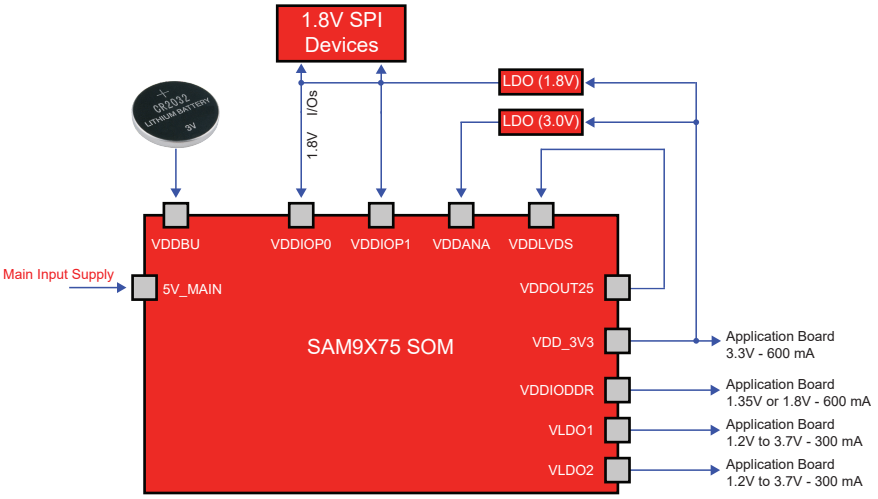


Figure 7-7. SAM9X75 SOM Series Multiple Supplies with LVDS Connection Example



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8. MPU and Memory Subsystem

8.1 SAM9X75 System-in-Package (SiP)

The Microchip SAM9X75 System-On-Module Series embeds the SAM9X75 SiP, which integrates the ARM926EJ-S Arm Thumb processor-based SAM9X75 MPU with an up to 2-Gbit DDR3L SDRAM (depending on the configuration) in a single package.

By combining the SAM9X75 with a DDRx memory in a single package, PCB routing complexity, area and number of layers are reduced. This makes board design easier and more robust by facilitating design for EMI, ESD and signal integrity.

For more information, refer to the SAM9X75 SiP data sheet (see Reference Documents).

The SAM9X75 SiP is available in a 16x16 mm 243-ball TFBGA package.

The Microchip SAM9X75 System-On-Module Series provides global system Reset (NRST) and Shutdown (SHDN) pins to the application board.

Notes:

- The NRST pin is an input/output pin generated by the internal power management unit (MCP16502) respecting the microprocessor power sequence timing. It is distributed internally to the microprocessor and can be forced externally for system level control.
- The SHDN pin is an output pin managed by the application software. In an application case, the pin can switch on/off the 5V_MAIN external main supply.

8.2 MPU Clocks

Two clock sources are necessary for the module microprocessor:

- A small size 24-MHz crystal to generate the SAM9X75 MPU main clock
- A small size 32.768-kHz crystal to generate the slow clock oscillator input and feed the embedded RTC of the SAM9X75 MPU

8.3 NAND Flash Memory

The Microchip SAM9X75 System-On-Module Series embeds an SLC NAND Flash memory supported through its External Bus Interface controller with different memory sizes depending on the part number.

The System-On-Module implements one of the following references, depending on the memory space. All are available in a VFBGA-63 package.

- 2-Gbit memory size[(1)]
  - Macronix MX30LF2G28AD-XKI
  - Micron MT29F2G08ABAEAH4-IT:G
- 4-Gbit memory size[(1)]
  - Macronix MX30LF4G28AD-XKI
  - Micron MT29F4G08ABAFAH4-IT:F

Note:

1. Either one of the above references can be mounted on the Microchip SAM9X75 System-On-Module Series.

For more information about NAND Flash memories, refer to the relevant data sheets (see Reference Documents).

Microchip Linux distribution supports all references. For details on how to build Linux software, refer to www.linux4microchip.com.

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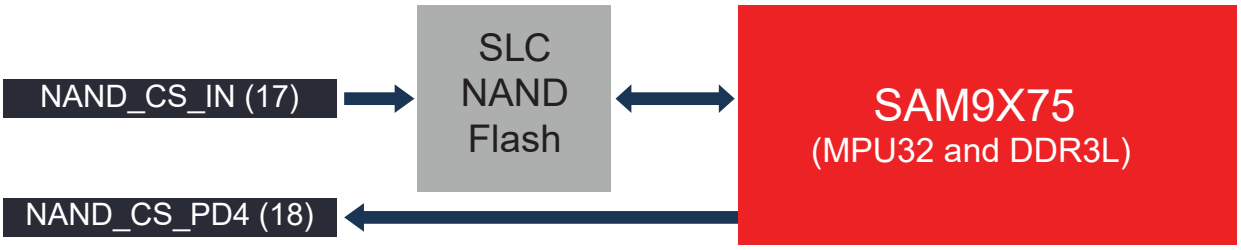
NAND_CS_IN (pin 17) is accessible externally and can be uncoupled from NAND_CS_PD4 (pin 18) so that the boot can be unselected from the NAND Flash memory during debug phases.

Figure 8-1. NAND Flash Memory Block Diagram



8.4 QSPI NOR Memory

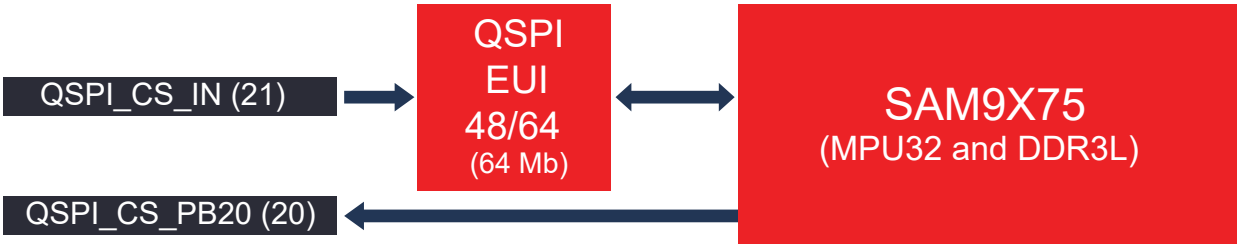
The Microchip SAM9X75 System-On-Module Series embeds the SST26VF064BEUIT-104I/MF, a 64-Mbit Serial Quad I/O Flash memory.

The SST26VF064BEUI SQI features a 6-wire, 4-bit I/O interface that allows for low-power, high performance operation in a low pin-count package.

The SST26VF064BEUI also embeds EUI-48 and EUI-64 MAC addresses.

The SST26VF064BEUI is available in a 6x5 mm 8-lead WDFN package. For more information, refer to the SST26VF064BEUI data sheet (see Reference Documents).

Figure 8-2. QSPI Memory Block Diagram



Note: For debug purposes, the embedded QSPI Chip Enable pin can be uncoupled from the microprocessor. QSPI_CS_IN (pin 21) is accessible externally and can be uncoupled from QSPI_CS_PB20 (pin 20) so that the boot can be unselected from the QSPI Flash memory during debug phases.

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9. LAN Subsystem

9.1 Ethernet Clocks

Two clock sources are necessary for the Ethernet functionality:

- A small size 25-MHz crystal is used to generate the main clock of the Gigabit Ethernet Transceiver LAN8840T-V/PSA.
- A small size 125-MHz MEMS oscillator (DSC1501MI2A-125.0000) is used to generate the clock source of the SAM9X75 MPU Gigabit Ehernet functionality. This functionality is externally controlled by GPIO 125MHz_EN (pin 22).

9.2 Gigabit Ethernet PHY

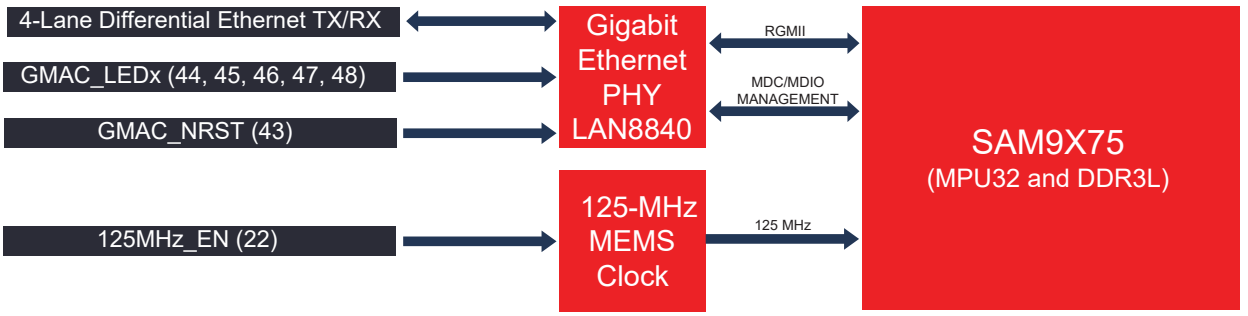
The SAM9X75 SOM Series embeds one low-power, single port, triple speed (10BASE-T/100BASE-TX/1000BASE-T) Ethernet physical layer transceiver (PHY) LAN8840 optimized for precision process timing.

The LAN8840T-V/PSA supports industry-standard RGMII (Reduced Gigabit Media Independent Interface) providing chip-to-chip connection to a host device with an integrated Gigabit Ethernet MAC.

The device is available in a 7x7 mm 48-pin VQFN package and is implemented in the system as shown in the figure below.

For more information, refer to the Ethernet PHY LAN8840 data sheet (see Reference Documents).

Figure 9-1. Ethernet PHY Digital/Analog Block Diagram



The SAM9X75 SOM Series embeds straps on the MODE[4:0] signals of the LAN8840 pins (PB0, PB1, PB8, PB11, PB12) to ensure that a set of features is configured automatically when the GMAC_NRST signal (pin 43) is released. The default settings are as follows:

- Auto-negotiation to automatically select the highest link-up speed and duplex: Enabled.
- Automatic MDI/MDI-X crossover to detect and correct pair swapping at all operating speeds: Enabled.
- Energy Efficient Ethernet (EEE) support: Enabled.
- Single port with triple speed (10BASE-T/100BASE-TX/1000BASE-T) link in full duplex modes: Enabled.

The LAN8840 PHY is not fully configured. Configuration straps (pull-up/down resistors) on the GMAC_LEDx pads (pins 44, 45, 46, 47 and 48) must be placed outside the module and GMAC_NRST (pin 43) can be connected as follows:

- The GMAC_LED5_ALLPHYAD pad (pin 44) allows the use of any value on the GMAC_LEDx_PHYAD[2:0] pads (pins 46, 47, 48), or 0 by default. This pin can be pulled up or down externally.

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- The GMAC_LEDx_PHYAD[2:0] pads (pins 46, 47, 48) are used to set the PHY address.
- The GMAC_NRST pad can be connected to the global NRST signal (pin 77) or to any system reset management.

Note: Any required external pulling configuration strap must be tied to either VDD_3V3 or GND, depending on customer needs. For more details, refer to the LAN8840 data sheet (see Reference Documents).

The LAN8840 PHY is supplied by:

- VDD_3V3 for digital interfacing with the SAM9X75 SiP device,
- VDD_1V15_ETH for the LAN8840 digital PLL and analog interfacing with the outside world.

Both are delivered by the MCP16502 PMIC.

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10. External Interfacing

10.1 Interfacing with FLEXCOM

10.1.1 Interfacing in I²C/TWI Mode

Twelve Flexible Serial Communication Controller (FLEXCOM) interfaces configurable in Two-Wire Interface (TWI) mode are available on the SAM9X75 SOM Series.

The TWI can interconnect with external components on a unique two-wire bus, made up of one clock line and one data line with speeds of up to 400 Kbits/s in Fast mode and up to 3.4 Mbits/s in High-Speed Client mode only, based on a byte-oriented transfer format.

It can be used with any Two-Wire Interface bus Serial EEPROM and I²C-compatible devices, such as a Real-Time Clock (RTC), a dot matrix/graphic LCD controller or a temperature sensor. The TWI is programmable as a host or a client with sequential or single-byte access. Multiple host capability is supported.

Table 10-1. I²C/TWI Interface Configurations

Interface Instance	IO Set	Pin No.	PIO	Pin Name	Comment
FLEXCOM0	1	138	PA30	FLEXCOM0_IO0	External pull-up needed in case the FLEXCOM interface is used as an I²C/TWI interface.
		136	PA31	FLEXCOM0_IO1	
FLEXCOM1	1	139	PA28	FLEXCOM1_IO0	
		141	PA29	FLEXCOM1_IO1	
FLEXCOM2	1	165	PA13	FLEXCOM2_IO0	
		164	PA14	FLEXCOM2_IO1	
FLEXCOM3	1	66	PC22	FLEXCOM3_IO0	
		51	PC23	FLEXCOM3_IO1	
FLEXCOM4	1, 2	12	PA10	FLEXCOM4_IO0	
		13	PA9	FLEXCOM4_IO1	
FLEXCOM5	1, 2	160	PA16	FLEXCOM5_IO0	
		162	PA15	FLEXCOM5_IO1	
FLEXCOM6	1	158	PA24	FLEXCOM6_IO0	No external pull-up needed. Already integrated in the SOM.
		157	PA25	FLEXCOM6_IO1	
FLEXCOM7	1	59	PC0	FLEXCOM7_IO0	External pull-up needed in case the FLEXCOM interface is used as an I²C/TWI interface.
		62	PC1	FLEXCOM7_IO1	
FLEXCOM9	1	55	PC8	FLEXCOM9_IO0	
		64	PC9	FLEXCOM9_IO1	
FLEXCOM10	1	73	PC16	FLEXCOM10_IO0	
		57	PC17	FLEXCOM10_IO1	
FLEXCOM11	1	23	PB15	FLEXCOM11_IO0	
		25	PB16	FLEXCOM11_IO1	
FLEXCOM12	1	26	PB17	FLEXCOM12_IO0	
		27	PB18	FLEXCOM12_IO1	

10.1.2 Interfacing in USART Mode

Twelve FLEXCOM interfaces configurable in Universal Synchronous Asynchronous Receiver Transceiver (USART) mode are available on the SAM9X75 SOM Series.

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Table 10-2. USART Interface Configurations

Interface Instance	IO Set	Pin No.	PIO	Pin Name
FLEXCOM0	1	138	PA30	FLEXCOM0_IO0
		136	PA31	FLEXCOM0_IO1
FLEXCOM1	1	139	PA28	FLEXCOM1_IO0
		141	PA29	FLEXCOM1_IO1
FLEXCOM2	1	165	PA13	FLEXCOM2_IO0
		164	PA14	FLEXCOM2_IO1
FLEXCOM3	1	66	PC22	FLEXCOM3_IO0
		51	PC23	FLEXCOM3_IO1
FLEXCOM4	1, 2	12	PA10	FLEXCOM4_IO0
		13	PA9	FLEXCOM4_IO1
FLEXCOM5	1, 2	160	PA16	FLEXCOM5_IO0
		162	PA15	FLEXCOM5_IO1
FLEXCOM6	1	158	PA24	FLEXCOM6_IO0
		157	PA25	FLEXCOM6_IO1
FLEXCOM7	1	59	PC0	FLEXCOM7_IO0
		62	PC1	FLEXCOM7_IO1
FLEXCOM9	1	55	PC8	FLEXCOM9_IO0
		64	PC9	FLEXCOM9_IO1
FLEXCOM10	1	73	PC16	FLEXCOM10_IO0
		57	PC17	FLEXCOM10_IO1
FLEXCOM11	1	23	PB15	FLEXCOM11_IO0
		25	PB16	FLEXCOM11_IO1
FLEXCOM12	1	26	PB17	FLEXCOM12_IO0
		27	PB18	FLEXCOM12_IO1

10.1.3 Interfacing in SPI Mode

Six FLEXCOM interfaces configured in Serial Peripheral Interface (SPI) mode are available on the SAM9X75 SOM Series.

The SPI circuit is a synchronous serial data link that provides communication with external devices in Host or Client mode. It also enables communication between processors if an external processor is connected to the system.

The Serial Peripheral Interface is essentially a shift register that serially transmits data bits to other SPI devices. During a data transfer, one SPI system acts as the “host” which controls the data flow, while the other devices act as “clients” which have data shifted in and out by the host. Different CPUs can take turn being hosts (multiple host protocol, as opposed to single host protocol where one CPU is always the host while all others are always clients). One host can simultaneously shift data into multiple clients. However, only one client can drive its output to write data back to the host at any given time.

A client device is selected when the host asserts its NSS signal. When multiple client devices are available, the host generates a separate client select signal (NPCS) for each.

The SPI system consists of two data lines and two control lines:

- Host Out Client In (MOSI)—This data line supplies the output data from the host shifted into the input(s) of the client(s).
- Host In Client Out (MISO)—This data line supplies the output data from a client to the input of the host. There may be no more than one client transmitting data during any particular transfer.

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- Serial Clock (SPCK)—This control line is driven by the host and regulates the flow of the data bits. The host can transmit data at a variety of baud rates; there is one SPCK pulse for each bit transmitted.
- Client Select (NSS)—This control line enables turning clients on and off by hardware.

Table 10-3. FLEXCOM Interface Configurations in SPI Mode

Interface Instance	IO set	Pin No.	PIO	Pin Name	Description
FLEXCOM0	1	138	PA30	FLEXCOM0_IO0	MOSI Signal
		136	PA31	FLEXCOM0_IO1	MISO Signal
		15	PA8	FLEXCOM0_IO2	SPCK Signal
		10	PA7	FLEXCOM0_IO3	NPCS0 Signal
		11	PA6	FLEXCOM0_IO4	NPCS1 Signal
FLEXCOM1	1	139	PA28	FLEXCOM1_IO0	MOSI Signal
		141	PA29	FLEXCOM1_IO1	MISO Signal
		70	PC28	FLEXCOM1_IO2	SPCK Signal
		53	PC27	FLEXCOM1_IO3	NPCS0 Signal
		67	PC26	FLEXCOM1_IO4	NPCS1 Signal
		57	PC17	FLEXCOM1_IO7	NPCS4 Signal
FLEXCOM3	1	66	PC22	FLEXCOM3_IO0	MOSI Signal
		51	PC23	FLEXCOM3_IO1	MISO Signal
		67	PC26	FLEXCOM3_IO2	SPCK Signal
		61	PC25	FLEXCOM3_IO3	NPCS0 Signal
		69	PC24	FLEXCOM3_IO4	NPCS1 Signal
		68	PC30	FLEXCOM3_IO7	NPCS4 Signal
FLEXCOM4	1	12	PA10	FLEXCOM4_IO0	MOSI Signal
		13	PA9	FLEXCOM4_IO1	MISO Signal
		14	PA11	FLEXCOM4_IO2	SPCK Signal
		165	PA13	FLEXCOM4_IO4	NPCS1 Signal
		154	PA14	FLEXCOM4_IO5	NPCS2 Signal
FLEXCOM4	2	12	PA10	FLEXCOM4_IO0	MOSI Signal
		13	PA9	FLEXCOM4_IO1	MISO Signal
		14	PA11	FLEXCOM4_IO2	SPCK Signal
		138	PA30	FLEXCOM4_IO4	NPCS1 Signal
		136	PA31	FLEXCOM4_IO5	NPCS2 Signal
FLEXCOM5	1	160	PA16	FLEXCOM5_IO0	MOSI Signal
		162	PA15	FLEXCOM5_IO1	MISO Signal
		171	PA17	FLEXCOM5_IO2	SPCK Signal
		154	PA14	FLEXCOM5_IO3	NPCS0 Signal
FLEXCOM5	2	160	PA16	FLEXCOM5_IO0	MOSI Signal
		162	PA15	FLEXCOM5_IO1	MISO Signal
		171	PA17	FLEXCOM5_IO2	SPCK Signal
		154	PA14	FLEXCOM5_IO3	NPCS0 Signal
		138	PA30	FLEXCOM5_IO4	NPCS1 Signal

10.2 Interfacing with an SDIO/SD/MMC Device

The SAM9X75 SOM Series includes two Secure Digital Multimedia Card (SDMMC) interfaces that support the MultiMedia Card (e.MMC) specification V4.51, the SD Memory Card specification V3.0,

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and the SDIO V3.0 specification. They are compliant with the SD Host Controller Standard V3.0 specification.

The two interfaces can be connected to a standard SD Card, e.MMC Flash or SDIO device.

Table 10-4. SDMMCx Interface Configurations

Interface Instance	IO Set	Pin No.	PIO	Pin Name	Description
SDMMC0	1	6	PA2	SDMMC0_CK	SD Card/e.MMC clock signal
		3	PA1	SDMMC0_CMD	SD Card/e.MMC command line
		8	PA0	SDMMC0_DAT0	SD Card/e.MMC data lines
		5	PA3	SDMMC0_DAT1	
		7	PA4	SDMMC0_DAT2	
		4	PA5	SDMMC0_DAT3	
SDMMC1	1	14	PA11	SDMMC1_CK	SD Card/e.MMC clock signal
		12	PA10	SDMMC1_CMD	SD Card/e.MMC command line
		13	PA9	SDMMC1_DAT0	SD Card/e.MMC data lines
		11	PA6	SDMMC1_DAT1	
		10	PA7	SDMMC1_DAT2	
		15	PA8	SDMMC1_DAT3	

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11. Electrical Characteristics

11.1 Absolute Maximum Ratings

The following table provides the maximum operating ratings for the SAM9X75 SOM Series.

Table 11-1. Absolute Maximum Ratings

Parameter	Pads	Range	Comments
I/O supply voltage	All GPIO	-0.3V to 4.0V	**Note:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. **Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**
VDDIOP0, VDDIOP1, VDDLVDS, VDDANA supplies voltage	VDDIOP0, VDDIOP1, VDDLVDS, VDDANA	-0.3V to 4.0V	
Main supply voltage	5V_MAIN	-0.3V to 6.0V	
Backup supply voltage	VDDBU	-0.3V to 4.0V	
Storage temperature	$T_{STORAGE}$	-55 to +150°C	
Maximum input current	VDD_MAIN	2A	

11.2 Recommended Operating Conditions

The following table provides the operating conditions for the Microchip SAM9X75 System-On-Module Series.

Table 11-2. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
GPIO @ VDD_3V3	I/O supply voltage @ VDD_3V3	3.23	3.37	V
VDDIOP0, VDDIOP1, VDDLVDS GIPOs	I/O supply voltage	1.7	3.6	V
5V_MAIN	Main supply voltage	3.3	5.5	V
VDDBU	Backup supply voltage	1.6	3.6	V
VDDANA	Analog supply voltage	3.0	3.6	V
T_A	Module operating ambient temperature	–40	85	°C

11.3 Power Consumption

The following current consumption values are provided for information only.

Current consumption can vary according to temperature, MPU and GPU activities and customer application implementation (hardware interfaces uses, clock speed setup and embedded software solution).

Table 11-3. Power Consumption

Node	Measurement	Conditions	Min	Typ	Max	Unit
5V_MAIN	Current consumption	Linux and Ethernet transfer. 5V_MAIN = 5.00V (CPU @ 800MHz)	–	(*)	(*)	mA
5V_MAIN	Current consumption	Linux in idle[(1)] 5V_MAIN = 5.00V (CPU @ 800MHz)	–	(*)	(*)	mA
5V_MAIN	Current consumption	System off, all supplies off. 5V_MAIN = 5.00V	–	(*)	(*)	µA
VDDBU	Current consumption	VDDBU = 3.3V @ 25°C	–	(*)	–	µA
VDDBU	Current consumption	1.6V < VDDBU < 3.6V. All temperature ranges, all modes	(*)	–	(*)	µA

Notes:

1. "Linux in idle" means that Linux is loaded and that the prompt is shown on the console, waiting for instructions.
2. (*) denotes data that will be forthcoming in the final data sheet publication.

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12. Mechanical Characteristics

12.1 SAM9X75 SOM Series Dimensions

Figure 12-1. Microchip SAM9X75 System-On-Module Series Dimensions

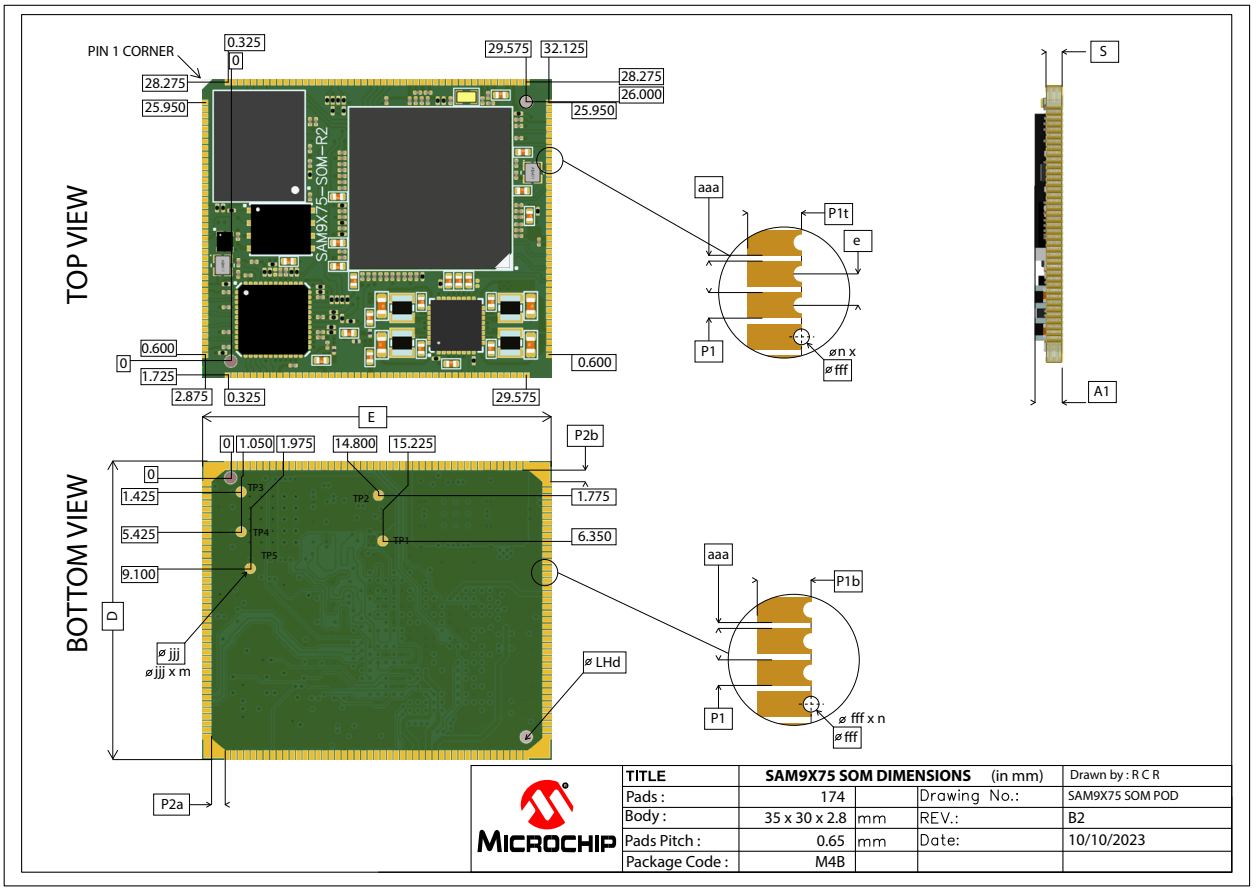

Table 12-1. Microchip SAM9X75 System-On-Module Series Dimensions (in mm)

Parameter		Symbol	Common Dimensions			Comments
			Min	Typ	Max	
Body overall dimensions	X	E	34.850	35.000	35.150	
	Y	D	29.850	30.000	30.150	
Pad pitch		e	–	0.650	–	
PCB thickness		S	1.440	1.600	1.760	
SOM total thickness		A1	–	2.800	2.850	
Pad length	Top side	P1t	–	0.550	–	
	Bottom side	P1b	–	0.900	–	
Pad width		P1	–	0.450	–	
Pad gap		aaa	–	0.200	–	
Opening drill diameter		fff	–	0.300	–	
Pad count		n	–	174	–	
Test point diameter		jjj	–	1.000	–	
Test point count		m	–	5	–	

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.....continued

Parameter		Symbol	Common Dimensions			Comments
			Min	Typ	Max	
Pad edge to SOM edge	X	P2a	–	1.450	–	
	Y	P2b	–	1.200	–	
Locating hole diameter		LHd	1.150	1.200	1.250	

Note: Test points placed under the Microchip SAM9X75 System-On-Module Series are for production purposes only. Avoid any contact with the main board vias or copper areas (see Figure 12-1).

Table 12-2. Test Point Position Compared to Locating Point (Bottom View)

Test Point Number	X (in mm)	Y (in mm)
TP1	15.225	6.350
TP2	14.800	1.775
TP3	1.050	1.425
TP4	1.050	5.425
TP5	1.975	9.100

12.2 Other Characteristics

Table 12-3. SAM9X75 SOM Series Weight

Ordering Code	Parameter	Measurement	
		Value	Unit
SAM9X75D2GN4-I/M4B	Weight	5.5	g
SAM9X75D1GN2-I/M4B		(*)	g

Note: (*) denotes data that will be forthcoming in the final data sheet publication.

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13. Ordering Information

For details on ordering codes, see Product Identification System.

Ordering Code	DDR3L Memory Configuration	NAND Memory Configuration	Package	Carrier Type	Module Ambient Temperature Range
SAM9X75D2GN4-I/M4B	2 Gbits	4 Gbits	35x30 mm 174-pin module	Tray	-40°C to +85°C
SAM9X75D1GN2-I/M4B	1 Gbit	2 Gbits			

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14. Revision History

14.1 DS60001857A - 07/2024

Changes
Initial Release

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Product Identification System

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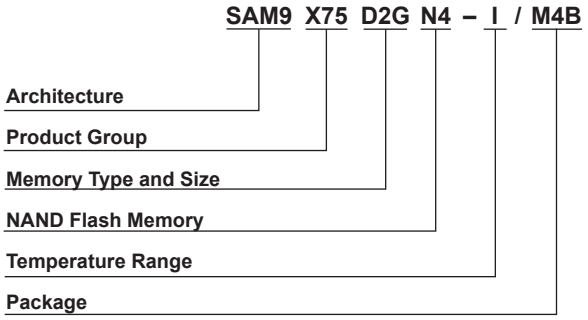

Architecture:	SAM9	= ARM926EJ–S Arm Thumb microprocessor
Product Group:	X75	= General purpose microprocessor
Memory Type and Size:	D2G	= 2-Gbit DDR3L SDRAM
	D1G	= 1-Gbit DDR3L SDRAM
NAND Flash Memory:	N4	= 4-Gbit NAND Flash memory
	N2	= 2-Gbit NAND Flash memory
Ambient Temperature Range:	I	= –40°C to +85°C (industrial)
Package:	M4B	= System-On-Module package code

Example:

- SAM9X75D2GN4-I/M4B = ARM926EJ–S Arm Thumb general purpose microprocessor with 2-Gbit DDR3L SDRAM and 4-Gbit NAND Flash memory for industrial applications, in an M4B package

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