SAMA7D65 MPU, up to 2-Gbit DDR SDRAM, up to 8-Gbit NAND Flash, Gigabit Ethernet PHY, Power Management IC, 64-Mbit Serial Quad I/O Flash

SAMA7D65 SOM Series Preliminary Data Sheet

Introduction

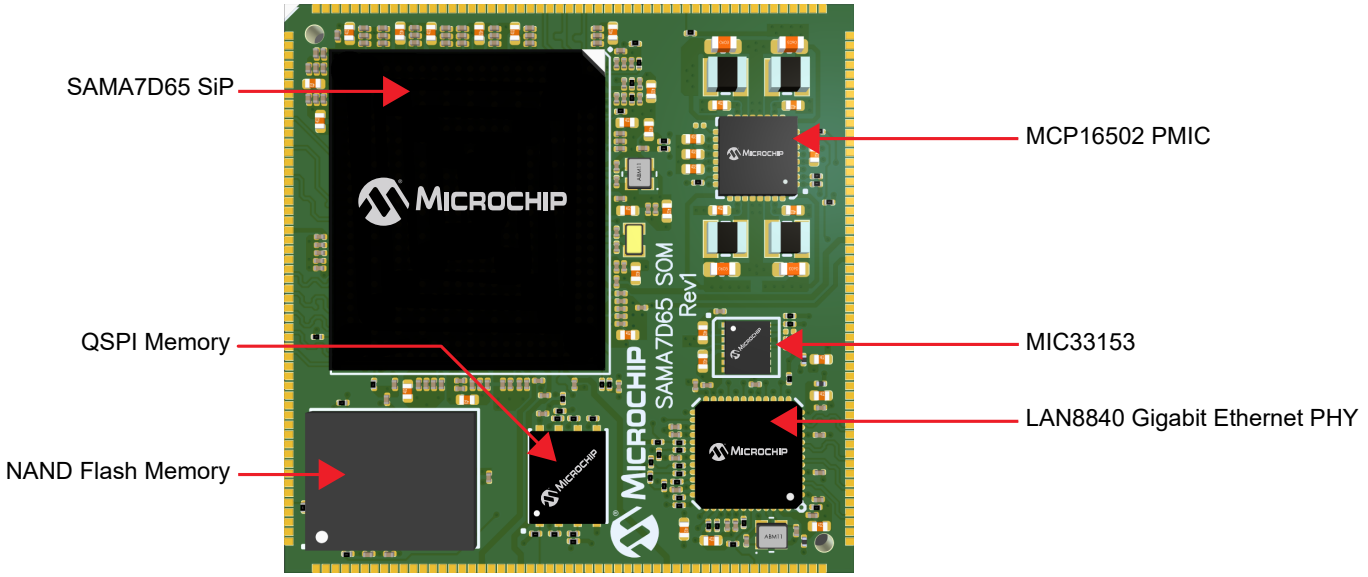
The Microchip SAMA7D65 System-On-Module Series is a small, single-sided SOM series based on a System-in-Package (SiP) Arm® Cortex®-A7 CPU-based embedded microprocessor running up to 1 GHz.

The SAMA7D65 SOM Series is built on a common set of proven Microchip components to reduce time to market by simplifying hardware design and software development.

The SOM embeds a SAMA7D65 SiP microprocessor with up to 2-Gbit DDR SDRAM, up to 8-Gbit NAND Flash memory, a Gigabit Ethernet PHY, a 64-Mbit serial Quad I/O Flash memory and a dedicated Power Management Unit.

The SAMA7D65 SOM Series also limits the design rules of the main application board, reducing overall PCB complexity and cost. The SAMA7D65 SOM Series is supported by a free Linux® distribution and bare-metal C examples.

Figure 1. SAMA7D65 SOM Series Overview



1. Features

- SAMA7D65 System-in-Package Including:
  - Arm Cortex-A7 processor-based SAMA7D65 MPU
  - CPU frequency up to 1 GHz, junction temperature range: –40°C to +105°C
  - Up to 2-Gbit DDR3L SDRAM memory
- Up to 8-Gbit NAND Flash Memory
- 64-Mbit Serial Quad I/O Flash Memory (SST26VF064BEUIT-104I/MF) with Embedded EUI-48™ and EUI-64™ MAC Addresses
- On-Board Power Management Unit (MCP16502TAB-E/S8B)
- Gigabit Ethernet Transceiver (LAN8840T-V/PSA)
- On-Board DC/DC Supply for Ethernet Transceiver Core (MIC33153-YHJ-TR)
- 24-MHz Crystal Oscillator for Microprocessor Main Clock Generation
- 25-MHz Crystal Oscillator for Ethernet Clock Generation
- 32.768-kHz Crystal Oscillator for Slow Clock Generation
- Three USB Interfaces:
  - 2x host/device with Type-C interface
  - 1x host interface
- Wake-up, Shutdown, Tamper and Reset Control Pins
- Up to 106 I/Os
- Independent Power Supplies Available for Serial Interfaces (UART, SPI, I²S, CAN), SD Cards, RGMII Ethernet, LVDS Display and Backup Depending on Voltage Domains
- Operational Conditions:
  - Main operating voltage (5V_MAIN) : 3.3V to 5.5V ±5%
  - Module ambient temperature (T_A) range: –40°C to +85°C
- Package:
  - 38 x 38 mm 212-pin 0.65 mm Pad Pitch Module, Manually Solderable for Prototyping

2. Applications

- Industrial control and automation
- Smart appliances
- Industrial and IoT gateways
- Access control panels
- Security and alarm systems
- Automotive EV chargers
- Digital audio subsystems

3. Design Resources

3.1 Hardware Design Resources

As the SAMA7D6 Series System-in-Package (SiP) MPU embeds a DDR3L memory chip, most of the design complexity related to high-speed DDR interface routing is avoided when using the SAMA7D65 System-On-Module.

For carrier board design, Microchip provides complete SAMA7D65 System-On-Module schematics and PCB design files in Altium format (on request and under license agreement), enabling electrical simulations for high-speed interfaces such as MIPI, LVDS and USB, as well as mechanical evaluation/simulation. For signal integrity simulation, Microchip provides IBIS models of the SAMA7D6 Series SiP device.

3.2 Software Resources

Microchip Technology provides complete embedded Linux solutions for MPUs. For more information, refer to Linux® OS for MPUs.

4. Reference Documents

Type	Document Title	Available	Literature No.
Data sheet	SAMA7D65 SiP	www.microchip.com	DS60001853
Errata sheet	SAMA7D6 Series Silicon Errata and Data Sheet Clarifications	www.microchip.com	DS80001131
Data sheet	LAN8840	www.microchip.com	DS00004727
Data sheet	MIC33153	www.microchip.com	DS20006223
Data sheet	SST26VF064BEUI	www.microchip.com	DS20006138
Data sheet	MCP16502	www.microchip.com	DS20006275
Data sheet	MX30LF2G28AD-XKI(1)	www.mxic.com.tw	PM2579
Data sheet	MT29F2G08ABAEAH4-IT(1)	www.micron.com/	–
Data sheet	MX60LF8G28AD-XKI(2)	www.mxic.com.tw	PM2783

Notes:

1. 2-Gbit NAND Flash memory
2. 8-Gbit NAND Flash memory

5. Description

The Microchip SAMA7D65 SOM Series is a high-performance System-On-Module based on the ultralow-power Arm Cortex-A7 CPU-based embedded microprocessor (MPU) SAMA7D65. The SAMA7D65 SOM Series is certified for industrial operating conditions over the [-40°C to 85°C] industrial ambient temperature range.

The SAMA7D65 SOM Series operates at a maximum CPU operating frequency of 1 GHz and a maximum bus speed of 533 MHz and features up to:

- DDRx SDRAM memory with one of the following configurations:
  - 1-Gbit DDR3L SDRAM memory size (SAMA7D65D1G-V/4UB)
  - 2-Gbit DDR3L SDRAM memory size (SAMA7D65D2G-V/4UB)
- 8-bit NAND Flash memory with one of the following configurations(1):
  - 2-Gbit memory size (MX30LF2G28AD-XKI or MT29F2G08ABAEAH4-IT)(2)
  - 8-Gbit memory size (MX60LF8G28AD-XKI)(3)
- 64 Mbits of Serial Quad I/O (SQI) Flash memory with EUI (SST26VF064BEUIT-104I/MF)
- A Gigabit Ethernet transceiver (LAN8840T-V/PSA)

The device offers an extensive peripheral set, system control and up to 106 I/Os featuring:

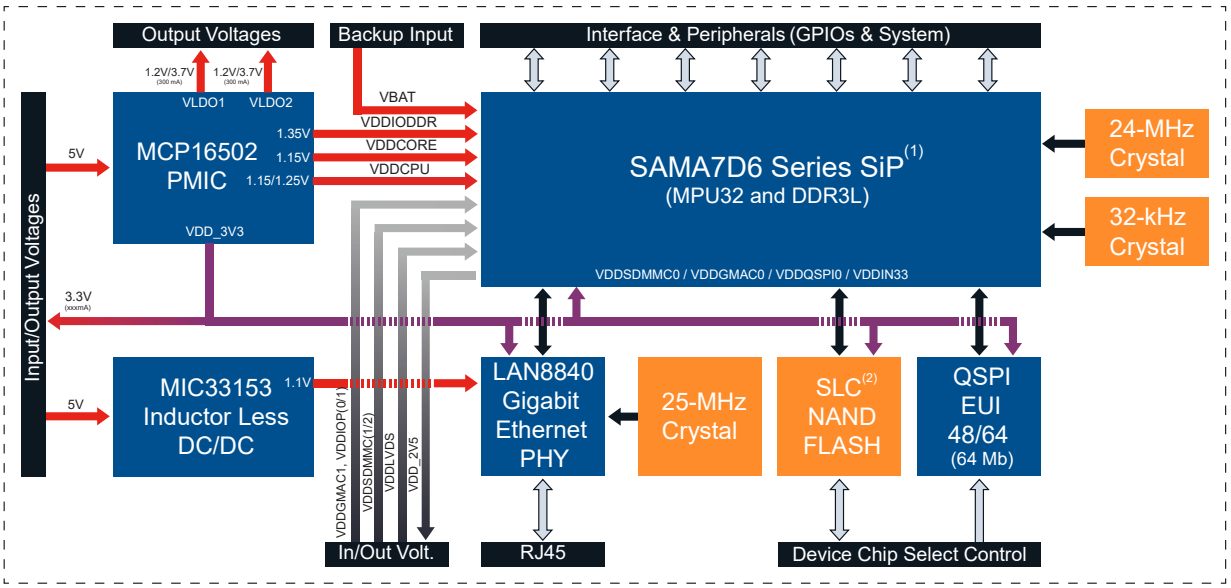
- Up to ten Flexible Serial Communication Controllers (FLEXCOM)
  - Universal Synchronous Asynchronous Receiver Transceiver (USART)
  - Two-Wire Interface (TWI)
  - Serial Peripheral Interface (SPI)
- Up to sixteen 12-bit ADC inputs, with a maximum of 1-Msps conversion rate
- Up to five CAN(FD) interfaces compliant with the CAN protocol version 2.0 Part A, B and ISO 11898-1
- Up to two SDMMC interfaces (MultiMedia Card/e.MMC) compliant with Specification V4.51, SD Memory Card Specification V3.0 and SDIO Specification V3.0
- One 4-lane LVDS or MIPI DSI® interface
- Audio interfaces with two I²S, two SSC, one SPDIF and up to eight microphones

Notes:

1. Read/write speed may vary depending on the NAND Flash reference fitted to the module. For more details, refer to the device data sheets.
2. Only available with 1-Gbit DDR3L SDRAM memory size (SAMA7D65D1G-V/4UB)
3. Only available with 2-Gbit DDR3L SDRAM memory size (SAMA7D65D2G-V/4UB)

6. Block Diagram

Figure 6-1. SAMA7D65 SOM Series Block Diagram



Notes:

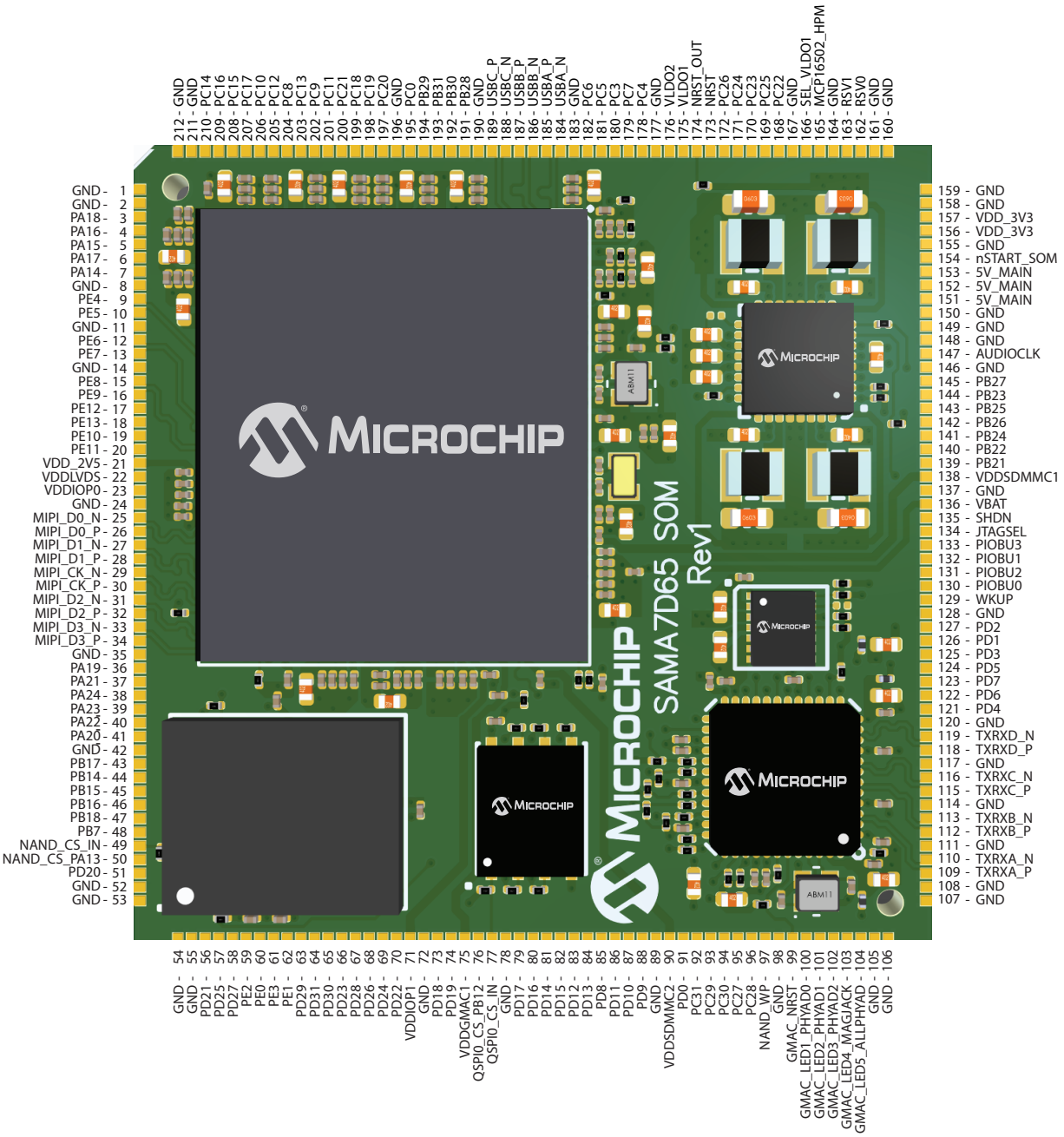
1. Several DDRx memory sizes are available depending on the memory configuration.
2. Several NAND Flash memory sizes are available depending on the memory configuration.

For more details, see Ordering Information.

7. Pinout

7.1 Pinout Overview

Figure 7-1. SAMA7D65 SOM Series Pin Assignment



7.2 Pin List

The following tables provide the SAMA7D65 SOM Series module pin description.

Important: Compared to the SAMA7D65 device, some PIO features are not listed. These features are used internally on the SAMA7D65 SOM Series and cannot have other uses.

The device features several PIO controllers that multiplex the I/O lines of the peripheral set. The following PIOx Pin Description tables define how the I/O lines are multiplexed on the different PIO controllers. The "Reset State" column shows whether the PIO line resets in I/O mode or in Peripheral mode. If I/O is shown, the PIO line resets with the characteristics (input, output, pull-up or pull-down) indicated in this same column, so that the device is configured in a known state as soon as the reset is released. As a result, PIO_CFGR.FUNC resets to '0'. If a signal name is shown in the "Reset State" column, the PIO line is assigned to this function and PIO_CFGR.FUNC is not set to '0'. That is the case for pins controlling memories, in particular address lines, which require the pin to be driven as soon as the reset is released.

7.2.1 PIOA Pin List

Table 7-1. PIOA Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State(1)	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
–	VDD_3V3	GPIOHS	NAND_WE_PA0	GPIO	–	C	NANDWE	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIOHS	NAND_ALE_PA1	GPIO	–	C	NANDALE	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIOHS	NAND_CLE_PA2	GPIO	–	C	NANDCLE	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIOHS	NAND_D0_PA3	GPIO	–	C	D0	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIOHS	NAND_D1_PA4	GPIO	–	C	D1	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIOHS	NAND_D4_PA5	GPIO	–	C	D4	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIOHS	NAND_D5_PA6	GPIO	–	C	D5	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIOHS	NAND_D6_PA7	GPIO	–	C	D6	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIOHS	NAND_D7_PA8	GPIO	–	C	D7	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIOHS	NAND_D2_PA9	GPIO	–	C	D2	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIOHS	NAND_D3_PA10	GPIO	–	C	D3	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIOHS	NAND_RDY_PA11	GPIO	–	C	NANDRDY	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIOHS	NAND_RE_PA12	GPIO	–	C	NRD/NANDOE	1	PIO, I, PU, ST	(2)
50	VDD_3V3	GPIOHS	NAND_CS_PA13	GPIO	–	C	NCS0/NANDCS0	1	PIO, I, PU, ST	(2)
7	VDDIOP0	GPIO	PA14	GPIO	–	A	FLEXCOM4_IO4	1	PIO, I, PU, ST	(3)
						C	FLEXCOM3_IO0	4		
5	VDDIOP0	GPIO	PA15	GPIO	–	A	FLEXCOM4_IO3	1	PIO, I, PU, ST	(3)
						C	FLEXCOM3_IO1	4		
4	VDDIOP0	GPIO	PA16	GPIO	–	A	FLEXCOM4_IO2	1	PIO, I, PU, ST	(3)
						D	PCK2	1		
						E	EXT_IRQ1	1		
6	VDDIOP0	GPIO	PA17	GPIO	–	A	FLEXCOM4_IO1	1	PIO, I, PU, ST	
3	VDDIOP0	GPIO	PA18	GPIO	–	A	FLEXCOM4_IO0	1	PIO, I, PU, ST	

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Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State(1)	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
36	VDDIOP0	GPIO	PA19	GPIO	–	A	TK0	1	PIO, I, PU, ST	
						C	FLEXCOM4_IO5	1		
						D	PWML0	3		
41	VDDIOP0	GPIO	PA20	GPIO	–	A	TD0	1	PIO, I, PU, ST	
						B	FLEXCOM3_IO4	2		
						C	FLEXCOM4_IO6	1		
						D	PWMH0	3		
37	VDDIOP0	GPIO	PA21	GPIO	–	A	TF0	1	PIO, I, PU, ST	
						B	FLEXCOM3_IO3	2		
						D	PWML1	3		
40	VDDIOP0	GPIO	PA22	GPIO	–	A	RD0	1	PIO, I, PU, ST	
						B	FLEXCOM3_IO2	2		
						C	PDMC0_DS1	1		
						D	PWMH1	3		
39	VDDIOP0	GPIO	PA23	GPIO	–	A	RK0	1	PIO, I, PU, ST	
						B	FLEXCOM3_IO1	2		
						C	PDMC0_CLK	1		
						D	PWML2	3		
38	VDDIOP0	GPIO	PA24	GPIO	–	A	RF0	1	PIO, I, PU, ST	
						B	FLEXCOM3_IO0	2		
						C	PDMC0_DS0	1		
						D	PWMH2	3		
–	VDD_3V3	GPIO	GMAC0_TXCTL_PA25	GPIO	–	A	G0_TXCTL	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIO	GMAC0_TX0_PA26	GPIO	–	A	G0_TX0	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIO	GMAC0_TX1_PA27	GPIO	–	A	G0_TX1	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIO	GMAC0_RXCTL_PA28	GPIO	–	A	G0_RXCTL	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIO	GMAC0_RX0_PA29	GPIO	–	A	G0_RX0	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIO	GMAC0_RX1_PA30	GPIO	–	A	G0_RX1	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIO	GMAC0_MDC_PA31	GPIO	–	A	G0_MDC	1	PIO, I, PU, ST	(2)

Notes:

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger
2. This feature is fixed due to the SAMA7D65 SOM Series internal connection.
3. Compared to SAMA7D65 SiP, this feature is limited, as it is partly used for other SAMA7D65 SOM Series features, for example GMAC or FLEXCOM.

7.2.2 PIOB Pin List

Table 7-2. PIOB Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State(1)	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
–	VDD_3V3	GPIO	GMAC0_MDIO_PB0	GPIO	--	A	G0_MDIO	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIO	GMAC0_TXCK_PB1	GPIO	--	A	G0_TXCK	1	PIO, I, PU, ST	(2)

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Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State(1)	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
–	VDD_3V3	GPIO	GMAC0_RX2_PB2	GPIO	--	A	G0_RX2	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIO	GMAC0_RXCK_PB3	GPIO	--	A	G0_RXCK	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIO	GMAC0_TX2_PB4	GPIO	--	A	G0_TX2	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIO	GMAC0_TX3_PB5	GPIO	--	A	G0_TX3	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIO	GMAC0_RX3_PB6	GPIO	--	A	G0_RX3	1	PIO, I, PU, ST	(2)
48	VDD_3V3	GPIO	PB7	GPIO	--	A	G0_TSUCOMP	1,2	PIO, I, PU, ST	(3)
						C	ADTRG	1		
–	VDD_3V3	GPIOHS	QSPI0_IO3_PB8	GPIO	--	A	QSPI0_IO3	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIOHS	QSPI0_IO2_PB9	GPIO	--	A	QSPI0_IO2	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIOHS	QSPI0_IO1_PB10	GPIO	--	A	QSPI0_IO1	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIOHS	QSPI0_IO0_PB11	GPIO	--	A	QSPI0_IO0	1	PIO, I, PU, ST	(2)
76	VDD_3V3	GPIOHS	QSPI0_CS_PB12	GPIO	--	A	QSPI0_CS	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIOHS	QSPI0_SCK_PB13	GPIO	--	A	QSPI0_SCK	1	PIO, I, PU, ST	(2)
44	VDD_3V3	GPIOHS	PB14	GPIO	--	C	I2SMCC0_CK	3	PIO, I, PU, ST	(3)
						E	PWMH3	1		
						G	FLEXCOM2_IO1	4		
45	VDD_3V3	GPIOHS	PB15	GPIO	--	C	I2SMCC0_WS	3	PIO, I, PU, ST	(3)
						E	PWML0	1		
						F	TCLK4	2		
						G	FLEXCOM2_IO0	4		
46	VDD_3V3	GPIOHS	PB16	GPIO	--	C	I2SMCC0_DIN0	3	PIO, I, PU, ST	(3)
						E	PWMH0	1		
						F	TIOB4	2		
43	VDD_3V3	GPIOHS	PB17	GPIO	--	C	I2SMCC0_DOUT0	3	PIO, I, PU, ST	(3)
						E	PWML1	1		
						F	TIOA4	2		
47	VDD_3V3	GPIOHS	PB18	GPIO	--	C	I2SMCC0_MCK	3	PIO, I, PU, ST	(3)
						E	PWMH1	1		
						F	TIOA5	2		
–	VDD_3V3	GPIOHS	FLEXCOM10_IO1_PB19	GPIO	--	D	FLEXCOM10_IO1	1	PIO, I, PU, ST	(2)
–	VDD_3V3	GPIOHS	FLEXCOM10_IO0_PB20	GPIO	--	D	FLEXCOM10_IO0	1	PIO, I, PU, ST	(2)
139	VDDSDMMC1	GPIOHS	PB21	GPIO	--	A	SDMMC1_RSTN	1	PIO, I, PU, ST	
						B	FLEXCOM6_IO4	2		
						C	TIOB2	2		
						D	ADTRG	2		
						E	EXT_IRQ0	2		
140	VDDSDMMC1	GPIOHS	PB22	GPIO	--	A	SDMMC1_CMD	1	PIO, I, PU, ST	
						B	FLEXCOM6_IO3	2		
						C	TCLK2	2		
144	VDDSDMMC1	GPIOHS	PB23	GPIO	--	A	SDMMC1_CK	1	PIO, I, PU, ST	
						B	FLEXCOM6_IO2	2		
						C	TIOA2	2		

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Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State(1)	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
141	VDDSDMMC1	GPIOHS	PB24	GPIO	--	A	SDMMC1_DAT0	1	PIO, I, PU, ST	
						B	FLEXCOM6_IO0	2		
143	VDDSDMMC1	GPIOHS	PB25	GPIO	--	A	SDMMC1_DAT1	1	PIO, I, PU, ST	
						B	FLEXCOM6_IO1	2		
						C	TIOB2	1		
142	VDDSDMMC1	GPIOHS	PB26	GPIO	--	A	SDMMC1_DAT2	1	PIO, I, PU, ST	
						B	FLEXCOM8_IO0	3		
						C	TCLK2	1		
145	VDDSDMMC1	GPIOHS	PB27	GPIO	--	A	SDMMC1_DAT3	1	PIO, I, PU, ST	
						B	FLEXCOM8_IO1	3		
						C	TIOA2	1		
191	VDD_3V3	GPIO	PB28	GPIO	AD12	A	SDMMC1_WP	1	PIO, I, PU, ST	
						C	FLEXCOM1_IO0	3		
						E	D15	1,2		
194	VDD_3V3	GPIO	PB29	GPIO	AD13	A	SDMMC1_CD	1	PIO, I, PU, ST	
						B	I2SMCC0_MCK	1		
						C	FLEXCOM1_IO1	3		
						E	D14	1,2		
192	VDD_3V3	GPIO	PB30	GPIO	AD14	A	SDMMC1_1V8SEL	1	PIO, I, PU, ST	
						B	I2SMCC1_MCK	1		
						C	FLEXCOM1_IO2	3		
						D	TIOA1	1		
						E	NCS1/NANDCS1	1,2		
193	VDD_3V3	GPIO	PB31	GPIO	HHSA_CC1	A	PCK7	2	PIO, I, PU, ST	
						B	I2SMCC1_DIN1	1		
						C	FLEXCOM1_IO3	3		
						D	TCLK1	1		
						E	NWE/NWR0/ NANDWE	2		

Notes:

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger
2. This feature is fixed due to the SAMA7D65 SOM Series internal connection.
3. Compared to SAMA7D65 SiP, this feature is limited, as it is partly used for other SAMA7D65 SOM Series features, for example GMAC or FLEXCOM.

7.2.3 PIOC Pin List

Table 7-3. PIOC Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State[1]	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
195	VDD_3V3	GPIO	PC0	GPIO	HHSA_CC2	A	PCK6	2	PIO, I, PU, ST	(3)
						B	I2SMCC1_DIN2	1		
						D	TIOB1	1		
						E	NWR1/NBS1	1,2		
--	VDD_3V3	GPIO	G0_INT	GPIO	--	--	--	--	PIO, I, PU, ST	(2)
--	VDD_3V3	GPIO	EXT_IRQ0_PC2	GPIO	--	--	--	--	PIO, I, PU, ST	(2)
180	VDD_3V3	GPIO	PC3	GPIO	AD0	A	SPDIF_RX	2	PIO, I, PU, ST	
						C	FLEXCOM9_IO0	2		
						D	FLEXCOM0_IO4	2		
						E	A10	1,2		
178	VDD_3V3	GPIO	PC4	GPIO	AD1	A	SPDIF_TX	2	PIO, I, PU, ST	
						C	FLEXCOM9_IO1	2		
						D	FLEXCOM0_IO3	2		
						E	D0	2		
181	VDD_3V3	GPIO	PC5	GPIO	AD2	A	I3CC_SDASPUE	1	PIO, I, PU, ST	
						B	I2SMCC1_DIN3	1		
						D	FLEXCOM0_IO2	2		
						E	D1	2		
182	VDD_3V3	GPIO	PC6	GPIO	AD3	A	I3CC_SCL	1	PIO, I, PU, ST	
						D	FLEXCOM0_IO1	2		
						E	D4	2		
179	VDD_3V3	GPIO	PC7	GPIO	AD4	A	I3CC_SDA	1	PIO, I, PU, ST	
						D	FLEXCOM0_IO0	2		
						E	D5	2		
204	VDD_3V3	GPIO	PC8	GPIO	ACC_INP1	A	I2SMCC0_DIN1	1	PIO, I, PU, ST	
						B	PDMC0_DS1	2		
						C	I2SMCC1_DOUT1	1		
						D	FLEXCOM9_IO0	1		
						E	D6	2		
202	VDD_3V3	GPIO	PC9	GPIO	ACC_INN1	A	I2SMCC0_DIN2	1	PIO, I, PU, ST	
						B	PDMC0_CLK	2		
						C	I2SMCC1_DOUT2	1		
						D	FLEXCOM9_IO1	1		
						E	D7	2		
206	VDD_3V3	GPIO	PC10	GPIO	AD5	A	I2SMCC0_DIN3	1	PIO, I, PU, ST	
						B	PDMC0_DS0	2		
						C	I2SMCC1_DOUT3	1		
						D	FLEXCOM9_IO2	1		
						E	D2	2		

.....continued

Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State(1)	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
201	VDD_3V3	GPIO	PC11	GPIO	AD6	A	I2SMCC0_DOUT1	1	PIO, I, PU, ST	
						B	PDMC1_DS0	1		
						D	FLEXCOM9_IO3	1		
						E	D3	2		
205	VDD_3V3	GPIO	PC12	GPIO	AD7	A	I2SMCC0_DOUT2	1	PIO, I, PU, ST	
						B	PDMC1_CLK	1		
						D	FLEXCOM9_IO4	1		
						E	A9	1,2		
203	VDD_3V3	GPIO	PC13	GPIO	AD8	A	I2SMCC0_DOUT3	1	PIO, I, PD, ST	
						B	PDMC1_DS1	1		
						E	A8	1,2		
210	VDD_3V3	GPIO	PC14	GPIO	AD9	A	I2SMCC1_DIN0	1	PIO, I, PD, ST	
						B	SPDIF_RX	3		
						C	FLEXCOM1_IO0	2		
						E	A7	1,2		
208	VDD_3V3	GPIO	PC15	GPIO	AD10	A	I2SMCC1_WS	1	PIO, I, PD, ST	
						B	PDMC1_DS1	2		
						C	FLEXCOM1_IO1	2		
						E	A6	1,2		
209	VDD_3V3	GPIO	PC16	GPIO	AD11	A	I2SMCC1_CK	1	PIO, I, PD, ST	
						B	PDMC1_CLK	2		
						C	FLEXCOM1_IO2	2		
						D	TIOA1	2		
						E	A5	1,2		
207	VDD_3V3	GPIO	PC17	GPIO	ACC_INP0	A	I2SMCC1_DOUT0	1	PIO, I, PU, ST	
						B	PDMC1_DS0	2		
						C	FLEXCOM1_IO3	2		
						D	TCLK1	2		
						E	A4	1,2		
199	VDD_3V3	GPIO	PC18	GPIO	ACC_INN2	A	I2SMCC0_DIN0	1	PIO, I, PU, ST	
						B	SPDIF_TX	3		
						C	FLEXCOM1_IO4	2		
						D	TIOB1	2		
						E	A3	1,2		
198	VDD_3V3	GPIO	PC19	GPIO	ACC_INP2	A	I2SMCC0_WS	1	PIO, I, PU, ST	
						B	PCK6	1		
						E	A2	1,2		
197	VDD_3V3	GPIO	PC20	GPIO	ACC_INN3	A	I2SMCC0_DOUT0	1	PIO, I, PU, ST	
						E	A1	1,2		
200	VDD_3V3	GPIO	PC21	GPIO	ACC_INP3	A	I2SMCC0_CK	1	PIO, I, PU, ST	
						B	PCK7	1		
						E	A0/NBS0	1,2		
168	VDD_3V3	GPIO	PC22	GPIO	AD15	A	NTRST	1	NTRST, PU, ST	
						E	NWAIT	1,2		

.....continued

Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State[1]	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
170	VDD_3V3	GPIO	PC23	GPIO	--	A	TCK_SWCLK	1	TCK_SWCLK, ST	
171	VDD_3V3	GPIO	PC24	GPIO	--	A	TMS_SWDIO	1	TMS_SWDIO, PU, ST	
169	VDD_3V3	GPIO	PC25	GPIO	--	A	TDI	1	TDI, PU, ST	
172	VDD_3V3	GPIO	PC26	GPIO	--	A	TDO	1	TDO, ST	
						E	A12	1,2		
95	VDDSDMMC2	GPIOHS	PC27	GPIO	--	A	SDMMC2_CMD	1	PIO, I, PU, ST	
						B	FLEXCOM8_IO0	2		
						D	TD1	2		
						E	D8	1,2		
96	VDDSDMMC2	GPIOHS	PC28	GPIO	--	A	SDMMC2_CK	1	PIO, I, PU, ST	
						B	FLEXCOM8_IO1	2		
						D	TF1	2		
						E	D9	1,2		
93	VDDSDMMC2	GPIOHS	PC29	GPIO	--	A	SDMMC2_DAT0	1	PIO, I, PU, ST	
						B	FLEXCOM8_IO2	2		
						D	TK1	2		
						E	D10	1,2		
						F	TCLK0	1		
94	VDDSDMMC2	GPIOHS	PC30	GPIO	--	A	SDMMC2_DAT1	1	PIO, I, PU, ST	
						B	FLEXCOM8_IO3	2		
						D	RD1	2		
						E	D11	1,2		
						F	TIOA0	1		
92	VDDSDMMC2	GPIOHS	PC31	GPIO	--	A	SDMMC2_DAT2	1	PIO, I, PU, ST	
						B	FLEXCOM8_IO4	2		
						C	PCK0	2		
						D	RK1	2		
						E	D12	1,2		
						F	TIOB0	1		

Notes:

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger
2. This feature is fixed due to the SAMA7D65 SOM Series internal connection.
3. Compared to SAMA7D65 SiP, this feature is limited, as it is partly used for other SAMA7D65 SOM Series features, for example GMAC or FLEXCOM.

7.2.4 PIOD Pin List

Table 7-4. PIOD Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State[1]	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
91	VDDSDMMC2	GPIOHS	PD0	GPIO	--	A	SDMMC2_DAT3	1	PIO, I, PU, ST	
						C	PCK1	2		
						D	RF1	2		
						E	D13	1,2		
126	VDDIOP1	GPIO	PD1	GPIO	--	A	SDMMC2_WP	1	PIO, I, PU, ST	
						B	FLEXCOM1_IO5	1		
						C	LCDC_HSYNC	2		
						D	FLEXCOM3_IO0	3		
127	VDDIOP1	GPIO	PD2	GPIO	--	A	SDMMC2_CD	1	PIO, I, PU, ST	
						B	FLEXCOM1_IO6	1		
						C	LCDC_VSYNC	2		
						D	FLEXCOM3_IO1	3		
125	VDDIOP1	GPIO	PD3	GPIO	--	A	SDMMC2_1V8SEL	1	PIO, I, PU, ST	
						B	FLEXCOM1_IO4	1		
						C	TIOA0	2		
						D	FLEXCOM3_IO2	3		
						E	EXT_IRQ1	3		
121	VDDIOP1	GPIO	PD4	GPIO	--	A	LCDC_HSYNC	1	PIO, I, PU, ST	
						B	FLEXCOM1_IO2	1		
						C	TIOB0	2		
						D	FLEXCOM7_IO1	3		
124	VDDIOP1	GPIO	PD5	GPIO	--	A	LCDC_VSYNC	1	PIO, I, PU, ST	
						B	FLEXCOM1_IO3	1		
						C	TCLK0	2		
						D	FLEXCOM7_IO0	3		
122	VDDIOP1	GPIO	PD6	GPIO	--	A	LCDC_PWM	1,2	PIO, I, PU, ST	
						B	FLEXCOM1_IO1	1		
						D	FLEXCOM7_IO2	3		
123	VDDIOP1	GPIO	PD7	GPIO	--	A	LCDC_DISP	1,2	PIO, I, PU, ST	
						B	FLEXCOM1_IO0	1		
						D	FLEXCOM7_IO3	3		
85	VDDIOP1	GPIO	PD8	GPIO	--	A	CANTX0	1	PIO, I, PU, ST	
						B	FLEXCOM7_IO0	1		
88	VDDIOP1	GPIO	PD9	GPIO	--	A	CANRX0	1	PIO, I, PU, ST	
						B	FLEXCOM7_IO1	1		
87	VDDIOP1	GPIO	PD10	GPIO	--	A	CANTX1	1	PIO, I, PU, ST	
						B	FLEXCOM7_IO2	1		
						C	TIOA1	3		
86	VDDIOP1	GPIO	PD11	GPIO	--	A	CANRX1	1	PIO, I, PU, ST	
						B	FLEXCOM7_IO3	1		
						C	TCLK1	3		

.....continued

Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State(1)	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
83	VDDIOP1	GPIO	PD12	GPIO	--	A	CANTX2	1	PIO, I, PU, ST	
						B	FLEXCOM7_IO4	1		
						C	TIOB1	3		
						D	PCK2	2		
						E	FLEXCOM3_IO3	3		
84	VDDIOP1	GPIO	PD13	GPIO	--	A	CANRX2	1	PIO, I, PU, ST	
						B	FLEXCOM5_IO4	1		
						C	TIOA2	3		
						D	PCK3	2		
81	VDDIOP1	GPIO	PD14	GPIO	--	A	CANTX3	1	PIO, I, PU, ST	
						B	FLEXCOM5_IO2	1		
						C	TIOB2	3		
82	VDDIOP1	GPIO	PD15	GPIO	--	A	CANRX3	1	PIO, I, PU, ST	
						B	FLEXCOM5_IO3	1		
						C	TCLK2	3		
80	VDDIOP1	GPIO	PD16	GPIO	--	A	CANTX4	1	PIO, I, PU, ST	
						B	FLEXCOM5_IO0	1		
79	VDDIOP1	GPIO	PD17	GPIO	--	A	CANRX4	1	PIO, I, PU, ST	
						B	FLEXCOM5_IO1	1		
73	VDDGMAC1	GPIO	PD18	GPIO	--	B	FLEXCOM6_IO0	4	PIO, I, PU, ST	
						C	CANTX1	2		
						D	PCK4	2		
74	VDDGMAC1	GPIO	PD19	GPIO	--	B	FLEXCOM6_IO1	4	PIO, I, PU, ST	
						C	CANRX1	2		
						D	PCK2	3		
51	VDDGMAC1	GPIO	PD20	GPIO	--	B	FLEXCOM6_IO2	4	PIO, I, PU, ST	
						C	I2SMCC1_MCK	2		
						D	PCK3	3		
56	VDDGMAC1	GPIO	PD21	GPIO	--	A	G1_TXCTL/G1_TXEN	1,2	PIO, I, PU, ST	
						B	FLEXCOM6_IO2	3		
						C	TK1	1		
70	VDDGMAC1	GPIO	PD22	GPIO	--	A	G1_TX0	1,2	PIO, I, PU, ST	
						B	FLEXCOM6_IO3	3,4		
						C	TF1	1		
66	VDDGMAC1	GPIO	PD23	GPIO	--	A	G1_TX1	1,2	PIO, I, PU, ST	
						B	FLEXCOM6_IO4	3,4		
						C	TD1	1		
69	VDDGMAC1	GPIO	PD24	GPIO	--	A	G1_RXCTL/G1_CRSDV	1,2	PIO, I, PU, ST	
						B	FLEXCOM6_IO0	3		
						C	RD1	1		
						E	PDMC0_DS1	3		

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Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral			Reset State(1)	Note
			Signal	Type		Func	Signal	IO Set	Signal, Dir, PU, PD, HiZ, ST	
57	VDDGMAC1	GPIO	PD25	GPIO	--	A	G1_MDC	1,2	PIO, I, PU, ST	
						B	FLEXCOM6_IO1	3		
						C	RK1	1		
						E	PDMC0_CLK	3		
68	VDDGMAC1	GPIO	PD26	GPIO	--	A	G1_MDIO	1,2	PIO, I, PU, ST	
						B	FLEXCOM7_IO4	2		
						C	RF1	1		
						D	I2SMCC1_DIN2	2		
						E	PDMC0_DS0	3		
58	VDDGMAC1	GPIO	PD27	GPIO	--	A	G1_RX0	1,2	PIO, I, PU, ST	
						B	FLEXCOM7_IO0	2		
						C	SPDIF_RX	1		
						D	I2SMCC1_DIN3	2		
67	VDDGMAC1	GPIO	PD28	GPIO	--	A	G1_RX1	1,2	PIO, I, PU, ST	
						B	FLEXCOM7_IO1	2		
						C	SPDIF_TX	1		
						D	I2SMCC1_DIN1	2		
63	VDDGMAC1	GPIO	PD29	GPIO	--	A	G1_REFCK/G1_TXCK	2,1	PIO, I, PU, ST	
						B	FLEXCOM7_IO2	2		
						C	I2SMCC1_DOUT3	2		
65	VDDGMAC1	GPIO	PD30	GPIO	--	A	G1_RX2	1	PIO, I, PU, ST	
						B	FLEXCOM7_IO3	2		
						C	I2SMCC1_DOUT1	2		
						D	PDMC1_DS1	3		
						E	G1_RXER	2		
64	VDDGMAC1	GPIO	PD31	GPIO	--	A	G1_RX3	1	PIO, I, PU, ST	
						B	FLEXCOM5_IO4	2		
						C	I2SMCC1_DOUT2	2		
						D	PDMC1_DS0	3		

Note:

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger

7.2.5 PIOE Pin List

Table 7-5. PIOE Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral				Reset State(1)	Note
			Signal	Type		Func	Signal		IO Set	Signal, Dir, PU, PD, HiZ, ST	
60	VDDGMAC1	GPIO	PE0	GPIO	--	A	G1_TX2	GPIO	1	PIO, I, PU, ST	
						B	FLEXCOM5_IO2	GPIO	2		
						C	I2SMCC1_DIN0	GPIO	2		
						D	PDMC1_CLK	GPIO	3		

.....continued

Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral				Reset State(1)	Note
			Signal	Type		Func	Signal		IO Set	Signal, Dir, PU, PD, HiZ, ST	
62	VDDGMAC1	GPIO	PE1	GPIO	--	A	G1_TX3	GPIO	1	PIO, I, PU, ST	
						B	FLEXCOM5_IO3	GPIO	2		
						C	I2SMCC1_WS	GPIO	2		
						D	PDMC0_DS1	GPIO	4		
59	VDDGMAC1	GPIO	PE2	GPIO	--	A	G1_RXCK	GPIO	1	PIO, I, PU, ST	
						B	FLEXCOM5_IO1	GPIO	2		
						C	I2SMCC1_CK	GPIO	2		
						D	PDMC0_CLK	GPIO	4		
61	VDDGMAC1	GPIO	PE3	GPIO	--	A	G1_TSUCOMP	GPIO	1,2	PIO, I, PU, ST	
						B	FLEXCOM5_IO0	GPIO	2		
						C	I2SMCC1_DOUT0	GPIO	2		
						D	PDMC0_DS0	GPIO	4		
9	VDDLVDS	GPIO	PE4	GPIO	LVDS_D0_N	A	LCDC_DAT0	GPIO	1,2	PIO, I, PU, ST	
						B	FLEXCOM2_IO2	GPIO	1		
						C	PWML0	GPIO	2		
						D	TIOA3	GPIO	1		
						E	I2SMCC0_DIN1	GPIO	2		
10	VDDLVDS	GPIO	PE5	GPIO	LVDS_D0_P	A	LCDC_DAT1	GPIO	1,2	PIO, I, PU, ST	
						B	FLEXCOM2_IO3	GPIO	1		
						C	PWMH0	GPIO	2		
						D	TIOB3	GPIO	1		
						E	I2SMCC0_DIN2	GPIO	2		
12	VDDLVDS	GPIO	PE6	GPIO	LVDS_D1_N	A	LCDC_DAT2	GPIO	1,2	PIO, I, PU, ST	
						B	FLEXCOM2_IO4	GPIO	1		
						C	PWML1	GPIO	2		
						D	TCLK3	GPIO	1		
						E	I2SMCC0_DIN3	GPIO	2		
13	VDDLVDS	GPIO	PE7	GPIO	LVDS_D1_P	A	LCDC_DAT3	GPIO	1,2	PIO, I, PU, ST	
						B	FLEXCOM2_IO5	GPIO	1		
						C	PWMH1	GPIO	2		
						D	TIOA4	GPIO	1		
						E	I2SMCC0_DOUT1	GPIO	2		
15	VDDLVDS	GPIO	PE8	GPIO	LVDS_D2_N	A	LCDC_DAT4	GPIO	1,2	PIO, I, PU, ST	
						B	FLEXCOM2_IO0	GPIO	1		
						C	PWML2	GPIO	2		
						D	TIOB4	GPIO	1		
						E	I2SMCC0_CK	GPIO	2		
16	VDDLVDS	GPIO	PE9	GPIO	LVDS_D2_P	A	LCDC_DAT5	GPIO	1,2	PIO, I, PU, ST	
						B	FLEXCOM2_IO1	GPIO	1		
						C	PWMH2	GPIO	2		
						D	TCLK4	GPIO	1		
						E	I2SMCC0_WS	GPIO	2		

.....continued

Pad No.	Power Rail	I/O Type	Primary		Alternate Signal	PIO Peripheral				Reset State[1]	Note
			Signal	Type		Func	Signal		IO Set	Signal, Dir, PU, PD, HiZ, ST	
19	VDDLVDS	GPIO	PE10	GPIO	LVDS_D3_N	A	LCDC_DAT6	GPIO	1,2	PIO, I, PU, ST	
						B	FLEXCOM2_IO6	GPIO	1		
						C	PWML3	GPIO	2		
						D	TIOA5	GPIO	1		
						E	I2SMCC0_DOUT2	GPIO	2		
20	VDDLVDS	GPIO	PE11	GPIO	LVDS_D3_P	A	LCDC_DAT7	GPIO	1,2	PIO, I, PU, ST	
						C	PWMH3	GPIO	2		
						D	TIOB5	GPIO	1		
						E	I2SMCC0_DOUT3	GPIO	2		
17	VDDLVDS	GPIO	PE12	GPIO	LVDS_CLK_N	A	LCDC_DEN	GPIO	1,2	PIO, I, PU, ST	
						B	PCK3	GPIO	4		
						C	PWMEXTRG0	GPIO	2		
						D	TCLK5	GPIO	1		
						E	I2SMCC0_DIN0	GPIO	2		
18	VDDLVDS	GPIO	PE13	GPIO	LVDS_CLK_P	A	LCDC_PCK	GPIO	1,2	PIO, I, PU, ST	
						B	PCK4	GPIO	3		
						C	PWMEXTRG1	GPIO	2		
						E	I2SMCC0_DOUT0	GPIO	2		

Note:

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger

7.2.6 System Pin List

Table 7-6. System Pin Description

Pin No.	Pin Name	Power Rail	I/O Type	Description	Active Level
29	MIPI_CK_N	VDD_2V5	PHY	MIPI DPHY negative differential output clock lane	–
30	MIPI_CK_P	VDD_2V5	PHY	MIPI DPHY positive differential output clock lane	–
25	MIPI_D0_N	VDD_2V5	PHY	MIPI DPHY negative differential output data lane 0	–
26	MIPI_D0_P	VDD_2V5	PHY	MIPI DPHY positive differential output data lane 0	–
27	MIPI_D1_N	VDD_2V5	PHY	MIPI DPHY negative differential output data lane 1	–
28	MIPI_D1_P	VDD_2V5	PHY	MIPI DPHY positive differential output data lane 1	–
31	MIPI_D2_N	VDD_2V5	PHY	MIPI DPHY negative differential output data lane 2	–
32	MIPI_D2_P	VDD_2V5	PHY	MIPI DPHY positive differential output data lane 2	–
33	MIPI_D3_N	VDD_2V5	PHY	MIPI DPHY negative differential output data lane 3	–
34	MIPI_D3_P	VDD_2V5	PHY	MIPI DPHY positive differential output data lane 3	–
185	USBA_P	VDD_3V3	USBPHY	USB host port A high-speed data +	–
184	USBA_N	VDD_3V3	USBPHY	USB host port A high-speed data -	–

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Pin No.	Pin Name	Power Rail	I/O Type	Description	Active Level
187	USBB_P	VDD_3V3	USBPHY	USB host port B high-speed data +	–
186	USBB_N	VDD_3V3	USBPHY	USB host port B high-speed data -	–
189	USBC_P	VDD_3V3	USBPHY	USB host port C high-speed data +	–
188	USBC_N	VDD_3V3	USBPHY	USB host port C high-speed data -	–
130	PIOBU0	VBAT	Backup I/O	Tamper input/output 0 / Wake-up 2 input	–
132	PIOBU1	VBAT	Backup I/O	Tamper input/output 1 / Wake-up 3 input	–
131	PIOBU2	VBAT	Backup I/O	Tamper input/output 2 / Wake-up 4 input	–
133	PIOBU3	VBAT	Backup I/O	Tamper input/output 3 / Wake-up 5 input	–
134	JTAGSEL	VBAT	Backup I/O	JTAG selection	–
129	WKUP	VBAT	Backup I/O	Wake-up input. 100 kΩ internal pull-up.	–
135	SHDN	VBAT	Backup I/O	Shutdown control	Low
173	NRST	VDD_3V3	Input/Output	External nReset input/output. 10 kΩ internal pull-up.	Low
174	NRST_OUT	VDD_3V3	Output I/O	Microprocessor reset output	Low
147	AUDIOCLK	VDD_3V3	Output	Audio clock output	–
162	RSV0	–	–	Reserved. Connect to GND.	–
163	RSV1	–	–	Reserved. Connect to GND.	–
97	NAND_WP	VDD_3V3	Input	NAND Flash write protect. 100 kΩ internal pull-up.	Low
49	NAND_CS_IN	VDD_3V3	Input	NAND Flash chip select input. 100 kΩ internal pull-up.	Low
77	QSPI0_CS_IN	VDD_3V3	Input	NOR Flash chip select input. 10 kΩ internal pull-up.	Low
109	TXRXA_P	VDD_1V1_ETH	Input/Output	Physical receive or transmit signal (+ differential)	–
110	TXRXA_M	VDD_1V1_ETH	Input/Output	Physical receive or transmit signal (– differential)	–
112	TXRXB_P	VDD_1V1_ETH	Input/Output	Physical receive or transmit signal (+ differential)	–
113	TXRXB_M	VDD_1V1_ETH	Input/Output	Physical receive or transmit signal (– differential)	–
115	TXRXC_P	VDD_1V1_ETH	Input/Output	Physical receive or transmit signal (+ differential)	–
116	TXRXC_M	VDD_1V1_ETH	Input/Output	Physical receive or transmit signal (– differential)	–
118	TXRXD_P	VDD_1V1_ETH	Input/Output	Physical receive or transmit signal (+ differential)	–
119	TXRXD_M	VDD_1V1_ETH	Input/Output	Physical receive or transmit signal (– differential)	–
104	GMAC_LED5_ALLPHYAD	VDD_3V3	Input/Output	Programmable LED5 output/PHY Address Strap pin	–
103	GMAC_LED4_MAGJACK	VDD_3V3	Input/Output	Programmable LED4 output/MagJack register settings. 10 kΩ internal pull-up.	–
102	GMAC_LED3_PHYAD2	VDD_3V3	Input/Output	Programmable LED3 output/PHYAD2	–
101	GMAC_LED2_PHYAD1	VDD_3V3	Input/Output	Programmable LED2 output/PHYAD1	–
100	GMAC_LED1_PHYAD0	VDD_3V3	Input/Output	Programmable LED1 output/PHYAD0	–
99	GMAC_NRST	VDD_3V3	Input	Gigabit PHY reset line. 10 kΩ internal pull-up.	Low
166	SEL_VLDO1	5V_MAIN	Input	VLDO1 Default Output Voltage Selection pin. Three-state input.	–
165	MCP16502_HPM	5V_MAIN	Input	High-Power Mode Input pin. In combination with PWRHLD and LPM, this pin defines the MCP16502 power mode status.	High

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Pin No.	Pin Name	Power Rail	I/O Type	Description	Active Level
154	nSTART_SOM	5V_MAIN	Input/Pull-up	Start event input. Drives nSTART_SOM to low to initiate a start-up sequence. nSTART_SOM is pulled up internally. A capacitor can be connected to automatically initiate a power-up sequence when the main supply rises.	Low

7.2.7 Power Pin List

Table 7-7. Power Pin Description

Pin No.	Pin Name	Type	Description
136	VBAT	Input power	Backup voltage input
75	VDDGMAC1	Input power	VDDGMAC1 voltage input
23	VDDIOP0	Input power	VDDIOP0 voltage input
71	VDDIOP1	Input power	VDDIOP1 voltage input
138	VDDSDMMC1	Input power	VDDSDMMC1 voltage input
90	VDDSDMMC2	Input power	VDDSDMMC2 voltage input
21	VDD_2V5	Output power	VDD_2V5 voltage output
22	VDDLVDS	Input power	VDDLVDS voltage input
151, 152, 153	5V_MAIN	Input power	5V main input supply
156, 157	VDD_3V3	Output power	3.3V I/Os voltage output
175	VLDO1	Output power	VLDO1 output voltage
176	VLDO2	Output power	VLDO2 output voltage
1, 2, 8, 11, 14, 24, 35, 42, 52, 53, 54, 55, 72, 78, 89, 98, 105, 106, 107, 108, 111, 114, 117, 120, 128, 137, 146, 148, 149, 150, 155, 158, 159, 160, 161, 164, 167, 177, 183, 190, 196, 211, 212	GND	Ground	Ground connection

8. Power Considerations

8.1 Power Supplies

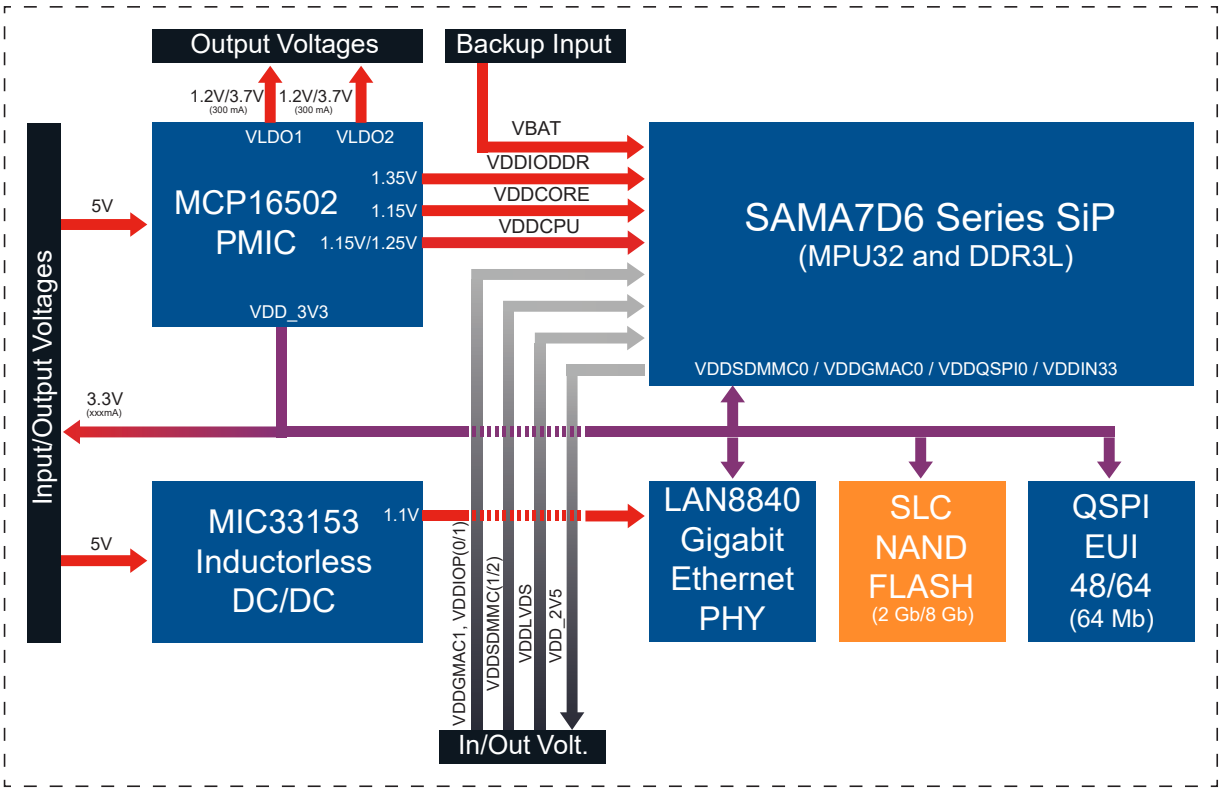
Table 8-1. SAMA7D65 SOM Series Power Supplies

Pin No.	Name	Power Type	Output Current Capability	Power Domain
136	VBAT	Input	–	Backup supply input
75	VDDGMAC1	Input	–	VDDGMAC1 power rail supply input
23	VDDIOP0	Input	–	VDDIOP0 power rail supply input
71	VDDIOP1	Input	–	VDDIOP1 power rail supply input
138	VDDSDMMC1	Input	–	VDDSDMMC1 power rail supply input
90	VDDSDMMC2	Input	–	VDDSDMMC2 power rail supply input
156, 157	VDD_3V3	Output	(*) mA	I/O supply and customer application output
151, 152, 153	5V_MAIN	Input	–	System power input
175	VLDO1	Output	300 mA	Adjustable output depending on application settings
176	VLDO2	Output	300 mA	Adjustable output depending on application settings
21	VDD_2V5	Output	N/A	2.5V output for LVDS interface. Do not use for any other purpose.
22	VDDLVDS	Input	–	I/O supply LVDS interface supply input

Note: (*) denotes data that will be forthcoming in the final data sheet publication.

The Microchip SAMA7D65 System-On-Module Series is supplied by a unique input (5V_MAIN) and its internal supplies are all delivered by a power management unit (MCP16502) and a DC/DC (MIC33153), as shown in the following figure.

Figure 8-1. SAMA7D65 SOM Series Power Architecture



8.2 Power-Up/Down Considerations

8.2.1 System Power-Up

At power-up, from a power supply sequencing perspective, the SAMA7D65 SOM Series power supplies are categorized into eight independent groups:

- 5V_MAIN (main supply)
- VBAT (backup supply)
- VDD_3V3 (internal periphery group) containing VDDIN33, VDDQSPI0, VDDSDMMC0 and VDDGMAC0 inputs
- VDD_1V1_ETH supply (internal Ethernet core group)
- External VDD_PERIPH (external periphery group) containing VDDGMAC1, VDDSDMMC1, VDDSDMMC2, VDDIOP0 and VDDIOP1 inputs
- VDDLVDS and VDDMIPI supplies (video group)
- VDDIODDR supply (memory group)
- VDDCORE and VDDCPU supplies (core group)

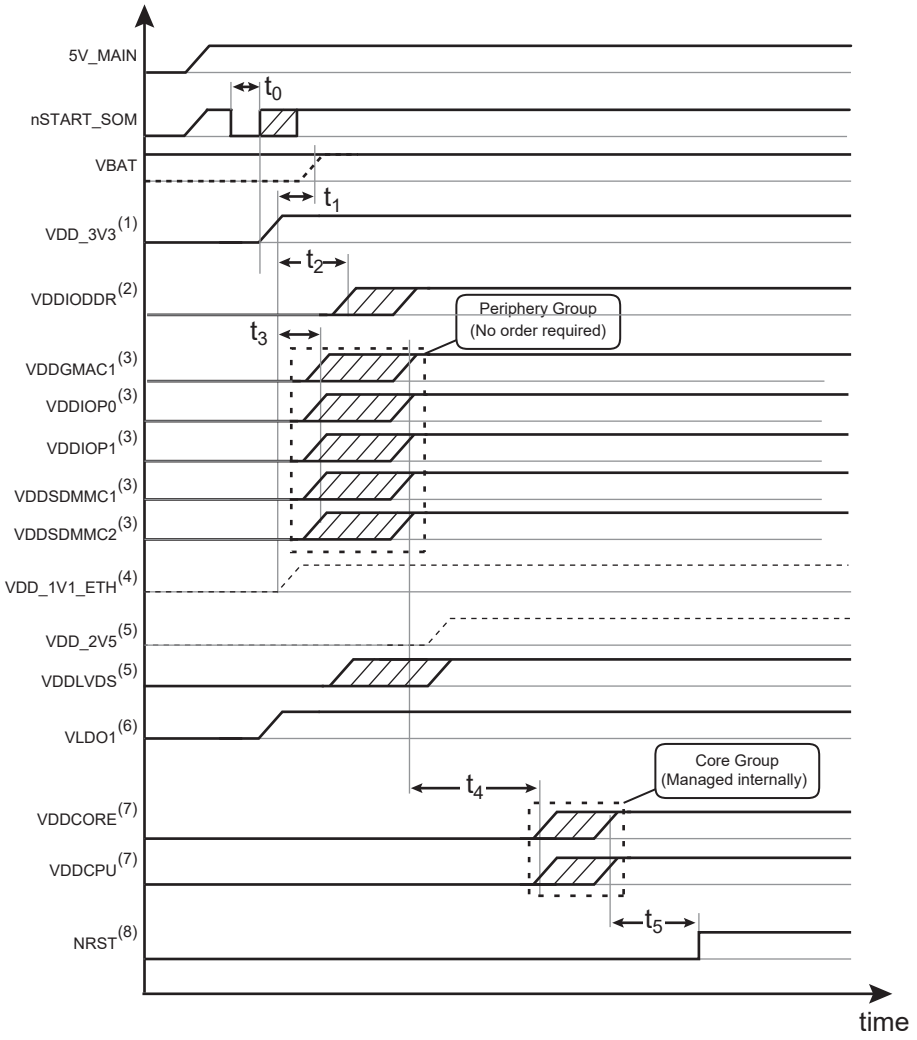
Figure 8-2 shows the recommended power-up sequence.

Note:

- VBAT
  - When supplied from a precharged storage element (battery, supercapacitor or micro-battery), VBAT is an always-on supply input and is therefore not part of the power supply sequencing.

  - When no storage element is used on VBAT in the application, VBAT must be tied to VDD_3V3.
  - When a supercapacitor or a micro-battery is used in the application to power VBAT in Backup mode, this element must be isolated from VBAT during its (slow) charge, so that VBAT closely follows VDD_3V3. In Table 8-2, the parameter t_1 limits the delay to establish VBAT after VDD_3V3.
- VDD_2V5 is the output of the internal 2.5V regulator; therefore, there is no power supply requirement on this pin.

Figure 8-2. Recommended Power-Up Sequence



Notes:

1. VDD_3V3 is generated internally by the MCP16502 PMIC and directly supplies the internal periphery group.
2. VDDIODDR is generated internally by the MCP16502 PMIC and directly supplies the memory group.
3. This group is supplied externally and requires no specific order. Only timing t_3 must be respected.
4. VDD_1V1_ETH is generated internally by the MIC33153 and directly supplies the internal Ethernet core group.
5. VDD_2V5 is generated internally by the SAMA7D65 SiP device and can be used to directly supply the internal video group.
6. VLDO1 is started at the same time as VDD_3V3. It is the default state at the first start-up. The VLDO1 “On” condition can be changed by the I²C interface.
7. VDDCORE and VDDCPU are generated internally by the MCP16502 PMIC and directly supplies the core and cpu groups.
8. The RESET general signal is generated internally by the MCP16502 PMIC and distributed throughout the whole system.

Table 8-2. Power-Up Timing Requirements

Symbol	Parameter	Conditions(1)	Min	Typ(2)	Max	Unit
t_0	nSTART_SOM deglitch time	From nSTART_SOM pin falling edge	–	0.5	–	ms
t_1	VBAT delay	Delay from established VDD_3V3 to established VDDBU	–	–	0.2	ms
t_2	VDD_3V3 to Memory group delay	Delay from established VDD_3V3 to the VDDIODDR supply turn-on	–	8	–	ms
t_3	VDD_3V3 to External Periphery group delay (3)	Delay from established VDD_3V3 to the external periphery group established supply	0	–	t_2	ms
t_4	Periphery group to VDDCORE, VDDCPU delay	Delay from the periphery group established supply to the VDDCORE, VDDCPU supplies turn-on	–	4	–	ms
t_5	Reset delay at power-up	From established VDDCORE to NRST high	–	16	–	ms

Notes:

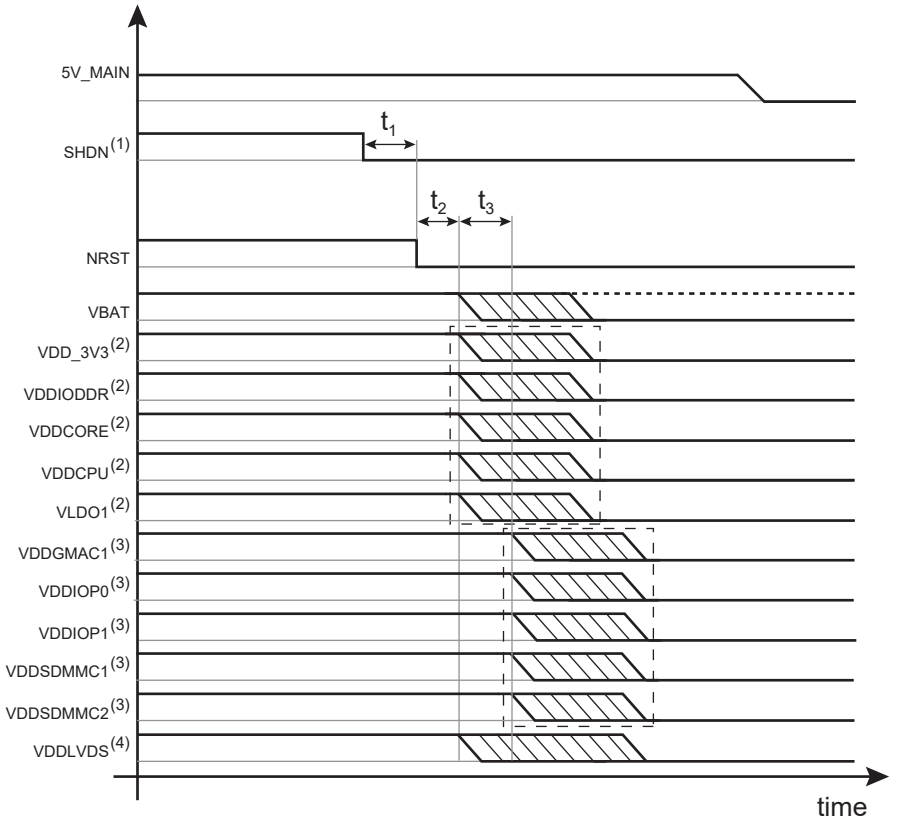
1. The term "established" refers to a power supply having reached 90% of its final value.
2. Typical timing values can be programmed in MCP16502 PMIC registers (RSTDLY[2:0]), but they must follow the timing sequence required by the SAMA7D65 SiP device.
3. If one of the power inputs of the group is supplied externally, the power must be applied at the same time or after the presence of VDD_3V3 and before the presence of VDDIODDR.

8.2.2 System Power-Down

The following figure shows the SAMA7D65 SOM Series power-down sequence that starts by asserting the SHDN line to "0".

Once SHDN and NRST are asserted, the supply inputs can be immediately shut down without any specific timing or order. VBAT may not be shut down if the application uses a backup storage element on this supply input.

Figure 8-3. Recommended Power-Down Sequence



Notes:

1. SHDN is generated internally by a software request from the SAMA7D65 SiP device.
2. All these signals and power rails are controlled internally by the MCP16502 PMIC and are switched off at the same time.
3. This group is supplied externally and there is no order required on this supply group. Only timing t_3 must be respected.
4. VDDLVDS is automatically switched off, as described in the above figure, if it is connected to VDD_2V5.

Table 8-3. Power-Down Timing Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_1	SHDN to NRST delay at power-down	Delay from SHDN asserted to NRST generation	0	–	50	µs
t_2	NRST delay at power-down	Delay from NRST asserted to first supply turn-off	0	–	10	µs
t_3	External supply delay at power-down	Delay from NRST asserted to external supplies turn-off	t_2	–	1	ms

8.2.3 Particular Considerations

Using the MCP16502 PMIC, the system can be configured for automatic start-up (see Power Management Unit). Start-up occurs as soon as 5V_MAIN voltage is present, provided that an external capacitor is between nSTART_SOM signal (pin 154) and GND.

For this configuration, the external capacitor value must be selected with great care. The recommendations described in the MCP16502 PMIC data sheet under "nSTRT Capacitor for

Automatic Turn-On on VIN ramping" must be followed. For more information, refer to the MCP16502 PMIC data sheet (see Reference Documents).

8.3 Power Management Unit

The Microchip SAMA7D65 System-On-Module Series is supplied by an external 5V supply (5V_MAIN) and generates its own internal supplies by interfacing with the Microchip MCP16502 power management unit.

The MCP16502 is a fully-featured Power Management Integrated Circuit (PMIC), cost and size-optimized for Microchip MPU devices such as the SAMA7D65 SiP.

The MCP16502 PMIC integrates four DC-DC buck regulators used for system supply and two auxiliary LDOs for customer purposes.

- All buck channels can support loads up to 1A. All bucks are 100% duty-cycle capable.
  - DCDC1, set to 3.3 V, supplies all pads of the embedded devices. This power rail offers an xxx mA (*) load to customer applications through VDD_3V3 (pins 156, 157).
    Note: (*) denotes data that will be forthcoming in the final data sheet publication.
  - DCDC2, set to 1.35V, supplies the DDR3L memory. It is used internally only.
  - DCDC3, set to 1.15V, supplies the microprocessor core. It is used internally only.
  - DCDC4, set to 1.15V, supplies the microprocessor CPU. It is used internally only.
- One 300 mA LDO is provided so that sensitive analog loads can be supported. The LDO output voltage, named VLDO1 (pin 175), is configured by a three-state signal named SEL_VLDO1 (pin 166) at power-up and can deliver 1.8V, 2.5V or 3.3V. Other voltage values can be reached after system initialization by an I²C interface access.
- One 300 mA LDO is provided so that sensitive analog loads can be supported. The LDO output voltage, named VLDO2 (pin 176), is disabled by default at power-up. Output voltage values are set through an I²C interface access after system initialization.

The default power channel sequencing is built-in as required by the Microchip SAMA7D65 MPU device.

Active discharge resistors are provided on each output. All buck channels support safe start-up into pre-biased outputs.

The MCP16502 is available in a 5 mm x 5 mm 32-pin VQFN package.

For more information, refer to the MCP16502 PMIC data sheet (see Reference Documents).

The VLDO1 voltage output of the LDO is controlled at boot by configuration of SEL_VLDO1 (pin 166). The default values are selectable among three options corresponding to three different states of the relevant pin: connected to ground (Low), connected to input supply (High) or left unconnected (High-Z). The VLDO1 default voltage can be selected by means of the SEL_VLDO1 pin, as shown in the table below.

Table 8-4. VLDO1 Voltage vs SEL_VLDO1 Pin

SEL_VLDO1 Status	VLDO1 Voltage
Low (grounded)	1.8V
High-Z (not connected)	2.5V
High (up to 5V_MAIN)	3.3V

The LPM pin of the Microchip SAMA7D65 System-On-Module Series, combined with the HPM and PWRHLD status pins of the MCP16502 PMIC, defines different power states as illustrated in the table below.

Table 8-5. MCP16502 Default Power States

PWRHLD	LPM	HPM	Buck1	Buck2	Buck3	Buck4	LDO1	LDO2	nRST	Power State(1)
0	0	0	Off	Off	Off	Off	Off	Off	Low	Off
0	1	0	Off	On(2)	Off	On(2)	Off	Off	Low	Hibernate mode
1	1	0	On(2)	On(2)	On(2)	On(2)	On	Off	HiZ	Low-Power mode
1	0	0	On(3)	On(3)	On(3)	On(3)	On	Off	HiZ	Active mode
1	0	1	On(3)	On(3)	On(3)	On(3)	On	Off	HiZ	High-Performance Active

Notes:

1. Only allowed modes are listed. If some PWRHLD/LPM/HPM combination is not listed, the mode is not allowed.
2. In this mode, the DCDC is configured in Automatic Pulse-Frequency Modulation (Auto-PFM) mode.
3. In this mode, the DCDC is configured in Force Pulse-Width Modulation (FPWM) mode.

For more information about the use of the MCP16502 PMIC LPM feature, refer to the MCP16502 data sheet (see Reference Documents).

8.4 Power Configurations

Three different configurations, depending on customer use, are available.

- Single supply — The SAMA7D65 SOM Series can be supplied by only one input supply (for example, a 5V AC/DC wall adapter) and other input supplies can be connected to the internal 3.3V regulator VDD_3V3. All the PIO lines are supplied at 3.3V.
- Multiple supplies — The SAMA7D65 SOM Series can be supplied by a 5V supply and a backup battery. Some PIO lines, such as VDDIOPx, VDDSDMMCx, are supplied by different LDOs for specific applications.
- Multiple supplies with LVDS — The SAMA7D65 SOM Series can be supplied by a 5V supply and a backup battery. Some PIO lines, such as VDDIOPx and VDDSDMMCx, are supplied by different LDOs for specific applications. The VDDLVDS power line is supplied by the VDD_2V5 output supply.

Figure 8-4. SAMA7D65 SOM Series Single Supply Connection Example

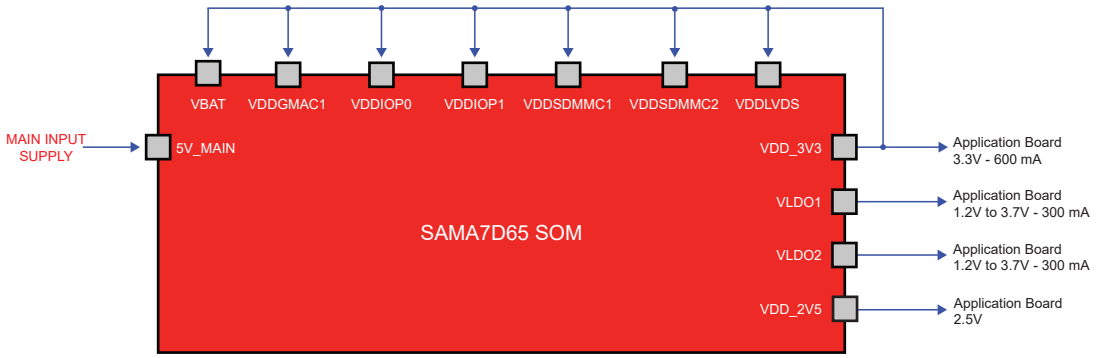


Figure 8-5. SAMA7D65 SOM Series Multiple Supplies Connection Example

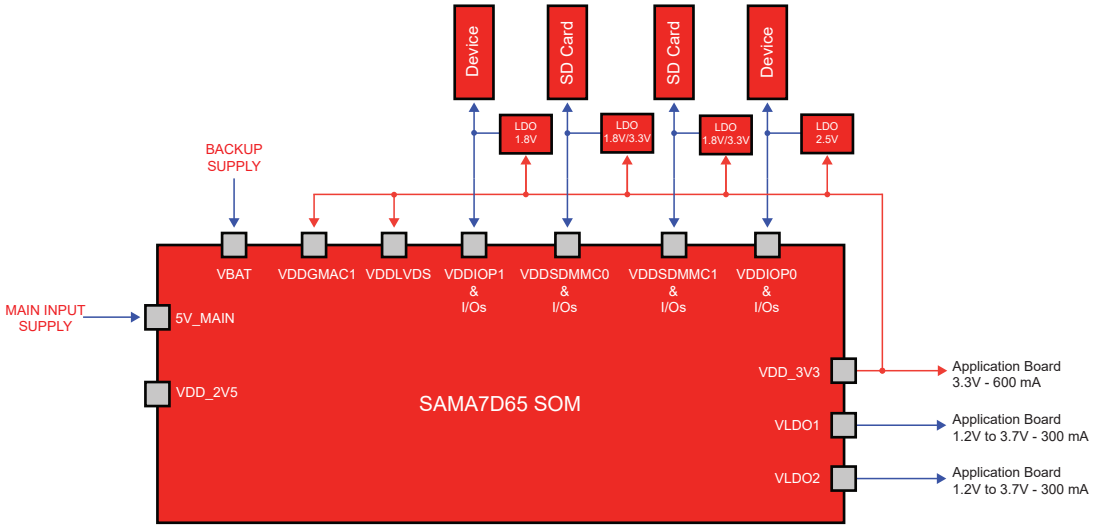
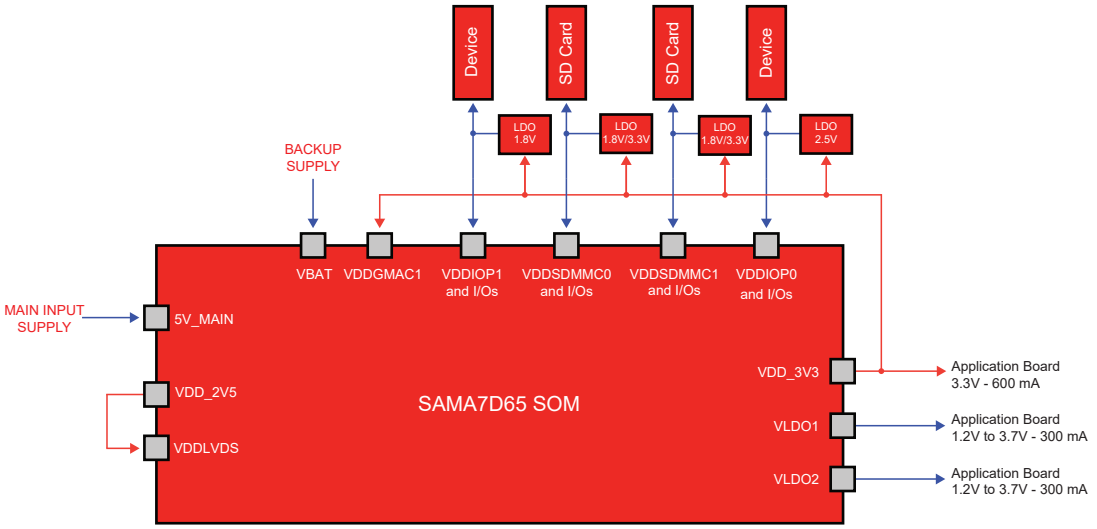


Figure 8-6. SAMA7D65 SOM Series Multiple Supplies with LVDS Connection Example



9. MPU and Memory Subsystem

9.1 SAMA7D65 System-in-Package (SiP)

The Microchip SAMA7D65 System-On-Module Series embeds the SAMA7D65 SiP Series, which integrates the Arm Cortex-A7 CPU-based SAMA7D65 MPU with an up to 2-Gbit DDR3L SDRAM (depending on the configuration) in a single package.

By combining the SAMA7D65 with a DDRx memory in a single package, PCB routing complexity, area and number of layers are reduced. This makes board design easier and more robust by facilitating design for EMI, ESD and signal integrity.

For more information, refer to the SAMA7D65 SiP Series data sheet (see Reference Documents).

The SAMA7D65 SiP Series is available in an 18 mm x 21 mm 427-ball TFBGA package.

The Microchip SAMA7D65 System-On-Module Series provides global system Reset (NRST, NRST_OUT) and Shutdown (SHDN) pins to the application board.

Notes:

- The NRST signal is an input/output pin generated by the MCP16502 internal Power Management Unit, respecting the microprocessor power sequence timing. It is distributed internally to the microprocessor and can be forced externally for system-level control.
- The NRST_OUT signal is an output pin generated by the SAMA7D65 reset controller. In the customer application, it can be used to reset specific interfaces such as the Ethernet PHY, Wireless Solution or another device.
- The SHDN pin is an output pin managed by the application software. In an application case, the pin can switch on/off the 5V_MAIN external main supply.

9.2 MPU Clocks

Two clock sources are necessary for the module microprocessor:

- A small size 24-MHz crystal to generate the SAMA7D65 MPU main clock.
- A small size 32.768-kHz crystal to generate the slow clock oscillator input and feed the embedded RTC of the SAMA7D65 MPU.

9.3 NAND Flash Memory

The Microchip SAMA7D65 System-On-Module Series embeds an SLC NAND Flash memory supported through its External Bus Interface (EBI) controller with different memory sizes depending on the part number.

The System-On-Module implements one of the following references, depending on the memory space. All are available in a VFBGA-63 package.

- 2-Gbit memory size(1)(2)
  - Macronix MX30LF2G28AD-XKI
  - Micron MT29F2G08ABAEAH4-IT
- 8-Gbit memory size
  - Macronix MX60LF8G28AD-XKI

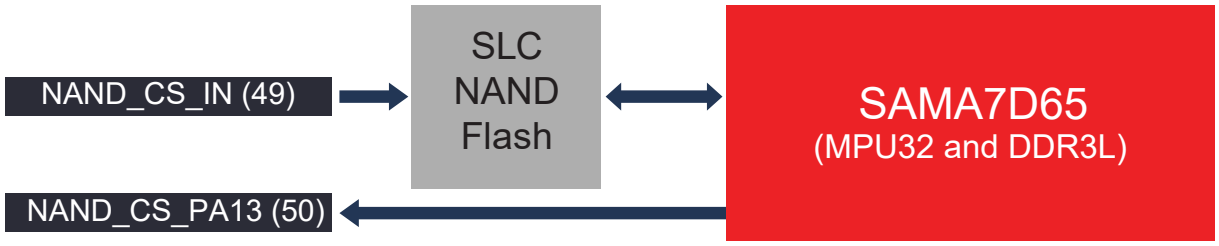
Notes:

1. Either one of the references that follow can be mounted on the Microchip SAMA7D65 System-On-Module Series.
2. Read/write speed may vary depending on the NAND Flash reference fitted to the module. For more details, refer to the device data sheets.

The software must be adapted to recognize the relevant NAND Flash manufacturer. Microchip Linux distribution supports all references. For details on how to build Linux software, refer to www.linux4microchip.com/.

The NAND_CS_IN signal (pin 49) is accessible externally and can be uncoupled from the NAND_CS_PA13 signal (pin 50) so that the boot can be unselected from the NAND Flash memory during debug phases.

Figure 9-1. NAND Flash Memory Block Diagram



9.4 QSPI NOR Memory

The Microchip SAMA7D65 System-On-Module Series embeds the SST26VF064BEUIT-104I/MF, a 64 Mbit Serial Quad I/O Flash memory.

The SST26VF064BEUI SQI features a 6-wire, 4-bit I/O interface that allows for low-power, high-performance operation in a low pin-count package.

The SST26VF064BEUI also embeds EUI-48 and EUI-64 MAC addresses.

The SST26VF064BEUI is available in an 8-lead 6×5 mm WDFN package. For more information, refer to the SST26VF064BEUI data sheet (see Reference Documents).

Figure 9-2. QSPI Memory Block Diagram

Note: For debug purposes, the embedded QSPI Chip Enable can be uncoupled from the microcontroller. The QSPI0_CS_IN signal (pin 77) is accessible externally and can be decoupled from the QSPI0_CS_PB12 signal (pin 76) so that the boot can be unselected from the QSPI Flash memory during debug phases.

10. LAN Subsystem

10.1 Ethernet Power

The LAN8840 Gigabit Ethernet transceiver is powered by two separated supplies:

- VDD_3V3 (delivered by the MCP16502 PMIC) for the RGMII digital interface with the SAMA7D65 SiP device.
- VDD_1V1_ETH (delivered by the MIC33153 inductorless DCDC) for the LAN8840 digital core, PLL and analog interface with the outside world.

The functionalities of the MCP16502 PMIC are described in Power Management Unit.

The MIC33153 is a high-efficiency synchronous buck regulator with an internal inductor and HyperLight Load® mode.

HyperLight Load® provides very high efficiency at light loads and ultra-fast transient response, which makes the MIC33153 perfectly suited for supplying the LAN8840 digital core, PLL and analog voltages.

The MIC33153 is supplied externally by 5V_MAIN and its start-up is managed by the MCP16502. When the VDD_3V3 output voltage of the MCP16502 is present, the MIC33153 delivers the VDD_1V1_ETH supply to the LAN8840.

The MIC33153 is available in a 14-pin TDFN (3.0 mm × 3.5 mm) Package.

For more details, refer to the MIC33153 data sheet (See Reference Documents)

10.2 Ethernet Interface

The SAMA7D65 SOM Series embeds one low-power, single-port triple-speed (10BASE-T/100BASE-TX/1000BASE-T) Ethernet physical layer transceiver (PHY) LAN8840, optimized for precision process timing.

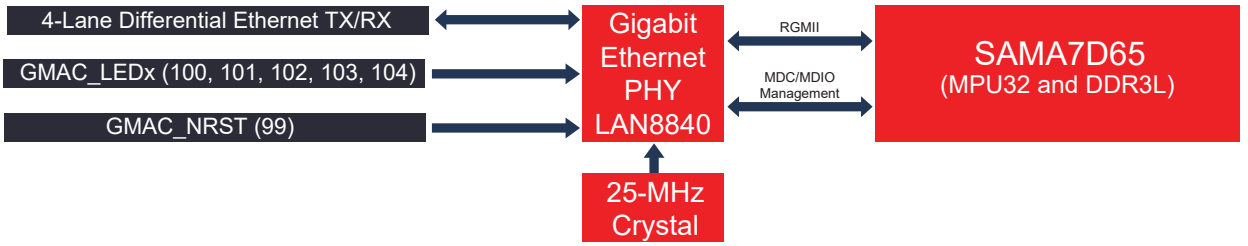
The LAN8840T-V/PSA supports industry-standard RGMII (Reduced Gigabit Media Independent Interface) providing chip-to-chip connection to a host device with an integrated Gigabit Ethernet MAC.

The LAN8840T-V/PSA is connected to a small size 25-MHz crystal used to generate its internal subsystem clocks.

The device is available in a 7 mm × 7 mm 48-pin VQFN Package and is implemented in the system as shown in the figure below.

For more information, refer to the Ethernet PHY LAN8840 data sheet (see Reference Documents).

Figure 10-1. Ethernet PHY Digital/Analog Block Diagram



The SAMA7D65 SOM Series embeds straps on the MODE[4:0] signals of the LAN8840 pins (PB3, PB6, PB2, PA30, PA29) to ensure that a set of features is configured automatically when the GMAC_NRST signal (pin 99) is released. The default settings are as follows.

- Auto-negotiation to automatically select the highest link-up speed and duplex: Enabled

- Automatic MDI/MDI-X crossover to detect and correct pair swap at all speeds of operation: Enabled
- Energy Efficient Ethernet (EEE) support: Enabled
- Single port with triple-speed (10BASE-T/100BASE-TX/1000BASE-T) link in full-duplex modes: Enabled

The LAN8840 PHY is not fully configured. Configuration straps (pull-up/down resistors) on the GMAC_LEDx pads (pins 100, 101, 102, 103 and 104) must be placed outside the module, and the GMAC_NRST signal (pin 99) can be connected as follows.

- The GMAC_LED5_ALLPHYAD pad (pin 104) allows the use of any value on the GMAC_LEDx_PHYAD[2:0] pads (pins 102, 101, 100), or 0 by default. This pin can be pulled up or down externally.
- The GMAC_LEDx_PHYAD[2:0] pads (pins 102, 101, 100) are used to set the PHY address.
- The GMAC_NRST pad can be connected to the global NRST signal (pin 173), to the microprocessor reset output NRST_OUT signal (pin 174), or to any system reset management.

Note: Any required external pulling configuration strap must be tied to either VDD_3V3 or GND, depending on customer needs. For more details, refer to the LAN8840 data sheet (see Reference Documents).

11. External Interfacing

11.1 Interfacing with FLEXCOM Interfaces

11.1.1 Interfacing in I²C/TWI Mode

Ten Flexible Serial Communication Controller (FLEXCOM) interfaces configurable in Two-Wire Interface (TWI) are available on the SAMA7D65 SOM Series.

The TWI can interconnect with external components on a unique two-wire bus, made up of one clock line and one data line.

The TWI supports the following modes/speeds:

- Standard mode speed (100 kHz): Host, Multi-Host, Client
- Fast mode speed (400 kHz): Host, Multi-Host, Client
- Fast mode plus speed (1 MHz): Host, Multi-Host, Client
- High-speed mode (1.7 MHz/3.4 MHz): Host, Client

It can be used with any Two-Wire Interface bus Serial EEPROM and I²C-compatible devices, such as a Real-Time Clock (RTC), a dot matrix/graphic LCD controller or a temperature sensor. The TWI is programmable as a host or a client with sequential or single-byte access. Multiple host capability is supported.

Table 11-1. I²C/TWI Interface Configurations

Interface Instance	IO Set	Pin No.	PIO	Pin Name	Comment
FLEXCOM0	2	179	PC7	FLEXCOM0_IO0	(1)
		182	PC6	FLEXCOM0_IO1	
FLEXCOM1	1	123	PD7	FLEXCOM1_IO0	(1)
		122	PD6	FLEXCOM1_IO1	
FLEXCOM1	2	210	PC14	FLEXCOM1_IO0	(1)
		208	PC15	FLEXCOM1_IO1	
FLEXCOM1	3	191	PB28	FLEXCOM1_IO0	(1)
		194	PB29	FLEXCOM1_IO1	
FLEXCOM2	1	15	PE8	FLEXCOM2_IO0	(1)
		16	PE9	FLEXCOM2_IO1	
FLEXCOM2	4	45	PB15	FLEXCOM2_IO0	(1)
		44	PB14	FLEXCOM2_IO1	
FLEXCOM3	2	38	PA24	FLEXCOM3_IO0	(1)
		39	PA23	FLEXCOM3_IO1	
FLEXCOM3	3	126	PD1	FLEXCOM3_IO0	(1)
		127	PD2	FLEXCOM3_IO1	
FLEXCOM3	4	7	PA14	FLEXCOM3_IO0	(1)
		5	PA15	FLEXCOM3_IO1	
FLEXCOM4	1	3	PA18	FLEXCOM4_IO0	(1)
		6	PA17	FLEXCOM4_IO1	
FLEXCOM5	1	80	PD16	FLEXCOM5_IO0	(1)
		79	PD17	FLEXCOM5_IO1	
FLEXCOM5	2	61	PE3	FLEXCOM5_IO0	(1)
		59	PE2	FLEXCOM5_IO1	

.....continued

Interface Instance	IO Set	Pin No.	PIO	Pin Name	Comment
FLEXCOM6	2	141	PB24	FLEXCOM6_IO0	(1)
		143	PB25	FLEXCOM6_IO1	
FLEXCOM6	3	69	PD24	FLEXCOM6_IO0	(1)
		57	PD25	FLEXCOM6_IO1	
FLEXCOM6	4	73	PD18	FLEXCOM6_IO0	(1)
		74	PD19	FLEXCOM6_IO1	
FLEXCOM7	1	85	PD8	FLEXCOM7_IO0	(1)
		88	PD9	FLEXCOM7_IO1	
FLEXCOM7	2	58	PD27	FLEXCOM7_IO0	(1)
		67	PD28	FLEXCOM7_IO1	
FLEXCOM7	3	124	PD5	FLEXCOM7_IO0	(1)
		121	PD4	FLEXCOM7_IO1	
FLEXCOM8	2	95	PC27	FLEXCOM8_IO0	(1)
		96	PC28	FLEXCOM8_IO1	
FLEXCOM8	3	142	PB26	FLEXCOM8_IO0	(1)
		145	PB27	FLEXCOM8_IO1	
FLEXCOM9	1	204	PC8	FLEXCOM9_IO0	(1)
		202	PC9	FLEXCOM9_IO1	
FLEXCOM9	2	180	PC3	FLEXCOM9_IO0	(1)
		178	PC4	FLEXCOM9_IO1	

Note:

1. External pull-up needed in case the FLEXCOM interface is used as an I²C/TWI interface.

11.1.2 Interfacing in USART Mode

Ten FLEXCOM interfaces configurable in Universal Synchronous Asynchronous Receiver Transceiver (USART) modes are available on the SAMA7D65 SOM Series.

Table 11-2. USART Interface Configurations

Interface Instance	IO Set	Pin No.	PIO	Pin Name	Description
FLEXCOM0	2	179	PC7	FLEXCOM0_IO0	UART Transmit Data Line (TXD)
		182	PC6	FLEXCOM0_IO1	UART Receive Data Line (RXD)
FLEXCOM1	1	123	PD7	FLEXCOM1_IO0	UART Transmit Data Line (TXD)
		122	PD6	FLEXCOM1_IO1	UART Receive Data Line (RXD)
FLEXCOM1	2	210	PC14	FLEXCOM1_IO0	UART Transmit Data Line (TXD)
		208	PC15	FLEXCOM1_IO1	UART Receive Data Line (RXD)
FLEXCOM1	3	191	PB28	FLEXCOM1_IO0	UART Transmit Data Line (TXD)
		194	PB29	FLEXCOM1_IO1	UART Receive Data Line (RXD)
FLEXCOM2	1	15	PE8	FLEXCOM2_IO0	UART Transmit Data Line (TXD)
		16	PE9	FLEXCOM2_IO1	UART Receive Data Line (RXD)
FLEXCOM2	4	45	PB15	FLEXCOM2_IO0	UART Transmit Data Line (TXD)
		44	PB14	FLEXCOM2_IO1	UART Receive Data Line (RXD)
FLEXCOM3	2	38	PA24	FLEXCOM3_IO0	UART Transmit Data Line (TXD)
		39	PA23	FLEXCOM3_IO1	UART Receive Data Line (RXD)

.....continued

Interface Instance	IO Set	Pin No.	PIO	Pin Name	Description
FLEXCOM3	3	126	PD1	FLEXCOM3_IO0	UART Transmit Data Line (TXD)
		127	PD2	FLEXCOM3_IO1	UART Receive Data Line (RXD)
FLEXCOM3	4	7	PA14	FLEXCOM3_IO0	UART Transmit Data Line (TXD)
		5	PA15	FLEXCOM3_IO1	UART Receive Data Line (RXD)
FLEXCOM4	1	3	PA18	FLEXCOM4_IO0	UART Transmit Data Line (TXD)
		6	PA17	FLEXCOM4_IO1	UART Receive Data Line (RXD)
FLEXCOM5	1	80	PD16	FLEXCOM5_IO0	UART Transmit Data Line (TXD)
		79	PD17	FLEXCOM5_IO1	UART Receive Data Line (RXD)
FLEXCOM5	2	61	PE3	FLEXCOM5_IO0	UART Transmit Data Line (TXD)
		59	PE2	FLEXCOM5_IO1	UART Receive Data Line (RXD)
FLEXCOM6	2	141	PB24	FLEXCOM6_IO0	UART Transmit Data Line (TXD)
		143	PB25	FLEXCOM6_IO1	UART Receive Data Line (RXD)
FLEXCOM6	3	69	PD24	FLEXCOM6_IO0	UART Transmit Data Line (TXD)
		57	PD25	FLEXCOM6_IO1	UART Receive Data Line (RXD)
FLEXCOM6	4	73	PD18	FLEXCOM6_IO0	UART Transmit Data Line (TXD)
		74	PD19	FLEXCOM6_IO1	UART Receive Data Line (RXD)
FLEXCOM7	1	85	PD8	FLEXCOM7_IO0	UART Transmit Data Line (TXD)
		88	PD9	FLEXCOM7_IO1	UART Receive Data Line (RXD)
FLEXCOM7	2	58	PD27	FLEXCOM7_IO0	UART Transmit Data Line (TXD)
		67	PD28	FLEXCOM7_IO1	UART Receive Data Line (RXD)
FLEXCOM7	3	124	PD5	FLEXCOM7_IO0	UART Transmit Data Line (TXD)
		121	PD4	FLEXCOM7_IO1	UART Receive Data Line (RXD)
FLEXCOM8	2	95	PC27	FLEXCOM8_IO0	UART Transmit Data Line (TXD)
		96	PC28	FLEXCOM8_IO1	UART Receive Data Line (RXD)
FLEXCOM8	3	142	PB26	FLEXCOM8_IO0	UART Transmit Data Line (TXD)
		145	PB27	FLEXCOM8_IO1	UART Receive Data Line (RXD)
FLEXCOM9	1	204	PC8	FLEXCOM9_IO0	UART Transmit Data Line (TXD)
		202	PC9	FLEXCOM9_IO1	UART Receive Data Line (RXD)
FLEXCOM9	2	180	PC3	FLEXCOM9_IO0	UART Transmit Data Line (TXD)
		178	PC4	FLEXCOM9_IO1	UART Receive Data Line (RXD)

Table 11-3. USART Interface Configurations with Flow Control

Interface Instance	IO Set	Pin No.	PIO	Pin Name	Description
FLEXCOM0	2	179	PC7	FLEXCOM0_IO0	Transmit Data
		182	PC6	FLEXCOM0_IO1	Receive Data
		178	PC4	FLEXCOM0_IO3	Clear To Send/Chip select
		180	PC3	FLEXCOM0_IO4	Request To Send/Chip select
FLEXCOM1	1	123	PD7	FLEXCOM1_IO0	Transmit Data
		122	PD6	FLEXCOM1_IO1	Receive Data
		124	PD5	FLEXCOM1_IO3	Clear To Send/Chip select
		125	PD3	FLEXCOM1_IO4	Request To Send/Chip select

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Interface Instance	IO Set	Pin No.	PIO	Pin Name	Description
FLEXCOM1	2	210	PC14	FLEXCOM1_IO0	Transmit Data
		208	PC15	FLEXCOM1_IO1	Receive Data
		207	PC17	FLEXCOM1_IO3	Clear To Send/Chip select
		199	PC18	FLEXCOM1_IO4	Request To Send/Chip select
FLEXCOM2	1	15	PE8	FLEXCOM2_IO0	Transmit Data
		16	PE9	FLEXCOM2_IO1	Receive Data
		10	PE5	FLEXCOM2_IO3	Clear To Send/Chip select
		12	PE6	FLEXCOM2_IO4	Request To Send/Chip select
FLEXCOM3	2	38	PA24	FLEXCOM3_IO0	Transmit Data
		39	PA23	FLEXCOM3_IO1	Receive Data
		37	PA21	FLEXCOM3_IO3	Clear To Send/Chip select
		41	PA20	FLEXCOM3_IO4	Request To Send/Chip select
FLEXCOM4	1	3	PA18	FLEXCOM4_IO0	Transmit Data
		6	PA17	FLEXCOM4_IO1	Receive Data
		5	PA15	FLEXCOM4_IO3	Clear To Send/Chip select
		7	PA14	FLEXCOM4_IO4	Request To Send/Chip select
FLEXCOM5	1	80	PD16	FLEXCOM5_IO0	Transmit Data
		79	PD17	FLEXCOM5_IO1	Receive Data
		82	PD15	FLEXCOM5_IO3	Clear To Send/Chip select
		84	PD13	FLEXCOM5_IO4	Request To Send/Chip select
FLEXCOM5	2	61	PE3	FLEXCOM5_IO0	Transmit Data
		59	PE2	FLEXCOM5_IO1	Receive Data
		62	PE1	FLEXCOM5_IO3	Clear To Send/Chip select
		64	PD31	FLEXCOM5_IO4	Request To Send/Chip select
FLEXCOM6	2	141	PB24	FLEXCOM6_IO0	Transmit Data
		143	PB25	FLEXCOM6_IO1	Receive Data
		140	PB22	FLEXCOM6_IO3	Clear To Send/Chip select
		139	PB21	FLEXCOM6_IO4	Request To Send/Chip select
FLEXCOM6	3	69	PD24	FLEXCOM6_IO0	Transmit Data
		57	PD25	FLEXCOM6_IO1	Receive Data
		70	PD22	FLEXCOM6_IO3	Clear To Send/Chip select
		66	PD23	FLEXCOM6_IO4	Request To Send/Chip select
FLEXCOM6	4	73	PD18	FLEXCOM6_IO0	Transmit Data
		74	PD19	FLEXCOM6_IO1	Receive Data
		70	PD22	FLEXCOM6_IO3	Clear To Send/Chip select
		66	PD23	FLEXCOM6_IO4	Request To Send/Chip select
FLEXCOM7	1	85	PD8	FLEXCOM7_IO0	Transmit Data
		88	PD9	FLEXCOM7_IO1	Receive Data
		86	PD11	FLEXCOM7_IO3	Clear To Send/Chip select
		83	PD12	FLEXCOM7_IO4	Request To Send/Chip select
FLEXCOM7	2	58	PD27	FLEXCOM7_IO0	Transmit Data
		67	PD28	FLEXCOM7_IO1	Receive Data
		65	PD30	FLEXCOM7_IO3	Clear To Send/Chip select
		68	PD26	FLEXCOM7_IO4	Request To Send/Chip select

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Interface Instance	IO Set	Pin No.	PIO	Pin Name	Description
FLEXCOM8	2	95	PC27	FLEXCOM8_IO0	Transmit Data
		96	PC28	FLEXCOM8_IO1	Receive Data
		94	PC30	FLEXCOM8_IO3	Clear To Send/Chip select
		92	PC31	FLEXCOM8_IO4	Request To Send/Chip select
FLEXCOM9	1	204	PC8	FLEXCOM9_IO0	Transmit Data
		202	PC9	FLEXCOM9_IO1	Receive Data
		201	PC11	FLEXCOM9_IO3	Clear To Send/Chip select
		205	PC12	FLEXCOM9_IO4	Request To Send/Chip select

11.1.3 Interfacing in SPI Mode

Six FLEXCOM interfaces configured in Serial Peripheral Interface (SPI) mode are available on the SAMA7D65 SOM Series.

The SPI circuit is a synchronous serial data link that provides communication with external devices in Host or Client mode. It also enables communication between processors if an external processor is connected to the system.

The Serial Peripheral Interface is essentially a shift register that serially transmits data bits to other SPI devices. During a data transfer, one SPI system acts as the “host” which controls the data flow, while the other devices act as “clients'' which have data shifted in and out by the host. Different CPUs can take turns being hosts (multiple host protocol, contrary to single host protocol where one CPU is always the host while all others are always clients). One host can simultaneously shift data into multiple clients. However, only one client can drive its output to write data back to the host at any given time.

A client device is selected when the host asserts its NSS signal. When multiple client devices are available, the host generates a separate client select signal (NPCS) for each.

The SPI system consists of two data lines and two control lines:

- Host Out Client In (MOSI)—This data line supplies the output data from the host shifted into the input(s) of the client(s).
- Host In Client Out (MISO)—This data line supplies the output data from a client to the input of the host. There may be no more than one client transmitting data during any particular transfer.
- Serial Clock (SPCK)—This control line is driven by the host and regulates the flow of the data bits. The host can transmit data at a variety of baud rates; there is one SPCK pulse for each bit transmitted.
- Client Select (NSS)—This control line allows clients to be turned on and off by hardware.

Table 11-4. FLEXCOM Interface Configurations in SPI Mode

Interface Instance	IO set	Pin No.	PIO	Pin Name	Description
FLEXCOM0	2	179	PC7	FLEXCOM0_IO0	MOSI Signal
		182	PC6	FLEXCOM0_IO1	MISO Signal
		181	PC5	FLEXCOM0_IO2	SPCK Signal
		178	PC4	FLEXCOM0_IO3	NPCS0 Signal
		180	PC3	FLEXCOM0_IO4	NPCS1 Signal

.....continued

Interface Instance	IO set	Pin No.	PIO	Pin Name	Description
FLEXCOM1	1	123	PD7	FLEXCOM1_IO0	MOSI Signal
		122	PD6	FLEXCOM1_IO1	MISO Signal
		121	PD4	FLEXCOM1_IO2	SPCK Signal
		124	PD5	FLEXCOM1_IO3	NPCS0 Signal
		125	PD3	FLEXCOM1_IO4	NPCS1 Signal
		126	PD1	FLEXCOM1_IO5	NPCS2 Signal
		127	PD2	FLEXCOM1_IO6	NPCS3 Signal
FLEXCOM1	2	210	PC14	FLEXCOM1_IO0	MOSI Signal
		208	PC15	FLEXCOM1_IO1	MISO Signal
		209	PC16	FLEXCOM1_IO2	SPCK Signal
		207	PC17	FLEXCOM1_IO3	NPCS0 Signal
		199	PC18	FLEXCOM1_IO4	NPCS1 Signal
FLEXCOM1	3	191	PB28	FLEXCOM1_IO0	MOSI Signal
		194	PB29	FLEXCOM1_IO1	MISO Signal
		192	PB30	FLEXCOM1_IO2	SPCK Signal
		193	PB31	FLEXCOM1_IO3	NPCS0 Signal
FLEXCOM2	1	15	PE8	FLEXCOM2_IO0	MOSI Signal
		16	PE9	FLEXCOM2_IO1	MISO Signal
		9	PE4	FLEXCOM2_IO2	SPCK Signal
		10	PE5	FLEXCOM2_IO3	NPCS0 Signal
		12	PE6	FLEXCOM2_IO4	NPCS1 Signal
		13	PE7	FLEXCOM2_IO5	NPCS2 Signal
		19	PE10	FLEXCOM2_IO6	NPCS3 Signal
FLEXCOM3	2	38	PA24	FLEXCOM3_IO0	MOSI Signal
		39	PA23	FLEXCOM3_IO1	MISO Signal
		40	PA22	FLEXCOM3_IO2	SPCK Signal
		37	PA21	FLEXCOM3_IO3	NPCS0 Signal
		41	PA20	FLEXCOM3_IO4	NPCS1 Signal
FLEXCOM3	3	126	PD1	FLEXCOM3_IO0	MOSI Signal
		127	PD2	FLEXCOM3_IO1	MISO Signal
		125	PD3	FLEXCOM3_IO2	SPCK Signal
		83	PD12	FLEXCOM3_IO3	NPCS0 Signal
FLEXCOM4	1	3	PA18	FLEXCOM4_IO0	MOSI Signal
		6	PA17	FLEXCOM4_IO1	MISO Signal
		4	PA16	FLEXCOM4_IO2	SPCK Signal
		5	PA15	FLEXCOM4_IO3	NPCS0 Signal
		7	PA14	FLEXCOM4_IO4	NPCS1 Signal
		36	PA19	FLEXCOM4_IO5	NPCS2 Signal
		41	PA20	FLEXCOM4_IO6	NPCS3 Signal
FLEXCOM5	1	80	PD16	FLEXCOM5_IO0	MOSI Signal
		79	PD17	FLEXCOM5_IO1	MISO Signal
		81	PD14	FLEXCOM5_IO2	SPCK Signal
		82	PD15	FLEXCOM5_IO3	NPCS0 Signal
		84	PD13	FLEXCOM5_IO4	NPCS1 Signal

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Interface Instance	IO set	Pin No.	PIO	Pin Name	Description
FLEXCOM5	2	61	PE3	FLEXCOM5_IO0	MOSI Signal
		59	PE2	FLEXCOM5_IO1	MISO Signal
		60	PE0	FLEXCOM5_IO2	SPCK Signal
		62	PE1	FLEXCOM5_IO3	NPCS0 Signal
		64	PD31	FLEXCOM5_IO4	NPCS1 Signal
FLEXCOM6	2	141	PB24	FLEXCOM6_IO0	MOSI Signal
		143	PB25	FLEXCOM6_IO1	MISO Signal
		144	PB23	FLEXCOM6_IO2	SPCK Signal
		140	PB22	FLEXCOM6_IO3	NPCS0 Signal
		139	PB21	FLEXCOM6_IO4	NPCS1 Signal
FLEXCOM6	3	69	PD24	FLEXCOM6_IO0	MOSI Signal
		57	PD25	FLEXCOM6_IO1	MISO Signal
		56	PD21	FLEXCOM6_IO2	SPCK Signal
		70	PD22	FLEXCOM6_IO3	NPCS0 Signal
		66	PD23	FLEXCOM6_IO4	NPCS1 Signal
FLEXCOM6	4	73	PD18	FLEXCOM6_IO0	MOSI Signal
		74	PD19	FLEXCOM6_IO1	MISO Signal
		51	PD20	FLEXCOM6_IO2	SPCK Signal
		70	PD22	FLEXCOM6_IO3	NPCS0 Signal
		66	PD23	FLEXCOM6_IO4	NPCS1 Signal
FLEXCOM7	1	85	PD8	FLEXCOM7_IO0	MOSI Signal
		88	PD9	FLEXCOM7_IO1	MISO Signal
		87	PD10	FLEXCOM7_IO2	SPCK Signal
		86	PD11	FLEXCOM7_IO3	NPCS0 Signal
		83	PD12	FLEXCOM7_IO4	NPCS1 Signal
FLEXCOM7	2	58	PD27	FLEXCOM7_IO0	MOSI Signal
		67	PD28	FLEXCOM7_IO1	MISO Signal
		63	PD29	FLEXCOM7_IO2	SPCK Signal
		65	PD30	FLEXCOM7_IO3	NPCS0 Signal
		68	PD26	FLEXCOM7_IO4	NPCS1 Signal
FLEXCOM7	3	124	PD5	FLEXCOM7_IO0	MOSI Signal
		121	PD4	FLEXCOM7_IO1	MISO Signal
		122	PD6	FLEXCOM7_IO2	SPCK Signal
		123	PD7	FLEXCOM7_IO3	NPCS0 Signal
FLEXCOM8	2	95	PC27	FLEXCOM8_IO0	MOSI Signal
		96	PC28	FLEXCOM8_IO1	MISO Signal
		93	PC29	FLEXCOM8_IO2	SPCK Signal
		94	PC30	FLEXCOM8_IO3	NPCS0 Signal
		92	PC31	FLEXCOM8_IO4	NPCS1 Signal
FLEXCOM9	1	204	PC8	FLEXCOM9_IO0	MOSI Signal
		202	PC9	FLEXCOM9_IO1	MISO Signal
		206	PC10	FLEXCOM9_IO2	SPCK Signal
		201	PC11	FLEXCOM9_IO3	NPCS0 Signal
		205	PC12	FLEXCOM9_IO4	NPCS1 Signal

11.2 Interfacing with an SD Card

The SD (Secure Digital) Card is a nonvolatile memory card format used as mass storage memory in mobile devices.

Secure Digital Multimedia Card (SDMMC) Controller

The SAMA7D65 SOM Series includes two Secure Digital Multimedia Card (SDMMC) interfaces that support the MultiMedia Card (e.MMC) specification V4.51, the SD Memory Card specification V3.0, and the SDIO V3.0 specification. They are compliant with the SD Host Controller Standard V3.0 specification.

The two interfaces can be connected to a standard SD card interface.

SDMMCx Card Connector

The board features two standard MMC/SD card connectors, connected to SDMMC1 and SDMMC2. Both interface communications are based on a 4-pin interface (clock, command, four data and power lines).

Table 11-5. SDMMCx Interface Configurations

Interface Instance	IO Set	Pin No.	PIO	Pin Name	Description
SDMMC1	1	144	PB23	SDMMC1_CK	SD card/e.MMC clock signal
		140	PB22	SDMMC1_CMD	SD card/e.MMC command Line
		141	PB24	SDMMC1_DAT0	SD card/e.MMC data lines
		143	PB25	SDMMC1_DAT1	
		142	PB26	SDMMC1_DAT2	
		145	PB27	SDMMC1_DAT3	
SDMMC2	1	96	PC28	SDMMC2_CK	SD card/e.MMC clock signal
		95	PC27	SDMMC2_CMD	SD card/e.MMC command line
		93	PC29	SDMMC2_DAT0	SD card/e.MMC data lines
		94	PC30	SDMMC2_DAT1	
		92	PC31	SDMMC2_DAT2	
		91	PD0	SDMMC2_DAT3	

11.3 Interfacing with LVDS Display

The SAMA7D65 SOM Series includes one 4-Lane Low-Voltage Differential Signaling (LVDS). The LVDS operates at low power and can run at very high speeds by only using twisted-pair interfaces.

The LVDS Controller manages data format conversion from the LCD Controller's internal DPI bus to OpenLDI LVDS output signals. LVDS Controller's functions include bit mapping, balanced mode management and serialization.

Table 11-6. LVDS Interface Configurations

Interface Instance	Power Rail	Pin No.	GPIO Name	Pin Name	Description
LVDS	VDDLVDS	9	PE4	LVDS_D0_N	Differential LVDS Data Line 0 Transceiver Output
LVDS	VDDLVDS	10	PE5	LVDS_D0_P	
LVDS	VDDLVDS	12	PE6	LVDS_D1_N	Differential LVDS Data Line 1 Transceiver Output
LVDS	VDDLVDS	13	PE7	LVDS_D1_P	
LVDS	VDDLVDS	15	PE8	LVDS_D2_N	Differential LVDS Data Line 2 Transceiver Output
LVDS	VDDLVDS	16	PE9	LVDS_D2_P	
LVDS	VDDLVDS	19	PE10	LVDS_D3_N	Differential LVDS Data Line 3 Transceiver Output
LVDS	VDDLVDS	20	PE11	LVDS_D3_P	

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Interface Instance	Power Rail	Pin No.	GPIO Name	Pin Name	Description
LVDS	VDDLVDS	17	PE12	LVDS_CLK_N	Differential LVDS Clock Line Transceiver Output
LVDS	VDDLVDS	18	PE13	LVDS_CLK_P	

Note: For the use of the LVDS features, the VDDLVDS input power must be connected to the VDD_2V5 output volltage.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

The following table provides the maximum operating ratings for the SAMA7D65 SOM Series.

Table 12-1. Absolute Maximum Ratings

Parameter	Pads	Range	Comments
I/O Supply Voltage	All GPIO	–0.3V to 4.0V	**Note:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. **Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**
I/O Supply Voltage	VDDGMAC1, VDDIOP0, VDDIOP1, VDDSDMMC1, VDDSDMMC2, VDDLVDS	–0.3V to 4.0V	
Main Supply Voltage	5V_MAIN	–0.3V to 6.0V	
Backup Supply Voltage	VBAT	–0.3V to 4.0V	
Storage Temperature	$T_{STORAGE}$	–55 to +150°C	
Maximum Input Current	5V_MAIN	2A	

12.2 Recommended Operating Conditions

The following table provides the operating ratings for the Microchip SAMA7D65 System-On-Module Series.

Table 12-2. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
All I/O	I/O Supply Voltage on VDD_3V3 Power Rail	3.23	3.37	V
VDDGMAC1	I/O Supply Voltage on VDDGMAC1 Power Rail	1.7	3.6	V
VDDIOP0	I/O Supply Voltage on VDDIOP0 Power Rail	1.7	3.6	V
VDDIOP1	I/O Supply Voltage on VDDIOP1 Power Rail	1.7	3.6	V
VDDSDMMC1	I/O Supply Voltage on VDDSDMMC1 Power Rail	1.7	1.9	V
		3.0	3.6	V
VDDSDMMC2	I/O Supply Voltage on VDDSDMMC1 Power Rail	1.7	1.9	V
		3.0	3.6	V
VDDLVDS	I/O Supply Voltage on VDDLVDS Power Rail	1.7	3.6	V
5V_MAIN	Main Supply Voltage	3.3	5.5	V
VBAT	Backup Supply Voltage	1.6	3.6	V
T_A	Module Operating Ambient Temperature	–40	85	°C
T_{J_MPU}(1)	MPU Junction Temperature	–40	105	°C
VDDANA	ADC Input Voltage(2)	0	2.5	V

Notes:

1. The MPU junction temperature can be read with the integrated temperature sensor. Refer to the "SAMA7D65 Series Temperature Sensor Calibration" application note (see Reference Documents). T_J must be characterized in-application to ensure this specification is met.
2. This voltage is set internally and connected to the internal 2.5V voltage supply.

12.3 Power Consumption

The following current consumption values are provided for information only.

Current consumption can vary according to temperature, MPU and GPU activities and customer application implementation (hardware interface uses, clock speed set-up and embedded software solution).

Table 12-3. Power Consumption

Node	Measurement	Conditions	Min	Typ	Max	Unit
5V_MAIN	Current consumption	Linux and Ethernet transfer. 5V_MAIN = 5.00V (CPU @ 1000 MHz)	–	(*)	(*)	mA
5V_MAIN	Current consumption	Linux in idle(1) 5V_MAIN = 5.00V (CPU @ 1000 MHz)	–	(*)	(*)	mA
5V_MAIN	Current consumption	System off, all supplies off. 5V_MAIN = 5.00V	–	(*)	(*)	µA
VBAT	Current consumption	VBAT = 3.3V @ 25°C	–	(*)	–	µA
VBAT	Current consumption	1.6V < VBAT < 3.6V. All temperature ranges, all modes	(*)	–	(*)	µA

Notes:

1. "Linux in idle" means that Linux is loaded and that the prompt is shown on the console, waiting for instructions.
2. (*) denotes data that will be forthcoming in the final data sheet publication.

13. Mechanical Characteristics

13.1 SAMA7D65 SOM Series Dimensions

Figure 13-1. SAMA7D65 SOM Series Dimensions

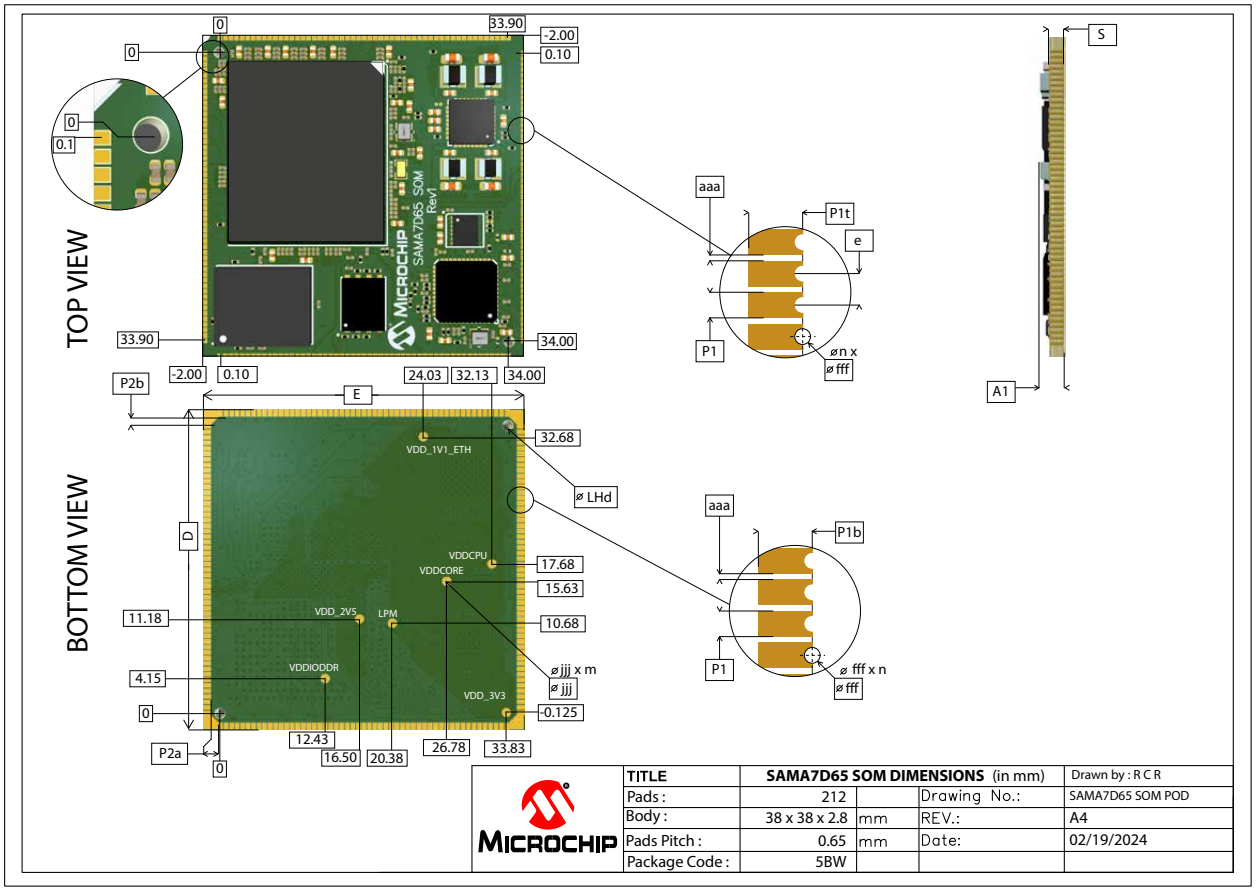

Table 13-1. SAMA7D65 SOM Series Dimensions (in mm)

Parameter		Symbol	Common Dimensions			Comments
			Min	Typ	Max	
Body overall dimensions	X	E	37.800	38.000	38.200	
	Y	D	37.800	38.000	38.200	
Pad pitch		e	–	0.650	–	
PCB thickness		S	1.450	1.600	1.750	
SOM total thickness		A1	–	2.800	3.000	
Pad length	Top side	P1t	–	0.550	–	
	Bottom side	P1b	–	0.900	–	
Pad width		P1	–	0.450	–	
Pad gap		aaa	–	0.200	–	
Opening drill diameter		fff	–	0.300	–	
Pad count		n	–	212	–	
Test point diameter(1)		jjj	–	1.000	–	
Test point count		m	–	7	–	

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Parameter		Symbol	Common Dimensions			Comments
			Min	Typ	Max	
Pad edge to SOM edge	X	P2a	–	0.925	–	
	Y	P2b	–	0.925	–	
Locating hole diameter[2]		LHd	1.150	1.200	1.250	

Notes:

1. Test points placed under the SAMA7D65 SOM Series are for production purposes only. Avoid any contact with the main board vias or copper areas (see Figure 13-1).
2. Locating holes are used for production purposes.

13.2 Other Characteristics

Table 13-2. SAMA7D65 SOM Series Weight

Ordering Code	Parameter	Measurement	
		Value	Unit
SAMA7D65D2GN8-I/5BW	Weight	7.6	g
SAMA7D65D1GN2-I/5BW		(*)	g

Note: (*) denotes data that will be forthcoming in the final data sheet publication.

14. Ordering Information

For details on ordering codes, see Product Identification System.

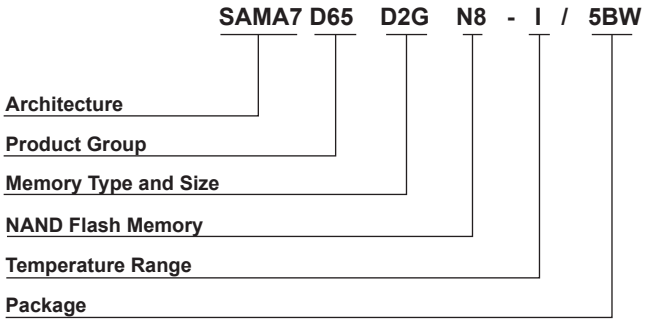
Ordering Code	SiP Device Revision	DDR3L Memory Configuration	NAND Memory Configuration	Package	Carrier Type	Module Ambient Temperature Range(1)
SAMA7D65D2GN8-I/5BW	A1	2 Gbits	8 Gbits	212-pin 38x38 mm module	Tray	–40°C to +85°C
SAMA7D65D1GN2-I/5BW	A1	1 Gbit	2 Gbits			

Note:

1. Indicative Ambient Temperature Range. Refer to Table 12-2 for complete information about the operating temperature range.

15. Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Architecture:	SAMA7	= Arm Cortex-A7 CPU
Product Group:	D65	= General purpose microprocessor with graphic features
Memory Type and Size:	D2G	= 2-Gbit DDR3L SDRAM
	D1G	= 1-Gbit DDR3L SDRAM
NAND Flash Memory:	N8	= 8-Gbit NAND Flash memory
	N2	= 2-Gbit NAND Flash memory
Ambient Temperature Range(1):	I	= –40°C to +85°C (industrial)
Package:	5BW	= Package code

Note:

1. Indicative Ambient Temperature Range. Refer to Table 12-2 for complete information about the operating temperature range.

Example:

- SAMA7D65D2GN8-I/5BW = Arm Cortex-A7 general purpose microprocessor with graphic features with 2-Gbit DDR3L SDRAM and 8-Gbit NAND Flash memory for industrial applications

16. Revision History

16.1 Rev. A - 11/2024

Changes
Preliminary issue

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