

SAM9X7 Series Silicon Errata and Data Sheet Clarifications

SAM9X7 Series

The SAM9X7 Series device that you have received conforms functionally to the current Device Data Sheet (DS6000XXXX), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following table. The silicon issues are summarized in [1. Silicon Issue Summary](#).

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in [4. Data Sheet Clarifications](#), following the discussion of silicon issues.

The Device and Revision ID values for the SAM9X7 Series silicon device are shown in the following table.

Table 1. SAM9X7 Series Silicon Device Identification

Part Number	Silicon Revision	Device Identification	
		CHIPID_CIDR[31:0]	CHIPID_EXID[31:0]
SAM9X70-I/4PB	A0	0x89750030	0x00000000
SAM9X70T-I/4PB			
SAM9X72-I/4PB			
SAM9X72T-I/4PB			
SAM9X75-I/4PB			
SAM9X75T-I/4PB			
SAM9X70-V/4PB			
SAM9X70T-V/4PB			
SAM9X72-V/4PB			
SAM9X72T-V/4PB			
SAM9X75-V/4PB			
SAM9X75T-V/4PB			
SAM9X75-V/4PBVAO			
SAM9X75T-V/4PBVAO			

Note: Refer to the “Chip Identifier” and “Product Identification System” sections in the current device data sheet (DS6000XXXX) for detailed information on chip identification and version for your specific device.

1. Silicon Issue Summary

Table 1-1. Silicon Issue Summary

Module	Item/Feature	Summary	Affected Silicon Revisions		
			A0		
SMC	Register Write Protection Not Effective on SMC_OCMS Register	The register write protection is not effective on the SMC_OCMS register.	X		
MPDDRC	DDR I/O Automatic Calibration Not Effective	The automatic calibration cell for DDR I/Os does not work.	X		

2. Static Memory Controller (SMC)

2.1 Register Write Protection Not Effective on SMC_OCMS Register

The register SMC_OCMS is not write-protected when the bit WPEN is set in SMC_WPMR.

Work Around

None

Affected Silicon Revisions

A0							
X							

3. DDR-SDRAM Controller (MPDDRC)

3.1 DDR I/O Automatic Calibration Not Effective

The automatic calibration cell for DDR I/Os does not work.

Work Around

Set the DDR I/Os calibration codes prior to initializing the DDR-SDRAM in SFR_CAL1 register. The provided calibration codes are valid over the voltage and temperature of the device. In the SFR_CAL1 register, write:

- 0x0000_0194 for DDR2-SDRAM,
- 0x0000_0186 for DDR3-SDRAM,
- 0x0000_0186 for DDR3L-SDRAM.

The SFR_CAL1 register is located at offset 0xB4 in the SFR peripheral memory space.

Affected Silicon Revisions

A0							
X							

4. Data Sheet Clarifications

4.1 OTP Controller (OTPC)

4.1.1 OTPC Dependency to Main RC Oscillator

The main RC oscillator must be turned on prior to reading or writing the OTP memory.

5. Revision History

5.1 DS8000xxxxA - 07/2022

Preliminary issue.

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