SAMA7G54 MPU, up to 2-Gbit DDR3L SDRAM, up to 4-Gbit NAND Flash, Power Management IC, 64-Mbit Serial Quad I/O Flash

SAMA7G54 SOM Series

Introduction

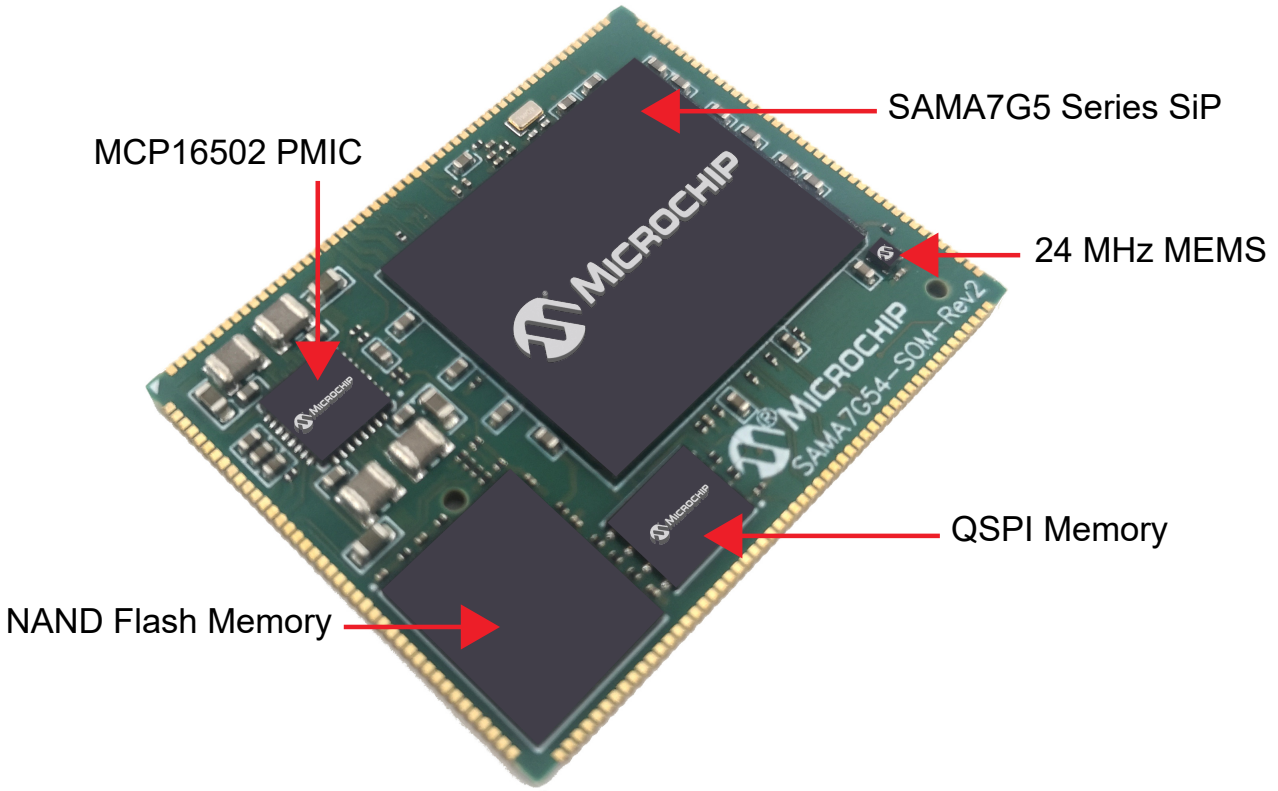
The Microchip SAMA7G54 System-On-Module Series is a small single-sided SOM series based on a System-in-Package (SiP) Arm® Cortex®-A7 CPU-based embedded microprocessor running up to 1 GHz.

The SAMA7G54 SOM Series is built on a common set of proven Microchip components to reduce time to market by simplifying hardware design and software development.

The SOM embeds a SAMA7G5 Series SiP microprocessor with up to 2-Gbit DDR3L SDRAM (with two possible configurations), up to 4-Gbit NAND Flash memory (with three possible configurations), a 64-Mbit serial Quad I/O Flash memory and a dedicated Power Management Unit.

The SAMA7G54 SOM Series also limits design rules of the main application board, reducing overall PCB complexity and cost. The SAMA7G54 SOM Series is supported by a free Linux® distribution and bare metal C examples.

Figure 1. SAMA7G54 SOM Series Overview



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1. Features

- SAMA7G5 Series SiP including:
  - Arm Cortex-A7 processor-based SAMA7G54 MPU
  - CPU frequency up to 1 GHz, junction temperature range: –40°C to +105°C
  - Up to 2-Gbit DDR3L SDRAM memory
- On-Board Power Management Unit (MCP16502TAB-E/S8B)
- Up to 4-Gbit NAND Flash Memory
- 64-Mbit Serial Quad I/O Flash Memory (SST26VF064BEUIT-104I/MF) with Embedded EUI-48™ and EUI-64™ MAC Addresses
- MEMS Oscillators and Crystal for clock generation
- Up to 113 I/Os
- Up to Four Tamper Pins
- Two High-Speed USB Devices and Three High-Speed USB Hosts sharing three On-Chip Transceivers
- Shutdown and Reset Control Pins
- Independent Power Supplies available for SD Cards, Octal SPI Memory, Camera Sensor and Backup depending on voltage domains
- Operational Conditions:
  - Main operating voltage: 3.3V to 5.5V ± 5%
  - Module ambient temperature range (T_A) range: –40°C to +85°C
- Package:
  - 38x30 mm, 190-Pin, 0.65 mm Pad Pitch Module, solderable manually for prototyping

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2. Applications

- Industrial control and automation
- Smart appliances
- Industrial and IoT gateways
- Access control panels
- Security and alarm systems
- Automotive EV chargers
- Digital audio subsystems

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3. Reference Documents

Type	Document Title	Available	Literature No.
Data sheet	SAMA7G5 Series SiP	www.microchip.com	DS50003577
Application note	SAMA7G5 Series Temperature Sensor Calibration	www.microchip.com	DS00004530
Data sheet	MCP16502	www.microchip.com	DS20006275
Data sheet	DSC60XXB	www.microchip.com	DS20006133
Data sheet	SST26VF064BEUI	www.microchip.com	DS20006138
Data sheet	MX30LF2G28AD-XKI	www.mxic.com.tw	PM2579
Data sheet	MT29F2G08ABAGAH4-IT:G	www.micron.com/	–
Data sheet	MX30LF4G28AD-XKI	www.mxic.com.tw	PM2579
Data sheet	MT29F4G08ABAFAH4-IT:F	www.micron.com/	–

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4. Description

The Microchip SAMA7G54 SOM Series is a high-performance System-On-Module series based on the ultra-low power Arm Cortex-A7 CPU-based embedded microprocessor (MPU) SAMA7G54. The SAMA7G54 SOM Series is certified for industrial operating conditions over the industrial temperature range.

The SAMA7G54 SOM Series operates at a maximum CPU operating frequency of 1 GHz and a maximum bus speed of 533 MHz and features up to:

- DDR3L SDRAM memory configuration with:
  - 1-Gbit memory size (SAMA7G54D1G-I/4UB)
  - 2-Gbit memory size (SAMA7G54D2G-I/4UB)
- 8-bit NAND Flash memory with:
  - 2-Gbit memory size (MX30LF2G28AD-XKI or MT29F2G08ABAGAH4-IT:G)
  - 4-Gbit memory size (MX30LF4G28AD-XKI or MT29F4G08ABAFAH4-IT:F)

  Note: A version with no NAND Flash memory is also available.
- 64 Mbits of QSPI Flash memory (SST26VF064BEUIT-104I/MF)

The SAMA7G54 SOM Series device is a 190-pin, 0.65-mm pad pitch module, 38 mm x 30 mm in size.

The device offers an extensive peripheral set, system control and up to 113 I/Os featuring:

- Up to 12 Flexible Serial Communication Controllers (FLEXCOM)
- Up to 8 ADC inputs
- Up to 6 CAN interfaces
- Up to 2 SD/MMC, SDIO interfaces
- Serial interfaces such as Octal SPI, up to 2 SSC, up to 2 I²S multichannel audio interfaces
- CMOS camera interface
- One 10/100/1000 Gigabit Ethernet MAC supporting RGMII, MII and RMII (GMAC0) and one 10/100 Ethernet MAC supporting MII and RMII (GMAC1)
- Up to 8 digital microphones and SPDIF interface

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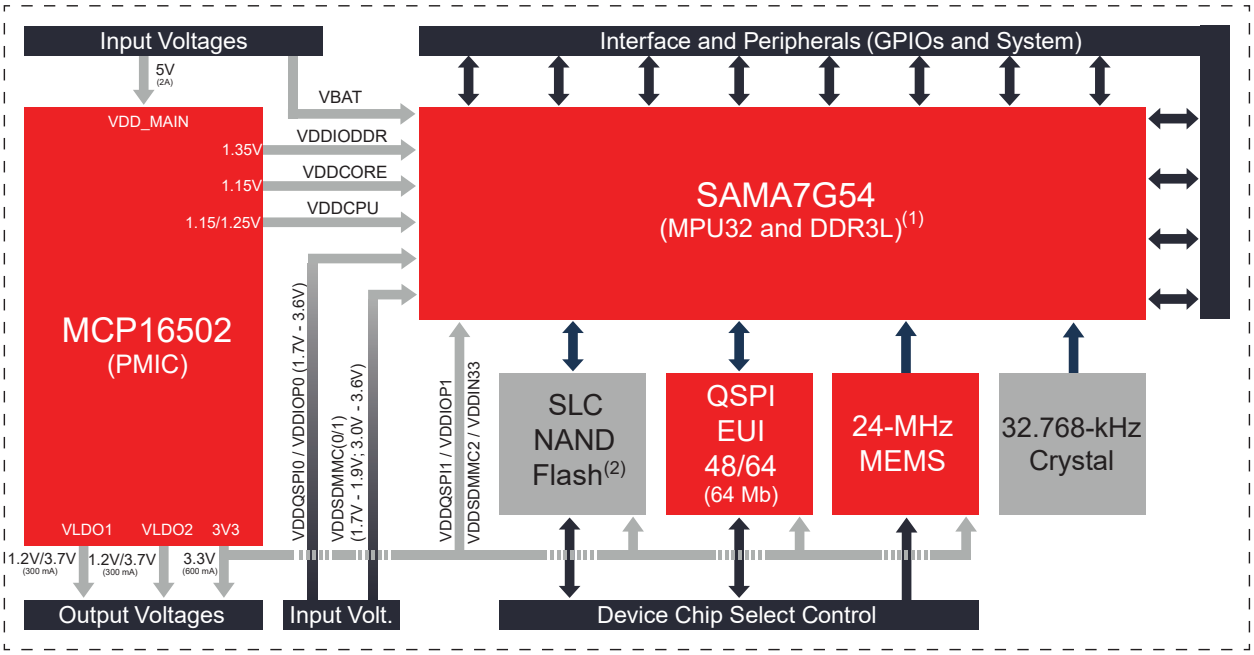
5. Block Diagram

Figure 5-1. SAMA7G54 SOM Series Block Diagram



Notes:

1. Several DDR3L memory sizes are available depending on the memory configuration.
2. Several NAND Flash memory sizes are available depending on the memory configuration.

For more details, see Ordering Information.

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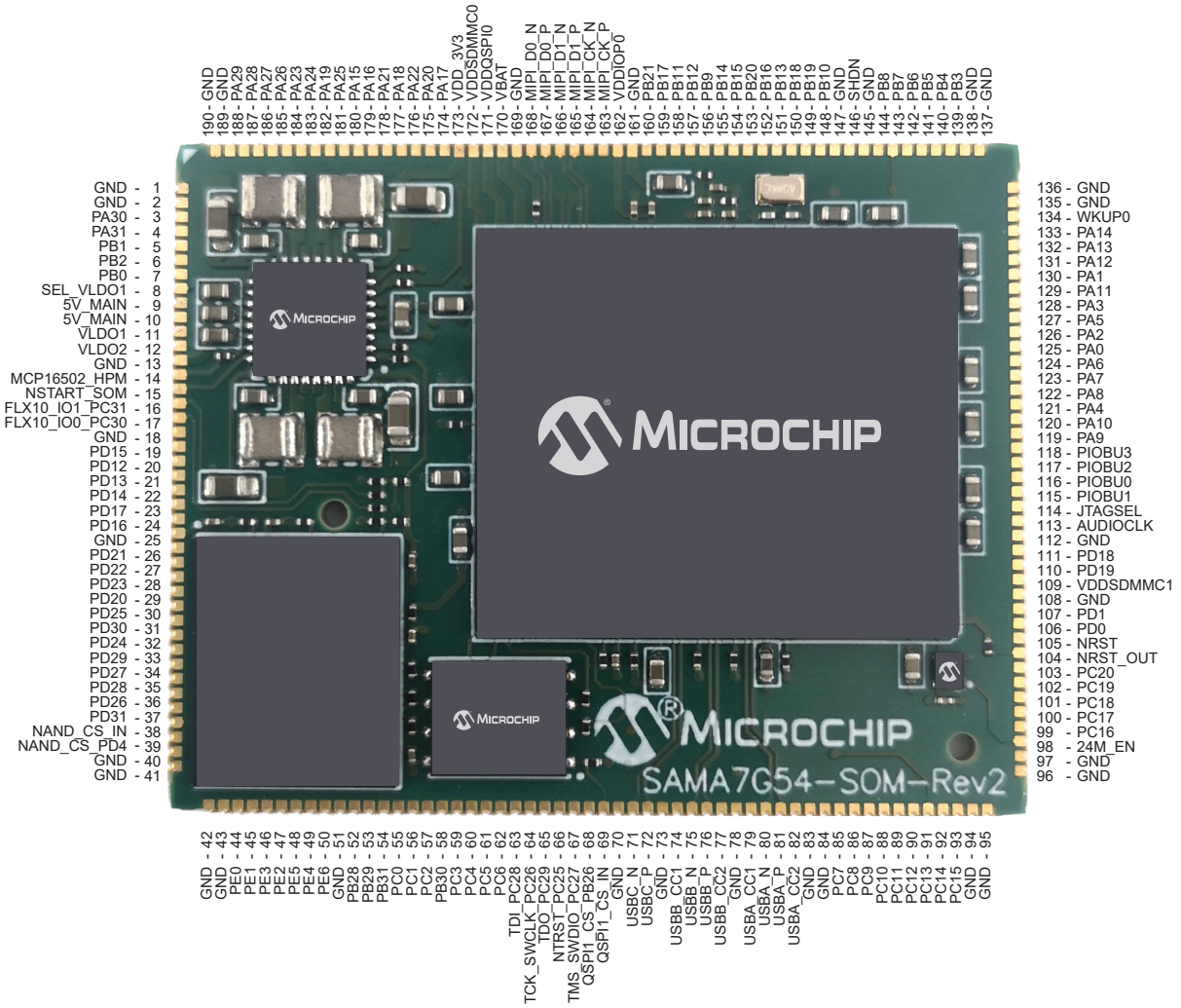
6. Pinout

6.1 Pinout Overview

Figure 6-1. SAMA7G54 SOM Series Pin Assignment



6.2 Pin List

The following tables provide the SAMA7G54 SOM Series module pin description.

Important: Compared to the SAMA7G54 device, some PIO features are not listed. These features are used internally on the SAMA7G54 SOM Series and cannot have other uses.

The device features several PIO controllers that multiplex the I/O lines of the peripheral set. The following PIOx Pin Description tables define how the I/O lines are multiplexed on the different PIO controllers. The "Reset State" column shows whether the PIO line resets in I/O mode or in Peripheral mode. If I/O is shown, the PIO line resets with the characteristics (input, output, pull-up or pull-down) indicated in this same column, so that the device is configured in a known state as soon as the reset is released. As a result, PIO_CFGR.FUNC resets to ‘0’. If a signal name is shown in the “Reset State”

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column, the PIO line is assigned to this function and PIO_CFGR.FUNC is not set to '0'. That is the case for pins controlling memories, in particular address lines, which require the pin to be driven as soon as the reset is released.

6.2.1 PIOA Pin List

Table 6-1. PIOA Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
125	VDDSDMMC0	GPIOHS	PA0	GPIO	–	–	A	SDMMC0_CK	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM0_IO0	I/O	1		
							C	CANTX3	I/O	1		
							E	PWML0	I/O	3		
130	VDDSDMMC0	GPIOHS	PA1	GPIO	–	–	A	SDMMC0_CMD	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM0_IO1	I/O	1		
							C	CANRX3	I/O	1		
							D	D14	I/O	1,2		
							E	PWMH0	I/O	3		
126	VDDSDMMC0	GPIO	PA2	GPIO	–	–	A	SDMMC0_RSTN	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM0_IO2	I/O	1		
							C	PDMC1_CLK	I/O	1		
							D	D15	I/O	1,2		
							E	PWMH1	I/O	3		
							F	FLEXCOM1_IO0	I/O	3		
128	VDDSDMMC0	GPIOHS	PA3	GPIO	–	–	A	SDMMC0_DAT0	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM0_IO3	I/O	1		
							C	PDMC1_DS0	I/O	1		
							D	NWR1/NBS1	I/O	1,2		
							E	PWML3	I/O	3		
							F	FLEXCOM1_IO1	I/O	3		
121	VDDSDMMC0	GPIOHS	PA4	GPIO	–	–	A	SDMMC0_DAT1	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM0_IO4	I/O	1		
							C	PDMC1_DS1	I/O	1		
							D	NCS2	I/O	1,2		
							E	PWMH3	I/O	3		
							F	FLEXCOM2_IO0	I/O	3		
127	VDDSDMMC0	GPIOHS	PA5	GPIO	–	–	A	SDMMC0_DAT2	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM1_IO0	I/O	1		
							C	CANTX2	I/O	1		
							D	A23	I/O	1,2		
							E	PWMEXTRG0	I/O	3		
							F	FLEXCOM2_IO1	I/O	3		
124	VDDSDMMC0	GPIOHS	PA6	GPIO	–	–	A	SDMMC0_DAT3	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM1_IO1	I/O	1		
							C	CANRX2	I/O	1		
							D	A24	I/O	1,2		
							E	PWMEXTRG1	I/O	3		
							F	FLEXCOM3_IO0	I/O	3		

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
123	VDDSDMMC0	GPIOHS	PA7	GPIO	–	–	A	SDMMC0_DAT4	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM2_IO0	I/O	1		
							C	CANTX1	I/O	1		
							D	NWAIT	I/O	1,2		
							E	PWMFI0	I/O	3		
							F	FLEXCOM3_IO1	I/O	3		
122	VDDSDMMC0	GPIOHS	PA8	GPIO	–	–	A	SDMMC0_DAT5	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM2_IO1	I/O	1		
							C	CANRX1	I/O	1		
							D	NCS0	I/O	1,2		
							E	PWMFI1	I/O	3		
							F	FLEXCOM4_IO0	I/O	3		
119	VDDSDMMC0	GPIOHS	PA9	GPIO	–	–	A	SDMMC0_DAT6	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM2_IO2	I/O	1		
							C	CANTX0	I/O	1		
							D	SMCK	I/O	1,2		
							E	SPDIF_RX	I/O	1		
							F	FLEXCOM4_IO1	I/O	3		
120	VDDSDMMC0	GPIOHS	PA10	GPIO	–	–	A	SDMMC0_DAT7	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM2_IO3	I/O	1		
							C	CANRX0	I/O	1		
							D	NCS1	I/O	1,2		
							E	SPDIF_TX	I/O	1		
							F	FLEXCOM5_IO0	I/O	3		
129	VDDSDMMC0	GPIOHS	PA11	GPIO	–	–	A	SDMMC0_DS	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM2_IO4	I/O	1		
							D	A0/NBS0	I/O	1,2		
							E	TIOA0	I/O	1		
							F	FLEXCOM5_IO1	I/O	3		
131	VDDIOP0	GPIO	PA12	GPIO	–	–	A	SDMMC0_WP	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM1_IO3	I/O	1		
							D	FLEXCOM3_IO5	I/O	1		
							E	PWML2	I/O	3		
							F	FLEXCOM6_IO0	I/O	3		
132	VDDIOP0	GPIO	PA13	GPIO	–	–	A	SDMMC0_1V8SEL	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM1_IO2	I/O	1		
							D	FLEXCOM3_IO6	I/O	1		
							E	PWMH2	I/O	3		
							F	FLEXCOM6_IO1	I/O	3		
133	VDDIOP0	GPIO	PA14	GPIO	–	–	A	SDMMC0_CD	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM1_IO4	I/O	1		
							D	A25	I/O	1,2		
							E	PWML1	I/O	3		

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
180	VDDIOP0	GPIO	PA15	GPIO	–	–	A	G0_TXEN/G0_TXCTL	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM3_IO0	I/O	1		
							C	ISC_MCK	I/O	1		
							D	A1	I/O	1,2		
							E	TIOB0	I/O	1		
179	VDDIOP0	GPIO	PA16	GPIO	–	–	A	G0_TX0	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM3_IO1	I/O	1		
							C	ISC_D0	I/O	1		
							D	A2	I/O	1,2		
							E	TCLK0	I/O	1		
174	VDDIOP0	GPIO	PA17	GPIO	–	–	A	G0_TX1	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM3_IO2	I/O	1		
							C	ISC_D1	I/O	1		
							D	A3	I/O	1,2		
							E	TIOA1	I/O	1		
177	VDDIOP0	GPIO	PA18	GPIO	–	–	A	G0_RXDV/ G0_CRSDV/ G0_RXCTL	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM3_IO3	I/O	1		
							C	ISC_D2	I/O	1		
							D	A4	I/O	1,2		
							E	TIOB1	I/O	1		
182	VDDIOP0	GPIO	PA19	GPIO	–	–	A	G0_RX0	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM3_IO4	I/O	1		
							C	ISC_D3	I/O	1		
							D	A5	I/O	1,2		
							E	TCLK1	I/O	1		
175	VDDIOP0	GPIO	PA20	GPIO	–	–	A	G0_RX1	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM4_IO0	I/O	1		
							C	ISC_D4	I/O	1		
							D	A6	I/O	1,2		
							E	TIOA2	I/O	1		
178	VDDIOP0	GPIO	PA21	GPIO	–	–	A	G0_RXER	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM4_IO1	I/O	1		
							C	ISC_D5	I/O	1		
							D	A7	I/O	1,2		
							E	TIOB2	I/O	1		
176	VDDIOP0	GPIO	PA22	GPIO	–	–	A	G0_MDC	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM4_IO2	I/O	1		
							C	ISC_D6	I/O	1		
							D	A8	I/O	1,2		
							E	TCLK2	I/O	1		

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
184	VDDIOP0	GPIO	PA23	GPIO	–	–	A	G0_MDIO	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM4_IO3	I/O	1		
							C	ISC_D7	I/O	1		
							D	A9	I/O	1,2		
183	VDDIOP0	GPIO	PA24	GPIO	–	–	A	G0_TXCK/G0_REFCK	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM4_IO4	I/O	1		
							C	ISC_HSYNC	I/O	1		
							D	A10	I/O	1,2		
							E	FLEXCOM0_IO5	I/O	1		
181	VDDIOP0	GPIO	PA25	GPIO	–	–	A	G0_125CK	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM5_IO4	I/O	1		
							C	ISC_VSYNC	I/O	1		
							D	A11	I/O	1,2		
							E	FLEXCOM0_IO6	I/O	1		
							F	FLEXCOM7_IO0	I/O	3		
185	VDDIOP0	GPIO	PA26	GPIO	–	–	A	G0_TX2	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM5_IO2	I/O	1		
							C	ISC_FIELD	I/O	1		
							D	A12	I/O	1,2		
							E	TF0	I/O	1		
							F	FLEXCOM7_IO1	I/O	3		
186	VDDIOP0	GPIO	PA27	GPIO	–	–	A	G0_TX3	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM5_IO3	I/O	1		
							C	ISC_PCK	I/O	1		
							D	A13	I/O	1,2		
							E	TK0	I/O	1		
							F	FLEXCOM8_IO0	I/O	3		
187	VDDIOP0	GPIO	PA28	GPIO	–	–	A	G0_RX2	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM5_IO0	I/O	1		
							C	ISC_D8	I/O	1		
							D	A14	I/O	1,2		
							E	RD0	I/O	1		
							F	FLEXCOM8_IO1	I/O	3		
188	VDDIOP0	GPIO	PA29	GPIO	–	–	A	G0_RX3	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM5_IO1	I/O	1		
							C	ISC_D9	I/O	1		
							D	A15	I/O	1,2		
							E	RF0	I/O	1		
							F	FLEXCOM9_IO0	I/O	3		

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
3	VDDIOP0	GPIO	PA30	GPIO	–	–	A	G0_RXCK	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM6_IO4	I/O	1		
							C	ISC_D10	I/O	1		
							D	A16	I/O	1,2		
							E	RK0	I/O	1		
							F	FLEXCOM9_IO1	I/O	3		
4	VDDIOP0	GPIO	PA31	GPIO	–	–	A	G0_TXER	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM6_IO2	I/O	1		
							C	ISC_D11	I/O	1		
							D	A17	I/O	1,2		
							E	TD0	I/O	1		

Note:

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger

6.2.2 PIOB Pin List

Table 6-2. PIOB Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
7	VDDIOP0	GPIO	PB0	GPIO	–	–	A	G0_COL	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM6_IO3	I/O	1		
							C	EXT_IRQ0	I/O	1		
							D	A18	I/O	1,2		
							E	SPDIF_RX	I/O	2		
5	VDDIOP0	GPIO	PB1	GPIO	–	–	A	G0_CRS	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM6_IO1	I/O	1		
							C	EXT_IRQ1	I/O	1		
							D	A19	I/O	1,2		
							E	SPDIF_TX	I/O	2		
							F	FLEXCOM11_IO0	I/O	3		
6	VDDIOP0	GPIO	PB2	GPIO	–	–	A	G0_TSUCOMP	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM6_IO0	I/O	1		
							C	ADTRG	I/O	1		
							D	A20	I/O	1,2		
							F	FLEXCOM11_IO1	I/O	3		
139	VDDIOP0	GPIO	PB3	GPIO	–	–	A	RF1	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM11_IO0	I/O	1		
							C	PCK2	I/O	2		
							D	D8	I/O	1,2		

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
140	VDDIOP0	GPIO	PB4	GPIO	–	–	A	TF1	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM11_IO1	I/O	1		
							C	PCK3	I/O	2		
							D	D9	I/O	1,2		
141	VDDIOP0	GPIO	PB5	GPIO	–	–	A	TK1	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM11_IO2	I/O	1,2,3,4,5		
							C	PCK4	I/O	2		
							D	D10	I/O	1,2		
142	VDDIOP0	GPIO	PB6	GPIO	–	–	A	RK1	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM11_IO3	I/O	1,2,3,4,5		
							C	PCK5	I/O	2		
							D	D11	I/O	1,2		
143	VDDIOP0	GPIO	PB7	GPIO	–	–	A	TD1	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM11_IO4	I/O	1,2,3,4,5		
							C	FLEXCOM3_IO5	I/O	2,3,4,5		
							D	D12	I/O	1,2		
144	VDDIOP0	GPIO	PB8	GPIO	–	–	A	RD1	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM8_IO0	I/O	1		
							C	FLEXCOM3_IO6	I/O	2,3,4,5		
							D	D13	I/O	1,2		
156	VDDQSPI0	GPIOHS	PB9	GPIO	–	–	A	QSPI0_IO3	I/O	1	PIO, I, PU, ST	NAND Flash and FLEXCOM10 interfaces are not accessible. They are already used internally.
							B	FLEXCOM8_IO1	I/O	1		
							C	PDMC0_CLK	I/O	1		
							E	PWML0	I/O	2		
148	VDDQSPI0	GPIOHS	PB10	GPIO	–	–	A	QSPI0_IO2	I/O	1	PIO, I, PU, ST	
							B	FLEXCOM8_IO2	I/O	1		
							C	PDMC0_DS0	I/O	1		
							E	PWMH0	I/O	2		
158	VDDQSPI0	GPIOHS	PB11	GPIO	–	–	A	QSPI0_IO1	I/O	1	PIO, I, PU, ST	
							B	FLEXCOM8_IO3	I/O	1		
							C	PDMC0_DS1	I/O	1		
							E	PWML1	I/O	2		
157	VDDQSPI0	GPIOHS	PB12	GPIO	–	–	A	QSPI0_IO0	I/O	1	PIO, I, PU, ST	
							B	FLEXCOM8_IO4	I/O	1		
							C	FLEXCOM6_IO5	I/O	1		
							E	PWMH1	I/O	2		
151	VDDQSPI0	GPIO	PB13	GPIO	–	–	A	QSPI0_CS	I/O	1	PIO, I, PU, ST	
							B	FLEXCOM9_IO0	I/O	1		
							C	FLEXCOM6_IO6	I/O	1		
							E	PWML2	I/O	2		

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
155	VDDQSPI0	GPIOHS	PB14	GPIO	–	–	A	QSPI0_SCK	I/O	1	PIO, I, PU, ST	NAND Flash and FLEXCOM10 interfaces are not accessible. They are already used internally.
							B	FLEXCOM9_IO1	I/O	1		
							E	PWMH2	I/O	2		
154	VDDQSPI0	GPIOHS	PB15	GPIO	–	–	A	QSPI0_SCKN	I/O	1	PIO, I, PU, ST	
							B	FLEXCOM9_IO2	I/O	1		
							E	PWML3	I/O	2		
152	VDDQSPI0	GPIOHS	PB16	GPIO	–	–	A	QSPI0_IO4	I/O	1	PIO, I, PU, ST	
							B	FLEXCOM9_IO3	I/O	1		
							C	PCK0	I/O	1		
							E	PWMH3	I/O	2		
							F	EXT_IRQ0	I/O	2		
159	VDDQSPI0	GPIOHS	PB17	GPIO	–	–	A	QSPI0_IO5	I/O	1	PIO, I, PU, ST	
							B	FLEXCOM9_IO4	I/O	1		
							C	PCK1	I/O	1		
							E	PWMEXTRG0	I/O	2		
							F	EXT_IRQ1	I/O	2		
150	VDDQSPI0	GPIOHS	PB18	GPIO	–	–	A	QSPI0_IO6	I/O	1	PIO, I, PU, ST	
							C	PCK2	I/O	1		
							E	PWMEXTRG1	I/O	2		
149	VDDQSPI0	GPIOHS	PB19	GPIO	–	–	A	QSPI0_IO7	I/O	1	PIO, I, PU, ST	
							C	PCK3	I/O	1		
							E	PWMFI0	I/O	2		
153	VDDQSPI0	GPIOHS	PB20	GPIO	–	–	A	QSPI0_DQS	I/O	1	PIO, I, PU, ST	
							E	PWMFI1	I/O	2		
160	VDDQSPI0	GPIO	PB21	GPIO	–	–	A	QSPI0_INT	I/O	1	PIO, I, PU, ST	
							C	FLEXCOM9_IO5	I/O	1		
–	VDD_3V3	GPIO	PB22	GPIO	–	–	A	QSPI1_IO3	I/O	1	PIO, I, PU, ST	Fixed function. Used for QSPI memory interface embeds in the module.
–	VDD_3V3	GPIO	PB23	GPIO	–	–	A	QSPI1_IO2	I/O	1	PIO, I, PU, ST	
–	VDD_3V3	GPIO	PB24	GPIO	–	–	A	QSPI1_IO1	I/O	1	PIO, I, PU, ST	
–	VDD_3V3	GPIO	PB25	GPIO	–	–	A	QSPI1_IO0	I/O	1	PIO, I, PU, ST	
68	VDD_3V3	GPIO	PB26	GPIO	–	–	A	QSPI1_CS	I/O	1	PIO, I, PU, ST	
–	VDD_3V3	GPIO	PB27	GPIO	–	–	A	QSPI1_SCK	I/O	1	PIO, I, PU, ST	
52	VDDSDMMC1	GPIO	PB28	GPIO	–	–	A	SDMMC1_RSTN	I/O	1	PIO, I, PU, ST	–
							B	ADTRG	I/O	2		
							E	PWMFI0	I/O	1		
							F	FLEXCOM7_IO0	I/O	4		
53	VDDSDMMC1	GPIOHS	PB29	GPIO	–	–	A	SDMMC1_CMD	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM3_IO2	I/O	2,3,4,5		
							C	FLEXCOM0_IO5	I/O	2		
							D	TIOA3	I/O	1		
							E	PWMFI1	I/O	1		
							F	FLEXCOM7_IO1	I/O	4		

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
58	VDDSDMMC1	GPIOHS	PB30	GPIO	–	–	A	SDMMC1_CK	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM3_IO3	I/O	2,3,4,5		
							C	FLEXCOM0_IO6	I/O	2		
							D	TIOB3	I/O	1		
							E	PWMH0	I/O	1		
							F	FLEXCOM8_IO0	I/O	4		
54	VDDSDMMC1	GPIOHS	PB31	GPIO	–	–	A	SDMMC1_DAT0	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM3_IO4	I/O	2,3,4,5		
							C	FLEXCOM9_IO5	I/O	2,3,4,5		
							D	TCLK3	I/O	1		
							E	PWML0	I/O	1		
							F	FLEXCOM8_IO1	I/O	4		

Note:

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger

6.2.3 PIOC Pin List

Table 6-3. PIOC Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
55	VDDSDMMC1	GPIOHS	PC0	GPIO	–	–	A	SDMMC1_DAT1	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM3_IO0	I/O	2		
							D	TIOA4	I/O	1		
							E	PWML1	I/O	1		
							F	FLEXCOM9_IO0	I/O	4		
56	VDDSDMMC1	GPIOHS	PC1	GPIO	–	–	A	SDMMC1_DAT2	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM3_IO1	I/O	2		
							D	TIOB4	I/O	1		
							E	PWMH1	I/O	1		
							F	FLEXCOM9_IO1	I/O	4		
57	VDDSDMMC1	GPIOHS	PC2	GPIO	–	–	A	SDMMC1_DAT3	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM4_IO0	I/O	2		
							D	TCLK4	I/O	1		
							E	PWML2	I/O	1		
59	VDD_3V3	GPIO	PC3	GPIO	–	–	A	SDMMC1_WP	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM4_IO1	I/O	2		
							D	TIOA5	I/O	1		
							E	PWMH2	I/O	1		

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
60	VDD_3V3	GPIO	PC4	GPIO	–	–	A	SDMMC1_CD	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM4_IO2	I/O	2,3,4,5		
							C	FLEXCOM9_IO6	I/O	2,3,4,5		
							D	TIOB5	I/O	1		
							E	PWML3	I/O	1		
							F	FLEXCOM11_IO0	I/O	4		
61	VDD_3V3	GPIO	PC5	GPIO	–	–	A	SDMMC1_1V8SEL	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM4_IO3	I/O	2,3,4,5		
							C	FLEXCOM6_IO5	I/O	2,3,4,5		
							D	TCLK5	I/O	1		
							E	PWMH3	I/O	1		
							F	FLEXCOM11_IO1	I/O	4		
62	VDD_3V3	GPIO	PC6	GPIO	ACC_INP0	I/O	B	FLEXCOM4_IO4	I/O	2,3,4,5	PIO, I, PU, ST	–
							C	FLEXCOM6_IO6	I/O	2,3,4,5		
85	VDD_3V3	GPIO	PC7	GPIO	ACC_INN1	I/O	B	FLEXCOM7_IO0	I/O	2	PIO, I, PU, ST	–
86	VDD_3V3	GPIO	PC8	GPIO	ACC_INP1	I/O	B	FLEXCOM7_IO1	I/O	2	PIO, I, PU, ST	–
87	VDD_3V3	GPIO	PC9	GPIO	ACC_INN2	I/O	B	FLEXCOM7_IO2	I/O	2,3,4,5	PIO, I, PU, ST	–
							F	FLEXCOM1_IO0	I/O	4		
88	VDD_3V3	GPIO	PC10	GPIO	ACC_INP2	I/O	B	FLEXCOM7_IO3	I/O	2,3,4,5	PIO, I, PU, ST	–
							F	FLEXCOM1_IO1	I/O	4		
89	VDD_3V3	GPIO	PC11	GPIO	ACC_INN3	I/O	A	I2SMCC1_CK	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM7_IO4	I/O	2,3,4,5		
							F	FLEXCOM2_IO0	I/O	4		
90	VDD_3V3	GPIO	PC12	GPIO	ACC_INP3	I/O	A	I2SMCC1_WS	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM8_IO2	I/O	2,3,4,5		
							F	FLEXCOM2_IO1	I/O	4		
91	VDD_3V3	GPIO	PC13	GPIO	AD0	I/O	A	I2SMCC1_MCK	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM8_IO1	I/O	2		
							F	FLEXCOM3_IO0	I/O	4		
92	VDD_3V3	GPIO	PC14	GPIO	AD1	I/O	A	I2SMCC1_DOUT0	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM8_IO0	I/O	2		
							F	FLEXCOM3_IO1	I/O	4		
93	VDD_3V3	GPIO	PC15	GPIO	AD2	I/O	A	I2SMCC1_DOUT1	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM8_IO3	I/O	2,3,4,5		
							F	FLEXCOM4_IO0	I/O	4		
99	VDD_3V3	GPIO	PC16	GPIO	AD3	I/O	A	I2SMCC1_DOUT2	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM8_IO4	I/O	2,3,4,5		
							F	FLEXCOM4_IO1	I/O	4		
100	VDD_3V3	GPIO	PC17	GPIO	AD4/ RTCOUT0	I/O	A	I2SMCC1_DOUT3	I/O	1	PIO, I, PU, ST	–
							B	EXT_IRQ0	I/O	3		
							F	FLEXCOM5_IO0	I/O	4		

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
101	VDD_3V3	GPIO	PC18	GPIO	AD5/ RTCOUT1	I/O	A	I2SMCC1_DIN0	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM9_IO0	I/O	2		
							F	FLEXCOM5_IO1	I/O	4		
102	VDD_3V3	GPIO	PC19	GPIO	AD6	I/O	A	I2SMCC1_DIN1	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM9_IO1	I/O	2		
							F	FLEXCOM6_IO0	I/O	4		
103	VDD_3V3	GPIO	PC20	GPIO	AD7	I/O	A	I2SMCC1_DIN2	I/O	1	PIO, I, PU, ST	–
							B	FLEXCOM9_IO4	I/O	2,3,4,5		
							F	FLEXCOM6_IO1	I/O	4		
–	VDD_3V3	GPIO	PC21	GPIO	AD8	I/O	D	D3	I/O	2	PIO, I, PU, ST	Fixed function. Used for NAND Flash interface embeds in the module.
–	VDD_3V3	GPIO	PC22	GPIO	AD9	I/O	D	D4	I/O	2	PIO, I, PU, ST	
–	VDD_3V3	GPIO	PC23	GPIO	AD10	I/O	D	D5	I/O	2	PIO, I, PU, ST	
–	VDD_3V3	GPIO	PC24	GPIO	AD11	I/O	D	D6	I/O	2	PIO, I, PU, ST	
66	VDD_3V3	GPIO	PC25	GPIO	–	–	A	NTRST	I/O	1	NTRST, PU, ST	–
64	VDD_3V3	GPIO	PC26	GPIO	–	–	A	TCK_SWCLK	I/O	1	TCK_SWCLK, ST	–
67	VDD_3V3	GPIO	PC27	GPIO	–	–	A	TMS_SWDIO	I/O	1	TMS_SWDIO, PU, ST	–
63	VDD_3V3	GPIO	PC28	GPIO	–	–	A	TDI	I/O	1	TDI, PU, ST	–
65	VDD_3V3	GPIO	PC29	GPIO	–	–	A	TDO	I/O	1	TDO, ST	–
17	VDD_3V3	GPIO	PC30	GPIO	–	–	B	FLEXCOM10_IO0	I/O	2	PIO, I, PD, ST	Fixed function. Used for PMIC control.
16	VDD_3V3	GPIO	PC31	GPIO	–	–	B	FLEXCOM10_IO1	I/O	2	PIO, I, PD, ST	

Note:

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger

6.2.4 PIOD Pin List

Table 6-4. PIOD Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
106	VDD_3V3	GPIO	PD0	GPIO	AD14	I/O	B	FLEXCOM11_IO0	I/O	2	PIO, I, PD, ST	–
107	VDD_3V3	GPIO	PD1	GPIO	AD15	I/O	B	FLEXCOM11_IO1	I/O	2	PIO, I, PD, ST	–

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
–	VDD_3V3	GPIO	PD2	GPIO	–	–	D	D7	I/O	2	PIO, I, PU, ST	Fixed function. Used for NAND Flash interface embeds in the module.
–	VDD_3V3	GPIOHS	PD3	GPIO	–	–	D	NANDRDY	I/O	2	PIO, I, PU, ST	
39	VDD_3V3	GPIOHS	PD4	GPIO	–	–	D	NCS3/NANDCS	I/O	2	PIO, I, PU, ST	
–	VDD_3V3	GPIOHS	PD5	GPIO	–	–	D	NWE/NWR0/ NANDWE	I/O	2	PIO, I, PU, ST	
–	VDD_3V3	GPIOHS	PD6	GPIO	–	–	D	NRD/NANDOE	I/O	2	PIO, I, PU, ST	
–	VDD_3V3	GPIOHS	PD7	GPIO	–	–	D	A21/NANDALE	I/O	2	PIO, I, PU, ST	
–	VDD_3V3	GPIOHS	PD8	GPIO	–	–	D	A22/NANDCLE	I/O	2	PIO, I, PU, ST	
–	VDD_3V3	GPIO	PD9	GPIO	–	–	D	D0	I/O	2	PIO, I, PU, ST	
–	VDD_3V3	GPIO	PD10	GPIO	–	–	D	D1	I/O	2	PIO, I, PU, ST	
–	VDD_3V3	GPIO	PD11	GPIO	–	–	D	D2	I/O	2	PIO, I, PU, ST	
20	VDD_3V3	GPIO	PD12	GPIO	–	–	A	PCK1	I/O	2	PIO, I, PU, ST	–
							B	FLEXCOM1_IO0	I/O	2		
							D	CANTX0	I/O	2		
							E	TIOB3	I/O	2		
21	VDD_3V3	GPIO	PD13	GPIO	–	–	A	I2SMCC0_CK	I/O	2	PIO, I, PU, ST	–
							B	FLEXCOM1_IO1	I/O	2		
							C	PWML0	I/O	4		
							D	CANRX0	I/O	2		
							E	TCLK3	I/O	2		
22	VDD_3V3	GPIO	PD14	GPIO	–	–	A	I2SMCC0_MCK	I/O	2	PIO, I, PU, ST	–
							B	FLEXCOM1_IO2	I/O	2,3,4		
							C	PWMH0	I/O	4		
							D	CANTX1	I/O	2		
							E	TIOA4	I/O	2		
							F	FLEXCOM2_IO0	I/O	5		
19	VDD_3V3	GPIO	PD15	GPIO	–	–	A	I2SMCC0_WS	I/O	2	PIO, I, PU, ST	–
							B	FLEXCOM1_IO3	I/O	2,3,4		
							C	PWML1	I/O	4		
							D	CANRX1	I/O	2		
							E	TIOB4	I/O	2		
							F	FLEXCOM2_IO1	I/O	5		
24	VDD_3V3	GPIO	PD16	GPIO	–	–	A	I2SMCC0_DOUT0	I/O	2	PIO, I, PU, ST	–
							B	FLEXCOM1_IO4	I/O	2,3,4		
							C	PWMH1	I/O	4		
							D	CANTX2	I/O	2		
							E	TCLK4	I/O	2		
							F	FLEXCOM3_IO0	I/O	5		
23	VDD_3V3	GPIO	PD17	GPIO	–	–	A	I2SMCC0_DOUT1	I/O	2	PIO, I, PU, ST	–
							B	FLEXCOM2_IO0	I/O	2		
							C	PWML2	I/O	4		
							D	CANRX2	I/O	2		
							E	TIOA5	I/O	2		
							F	FLEXCOM3_IO1	I/O	5		

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
111	VDD_3V3	GPIO	PD18	GPIO	–	–	A	I2SMCC0_DOUT2	I/O	2	PIO, I, PU, ST	–
							B	FLEXCOM2_IO1	I/O	2		
							C	PWMH2	I/O	4		
							D	CANTX3	I/O	2		
							E	TIOB5	I/O	2		
							F	FLEXCOM4_IO0	I/O	5		
110	VDD_3V3	GPIO	PD19	GPIO	–	–	A	I2SMCC0_DOUT3	I/O	2	PIO, I, PU, ST	–
							B	FLEXCOM2_IO2	I/O	2,3,4,5		
							C	PWML3	I/O	4		
							D	CANRX3	I/O	2		
							E	TCLK5	I/O	2		
							F	FLEXCOM4_IO1	I/O	5		
29	VDD_3V3	GPIO	PD20	GPIO	–	–	A	PCK0	I/O	3	PIO, I, PU, ST	–
							B	FLEXCOM2_IO3	I/O	2,3,4,5		
							C	PWMH3	I/O	4		
							D	CANTX4	I/O	2		
							F	FLEXCOM5_IO0	I/O	5		
26	VDD_3V3	GPIO	PD21	GPIO	–	–	A	PCK1	I/O	3	PIO, I, PU, ST	–
							B	FLEXCOM2_IO4	I/O	2,3,4,5		
							D	CANRX4	I/O	2		
							F	FLEXCOM5_IO1	I/O	5		
							G	G1_TXEN	I/O	1		
27	VDD_3V3	GPIO	PD22	GPIO	–	–	A	PDMC0_CLK	I/O	2	PIO, I, PU, ST	–
							C	PWMEXTRG0	I/O	4		
							D	RD1	I/O	2		
							F	CANTX5	I/O	2		
							G	G1_TX0	I/O	1		
28	VDD_3V3	GPIO	PD23	GPIO	–	–	A	PDMC0_DS0	I/O	2	PIO, I, PU, ST	–
							C	PWMEXTRG1	I/O	4		
							D	RF1	I/O	2		
							E	ISC_MCK	I/O	2		
							F	CANRX5	I/O	2		
							G	G1_TX1	I/O	1		
32	VDD_3V3	GPIO	PD24	GPIO	–	–	A	PDMC0_DS1	I/O	2	PIO, I, PU, ST	–
							C	PWMFI0	I/O	4		
							D	RK1	I/O	2		
							E	ISC_D0	I/O	2		
							G	G1_RXDV/G1_CRSDV	I/O	1		

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
30	VDD_3V3	GPIO	PD25	GPIO	–	–	A	PDMC1_CLK	I/O	2	PIO, I, PU, ST	–
							B	FLEXCOM5_IO0	I/O	2		
							C	PWMFI1	I/O	4		
							D	TD1	I/O	2		
							E	ISC_D1	I/O	2		
							G	G1_RX0	I/O	1		
36	VDD_3V3	GPIO	PD26	GPIO	–	–	A	PDMC1_DS0	I/O	2	PIO, I, PU, ST	–
							B	FLEXCOM5_IO1	I/O	2		
							C	ADTRG	I/O	3		
							D	TF1	I/O	2		
							E	ISC_D2	I/O	2		
							G	G1_RX1	I/O	1		
34	VDD_3V3	GPIO	PD27	GPIO	–	–	A	PDMC1_DS1	I/O	2	PIO, I, PU, ST	–
							B	FLEXCOM5_IO2	I/O	2,3,4,5		
							C	TIOA0	I/O	3		
							D	TK1	I/O	2		
							E	ISC_D3	I/O	2		
							G	G1_RXER	I/O	1		
35	VDD_3V3	GPIO	PD28	GPIO	–	–	A	RD0	I/O	2	PIO, I, PU, ST	–
							B	FLEXCOM5_IO3	I/O	2,3,4,5		
							C	TIOB0	I/O	3		
							D	I2SMCC1_CK	I/O	2		
							E	ISC_D4	I/O	2		
							F	PWML3	I/O	5		
							G	G1_MDC	I/O	1		
33	VDD_3V3	GPIO	PD29	GPIO	–	–	A	RF0	I/O	2	PIO, I, PU, ST	–
							B	FLEXCOM5_IO4	I/O	2,3,4,5		
							C	TCLK0	I/O	3		
							D	I2SMCC1_WS	I/O	2		
							E	ISC_D5	I/O	2		
							F	PWMH3	I/O	5		
							G	G1_MDIO	I/O	1		
31	VDD_3V3	GPIO	PD30	GPIO	–	–	A	RK0	I/O	2	PIO, I, PU, ST	–
							B	FLEXCOM6_IO0	I/O	2		
							C	TIOA1	I/O	3		
							D	I2SMCC1_MCK	I/O	2		
							E	ISC_D6	I/O	2		
							F	PWMEXTRG0	I/O	5		
							G	G1_TXCK/G1_REFCK	I/O	1		

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
37	VDD_3V3	GPIO	PD31	GPIO	–	–	A	TD0	I/O	2	PIO, I, PU, ST	–
							B	FLEXCOM6_IO1	I/O	2		
							C	TIOB1	I/O	3		
							D	I2SMCC1_DOUT0	I/O	2		
							E	ISC_D7	I/O	2		
							F	PWMEXTRG1	I/O	5		
							G	G1_TX2	I/O	1		

Note:

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger

6.2.5 PIOE Pin List

Table 6-5. PIOE Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
44	VDD_3V3	GPIO	PE0	GPIO	–	–	A	TF0	I/O	2	PIO, I, PU, ST	–
							B	FLEXCOM6_IO2	I/O	2,3,4,5		
							C	TCLK1	I/O	3		
							D	I2SMCC1_DOUT1	I/O	2		
							E	ISC_HSYNC	I/O	2		
							F	PWMFI0	I/O	5		
							G	G1_TX3	I/O	1		
45	VDD_3V3	GPIO	PE1	GPIO	–	–	A	TK0	I/O	2	PIO, I, PU, ST	–
							B	FLEXCOM6_IO3	I/O	2,3,4,5		
							C	TIOA2	I/O	3		
							D	I2SMCC1_DOUT2	I/O	2		
							E	ISC_VSYNC	I/O	2		
							F	PWMFI1	I/O	5		
							G	G1_RX2	I/O	1		
47	VDD_3V3	GPIO	PE2	GPIO	–	–	A	PWML0	I/O	5	PIO, I, PU, ST	–
							B	FLEXCOM6_IO4	I/O	2,3,4,5		
							C	TIOB2	I/O	3		
							D	I2SMCC1_DOUT3	I/O	2		
							E	ISC_FIELD	I/O	2		
							G	G1_RX3	I/O	1		
46	VDD_3V3	GPIO	PE3	GPIO	–	–	A	PWMH0	I/O	5	PIO, I, PU, ST	–
							B	FLEXCOM0_IO0	I/O	4		
							C	TCLK2	I/O	3		
							D	I2SMCC1_DIN0	I/O	2		
							E	ISC_PCK	I/O	2		
							G	G1_RXCK	I/O	1		

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.....continued

Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST	
49	VDD_3V3	GPIO	PE4	GPIO	–	–	A	PWML1	I/O	5	PIO, I, PU, ST	–
							B	FLEXCOM0_IO1	I/O	4		
							C	TIOA3	I/O	3		
							D	I2SMCC1_DIN1	I/O	2		
							E	ISC_D8	I/O	2		
							G	G1_TXER	I/O	1		
48	VDD_3V3	GPIO	PE5	GPIO	–	–	A	PWMH1	I/O	5	PIO, I, PU, ST	–
							B	FLEXCOM0_IO2	I/O	4		
							C	TIOB3	I/O	3		
							D	I2SMCC1_DIN2	I/O	2		
							E	ISC_D9	I/O	2		
							G	G1_COL	I/O	1		
50	VDD_3V3	GPIO	PE6	GPIO	–	–	A	PWML2	I/O	5	PIO, I, PU, ST	–
							B	FLEXCOM0_IO3	I/O	4		
							C	TCLK3	I/O	3		
							D	I2SMCC1_DIN3	I/O	2		
							E	ISC_D10	I/O	2		
							G	G1_CRS	I/O	1		
–	VDD_3V3	GPIO	PE7	GPIO	–	–	MCP16502 Interrupt				PIO, I, PU, ST	–

Note:

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger

6.2.6 System Pin List

Table 6-6. System Pin Description

Pin No.	Pin Name	Power Rail	I/O Type	Description	Active Level
116	PIOBU0	VBAT	I/O	Tamper I/Os	–
115	PIOBU1	VBAT	I/O	Tamper I/Os	–
117	PIOBU2	VBAT	I/O	Tamper I/Os	–
118	PIOBU3	VBAT	I/O	Tamper I/Os	–
79	HHSA_CC1	VDD_3V3	I/O	Pins to identify the USBA male side	–
82	HHSA_CC2	VDD_3V3	I/O	Pins to identify the USBA male side	–
80	HHSA_DM	VDD_3V3	I/O	USB host/device port A high speed data -	–
81	HHSA_DP	VDD_3V3	I/O	USB host/device port A high speed data +	–
74	HHSB_CC1	VDD_3V3	I/O	Pins to identify the USBB male side	–
77	HHSB_CC2	VDD_3V3	I/O	Pins to identify the USBB male side	–
75	HHSB_DM	VDD_3V3	I/O	USB host/device port B high speed data -	–
76	HHSB_DP	VDD_3V3	I/O	USB host/device port B high speed data +	–
71	HHSC_DM	VDD_3V3	I/O	USB host port C high speed data -	–
72	HHSC_DP	VDD_3V3	I/O	USB host port C high speed data +	–
164	MIPI_CLKN	VDDOUT25	I	MIPI DPHY differential input clock lane -	–
163	MIPI_CLKP	VDDOUT25	I	MIPI DPHY differential input clock lane +	–
168	MIPI_DN0	VDDOUT25	I	MIPI DPHY differential input data lane 0 -	–

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Pin No.	Pin Name	Power Rail	I/O Type	Description	Active Level
166	MIPI_DN1	VDDOUT25	I	MIPI DPHY differential input data lane 1 -	–
167	MIPI_DP0	VDDOUT25	I	MIPI DPHY differential input data lane 0 +	–
165	MIPI_DP1	VDDOUT25	I	MIPI DPHY differential input data lane 1 +	–
105	NRST	VDD_3V3	I/O, PU	External nReset input/output	Low
104	NRST_OUT	VDD_3V3	O	Microprocessor reset output	Low
146	SHDN	VBAT	O	Shutdown control	–
134	WKUP0	VBAT	I	Wake-up input	–
113	AUDIOCLK	VDD_3V3	O	Audio clock output	–
114	JTAGSEL	VBAT	I, PD	JTAG selection	High
14	MCP16502_HPM	5V_MAIN	I	High Performance mode input pin. In combination with PWRHLD and LPM, this pin defines the MCP16502 power mode status. Connect to ground if not used.	High
15	NSTART_SOM	5V_MAIN	I, PU	Start Event input. Drive nSTRT to low to initiate a start-up sequence. nSTRT is pulled up internally. A capacitor can be connected to nSTRT to automatically initiate a power-up sequence when the main supply rises.	Low
8	SEL_VLDO1	5V_MAIN	I	LDO1 Default Output Voltage Selection pin. Three-state input	–
98	24M_EN	VDD_3V3	I	24-MHz MEMS oscillator input pin used for the main clock	High
38	NAND_CS_IN	VDD_3V3	I, PU	NAND Flash chip select input. Connect to pin 39.	Low
69	QSPI1_CS_IN	VDD_3V3	I, PU	NAND Flash chip select input. Connect to pin 68.	Low

6.2.7 Power Pin List

Table 6-7. Power Pin Description

Pin No.	Pin Name	Type	Description
170	VBAT	Input power	Backup voltage input
162	VDDIOP0	Input power	VDDIOP0 voltage input
171	VDDQSPI0	Input power	QSPI0 voltage input
172	VDDSDMMC0	Input power	VDDSDMMC0 voltage input
109	VDDSDMMC1	Input power	VDDSDMMC1 voltage input
9	5V_MAIN	Input power	5V main input supply
10	5V_MAIN	Input power	5V main input supply
173	VDD_3V3	Output power	3.3V I/Os voltage output
11	VLDO1	Output power	VLDO1 output voltage
12	VLDO2	Output power	VLDO2 output voltage
1,2,13,18,25,40,41,42,43,51,70,73,78, 83,84,94,95,96,97,108,112,135,136,137, 138,145,147,161,169,189,190	GND	Ground power	Module ground

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7. Power Considerations

7.1 Power Supplies

Table 7-1. SAMA7G54 SOM Series Power Supplies

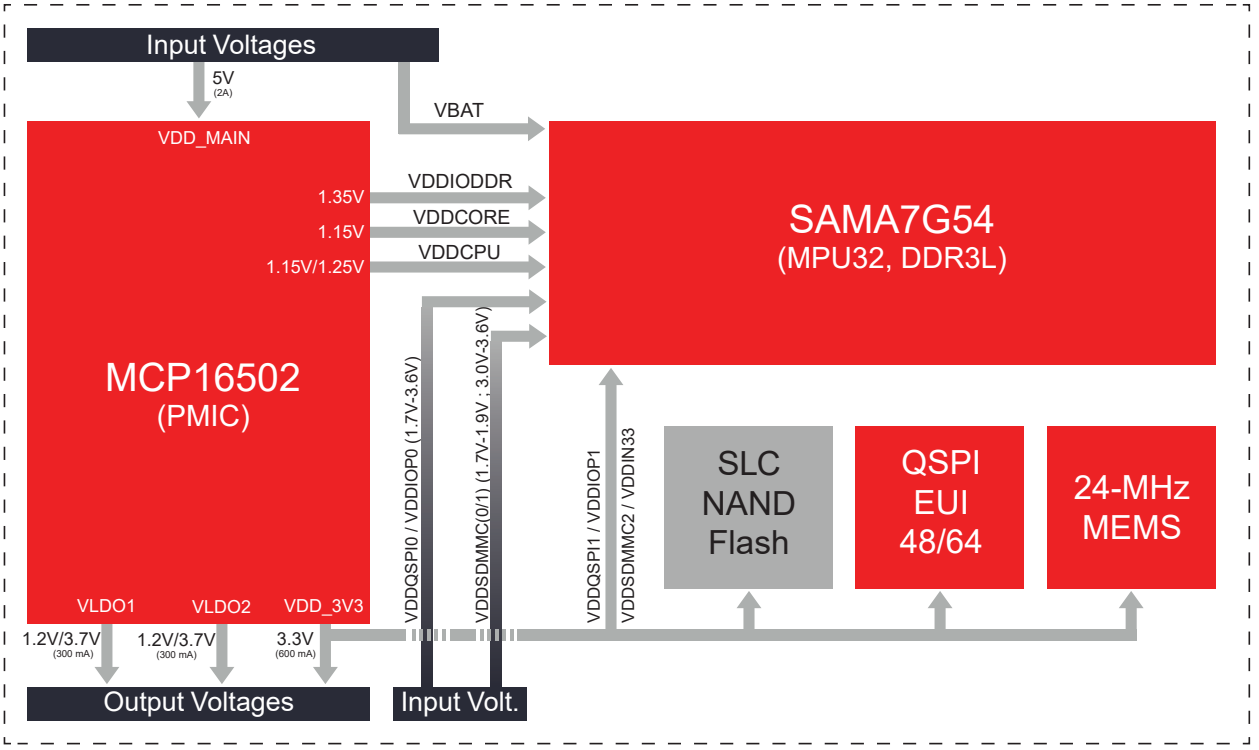
Pin No.	Name	Power Type	Voltage Range	Output Current Capability	Power Domain
170	VBAT	Input	(1)	–	Backup supply input
162	VDDIOP0	Input	(1)	–	VDDIOP0 power rail supply input
171	VDDQSPI0	Input	(1)	–	QSPI0 power rail supply input
172	VDDSDMMC0	Input	(1)	–	VDDSDMMC0 power rail supply input
109	VDDSDMMC1	Input	(1)	–	VDDSDMMC1 power rail supply input
9, 10	5V_MAIN	Input	(1)	–	System power input
173	VDD_3V3	Output	3.3V ±2%	600 mA	I/O supply and customer application output
11	VLDO1	Output	[1.2V - 3.7V]	300 mA	Adjustable output depending on application settings
12	VLDO2	Output	[1.2V - 3.7V] - 3.3V	300 mA	Adjustable output depending on application settings

Note:

1. See voltage range in Table 10-2.

The Microchip SAMA7G54 System-On-Module Series is supplied by a unique input (5V_MAIN) and its internal supplies are delivered by a power management unit (MCP16502), as shown in the following figure.

Figure 7-1. SAMA7G54 SOM Series Power Architecture



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7.2 Power-Up/Power-Down Considerations

At power-up, from a power supply sequencing perspective, the SAMA7G54 SOM Series power supplies are categorized into six independent groups:

- 5V_MAIN (main supply)
- VBAT (backup supply)
- VDD_3V3 (internal periphery group) containing VDDIN33, VDDIOP1, VDDSDMMC2 and VDDQSPI1 supplies
- VDDIODDR supply (internal memory group)
- VDDQSPI0, VDDIOP0, VDDSDMMC0 and VDDSDMMC1 input supplies (external periphery group)
- VDDCORE and VDDCPU supplies (core group)

Figure 7-2 shows the recommended power-up sequence.

Notes:

- VBAT
  - When supplied from a precharged storage element (battery, supercapacitor or micro-battery), VBAT is an always-on supply input and is therefore not part of the power supply sequencing.
  - When no storage element is used on VBAT in the application, VBAT must be tied to VDD_3V3.
  - When a supercapacitor or a micro-battery is used in the application to power VBAT in Backup mode, this element must be isolated from VBAT during its (slow) charge, so that VBAT closely follows VDD_3V3. In Table 7-2, the parameter t_1 limits the delay to establish VBAT after VDD_3V3.
- VDDOUT25 is the output of the internal 2.5V regulator and therefore there is no power supply requirement on this pin. VDDOUT25 is automatically started at VDD_3V3 rise when VDD_3V3 is above its Power-On Reset threshold.

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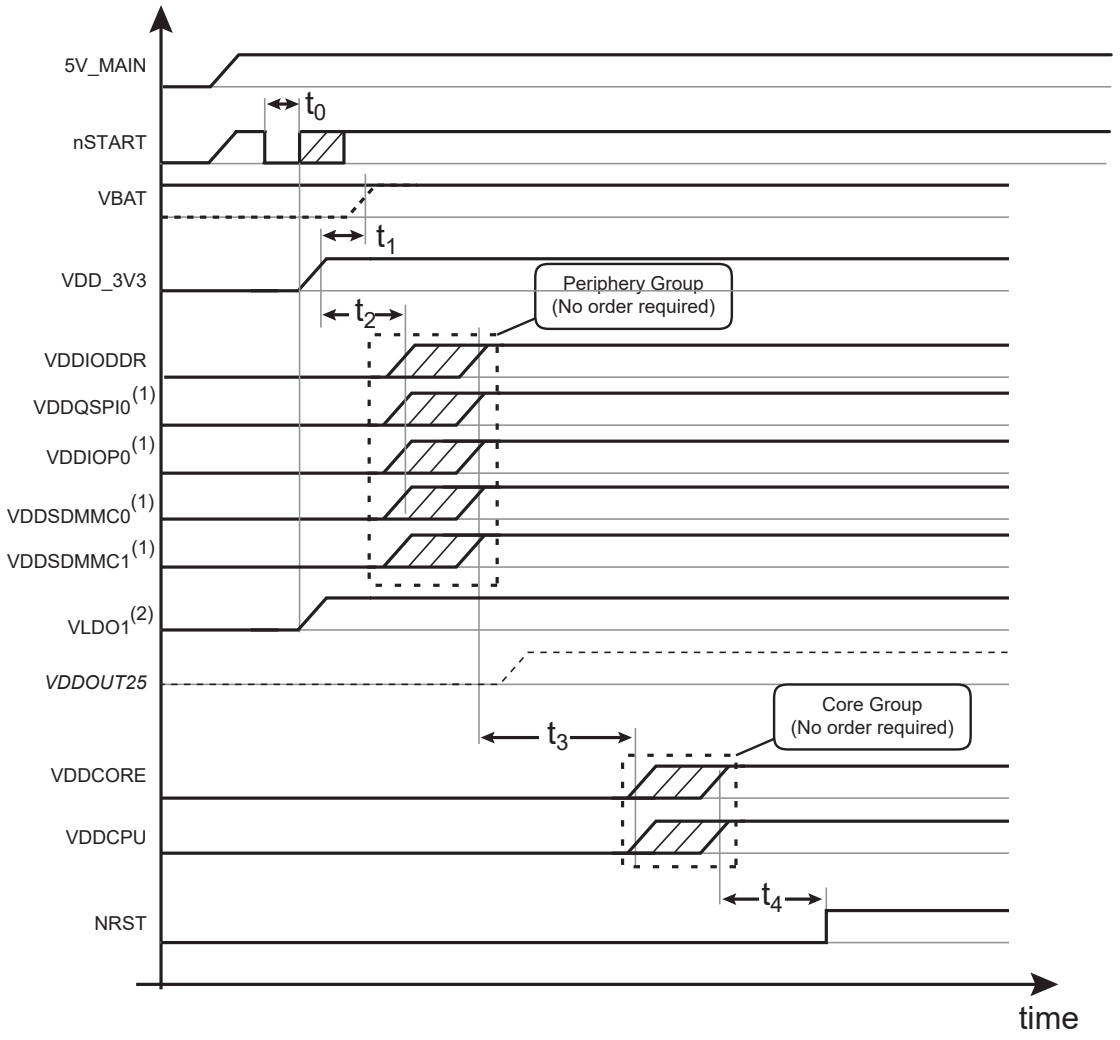
Figure 7-2. Recommended Power-Up Sequence



Notes:

1. If one or all VDDQSPI0, VDDIOP0, VDDSDMMC0 and VDDSDMMC1 are supplied externally, the power must be applied at the same time or after the presence of VDD_3V3.
2. VLDO1 is started at the same time as VDD_3V3. It is the default state at the first start-up. The VLDO1 "On" condition can be changed by the I²C interface.

Table 7-2. Power-Up Timing Requirements

Symbol	Parameter	Conditions(1)	Min	Typ(2)	Max	Unit
t_0	NSTART_SOM deglitch time	NSTART_SOM pin falling edge	0.5	–	–	ms
t_1	VBAT delay	Delay from established VDD_3V3 to established VBAT	–	–	0.2	ms
t_2(2)	VDD_3V3 to Periphery group delay	Delay from established VDD_3V3 to the periphery group established supply	–	8	–	ms
t_3(2)	Periphery group to VDDCORE/ VDDCPU delay	Delay from the periphery group established supply to the VDDCORE and VDDCPU supplies turn-on	–	4	–	ms
t_4(2)	Reset delay at power-up	From established VDDCORE/VDDCPU to NRST high	–	16	–	ms

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Notes:

1. The term "established" refers to a power supply having reached 90% of its final value.
2. t_2, t_3 and t_4 can be configured after the first start-up by interfacing with PMIC on the I²C interface.

The following figure shows the SAMA7G54 SOM Series power-down sequence that starts by asserting the NRST line to 0.

Once NRST is asserted, the supply inputs can be immediately shut down without any specific timing or order. VBAT may not be shut down if the application uses a backup storage element on this supply input.

Figure 7-3. Recommended Power-Down Sequence

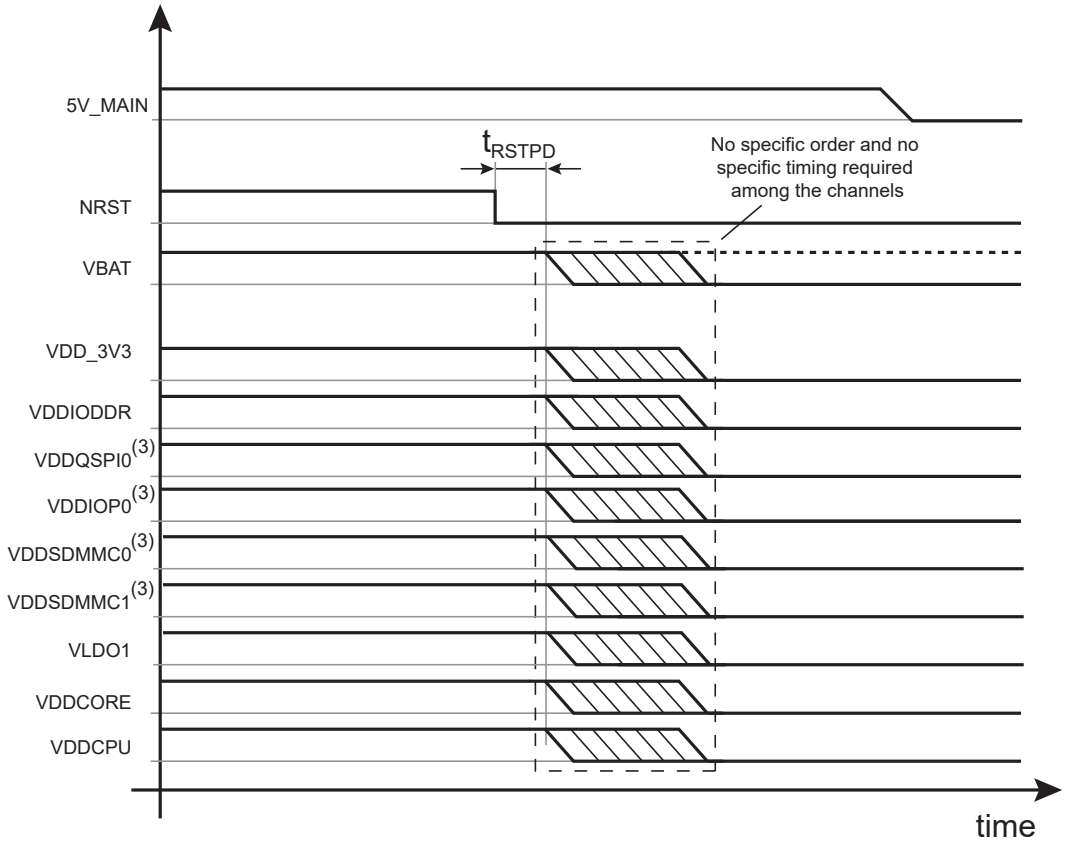

Table 7-3. Power-Down Timing Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{RSTPD}	NRST delay at power-down	Delay from NRST asserted to first supply turn-off	0	–	–	ms

7.3 Power Management Unit

The Microchip SAMA7G54 System-On-Module is supplied by an external supply (5V_MAIN) and generates its own internal supplies by interfacing with the Microchip MCP16502 Power Management Unit.

The MCP16502 is a fully-featured Power Management Integrated Circuit (PMIC), cost and size-optimized for Microchip MPU devices such as SAMA7G54.

The MCP16502 integrates four DC-DC buck regulators used for system supplying and two auxiliary LDOs for customer purpose.

- All buck channels can support loads up to 1A. All bucks are 100% duty cycle capable.

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  - DCDC1 set to 3.3 V supplies all pads of the embedded devices. This power rail offers a 600-mA load to customer applications through VDD_3V3 (pin 173).
  - DCDC2 set to 1.35V supplies the DDR3L memory. It is used internally only.
  - DCDC3 set to 1.15V supplies the microprocessor core. It is used internally only.
  - DCDC4 set to 1.15V/1.25V supplies the microprocessor CPU. It is used internally only.
- One 300 mA LDO is provided so that sensitive analog loads can be supported. The LDO output voltage, named VLDO1 (pin 11), is configured by a three-state pin named SEL_VLDO1 (pin 8) at power-up and can deliver 1.8V, 2.5V or 3.3V. Other voltage values can be reached after system initialization by a I²C interface access.
- One 300 mA LDO is provided so that sensitive analog loads can be supported. The LDO output voltage, named VLDO2 (pin 12), is disabled by default at power-up. Output voltage values are set through an I²C interface access after system initialization.

The default power channel sequencing is built-in, as required by the Microchip SAMA7G54 MPU device.

Active discharge resistors are provided on each output. All buck channels support safe start-up into pre-biased outputs.

The MCP16502 is available in a 5x5 mm 32-pin VQFN package.

For more information, refer to the MCP16502 data sheet (see Reference Documents).

The SEL_VLDO1 pin is meant to program the default settings of the VLDO1 power rail, which must be activated during the power-up sequence. It cannot be managed dynamically by the host.

The default value is selectable among three options corresponding to three different states of the relevant pin: connected to ground (Low), connected to input supply (High) or left unconnected (High-Z).

The VLDO1 default voltage can be selected by means of the SEL_VLDO1 pin, as shown in the table below.

Table 7-4. VLDO1 Voltage vs. SEL_VLDO1 Pin

SEL_VLDO1 Status	VLDO1 Output Voltage
Low	1.8V
High-Z	2.5V
High	3.3V

The LPM pin of the Microchip SAMA7G54 System-On-Module, combined with the HPM and PWRHLD status pins of the MCP16502 PMIC, defines different power states, which are illustrated in Table 7-5.

Note: LPM is controlled by the MPU, and HPM is controlled externally. For more information, refer to the MCP16502 data sheet (see Reference Documents).

Table 7-5. MCP16502 Default Power States

PWRHLD	LPM	HPM	Buck1	Buck2	Buck3	Buck4	LDO1	LDO2	nRST	Power State(1)
0	0	0	Off	Off	Off	Off	Off	Off	Low	Off
0	1	0	Off	On(2)	Off	On(2)	Off	Off	Low	Hibernate mode
1	1	0	On(2)	On(2)	On(2)	On(2)	On	Off	HiZ	Low-Power mode
1	0	0	On(3)	On(3)	On(3)	On(3)	On	Off	HiZ	Active mode
1	0	1	On(3)	On(3)	On(3)	On(3)	On	Off	HiZ	High Performance Active mode

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Notes:

1. Only allowed modes are listed. If some PWRHLD/LPM/HPM combination is not listed, the mode is not allowed.
2. In this mode, the DCDC is configured in Automatic Pulse-Frequency Modulation (Auto-PFM) mode.
3. In this mode, the DCDC is configured in Force Pulse-Width Modulation (FPWM) mode.

For more information about the use of the MCP16502 PMIC LPM feature, refer to the MCP16502 data sheet (see Reference Documents).

7.4 Power Configurations

Two different configurations, depending on customer use, are available.

- Single supply—The SAMA7G54 SOM Series can be supplied by only one input supply (for example, a 5V AC/DC wall adapter), and other input supplies can be connected to the internal 3.3V regulator VDD_3V3. All the PIO lines are supplied at 3.3V.
- Multiple supplies—The SAMA7G54 SOM Series can be supplied by a 5V supply and a backup battery. Some PIO lines, such as VDDQSPI0, VDDIOP0, VDDSDMMC0 and VDDSDMMC1, are supplied by different LDOs for specific applications.

Figure 7-4. SAMA7G54 SOM Series Single Supply Connection Example

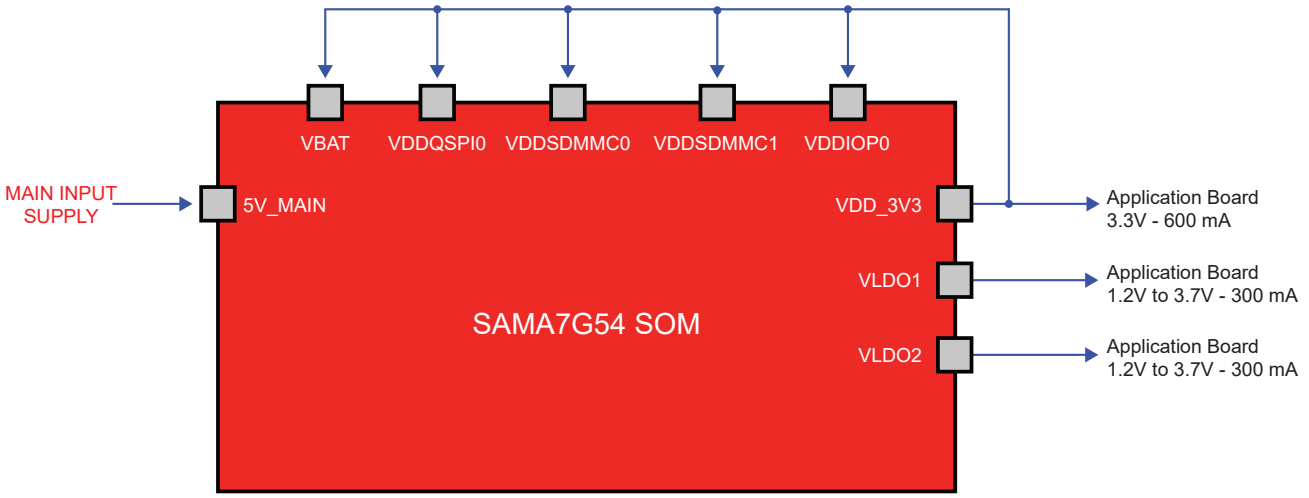

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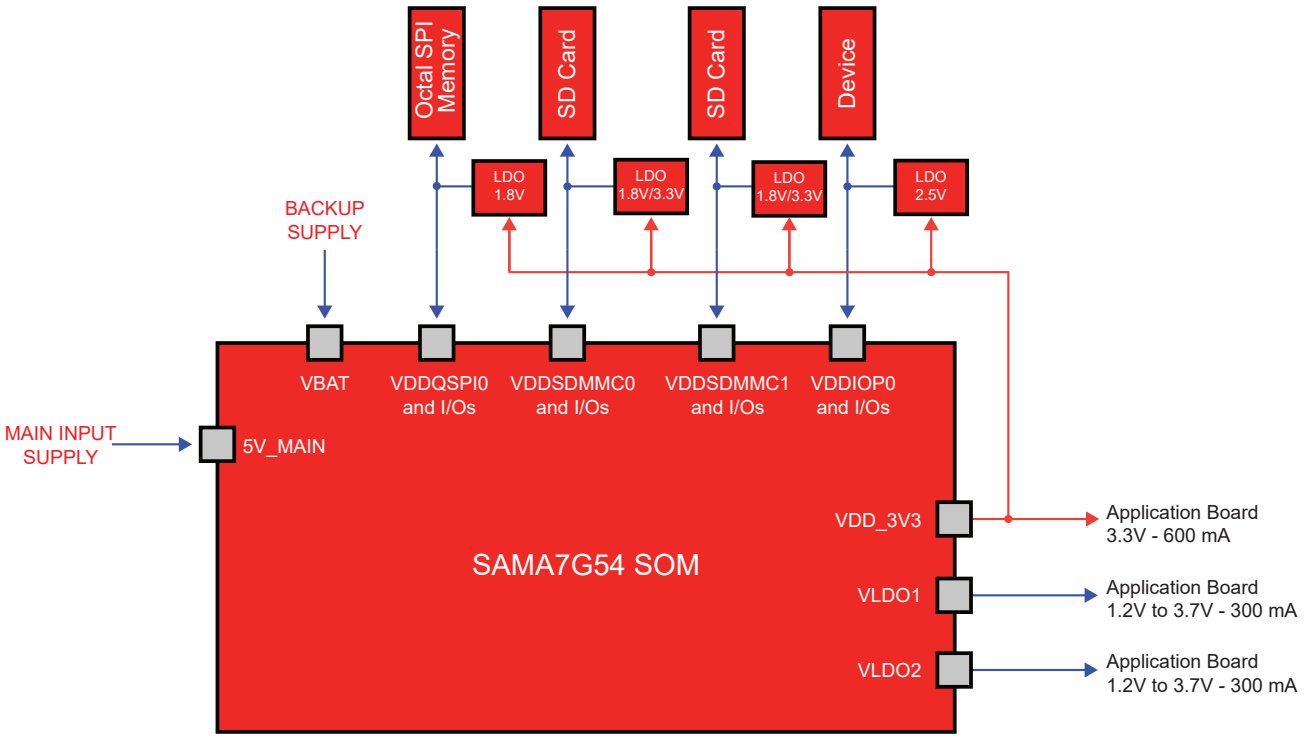
Figure 7-5. SAMA7G54 SOM Series Multiple Supplies Connection Example



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8. MPU and Memory Subsystem

8.1 SAMA7G5 Series System-in-Package (SiP)

The Microchip SAMA7G54 System-On-Module Series embeds the SAMA7G5 Series SiP, which integrates the Arm Cortex-A7 CPU-based SAMA7G54 MPU with a 1-Gbit or 2-Gbit DDR3L SDRAM (depending on the System-On-Module configuration) in a single package.

By combining the SAMA7G54 with DDR3L in a single package, PCB routing complexity, area and number of layers are reduced. This makes board design easier and more robust by facilitating design for EMI, ESD and signal integrity.

For more information, refer to the SAMA7G5 Series SiP data sheet (see Reference Documents).

The SAMA7G5 Series SiP is available in a 18x21 mm 427-ball SBS TFBGA package.

The Microchip SAMA7G54 System-On-Module provides global system Reset (NRST, NRST_OUT) and Shutdown (SHDN) pins to the application board.

Notes:

- The NRST signal is an input/output pin generated by the internal Power Management Unit (MCP16502) respecting the microprocessor power sequence timing. It is used to reset the internal microprocessor and the rest of the customer application board. It can then be forced externally in case of a system crash.
- The NRST_OUT signal is an output pin generated by the SAMA7G54 reset controller. On the customer application, it can be used to reset specific interfaces such as Ethernet PHY, Wireless Solution or another device.
- The SHDN pin is an output pin managed by the application software. In an application case, the pin can switch on/off the 5V_MAIN external main supply.

8.2 MPU Clocks

Two clock sources are necessary for the module microprocessor:

- A 24-MHz main oscillator to generate the SAMA7G54 MPU main clock
- A small size 32.768-kHz oscillator to generate the slow clock oscillator input and feed the SAMA7G54 MPU embedded RTC

The 24-MHz clock is generated by a Microchip Ultra-Low Power MEMS oscillator DSC6001HI1B-024.0000T. The 24-MHz clock is delivered to the MPU with an ultra-low power consumption of about 1.3 mA in Active mode.

For more information, refer to the DSC60XXB MEMS data sheet (see Reference Documents).

The 24-MHz clock can be enabled/disabled as required by the application through the 24M_EN signal available on pin 98.

Three configurations are available:

- 24M_EN pin connected to VDD (VDD_3V3). The clock is enabled.
- 24M_EN connected to GND. The clock is stopped.
- 24M_EN connected to a GPIO. The clock is dynamically controlled by software.

The 32.768-kHz clock is generated by a small size crystal. An accurate 32.768-kHz clock is delivered to the SAMA7G54 for its embedded RTC.

8.3 NAND Flash Memory

The Microchip SAMA7G54 System-On-Module embeds an SLC NAND Flash memory supported through its External Bus Interface controller with different memory sizes depending on the part number.

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The System-On-Module implements one of the following references, depending on the memory space. All are available in a VFBGA-63 package.

- 2-Gbit memory size[(1)]
  - Macronix MX30LF2G28AD-XKI
  - Micron MT29F2G08ABAGAH4-IT:G
- 4-Gbit memory size[(1)]
  - Macronix MX30LF4G28AD-XKI
  - Micron MT29F4G08ABAFAH4-IT:F

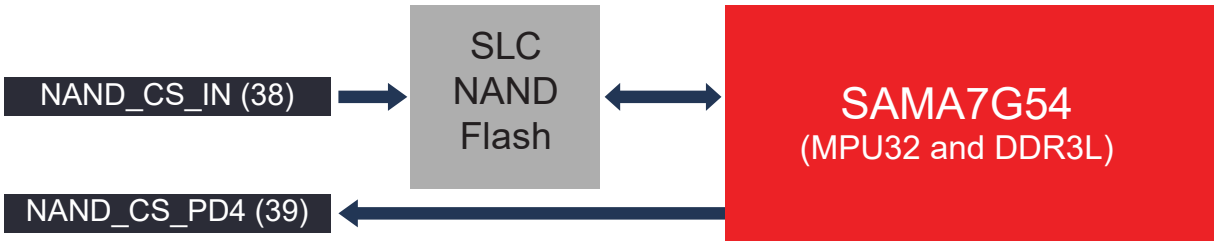
Note:

1. Either one of the above references can be mounted on the Microchip SAMA7G54 System-On-Module.

The software must be adapted to recognize the relevant NAND Flash manufacturer. Microchip Linux distribution supports all references. For details on how to build Linux software, refer to www.linux4microchip.com/.

NAND_CS_IN (pin 38) is accessible externally and can be uncoupled from NAND_CS_PD4 (pin 39) so that the boot can be unselected from the NAND Flash memory during debug phases.

Figure 8-1. NAND Flash Memory Block Diagram



8.4 QSPI NOR Memory

The Microchip SAMA7G54 System-On-Module embeds the SST26VF064BEUIT-104I/MF, a 64 Mbit Serial Quad I/O Flash memory.

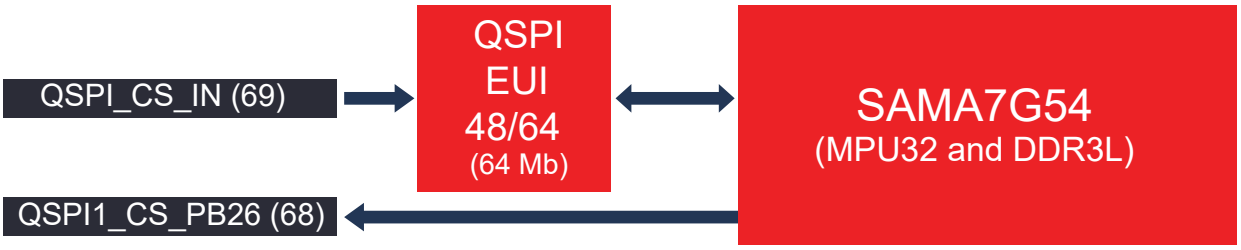
The SST26VF064BEUI SQI features a 6-wire, 4-bit I/O interface that allows for low-power, high performance operation in a low pin-count package.

The SST26VF064BEUI also embeds EUI-48 and EUI-64 MAC addresses.

The SST26VF064BEUI is available in an 8-lead 6×5 mm WDFN package.

For more information, refer to the SST26VF064BEUI data sheet (see Reference Documents).

Figure 8-2. QSPI Memory Block Diagram



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Note: For debug purposes, the embedded QSPI Chip Enable can be uncoupled from the microprocessor. QSPI1_CS_IN (pin 69) is accessible externally and can be uncoupled from QSPI1_CS_PB26 (pin 68) so that the boot can be unselected from the QSPI Flash memory during debug phases.

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9. External Interfacing

9.1 Interfacing with FLEXCOM Interfaces

FLEXCOM offers several serial communication protocols managed by the Two-Wire Interface (TWI), Universal Synchronous Asynchronous Receiver Transceiver (USART) and Serial Peripheral Interface (SPI) submodules.

9.1.1 Interfacing in I²C/TWI Mode

The SAMA7G54 SOM Series offers 12 FLEXCOM interfaces configurable in TWI mode and one TWI interface.

The TWI can interconnect with external components on a unique two-wire bus made up of one clock line and one data line with speeds of up to 400 Kbits/s in Fast mode and up to 3.4 Mbits/s in High-Speed Client mode, based on a byte-oriented transfer format.

It can be used with any TWI bus serial EEPROM and I²C-compatible devices, such as a Real-Time Clock (RTC), a dot matrix/graphic LCD controller or a temperature sensor. The TWI is programmable as a host or a client with sequential or single-byte access. Multiple host capability is supported.

Table 9-1. I²C/TWI Interface FLEXCOM0 Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function	Comment
FLEXCOM0	1	125	PA0	Data line (TWD/SDA)	External pull-up needed if the FLEXCOM interface is used as an I²C/TWI interface
		130	PA1	Clock line (TWCK/SCL)	
FLEXCOM0	4	46	PE3	Data line (TWD/SDA)	
		49	PE4	Clock line (TWCK/SCL)	

Table 9-2. I²C/TWI Interface FLEXCOM1 Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function	Comment
FLEXCOM1	1	127	PA5	Data line (TWD/SDA)	External pull-up needed if the FLEXCOM interface is used as an I²C/TWI interface
		124	PA6	Clock line (TWCK/SCL)	
FLEXCOM1	2	20	PD12	Data line (TWD/SDA)	
		21	PD13	Clock line (TWCK/SCL)	
FLEXCOM1	3	126	PA2	Data line (TWD/SDA)	
		128	PA3	Clock line (TWCK/SCL)	
FLEXCOM1	4	87	PC9	Data line (TWD/SDA)	
		88	PC10	Clock line (TWCK/SCL)	

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Table 9-3. I²C/TWI Interface FLEXCOM2 Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function	Comment
FLEXCOM2	1	123	PA7	Data line (TWD/SDA)	External pull-up needed if the FLEXCOM interface is used as an I²C/TWI interface
		122	PA8	Clock line (TWCK/SCL)	
FLEXCOM2	2	23	PD17	Data line (TWD/SDA)	
		111	PD18	Clock line (TWCK/SCL)	
FLEXCOM2	3	121	PA4	Data line (TWD/SDA)	
		127	PA5	Clock line (TWCK/SCL)	
FLEXCOM2	4	89	PC11	Data line (TWD/SDA)	
		90	PC12	Clock line (TWCK/SCL)	
FLEXCOM2	5	22	PD14	Data line (TWD/SDA)	
		19	PD15	Clock line (TWCK/SCL)	

Table 9-4. I²C/TWI Interface FLEXCOM3 Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function	Comment
FLEXCOM3	1	180	PA15	Data line (TWD/SDA)	External pull-up needed if the FLEXCOM interface is used as an I²C/TWI interface
		179	PA16	Clock line (TWCK/SCL)	
FLEXCOM3	2	55	PC0	Data line (TWD/SDA)	
		56	PC1	Clock line (TWCK/SCL)	
FLEXCOM3	3	124	PA6	Data line (TWD/SDA)	
		123	PA7	Clock line (TWCK/SCL)	
FLEXCOM3	4	91	PC13	Data line (TWD/SDA)	
		92	PC14	Clock line (TWCK/SCL)	
FLEXCOM3	5	24	PD16	Data line (TWD/SDA)	
		23	PD17	Clock line (TWCK/SCL)	

Table 9-5. I²C/TWI Interface FLEXCOM4 Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function	Comment
FLEXCOM4	1	175	PA20	Data line (TWD/SDA)	External pull-up needed if the FLEXCOM interface is used as an I²C/TWI interface
		178	PA21	Clock line (TWCK/SCL)	
FLEXCOM4	2	57	PC2	Data line (TWD/SDA)	
		59	PC3	Clock line (TWCK/SCL)	
FLEXCOM4	3	122	PA8	Data line (TWD/SDA)	
		119	PA9	Clock line (TWCK/SCL)	
FLEXCOM4	4	93	PC15	Data line (TWD/SDA)	
		99	PC16	Clock line (TWCK/SCL)	
FLEXCOM4	5	111	PD18	Data line (TWD/SDA)	
		110	PD19	Clock line (TWCK/SCL)	

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Table 9-6. I²C/TWI Interface FLEXCOM5 Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function	Comment
FLEXCOM5	1	187	PA28	Data line (TWD/SDA)	External pull-up needed if the FLEXCOM interface is used as an I²C/TWI interface
		188	PA29	Clock line (TWCK/SCL)	
FLEXCOM5	2	30	PD25	Data line (TWD/SDA)	
		36	PD26	Clock line (TWCK/SCL)	
FLEXCOM5	3	120	PA10	Data line (TWD/SDA)	
		129	PA11	Clock line (TWCK/SCL)	
FLEXCOM5	4	100	PC17	Data line (TWD/SDA)	
		101	PC18	Clock line (TWCK/SCL)	
FLEXCOM5	5	29	PD20	Data line (TWD/SDA)	
		26	PD21	Clock line (TWCK/SCL)	

Table 9-7. I²C/TWI Interface FLEXCOM6 Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function	Comment
FLEXCOM6	1	6	PB2	Data line (TWD/SDA)	External pull-up needed if the FLEXCOM interface is used as an I²C/TWI interface
		5	PB1	Clock line (TWCK/SCL)	
FLEXCOM6	2	31	PD30	Data line (TWD/SDA)	
		37	PD31	Clock line (TWCK/SCL)	
FLEXCOM6	3	131	PA12	Data line (TWD/SDA)	
		132	PA13	Clock line (TWCK/SCL)	
FLEXCOM6	4	102	PC19	Data line (TWD/SDA)	
		103	PC20	Clock line (TWCK/SCL)	

Table 9-8. I²C/TWI Interface FLEXCOM7 Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function	Comment
FLEXCOM7	2	85	PC7	Data line (TWD/SDA)	External pull-up needed if the FLEXCOM interface is used as an I²C/TWI interface
		86	PC8	Clock line (TWCK/SCL)	
FLEXCOM7	3	181	PA25	Data line (TWD/SDA)	
		185	PA26	Clock line (TWCK/SCL)	
FLEXCOM7	4	52	PB28	Data line (TWD/SDA)	
		53	PB29	Clock line (TWCK/SCL)	

Table 9-9. I²C/TWI Interface FLEXCOM8 Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function	Comment
FLEXCOM8	1	144	PB8	Data line (TWD/SDA)	External pull-up needed if the FLEXCOM interface is used as an I²C/TWI interface
		156	PB9	Clock line (TWCK/SCL)	
FLEXCOM8	2	92	PC14	Data line (TWD/SDA)	
		91	PC13	Clock line (TWCK/SCL)	
FLEXCOM8	3	186	PA27	Data line (TWD/SDA)	
		187	PA28	Clock line (TWCK/SCL)	
FLEXCOM8	4	58	PB30	Data line (TWD/SDA)	
		54	PB31	Clock line (TWCK/SCL)	

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Table 9-10. I²C/TWI Interface FLEXCOM9 Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function	Comment
FLEXCOM9	1	151	PB13	Data line (TWD/SDA)	External pull-up needed if the FLEXCOM interface is used as an I²C/TWI interface
		155	PB14	Clock line (TWCK/SCL)	
FLEXCOM9	2	101	PC18	Data line (TWD/SDA)	
		102	PC19	Clock line (TWCK/SCL)	
FLEXCOM9	3	188	PA29	Data line (TWD/SDA)	
		3	PA30	Clock line (TWCK/SCL)	
FLEXCOM9	4	55	PC0	Data line (TWD/SDA)	
		56	PC1	Clock line (TWCK/SCL)	

Table 9-11. I²C/TWI Interface FLEXCOM10 Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function	Comment
FLEXCOM10	2	17	PC30	Data line (TWD/SDA)	No external pull-up needed. Already integrated in the SAMA7G54 SOM Series
		16	PC31	Clock line (TWCK/SCL)	

Table 9-12. I²C/TWI Interface FLEXCOM11 Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function	Comment
FLEXCOM11	1	139	PB3	Data line (TWD/SDA)	External pull-up needed if the FLEXCOM interface is used as an I²C/TWI interface
		140	PB4	Clock line (TWCK/SCL)	
FLEXCOM11	2	106	PD0	Data line (TWD/SDA)	
		107	PD1	Clock line (TWCK/SCL)	
FLEXCOM11	3	5	PB1	Data line (TWD/SDA)	
		6	PB2	Clock line (TWCK/SCL)	
FLEXCOM11	4	60	PC4	Data line (TWD/SDA)	
		61	PC5	Clock line (TWCK/SCL)	

9.1.2 Interfacing in USART Mode

The SAMA7G54 SOM Series offers 11 FLEXCOM interfaces configured in USART mode.

The USART provides one full-duplex universal synchronous asynchronous serial link. The data frame format is widely programmable (data length, parity, number of stop bits) to support a high number of standards. The receiver implements parity error, framing error and overrun error detection. The receiver timeout enables handling variable-length frames and the transmitter timeguard facilitates communications with slow remote devices. Multidrop communications are also supported through address bit handling in reception and transmission.

The USART features three test modes: Remote Loopback, Local Loopback and Automatic Echo.

The USART supports specific operating modes providing interfaces on RS485, LIN, with ISO7816 T = 0 or T = 1 smart card slots, and infrared transceivers. The hardware handshaking feature enables an out-of-band flow control by automatic management of the pins RTS and CTS.

The USART supports the connection to the DMA Controller, which enables data transfers to the transmitter and from the receiver. The DMAC provides chained buffer management without any intervention of the processor.

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Table 9-13. FLEXCOM0 Interface Configuration in USART Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM0	1	125	PA0	Transmit Data (TXD)
		130	PA1	Receive Data (RXD)
		128	PA3	Clear To Send (CTS)
		121	PA4	Request To Send (RTS)

Table 9-14. FLEXCOM1 Interface Configuration in USART Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM1	1	127	PA5	Transmit Data (TXD)
		124	PA6	Receive Data (RXD)
		131	PA12	Clear To Send (CTS)
		133	PA14	Request To Send (RTS)
FLEXCOM1	2	20	PD12	Transmit Data (TXD)
		21	PD13	Receive Data (RXD)
		19	PD15	Clear To Send (CTS)
		24	PD16	Request To Send (RTS)
FLEXCOM1	3	126	PA2	Transmit Data (TXD)
		128	PA3	Receive Data (RXD)
		19	PD15	Clear To Send (CTS)
		24	PD16	Request To Send (RTS)
FLEXCOM1	4	87	PC9	Transmit Data (TXD)
		88	PC10	Receive Data (RXD)
		19	PD15	Clear To Send (CTS)
		24	PD16	Request To Send (RTS)

Table 9-15. FLEXCOM2 Interface Configuration in USART Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM2	1	123	PA7	Transmit Data (TXD)
		122	PA8	Receive Data (RXD)
		120	PA10	Clear To Send (CTS)
		129	PA11	Request To Send (RTS)
FLEXCOM2	2	23	PD17	Transmit Data (TXD)
		111	PD18	Receive Data (RXD)
		29	PD20	Clear To Send (CTS)
		26	PD21	Request To Send (RTS)
FLEXCOM2	3	121	PA4	Transmit Data (TXD)
		127	PA5	Receive Data (RXD)
		29	PD20	Clear To Send (CTS)
		26	PD21	Request To Send (RTS)
FLEXCOM2	4	89	PC11	Transmit Data (TXD)
		90	PC12	Receive Data (RXD)
		29	PD20	Clear To Send (CTS)
		26	PD21	Request To Send (RTS)

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Table 9-16. FLEXCOM3 Interface Configuration in USART Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM3	1	180	PA15	Transmit Data (TXD)
		179	PA16	Receive Data (RXD)
		177	PA18	Clear To Send (CTS)
		182	PA19	Request To Send (RTS)
FLEXCOM3	2	55	PC0	Transmit Data (TXD)
		56	PC1	Receive Data (RXD)
		58	PB30	Clear To Send (CTS)
		54	PB31	Request To Send (RTS)
FLEXCOM3	3	124	PA6	Transmit Data (TXD)
		123	PA7	Receive Data (RXD)
		58	PB30	Clear To Send (CTS)
		54	PB31	Request To Send (RTS)
FLEXCOM3	4	91	PC13	Transmit Data (TXD)
		92	PC14	Receive Data (RXD)
		58	PB30	Clear To Send (CTS)
		54	PB31	Request To Send (RTS)
FLEXCOM3	5	24	PD16	Transmit Data (TXD)
		23	PD17	Receive Data (RXD)
		58	PB30	Clear To Send (CTS)
		54	PB31	Request To Send (RTS)

Table 9-17. FLEXCOM4 Interface Configuration in USART Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM4	1	175	PA20	Transmit Data (TXD)
		178	PA21	Receive Data (RXD)
		184	PA23	Clear To Send (CTS)
		183	PA24	Request To Send (RTS)
FLEXCOM4	2	57	PC2	Transmit Data (TXD)
		59	PC3	Receive Data (RXD)
		61	PC5	Clear To Send (CTS)
		62	PC6	Request To Send (RTS)
FLEXCOM4	3	122	PA8	Transmit Data (TXD)
		119	PA9	Receive Data (RXD)
		61	PC5	Clear To Send (CTS)
		62	PC6	Request To Send (RTS)
FLEXCOM4	4	93	PC15	Transmit Data (TXD)
		99	PC16	Receive Data (RXD)
		61	PC5	Clear To Send (CTS)
		62	PC6	Request To Send (RTS)
FLEXCOM4	5	111	PD18	Transmit Data (TXD)
		110	PD19	Receive Data (RXD)
		61	PC5	Clear To Send (CTS)
		62	PC6	Request To Send (RTS)

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Table 9-18. FLEXCOM5 Interface Configuration in USART Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM5	1	187	PA28	Transmit Data (TXD)
		188	PA29	Receive Data (RXD)
		186	PA27	Clear To Send (CTS)
		181	PA25	Request To Send (RTS)
FLEXCOM5	2	30	PD25	Transmit Data (TXD)
		36	PD26	Receive Data (RXD)
		35	PD28	Clear To Send (CTS)
		33	PD29	Request To Send (RTS)
FLEXCOM5	3	120	PA10	Transmit Data (TXD)
		129	PA11	Receive Data (RXD)
		35	PD28	Clear To Send (CTS)
		33	PD29	Request To Send (RTS)
FLEXCOM5	4	100	PC17	Transmit Data (TXD)
		101	PC18	Receive Data (RXD)
		35	PD28	Clear To Send (CTS)
		33	PD29	Request To Send (RTS)
FLEXCOM5	5	29	PD20	Transmit Data (TXD)
		26	PD21	Receive Data (RXD)
		35	PD28	Clear To Send (CTS)
		33	PD29	Request To Send (RTS)

Table 9-19. FLEXCOM6 Interface Configuration in USART Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM6	1	6	PB2	Transmit Data (TXD)
		5	PB1	Receive Data (RXD)
		7	PB0	Clear To Send (CTS)
		3	PA30	Request To Send (RTS)

Table 9-20. FLEXCOM7 Interface Configuration in USART Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM7	2	85	PC7	Transmit Data (TXD)
		86	PC8	Receive Data (RXD)
		88	PC10	Clear To Send (CTS)
		89	PC11	Request To Send (RTS)
FLEXCOM7	3	181	PA25	Transmit Data (TXD)
		185	PA26	Receive Data (RXD)
		88	PC10	Clear To Send (CTS)
		89	PC11	Request To Send (RTS)
FLEXCOM7	4	52	PB28	Transmit Data (TXD)
		53	PB29	Receive Data (RXD)
		88	PC10	Clear To Send (CTS)
		89	PC11	Request To Send (RTS)

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Table 9-21. FLEXCOM8 Interface Configuration in USART Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM8	1	144	PB8	Transmit Data (TXD)
		156	PB9	Receive Data (RXD)
		158	PB11	Clear To Send (CTS)
		157	PB12	Request To Send (RTS)
FLEXCOM8	2	92	PC14	Transmit Data (TXD)
		91	PC13	Receive Data (RXD)
		93	PC15	Clear To Send (CTS)
		99	PC16	Request To Send (RTS)
FLEXCOM8	3	186	PA27	Transmit Data (TXD)
		187	PA28	Receive Data (RXD)
		93	PC15	Clear To Send (CTS)
		99	PC16	Request To Send (RTS)
FLEXCOM8	4	58	PB30	Transmit Data (TXD)
		54	PB31	Receive Data (RXD)
		93	PC15	Clear To Send (CTS)
		99	PC16	Request To Send (RTS)

Table 9-22. FLEXCOM9 Interface Configuration in USART Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM9	1	151	PB13	Transmit Data (TXD)
		155	PB14	Receive Data (RXD)
		152	PB16	Clear To Send (CTS)
		159	PB17	Request To Send (RTS)

Table 9-23. FLEXCOM11 Interface Configuration in USART Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM11	1	139	PB3	Transmit Data (TXD)
		140	PB4	Receive Data (RXD)
		142	PB6	Clear To Send (CTS)
		143	PB7	Request To Send (RTS)
FLEXCOM11	3	5	PB1	Transmit Data (TXD)
		6	PB2	Receive Data (RXD)
		142	PB6	Clear To Send (CTS)
		143	PB7	Request To Send (RTS)
FLEXCOM11	4	60	PC4	Transmit Data (TXD)
		61	PC5	Receive Data (RXD)
		142	PB6	Clear To Send (CTS)
		143	PB7	Request To Send (RTS)

9.1.3 Interfacing in SPI Mode

The SAMA7G54 SOM Series offers 11 FLEXCOM interfaces configured in SPI mode.

The SPI circuit is a synchronous serial data link that provides communication with external devices in Host or Client mode. It also enables communication between processors if an external processor is connected to the system.

The Serial Peripheral Interface is essentially a shift register that serially transmits data bits to other SPI devices. During a data transfer, one SPI system acts as the “host,” which controls the data flow,

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while the other devices act as "clients," which have data shifted in and out by the host. Different CPUs can take turns being hosts (multiple host protocol, as opposed to single host protocol, where one CPU is always the host while all others are always clients). One host can simultaneously shift data into multiple clients. However, only one client can drive its output to write data back to the host at any given time.

A client device is selected when the host asserts its NSS signal. When multiple client devices are available, the host generates a separate client select signal (NPCS) for each.

The SPI system consists of two data lines and two control lines:

- Host Out Client In (MOSI)—This data line supplies the output data from the host shifted into the input(s) of the client(s).
- Host In Client Out (MISO)—This data line supplies the output data from a client to the input of the host. There may be no more than one client transmitting data during any particular transfer.
- Serial Clock (SPCK)—This control line is driven by the host and regulates the flow of the data bits. The host can transmit data at a variety of baud rates; there is one SPCK pulse for each bit transmitted.
- Client Select (NSS)—This control line allows clients to be turned on and off by hardware.

Table 9-24. FLEXCOM0 Interface Configurations in SPI Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM0	1	125	PA0	SPI Host Output Client Input (MOSI)
		130	PA1	SPI Host Input Client Output (MISO)
		126	PA2	SPI Serial Clock (SPCK)
		128	PA3	SPI Chip Select 0 (NPCS0)
		121	PA4	SPI Chip Select 1 (NPCS1)
FLEXCOM0	4	46	PE3	SPI Host Output Client Input (MOSI)
		49	PE4	SPI Host Input Client Output (MISO)
		48	PE5	SPI Serial Clock (SPCK)
		50	PE6	SPI Chip Select 0 (NPCS0)

Table 9-25. FLEXCOM1 Interface Configurations in SPI Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM1	1	127	PA5	SPI Host Output Client Input (MOSI)
		124	PA6	SPI Host Input Client Output (MISO)
		132	PA13	SPI Serial Clock (SPCK)
		131	PA12	SPI Chip Select 0 (NPCS0)
		133	PA14	SPI Chip Select 1 (NPCS1)
FLEXCOM1	2	20	PD12	SPI Host Output Client Input (MOSI)
		21	PD13	SPI Host Input Client Output (MISO)
		22	PD14	SPI Serial Clock (SPCK)
		19	PD15	SPI Chip Select 0 (NPCS0)
		24	PD16	SPI Chip Select 1 (NPCS1)
FLEXCOM1	3	126	PA2	SPI Host Output Client Input (MOSI)
		128	PA3	SPI Host Input Client Output (MISO)
		22	PD14	SPI Serial Clock (SPCK)
		19	PD15	SPI Chip Select 0 (NPCS0)
		24	PD16	SPI Chip Select 1 (NPCS1)

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.....continued

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM1	4	87	PC9	SPI Host Output Client Input (MOSI)
		88	PC10	SPI Host Input Client Output (MISO)
		22	PD14	SPI Serial Clock (SPCK)
		19	PD15	SPI Chip Select 0 (NPCS0)
		24	PD16	SPI Chip Select 1 (NPCS1)

Table 9-26. FLEXCOM2 Interface Configurations in SPI Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM2	1	123	PA7	SPI Host Output Client Input (MOSI)
		122	PA8	SPI Host Input Client Output (MISO)
		119	PA9	SPI Serial Clock (SPCK)
		120	PA10	SPI Chip Select 0 (NPCS0)
		129	PA11	SPI Chip Select 1 (NPCS1)
FLEXCOM2	2	23	PD17	SPI Host Output Client Input (MOSI)
		111	PD18	SPI Host Input Client Output (MISO)
		110	PD19	SPI Serial Clock (SPCK)
		29	PD20	SPI Chip Select 0 (NPCS0)
		26	PD21	SPI Chip Select 1 (NPCS1)
FLEXCOM2	3	121	PA4	SPI Host Output Client Input (MOSI)
		127	PA5	SPI Host Input Client Output (MISO)
		110	PD19	SPI Serial Clock (SPCK)
		29	PD20	SPI Chip Select 0 (NPCS0)
		26	PD21	SPI Chip Select 1 (NPCS1)
FLEXCOM2	4	89	PC11	SPI Host Output Client Input (MOSI)
		90	PC12	SPI Host Input Client Output (MISO)
		110	PD19	SPI Serial Clock (SPCK)
		29	PD20	SPI Chip Select 0 (NPCS0)
		26	PD21	SPI Chip Select 1 (NPCS1)

Table 9-27. FLEXCOM3 Interface Configurations in SPI Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM3	1	180	PA15	SPI Host Output Client Input (MOSI)
		179	PA16	SPI Host Input Client Output (MISO)
		178	PA17	SPI Serial Clock (SPCK)
		177	PA18	SPI Chip Select 0 (NPCS0)
		182	PA19	SPI Chip Select 1 (NPCS1)
FLEXCOM3	2	55	PC0	SPI Host Output Client Input (MOSI)
		56	PC1	SPI Host Input Client Output (MISO)
		53	PB29	SPI Serial Clock (SPCK)
		58	PB30	SPI Chip Select 0 (NPCS0)
		54	PB31	SPI Chip Select 1 (NPCS1)
FLEXCOM3	3	124	PA6	SPI Host Output Client Input (MOSI)
		123	PA7	SPI Host Input Client Output (MISO)
		53	PB29	SPI Serial Clock (SPCK)
		58	PB30	SPI Chip Select 0 (NPCS0)
		54	PB31	SPI Chip Select 1 (NPCS1)

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Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM3	4	91	PC13	SPI Host Output Client Input (MOSI)
		92	PC14	SPI Host Input Client Output (MISO)
		53	PB29	SPI Serial Clock (SPCK)
		58	PB30	SPI Chip Select 0 (NPCS0)
		54	PB31	SPI Chip Select 1 (NPCS1)
FLEXCOM3	5	24	PD16	SPI Host Output Client Input (MOSI)
		23	PD17	SPI Host Input Client Output (MISO)
		53	PB29	SPI Serial Clock (SPCK)
		58	PB30	SPI Chip Select 0 (NPCS0)
		54	PB31	SPI Chip Select 1 (NPCS1)

Table 9-28. FLEXCOM4 Interface Configurations in SPI Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM4	1	175	PA20	SPI Host Output Client Input (MOSI)
		178	PA21	SPI Host Input Client Output (MISO)
		176	PA22	SPI Serial Clock (SPCK)
		184	PA23	SPI Chip Select 0 (NPCS0)
		183	PA24	SPI Chip Select 1 (NPCS1)
FLEXCOM4	2	57	PC2	SPI Host Output Client Input (MOSI)
		59	PC3	SPI Host Input Client Output (MISO)
		60	PC4	SPI Serial Clock (SPCK)
		61	PC5	SPI Chip Select 0 (NPCS0)
		62	PC6	SPI Chip Select 1 (NPCS1)
FLEXCOM4	3	122	PA8	SPI Host Output Client Input (MOSI)
		119	PA9	SPI Host Input Client Output (MISO)
		60	PC4	SPI Serial Clock (SPCK)
		61	PC5	SPI Chip Select 0 (NPCS0)
		62	PC6	SPI Chip Select 1 (NPCS1)
FLEXCOM4	4	93	PC15	SPI Host Output Client Input (MOSI)
		99	PC16	SPI Host Input Client Output (MISO)
		60	PC4	SPI Serial Clock (SPCK)
		61	PC5	SPI Chip Select 0 (NPCS0)
		62	PC6	SPI Chip Select 1 (NPCS1)
FLEXCOM4	5	111	PD18	SPI Host Output Client Input (MOSI)
		110	PD19	SPI Host Input Client Output (MISO)
		60	PC4	SPI Serial Clock (SPCK)
		61	PC5	SPI Chip Select 0 (NPCS0)
		62	PC6	SPI Chip Select 1 (NPCS1)

Table 9-29. FLEXCOM5 Interface Configurations in SPI Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM5	1	187	PA28	SPI Host Output Client Input (MOSI)
		188	PA29	SPI Host Input Client Output (MISO)
		185	PA26	SPI Serial Clock (SPCK)
		186	PA27	SPI Chip Select 0 (NPCS0)
		181	PA25	SPI Chip Select 1 (NPCS1)

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Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM5	2	30	PD25	SPI Host Output Client Input (MOSI)
		36	PD26	SPI Host Input Client Output (MISO)
		34	PD27	SPI Serial Clock (SPCK)
		35	PD28	SPI Chip Select 0 (NPCS0)
		33	PD29	SPI Chip Select 1 (NPCS1)
FLEXCOM5	3	120	PA10	SPI Host Output Client Input (MOSI)
		129	PA11	SPI Host Input Client Output (MISO)
		34	PD27	SPI Serial Clock (SPCK)
		35	PD28	SPI Chip Select 0 (NPCS0)
		33	PD29	SPI Chip Select 1 (NPCS1)
FLEXCOM5	4	100	PC17	SPI Host Output Client Input (MOSI)
		101	PC18	SPI Host Input Client Output (MISO)
		34	PD27	SPI Serial Clock (SPCK)
		35	PD28	SPI Chip Select 0 (NPCS0)
		33	PD29	SPI Chip Select 1 (NPCS1)
FLEXCOM5	5	29	PD20	SPI Host Output Client Input (MOSI)
		26	PD21	SPI Host Input Client Output (MISO)
		34	PD27	SPI Serial Clock (SPCK)
		35	PD28	SPI Chip Select 0 (NPCS0)
		33	PD29	SPI Chip Select 1 (NPCS1)

Table 9-30. FLEXCOM6 Interface Configurations in SPI Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM6	1	6	PB2	SPI Host Output Client Input (MOSI)
		5	PB1	SPI Host Input Client Output (MISO)
		4	PA31	SPI Serial Clock (SPCK)
		7	PB0	SPI Chip Select 0 (NPCS0)
		3	PA30	SPI Chip Select 1 (NPCS1)

Table 9-31. FLEXCOM7 Interface Configurations in SPI Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM7	2	85	PC7	SPI Host Output Client Input (MOSI)
		86	PC8	SPI Host Input Client Output (MISO)
		87	PC9	SPI Serial Clock (SPCK)
		88	PC10	SPI Chip Select 0 (NPCS0)
		89	PC11	SPI Chip Select 1 (NPCS1)
FLEXCOM7	3	181	PA25	SPI Host Output Client Input (MOSI)
		185	PA26	SPI Host Input Client Output (MISO)
		87	PC9	SPI Serial Clock (SPCK)
		88	PC10	SPI Chip Select 0 (NPCS0)
		89	PC11	SPI Chip Select 1 (NPCS1)
FLEXCOM7	4	52	PB28	SPI Host Output Client Input (MOSI)
		53	PB29	SPI Host Input Client Output (MISO)
		87	PC9	SPI Serial Clock (SPCK)
		88	PC10	SPI Chip Select 0 (NPCS0)
		89	PC11	SPI Chip Select 1 (NPCS1)

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Table 9-32. FLEXCOM8 Interface Configurations in SPI Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM8	1	144	PB8	SPI Host Output Client Input (MOSI)
		156	PB9	SPI Host Input Client Output (MISO)
		148	PB10	SPI Serial Clock (SPCK)
		158	PB11	SPI Chip Select 0 (NPCS0)
		157	PB12	SPI Chip Select 1 (NPCS1)
FLEXCOM8	2	92	PC14	SPI Host Output Client Input (MOSI)
		91	PC13	SPI Host Input Client Output (MISO)
		90	PC12	SPI Serial Clock (SPCK)
		93	PC15	SPI Chip Select 0 (NPCS0)
		99	PC16	SPI Chip Select 1 (NPCS1)
FLEXCOM8	3	186	PA27	SPI Host Output Client Input (MOSI)
		187	PA28	SPI Host Input Client Output (MISO)
		90	PC12	SPI Serial Clock (SPCK)
		93	PC15	SPI Chip Select 0 (NPCS0)
		99	PC16	SPI Chip Select 1 (NPCS1)
FLEXCOM8	4	58	PB30	SPI Host Output Client Input (MOSI)
		54	PB31	SPI Host Input Client Output (MISO)
		90	PC12	SPI Serial Clock (SPCK)
		93	PC15	SPI Chip Select 0 (NPCS0)
		99	PC16	SPI Chip Select 1 (NPCS1)

Table 9-33. FLEXCOM9 Interface Configurations in SPI Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM9	1	151	PB13	SPI Host Output Client Input (MOSI)
		155	PB14	SPI Host Input Client Output (MISO)
		154	PB15	SPI Serial Clock (SPCK)
		152	PB16	SPI Chip Select 0 (NPCS0)
		159	PB17	SPI Chip Select 1 (NPCS1)

Table 9-34. FLEXCOM11 Interface Configurations in SPI Mode

Interface Instance	IO Set	Pin No.	Pin Name	Function
FLEXCOM11	1	139	PB3	SPI Host Output Client Input (MOSI)
		140	PB4	SPI Host Input Client Output (MISO)
		141	PB5	SPI Serial Clock (SPCK)
		142	PB6	SPI Chip Select 0 (NPCS0)
		143	PB7	SPI Chip Select 1 (NPCS1)
FLEXCOM11	3	5	PB1	SPI Host Output Client Input (MOSI)
		6	PB2	SPI Host Input Client Output (MISO)
		141	PB5	SPI Serial Clock (SPCK)
		142	PB6	SPI Chip Select 0 (NPCS0)
		143	PB7	SPI Chip Select 1 (NPCS1)
FLEXCOM11	4	60	PC4	SPI Host Output Client Input (MOSI)
		61	PC5	SPI Host Input Client Output (MISO)
		141	PB5	SPI Serial Clock (SPCK)
		142	PB6	SPI Chip Select 0 (NPCS0)
		143	PB7	SPI Chip Select 1 (NPCS1)

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9.2 Interfacing with CAN

The SAMA7G54 SOM Series offers six Controller Area Network (MCAN) interfaces.

The MCAN performs communication according to ISO 11898-1:2015 and to Bosch CAN FD specification. Additional transceiver hardware is required for connection to the physical layer.

All functions concerning the handling of messages are implemented by the Rx Handler and the Tx Handler. The Rx Handler manages message acceptance filtering and transfer of received messages from the CAN core to the Message RAM and provides received message status information. The Tx Handler is responsible for the transfer of transmit messages from the Message RAM to the CAN core, as well as providing transmit status information.

Acceptance filtering is implemented by a combination of up to 128 filter elements, where each element can be configured as a range, as a bit mask, or as a dedicated ID filter.

For more information about the Controller Area Network features, refer to the SAMA7G5 Series SiP data sheet (see Reference Documents).

Table 9-35. CAN Interface Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function
MCAN0	1	119	PA9	CAN Transmit Line (CANTX)
		120	PA10	CAN Receive Line (CANRX)
MCAN0	2	20	PD12	CAN Transmit Line (CANTX)
		21	PD13	CAN Receive Line (CANRX)
MCAN1	1	123	PA7	CAN Transmit Line (CANTX)
		122	PA8	CAN Receive Line (CANRX)
MCAN1	2	22	PD14	CAN Transmit Line (CANTX)
		19	PD15	CAN Receive Line (CANRX)
MCAN2	1	127	PA5	CAN Transmit Line (CANTX)
		124	PA6	CAN Receive Line (CANRX)
MCAN2	2	24	PD16	CAN Transmit Line (CANTX)
		23	PD17	CAN Receive Line (CANRX)
MCAN3	1	125	PA0	CAN Transmit Line (CANTX)
		130	PA1	CAN Receive Line (CANRX)
MCAN3	2	111	PD18	CAN Transmit Line (CANTX)
		110	PD19	CAN Receive Line (CANRX)
MCAN4	2	29	PD20	CAN Transmit Line (CANTX)
		26	PD21	CAN Receive Line (CANRX)
MCAN5	2	27	PD22	CAN Transmit Line (CANTX)
		29	PD23	CAN Receive Line (CANRX)

9.3 Interfacing with an SD Card or an eMMC

The SD (Secure Digital) Card is a nonvolatile memory card format used as mass storage memory in mobile devices.

The SAMA7G54 SOM Series includes two Secure Digital Multimedia Card (SDMMC) interfaces that support the MultiMedia Card (eMMC) specification V5.1, the SD Memory Card specification V3.0, and the SDIO V3.0 specification. They are compliant with the SD Host Controller Standard V3.0 specification.

The two interfaces can be connected to a standard SD Card interface.

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The SAMA7G54 SOM Series features one 8-bit SDMMC interface on SDMMC0 and one 4-bit SDMMC interface on SDMMC1. Both interface communications are based on a clock, command, reset, card detect, bus data and power selection.

Table 9-36. SDMMCx Interface Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function
SDMMC0	1	125	PA0	SDMMC0 Clock Line
		130	PA1	SDMMC0 Command Line
		126	PA2	SDMMC0 Reset Signal
		128	PA3	SDMMC0 Data 0 Line
		121	PA4	SDMMC0 Data 1 Line
		127	PA5	SDMMC0 Data 2 Line
		124	PA6	SDMMC0 Data 3 Line
		123	PA7	SDMMC0 Data 4 Line
		122	PA8	SDMMC0 Data 5 Line
		119	PA9	SDMMC0 Data 6 Line
		120	PA10	SDMMC0 Data 7 Line
		129	PA11	SDMMC0 Data Strobe Line
		131	PA12	SDMMC0 Write Protect Signal
		132	PA13	SDMMC0 1.8V/3.3V Selection
		133	PA14	SDMMC0 Card Detect
SDMMC1	1	52	PB28	SDMMC1 Reset Signal
		53	PB29	SDMMC1 Command Line
		58	PB30	SDMMC1 Clock Line
		54	PB31	SDMMC1 Data 0 Line
		55	PC0	SDMMC1 Data 1 Line
		56	PC1	SDMMC1 Data 2 Line
		57	PC2	SDMMC1 Data 3 Line
		59	PC3	SDMMC1 Write Protect Signal
		60	PC4	SDMMC1 Card Detect
		61	PC5	SDMMC1 1.8V/3.3V Selection

9.4 Interfacing with an I²S Interface

The SAMA7G54 SOM Series embeds two Inter-IC Sound Multi-Channel Controllers (I2SMCC) which provide an up to 11-wire, bidirectional, synchronous, digital audio link to external audio devices.

The I2SMCC complies with the Inter-IC Sound (I^2S) bus specification and supports a Time Division Multiplexed (TDM) interface with external multi-channel audio codecs.

The I2SMCC consists of a receiver, a transmitter and a common clock generator that can be enabled separately to provide Host, Client or Controller modes with receiver and/or transmitter active.

In Host mode, the I2SMCC can produce a 16 fs to 1024 fs host clock that provides an over-sampling clock to an external audio codec or Digital Signal Processor (DSP).

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Table 9-37. I²S Interface Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function
I2SMMC0	2	21	PD13	I²S Serial Clock (I2S_CK)
		22	PD14	I²S Bus Clock (I2S_MCK)
		119	PD15	I²S Word Select (I2S_WS)
		24	PD16	I²S Serial Data 0 Output (I2S_DOUT0)
		26	PD17	I²S Serial Data 1 Output (I2S_DOUT1)
		111	PD18	I²S Serial Data 2 Output (I2S_DOUT2)
		110	PD19	I²S Serial Data 3 Output (I2S_DOUT3)
I2SMMC1	1	89	PC11	I²S Serial Clock (I2S_CK)
		91	PC13	I²S Bus Clock (I2S_MCK)
		90	PC12	I²S Word Select (I2S_WS)
		92	PC14	I²S Serial Data 0 Output (I2S_DOUT0)
		93	PC15	I²S Serial Data 1 Output (I2S_DOUT1)
		99	PC16	I²S Serial Data 2 Output (I2S_DOUT2)
		100	PC17	I²S Serial Data 3 Output (I2S_DOUT3)
		101	PC18	I²S Serial Data 0 Input (I2S_DIN0)
		102	PC19	I²S Serial Data 1 Input (I2S_DIN1)
		103	PC20	I²S Serial Data 2 Input (I2S_DIN2)
I2SMMC1	2	35	PD28	I²S Serial Clock (I2S_CK)
		31	PD30	I²S Bus Clock (I2S_MCK)
		33	PD29	I²S Word Select (I2S_WS)
		34	PD31	I²S Serial Data 0 Output (I2S_DOUT0)
		44	PE0	I²S Serial Data 1 Output (I2S_DOUT1)
		45	PE1	I²S Serial Data 2 Output (I2S_DOUT2)
		47	PE2	I²S Serial Data 3 Output (I2S_DOUT3)
		46	PE3	I²S Serial Data 0 Input (I2S_DIN0)
		48	PE4	I²S Serial Data 1 Input (I2S_DIN1)
		48	PE5	I²S Serial Data 2 Input (I2S_DIN2)
		50	PE6	I²S Serial Data 3 Input (I2S_DIN3)

9.5 Interfacing with a Digital Microphone

The SAMA7G54 SOM Series integrates two Pulse Density Modulation Interface Controllers (PDMC). Each PDMC interface controls and decodes up to four digital microphones on the line with a 48 kHz sampling rate.

Table 9-38. PDMC Interface Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function
PDMC0	1	156	PB9	PDM Clock Line
		148	PB10	PDM0 Data 0 Line
		158	PB11	PDM0 Data 1 Line
PDMC0	2	24	PD22	PDM0 Clock Line
		28	PD23	PDM0 Data 0 Line
		32	PD24	PDM0 Data 1 Line
PDMC1	1	126	PA2	PDM1 Clock Line
		128	PA3	PDM1 Data 0 Line
		121	PA4	PDM1 Data 1 Line

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Interface Instance	IO Set	Pin No.	Pin Name	Function
PDMC1	2	30	PD25	PDM1 Clock Line
		36	PD26	PDM1 Data 0 Line
		34	PD27	PDM1 Data 1 Line

9.6 Interfacing with an Image Sensor

The SAMA7G54 SOM Series embeds an Image Subsystem connecting to an image sensor through an RGB parallel interface (ISC interface) or through a dual-lane high-speed MIPI interface (CSI interface).

The Image Sensor Controller (ISC) system manages incoming data from a parallel sensor. The ISC supports an 8- to 12-bit interface camera sensor with a resolution up to 3264x2464.

Table 9-39. ISC Interface Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function
ISC	1	186	PA27	Image Sensor Pixel clock
		181	PA25	Image Sensor Vertical Synchronization
		183	PA24	Image Sensor Horizontal Synchronization
		180	PA15	Image Sensor Main clock
		185	PA26	Field Identification Signal
		179	PA16	Image Sensor Data 0 Line
		174	PA17	Image Sensor Data 1 Line
		177	PA18	Image Sensor Data 2 Line
		185	PA19	Image Sensor Data 3 Line
		175	PA20	Image Sensor Data 4 Line
		178	PA21	Image Sensor Data 5 Line
		176	PA22	Image Sensor Data 6 Line
		184	PA23	Image Sensor Data 7 Line
		187	PA28	Image Sensor Data 8 Line
		188	PA29	Image Sensor Data 9 Line
		3	PA30	Image Sensor Data 10 Line
		4	PA31	Image Sensor Data 11 Line

The Camera Serial Interface (CSI) receives data from a CSI-2-compliant camera sensor. A D-PHY configured as a client (RX) acts as the physical layer.

The CSI implements the MIPI CSI-2 protocol specification. The CSI-2 link protocol specification is part of communication protocols defined by MIPI Alliance standards intended for mobile system chip-to-chip communications. The CSI-2 specification applies to image application processor communication in cameras.

For more information about the Camera Serial Interface features, refer to the SAMA7G5 Series SiP data sheet (see Reference Documents).

Table 9-40. MIPI CSI Interface Configurations

Interface Instance	Pin No.	Pin Name	Function
MIPI CSI	168	MIPI_D0_N	Negative D-PHY differential data line receiver, Lane 0
	167	MIPI_D0_P	Positive D-PHY differential data line receiver, Lane 0
	166	MIPI_D1_N	Negative D-PHY differential data line receiver, Lane 1
	165	MIPI_D1_P	Positive D-PHY differential data line receiver, Lane 1
	164	MIPI_CK_N	Negative D-PHY differential clock line receiver
	163	MIPI_CK_P	Positive D-PHY differential clock line receiver

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9.7 Interfacing with an Octal SPI Memory

The Quad Serial Peripheral Interface (QSPI) is a synchronous serial data link that provides communication with external devices in Host mode.

The QSPI can be used in SPI mode to interface to serial peripherals such as ADCs, DACs, LCD controllers, CAN controllers and sensors, or in Serial Memory mode to interface to serial Flash memories.

The QSPI allows the system to execute code directly from a serial Flash memory (eXecute In Place/ XIP) without code shadowing to RAM. The serial Flash memory mapping is seen in the system as other memories such as ROM, SRAM, DRAM, embedded Flash memory, etc.

With the support of the Quad SPI protocol, the QSPI allows the system to use high-performance serial Flash memories, which are small and inexpensive, instead of larger and more expensive parallel Flash memories.

Note: Stacked devices with a rollover in the memory address space at each die boundary are not supported.

Table 9-41. Octal SPI Interface Configuration

Interface Instance	IO Set	Pin No.	Pin Name	Description
QSPI0	1	156	PB9	QSPI0_IO3, Data Input Output 3
		148	PB10	QSPI0_IO2, Data Input Output 2
		158	PB11	QSPI0_IO1, Data Input Output 1
		157	PB12	QSPI0_IO0, Data Input Output 0
		151	PB13	QSPI0_CS, Peripheral Chip Select
		155	PB14	QSPI0_SCK, Serial Clock
		154	PB15	QSPI0_SCKN, QSPI0 Negated Serial Clock for HyperFlash only
		152	PB16	QSPI0_IO4, Data Input Output 4
		159	PB17	QSPI0_IO5, Data Input Output 5
		150	PB18	QSPI0_IO6, Data Input Output 6
		149	PB19	QSPI0_IO7, Data Input Output 7
		153	PB20	QSPI0_DQS, Data Strobe
		160	PB21	QSPI0_INT, Interrupt Input

9.8 Interfacing with an Ethernet PHY

The SAMA7G54 SOM Series embeds two separate Ethernet MAC interfaces: one Gigabit Ethernet MAC (GMAC0) and one 10/100 Ethernet MAC (GMAC1). The two interfaces can be used at the same time.

For more information about the Ethernet interface features, refer to the SAMA7G5 Series SiP data sheet (see Reference Documents).

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Table 9-42. Gigabit Ethernet MAC (GMAC0) Interface Configuration

Interface Instance	IO Set	Pin No.	Pin Name	Function
GMAC0	1	180	PA15	Transmit Clock or 50 MHz Reference Clock
		179	PA16	Transmit Data 0
		174	PA17	Transmit Data 1
		177	PA18	Receive Data Valid or Carrier Sense and Data Valid or Receive Control Signal
		182	PA19	Receive Data 0
		175	PA20	Receive Data 1
		178	PA21	Receive Error
		176	PA22	Management Data Clock
		184	PA23	Management Data Input/Output
		183	PA24	Transmit Clock or 50 MHz Reference Clock
		181	PA25	125 MHz Clock
		185	PA26	Transmit Data 2
		186	PA27	Transmit Data 3
		187	PA28	Receive Data 2
		188	PA29	Receive Data 3
		3	PA30	Receive Clock
		4	PA31	Transmit Coding Error
		7	PB0	Collision Detect
		5	PB1	Carrier Sense
		6	PB2	TSU Timer Comparison Valid

Table 9-43. 10/100 Ethernet MAC (GMAC1) Interface Configuration

Interface Instance	IO Set	Pin No.	Pin Name	Function
GMAC1	1	26	PD21	Transmit Clock or 50 MHz Reference Clock
		27	PD22	Transmit Data 0
		28	PD23	Transmit Data 1
		32	PD24	Receive Data Valid or Carrier Sense and Data Valid or Receive Control Signal
		30	PD25	Receive Data 0
		36	PD26	Receive Data 1
		34	PD27	Receive Error
		35	PD28	Management Data Clock
		33	PD29	Management Data Input/Output
		31	PD30	Transmit Clock or 50 MHz Reference Clock
		37	PD31	Transmit Data 2
		44	PE0	Transmit Data 3
		45	PE1	Receive Data 2
		47	PE2	Receive Data 3
		46	PE3	Receive Clock
		49	PE4	Transmit Coding Error
		48	PE5	Collision Detect
		50	PE6	Carrier Sense

9.9 Interfacing with a Wireless Module

To interface a Microchip SAMA7G54 System-On-Module Series device with a wireless feature like Wi-Fi, Bluetooth or Zigbee, several interfaces can be used, such as SPI, SDIO and/or USART interfaces.

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For example, the device can be interfaced through SDIO to the Microchip Wi-Fi ATWILC3000 module and through USART to Bluetooth. This wireless module is a single chip IEEE 802.11 b/g/n RF/Baseband/MAC link controller with integrated Bluetooth® 5.0.

If an SPI or USART interface is used, see Interfacing in SPI Mode and Interfacing in USART Mode, respectively.

If an SDIO interface is needed, use one of the following interfaces.

Table 9-44. SDIO Interface Configurations

Interface Instance	IO Set	Pin No.	Pin Name	Function
SDMMC0	1	125	PA0	SDIO/SDMMC0 Clock Line
		130	PA1	SDIO/SDMMC0 Command Line
		128	PA3	SDIO/SDMMC0 Data 0 Line
		121	PA4	SDIO/SDMMC0 Data 1 Line
		127	PA5	SDIO/SDMMC0 Data 2 Line
		124	PA6	SDIO/SDMMC0 Data 3 Line
SDMMC1	1	53	PB29	SDIO/SDMMC1 Command Line
		58	PB30	SDIO/SDMMC1 Clock Line
		54	PB31	SDIO/SDMMC1 Data 0 Line
		55	PC0	SDIO/SDMMC1 Data 1 Line
		56	PC1	SDIO/SDMMC1 Data 2 Line
		57	PC2	SDIO/SDMMC1 Data 3 Line

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10. Electrical Characteristics

10.1 Absolute Maximum Ratings

The following table provides the maximum operating ratings for the Microchip SAMA7G54 System-On-Module.

Table 10-1. Absolute Maximum Ratings

Parameter	Pads	Range	Comments
I/O Supply Voltage	All GPIO	-0.3V to 4.0V	**Note:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. **Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**
VDDQSPI0, VDDIOP0, VDDSDMMC0, VDDSDMMC1 Supplies Voltage	VDDQSPI0, VDDIOP0, VDDSDMMC0, VDDSDMMC1	-0.3V to 4.0V	
Main Supply Voltage	5V_MAIN	-0.3V to 6.0V	
Backup Supply Voltage	VBAT	-0.3V to 4.0V	
Storage Temperature	$T_{STORAGE}$	-55 to +150°C	
Maximum Input Current	5V_MAIN	2A max.	

10.2 Recommended Operating Conditions

The following table provides the recommended operating conditions for the Microchip SAMA7G54 System-On-Module.

Table 10-2. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
All I/O	I/O Supply Voltage on VDD_3V3 Power rail	3.23	3.37	V
VDDQSPI0	QSPI0 Supply Voltage	1.7	3.6	V
VDDIOP0	I/O Supply Voltage on VDDIOP0 Power Rail	1.7	3.6	V
VDDSDMMC0	I/O Supply Voltage on VDDSDMMC0 Power Rail	1.7	1.9	V
		3.0	3.6	V
VDDSDMMC1	I/O Supply Voltage on VDDSDMMC1 Power Rail	1.7	1.9	V
		3.0	3.6	V
5V_MAIN	Main Supply Voltage	3.3	5.5	V
VBAT	Backup Supply Voltage	1.7	3.6	V
T_A	Module Operating Ambient Temperature	-40	+85	°C
T_{J_MPU}[(1)]	MPU Junction Temperature	-40	+105	°C

Note:

1. The MPU junction temperature can be read with the integrated temperature sensor. Refer to the "SAMA7G5 Series Temperature Sensor Calibration" application note (see Reference Documents). T_J must be characterized in-application to make sure this specification is met.

10.3 Power Consumption

The following current consumption values are provided for information only.

Current consumption can vary according to temperature, MPU load and customer application (hardware connections, software application not listed).

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Table 10-3. Power Consumption

Node	Measurement	Conditions	Min	Typ	Max	Unit
5V_MAIN	Current consumption	Linux and Ethernet transfer on Gigabit Interface 5V_MAIN @ 5.00V (CPU @ 1GHz)	–	500	–	mA
VBAT	Current consumption	VBAT @ 3.3V VDD_3V3 @ 3.3V T_A @ 25°C	–	3.2	–	µA
		1.7V < VBAT < 3.6V VDDIN33 = 3.3V All temperature ranges, all modes	–	5	–	µA

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11. Mechanical Characteristics

11.1 SAMA7G54 SOM Dimensions

Figure 11-1. Microchip SAMA7G54 System-On-Module Dimensions

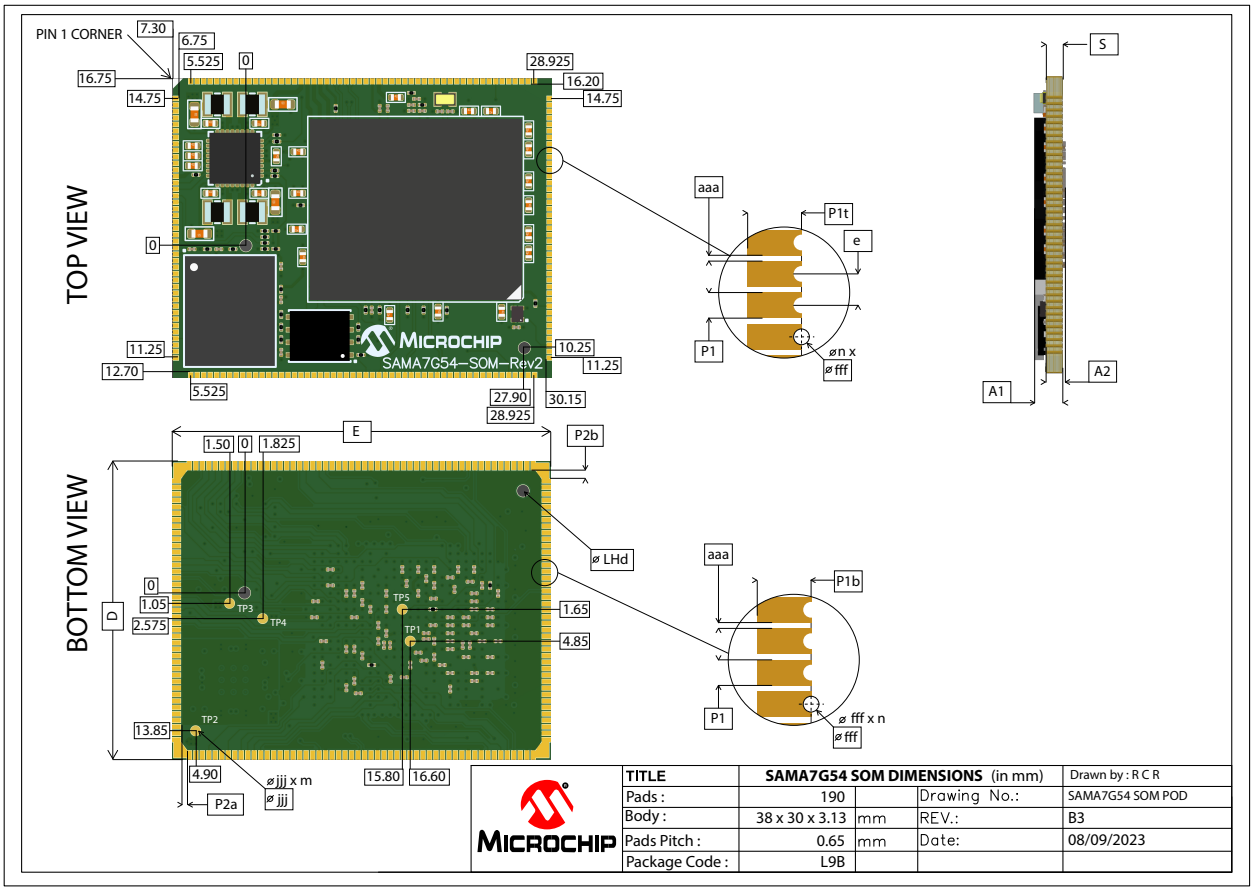

Table 11-1. Microchip SAMA7G54 System-On-Module Dimensions (in mm)

Parameter		Symbol	Common Dimensions		
			Min	Typ	Max
Body overall dimensions	X	E	37.800	38.000	38.200
	Y	D	29.800	30.000	30.200
Pad pitch		e	–	0.650	–
PCB thickness		S	1.450	1.600	1.750
Top thickness (PCB and components)		A1	–	2.800	3.000
Bottom thickness (PCB and components)		A2	–	1.930	2.100
Pad length	Top side	P1t	–	0.550	–
	Bottom side	P1b	–	0.900	–
Pad width		P1	–	0.450	–
Pad gap		aaa	–	0.200	–
Opening drill diameter		fff	–	0.300	–
Pad count		n	–	190	–
Test point diameter[(1)]		jjj	–	1.000	–

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.....continued

Parameter		Symbol	Common Dimensions		
			Min	Typ	Max
Test point count		m	–	5	–
Pad edge to SOM edge	X	P2a	–	0.650	–
	Y	P2b	–	0.875	–
Locating pad hole diameter[(2)]		LHd	1.150	1.200	1.250

Notes:

1. Test points placed under the Microchip SAMA7G54 System-On-Module are for production purposes only. No connection to these points is allowed. Avoid any contact with the main board vias or copper areas (see Figure 11-1).
2. Locating pads are used for production purposes.

11.2 Other Characteristics

Table 11-2. SAMA7G54 SOM Weight

Ordering Code	Parameter	Measurement	
		Value	Unit
SAMA7G54D2GN4-I/L9B	Weight	6.21	g
SAMA7G54D1GN2-I/L9B		6.19	g
SAMA7G54D1GN0-I/L9B		6.02	g

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12. Ordering Information

For details on ordering codes, see Product Identification System.

Ordering Code	DDR3L Memory Configuration	NAND Memory Configuration	Package	Carrier Type	Module Ambient Temperature Range(1)
SAMA7G54D2GN4-I/L9B	2 Gbits	4 Gbits	190-pin 38x30 mm module	Tray	-40°C to +85°C
SAMA7G54D1GN2-I/L9B	1 Gbit	2 Gbits			
SAMA7G54D1GN0-I/L9B	1 Gbit	N/A			

Note:

1. Indicative Ambient Temperature Range. Refer to Table 10-2 for complete information about the operating temperature range.

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13. Revision History

13.1 DS60001841A - 02/2024

Changes
Preliminary issue

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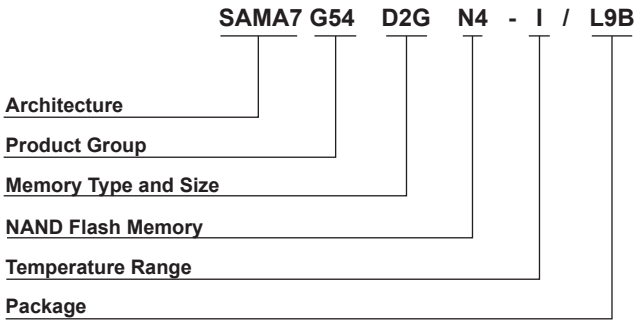

Architecture:	SAMA7	= Arm Cortex-A7 CPU
Product Group:	G54	= 427-ball general-purpose microprocessors
Memory Type and Size:	D1G	= 1-Gbit DDR3L SDRAM
	D2G	= 2-Gbit DDR3L SDRAM
NAND Flash Memory:	N0	= No NAND Flash memory
	N2	= 2-Gbit NAND Flash memory
	N4	= 4-Gbit NAND Flash memory
Ambient Temperature Range[(1)]:	I	= -40°C to +85°C (industrial)
Package:	L9B	= System-On-Module package code

Note:

1. Indicative Ambient Temperature Range. Refer to Table 10-2 for complete information about the operating temperature range.

Example:

- SAMA7G54D2GN4-I/L9B = Arm Cortex-A7 general purpose microprocessor, 2-Gbit DDR3L SDRAM, 4-Gbit NAND Flash memory for industrial applications

Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package.

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