PIC32CX-BZ2 and WBZ45 Family

High-performance 2.4 GHz Multi-protocol Wireless MCUs and Modules, supporting Bluetooth Low Energy and 802.15.4 protocols with 32-bit ARM® Cortex®-M4F, 2 Msps 12-bit ADC Product Brief

Introduction

The PIC32CX-BZ2 family is a general purpose, low-cost, 32-bit Microcontroller (MCU) family of devices supporting Multiprotocol wireless interfaces (Bluetooth® and Zigbee®), hardware-based security accelerator, transceiver and Power Management Unit (PMU).

The WBZ45 module is a series of fully RF certified wireless modules that contains the PIC32CX-BZ2 wireless MCUs with the following antenna options:

- PCB Antenna
- U.FL Connector for External Antenna

In addition, to the Bluetooth Low Energy (Bluetooth® 5.2) and Zigbee (Zigbee® 3.0) wireless protocol support, the PIC32CX-BZ2 devices and the WBZ45 modules also support a rich set of standard MCU peripherals such as ADC, SPI, I2C, SQI, UART and SWD.

PIC32CX-BZ2 SoC Family Features

The following section lists the PIC32CX-BZ2 SoC related features:

Operating Conditions MCUs

- 1.9V to 3.6V, −40°C to +125°C, DC to 64 MHz
  - AEC Q100 Grade 1 qualified

Core: 64 MHz ARM® Cortex®-M4

- 3.35 Coremark®/MHz
- 4 KB Combined Instruction Cache and Data Cache
- 8-Zone Memory Protection Unit (MPU)
- Thumb®-2 Instruction Set
- Digital Signal Processing ASE Rev 2
- Nested Vector Interrupt Controller (NVIC)
- Embedded Trace Module (ETM) with Instruction Trace Stream
- Core Sight Embedded Trace Buffer (ETB)
- Trace Port Interface Unit (TPIU)
- IEEE 754-Compliant Floating Point Unit (FPU)

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Memories

- 1 MB On-Chip Self-programmable Flash With:
    - Error Correction Code (ECC)
    - Prefetch module to speed up Flash accesses
    - 20-years of data retention support
- 32 KB NVR Flash (8 Sectors)
    - Private/public boot code and data
    - NV calibration data
- 128 KB Multi-port Programmable QoS SRAM Main Memory
    - 64 KB of Error Correction Code (ECC) RAM option
- Up to 4 KB of Tightly Coupled Memory (TCM)
- Up to 8 KB Backup SRAM
- Single 32-bit Backup Register

System

- Power-on Reset (POR) and Brown-out Detection (BOD)
- Internal and External Clock Options
- External Interrupt Controller (EIC)
- Up to 4 External Interrupts
- One Non-maskable Interrupt
- 2-pin Serial Wire Debug (SWD) Programming, Test, and Debugging Interface

Supported Connectivity Standards

- Complies With:
    - Bluetooth® v5.2
    - IEEE 802.15.4, Zigbee® 3.0
    - ETSI EN 300 328 and EN 300 440 Class 2
    - FCC CFR47 Part 15 and ARIB STD-T66

Power Supply

- Integrated PMU With:
    - Buck (DC-DC/switching) mode; supports High Power (PWM) and Low Power (PSK) mode
    - MLDO (linear) mode
- On-board 1.2V Voltage Regulator (CLDO)
- Power-on Reset (POR) and Brown Out Detector (BOR) on 3.3V and 1.2V Rails
- Run, Idle, Dream, Sleep, Deep Sleep, and Extreme Deep Sleep Modes
- Sleep Walking Peripherals
- Embedded Buck/LDO Regulator Supporting On-the-fly (OTF) Selection

2.4 GHz RF Transceiver

- Integrated 2.4 GHz Ultra-low Power RF Transceiver shared between Bluetooth and Zigbee Modems and Link (MAC) Controllers
- Integrated 16 MHz ±20 ppm Crystal Oscillator (External Low Cost Crystal)
- Two PA Design Architecture (LPA (+4 dBm) and MPA (+10dBm)) to Improve TX Power Efficiency

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- Low RBOM Two-port TRX RFFE Architecture
  – Integrated balun (single ended RF output) and TRX switch
- Hardware Radio Arbiter with Programmable QoS:
  – Resolution per packet level
  – Time-division coexistence between Bluetooth and 802.15.4
  – Based on shared transceiver and antenna
  – Maintains connections of 802.15.4 and Bluetooth simultaneously

Bluetooth

- Bluetooth Low Energy 5.2 Certified
- Up to +10 dBm Programmable Transmit Output Power
- Typical Receiver Power Sensitivity:
  – −95 dBm for Bluetooth Low Energy 1 Mbps
  – −92 dBm for Bluetooth Low Energy 2 Mbps
  – −102 dBm for Bluetooth Low Energy 125 Kbps
  – −99 dBm for Bluetooth Low Energy 500 Kbps
  – Digital RSSI indicator (−50 dBm ~ −90 dBm)
- Bluetooth Supported Features:
  – 2M uncoded PHY
  – Long range (Coded PHY)
  – Channel selection algorithm #2
  – Advertising extensions, offloads CPU with hardware based scheduler
  – High duty cycle non-connectible advertising
  – Data length extensions
  – Secure connections
  – Privacy upgrades (with hardware white-list support)
- ECDH P256 Hardware Engine for Link Key Generation When Bluetooth Pairing
- AES128 Hardware Module for Real-Time Bluetooth Payload Data Encryption
- Bluetooth Qualification Test Facility (BQTF) Certification
- Bluetooth Low Energy Profiles:
  – Bluetooth Low Energy peripheral and central roles
  – Bluetooth Low Energy APIs for application layer to implement standard or customize GATT based profiles/services
  – Microchip Transparent UART Service
  – Battery Service
  – Device Information Service
  – Custom Service
  – Multi-link and multi-role
- Bluetooth Low Energy Services:
  – Provisioning
  – Over-the-air (OTA) update (also known as DFU)
  – Advertisement/Beacon
  – Personalized configuration
  – Alert notification service

Zigbee

- Physical Layer Service Unit (PSDU) data rate: 250 Kbps
  – Proprietary data rates: 500 Kbps, 1 Mbps, and 2 Mbps

- Programmable RX Mode
    - −103 dBm RX sensitivity in the Continuous mode
    - −98 dBm sensitivity in the RPC mode
    - RPC mode provides lower power consumption in RX mode to support California Green Energy Specification at the system level
- TX Output Power up to +10 dBm
- Hardware Assisted MAC
    - Auto acknowledge
    - Auto retry
    - Channel access back-off
- SFD Detection; Spreading; De-spreading; Framing; CRC-16 Computation
- Independent TX/RX Buffers for Improved CPU Offloading While Handling Zigbee Data
    - 128-byte TX and 128-byte RX frame buffer
- Hardware Security
    - Advanced Encryption Standard (AES)
    - True Random Number Generator (TRNG)
- Zigbee Stack Support
    - Zigbee 3.0 ready
    - Zigbee Pro 2017
    - Zigbee green power support (proxy, sink, and multi sensor)

High Performance Peripherals

- 16-Channel Direct Memory Access Controller (DMAC)
    - Built-in CRC with memory CRC generation/monitor hardware support
- One Quad I/O Serial Peripheral Interface (QSPI)
    - execute-In-Place (xIP) support
    - Dedicated AHB memory zone

System Peripherals

- 32-Channel Event System
    - All channels can be connected to any event generator
    - All channels provide a pure asynchronous path
    - Twelve channels support synchronous and re-synchronous
- Four Serial Communication Interfaces (SERCOM), Each Configurable to Operate as:
    - USART with full-duplex and single-wire half-duplex configuration
    - ISO7816
    - I^2C up to 1 MHz (three SERCOMs support I^2C)
    - LIN Master/Slave
    - RS485
    - SPI inter-byte space
- Four 16-bit Timers/Counters (TC), Each Configurable as:
    - 16-bit TC with two compare/capture channels
    - 8-bit TC with two compare/capture channels
    - 32-bit TC with two compare/capture channels
- Two 24-bit Timer/Counters for Control (TCC) with Extended Functions:
    - Up to six compare channels with optional complementary output
    - Generation of synchronized Pulse Width Modulation (PWM) pattern across port pins
    - Deterministic fault protection, fast decay, and configurable dead-time between complementary output

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- Dithering that increase resolution with up to 5 bits and reduce quantization error
- One 16-bit Timer/Counters for Control (TCC) with Extended Functions:
  - Up to two compare channels with optional complementary output
- 32-bit Real Time Counter (RTC) with Clock/Calendar Function
- Up to four Wake-up Pins with Tamper Detection and Debouncing Filter
- Watchdog Timer (WDT) with Window Mode
- Deadman Timer (DMT)
- CRC-32 Generator
- Frequency Meter (FREQM)
- Two Configurable Custom Logic (CCL)
- One Analog Comparator (AC) with Window Compare function
- One Temperature Sensor (Die Temperature)

Advanced Analog

12-bit ADC SAR Module (ADC):

- Up to 8 Analog Channels
- Up to 2 MSPS conversion rate
- Multiple trigger sources
- Supports die temperature sensor built into RF-Analog (not an external "ambient" temperature sensor)
- Two Analog Comparator (AC) with Window Compare Function or single Analog Comparator
- One dedicated AC and second AC is shared with MVREF FSM

Security

- AES Engine with Support for 128/192/256 bit Cryptographic Key
- One AES with 256-bit Key Length and up to 2 MB/s Data Rate
  - Five confidential modes of operation (ECB, CBC, CFB, OFB, and CTR)
  - Supports counter with CBC-MAC mode
  - Galois Counter Mode (GCM)
- True Random Number Generator (TRNG)
- Public Key Cryptography Controller (PUKCC) and Associated Classical Public Key Cryptography Library (PUKCL)
  - RSA and DSA algorithm
  - Elliptic Curves Cryptography (ECC), ECC GF (2n), and ECCGF (p)
- Integrity Check Module (ICM) Based on Secure Hash Algorithm (SHA1, SHA224, and SHA256), DMA Assisted

Oscillators

- 16 MHz, ±20 PPM Crystal/Resonator Oscillator or External Clock (POSC) for 2.4G RF Transceiver
- Shared System PLL with Bluetooth/Zigbee RF Data Converter PLL
- 32.768 kHz Ultra-low Power Internal Oscillator
  - ±5% trimmed accuracy
- Higher Accuracy 32.768 kHz, ±250 ppm Clock Options
  - POSC derived 32 kHz clock
  - 32.768 kHz crystal/resonator oscillator (SOSC)
  - External 32.768 kHz clock source
- 8 MHz Internal RC Oscillator (FRC)

– Trimmed accuracy under ±1%

I/O

- Flexible Peripheral Pin Select (PPS) Support
- High-current Sink/Source on Most I/O Pins
- Configurable Open-Drain Output on Digital I/O Pins
- 5V Tolerant Input Pins (Digital Pins Only)[1]
- Up to 27 Programmable I/O Pins [2]

Notes:
1. Certain pins are limited to 3.3V tolerance, see Electrical Specifications.
2. Two additional input only pins are available if not using SOSC.

Package

- PIC32CX1012BZ25032
  - 32-pin QFN
  - Size - 5 x 5 x 1 mm
- PIC32CX1012BZ25048
  - 48-pin QFN
  - Size - 7 x 7 x 1 mm
- PIC32CX1012BZ24032
  - 32-pin QFN
  - Size - 5 x 5 x 1 mm

WBZ45 Module Features

The following section lists the WBZ45 Module related features, which complements SoC features:

WBZ45 Module Variants

- WBZ451 based on (PIC32CX1012BZ25048 SoC)
  - WBZ451PE (PCB)
  - WBZ451UE (u.FL)
- WBZ450 based on (PIC32CX1012BZ24032 SoC)
  - WBZ450PE (PCB)
  - WBZ450UE (u.FL)

Antenna

- On-Board PCB Antenna
- External Antenna

Clock Management

- Integrated 16 MHz POSC

System Peripheral, Advanced Analog and Security

• All features of SoC are accessible

Package and Operating Conditions

• WBZ451
    – 39-pin SMD package with Shield CAN
    – Size - 15.5 x 20.7 x 2.8 mm
• WBZ450
    – 30 pin SMD package with Shield CAN
    – Size - 13.4 x 18.7x 2.8 mm
• Operating Conditions
    – 1.9V to 3.6V, −40°C to +85°C, DC to 64 MHz

Certifications

• Certified to FCC, ISED and CE Radio Regulations
• RoHS and REACH Compliant
  Note: Certifications in progress.

Table of Contents

Confidential

1. System Block Diagram

Figure 1-1. System Block Diagram
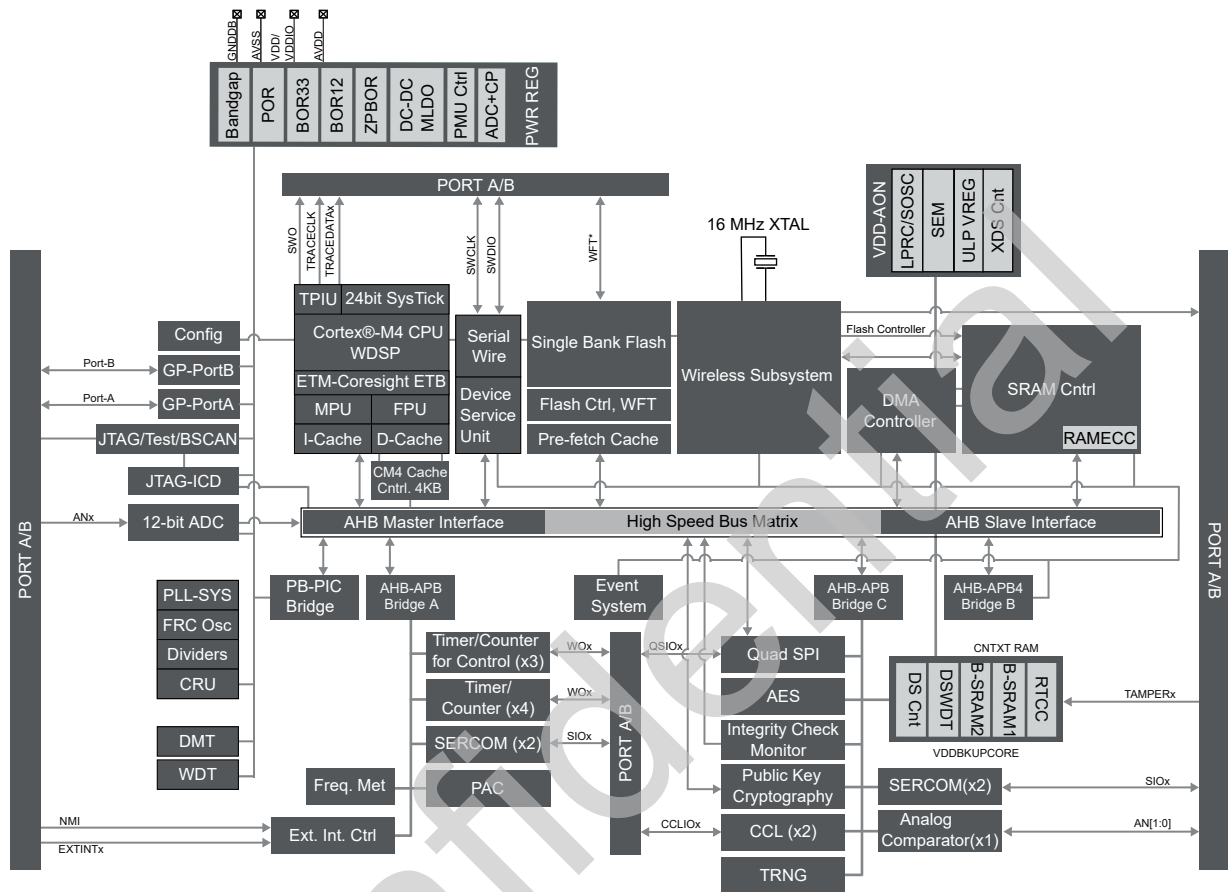
2. Configuration Summary

Table 2-1. PIC32CX-BZ2 and WBZ45 Family Features

Device	Program Memory (KB)	Data Memory (KB)	Pins	Package	Peripherals													Analog			Security				Wireless		
					SERCOM	Timer/Counter (TC)	TCC (24-bit/16-bit)	QSPI	DMA Channels	RTC	CCL/LUT	WDT	DMT	Frequency Measurement	Event System (Channels)	External Interrupt Lines	GPIO Pins	Analog Comparators (Channels)	ADC (Channels)	Temperature Sensor	AES	TRNG	Public Key Cryptography (PUKCC)	Integrity Check Monitor	Max TX Power (dBm)	Bluetooth 5.1	802.15.4/Zigbee 3.0
PIC32CX1012BZ25048	1024	128	48	QFN	4										32	4	27	2	8						10		
PIC32CX1012BZ25032	1024	128	32	QFN	2										32	4	14	—	4						10		
PIC32CX1012BZ24032	1024	128	32	QFN	2	4	2/1	Y	16	Y	1/2	Y	Y	Y	32	4	16	1	6	Y	Y	Y	Y	Y	4	Y	Y
WBZ451	1024	128	37	LGA	4										32	4	27	2	8						10		
WBZ450	1024	128	30	LGA	2										32	4	16	1	6						4		

3. Pin Details of PIC32CX-BZ2 and WBZ45 Family

This section provides details on pin diagrams and signal names along with the device pinout for each variant of SoC and module type of the PIC32CX-BZ2 and WBZ45 family.

Figure 3-1. PIC32CX1012BZ25048 PIC32CX1012BZ24032 and PIC32CX1012BZ25032 SoC Pin Diagram (Bottom View)

PIC32CX1012BZ25048

PIC32CX1012BZ24032
and
PIC32CX1012BZ25032
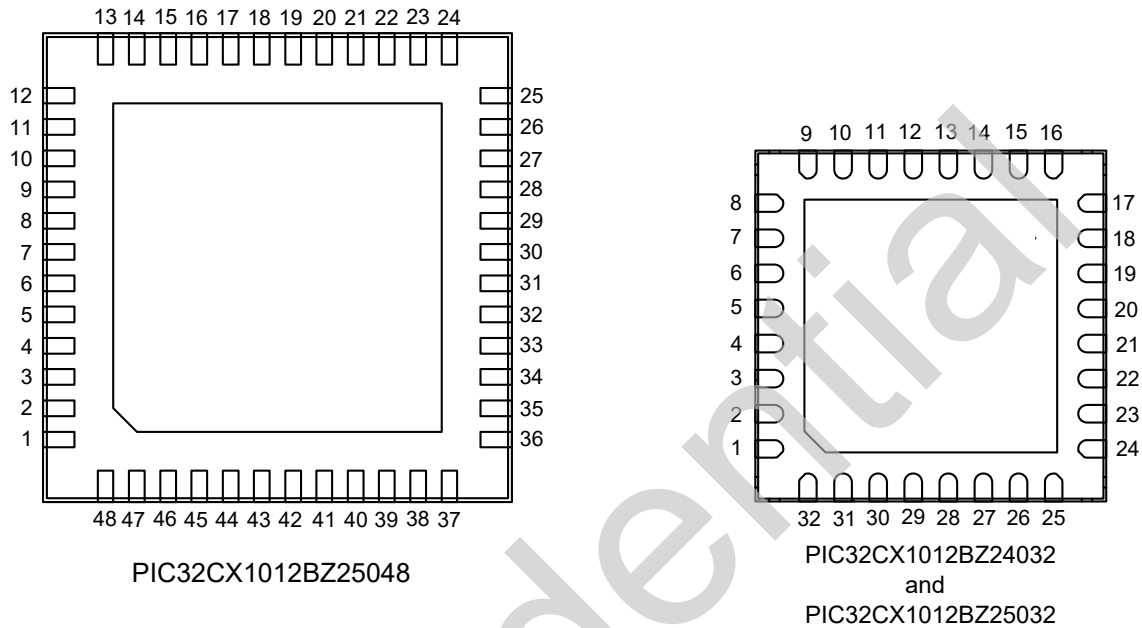
Figure 3-2. WBZ451 and WBZ450 Module Pin Diagram (Top View)
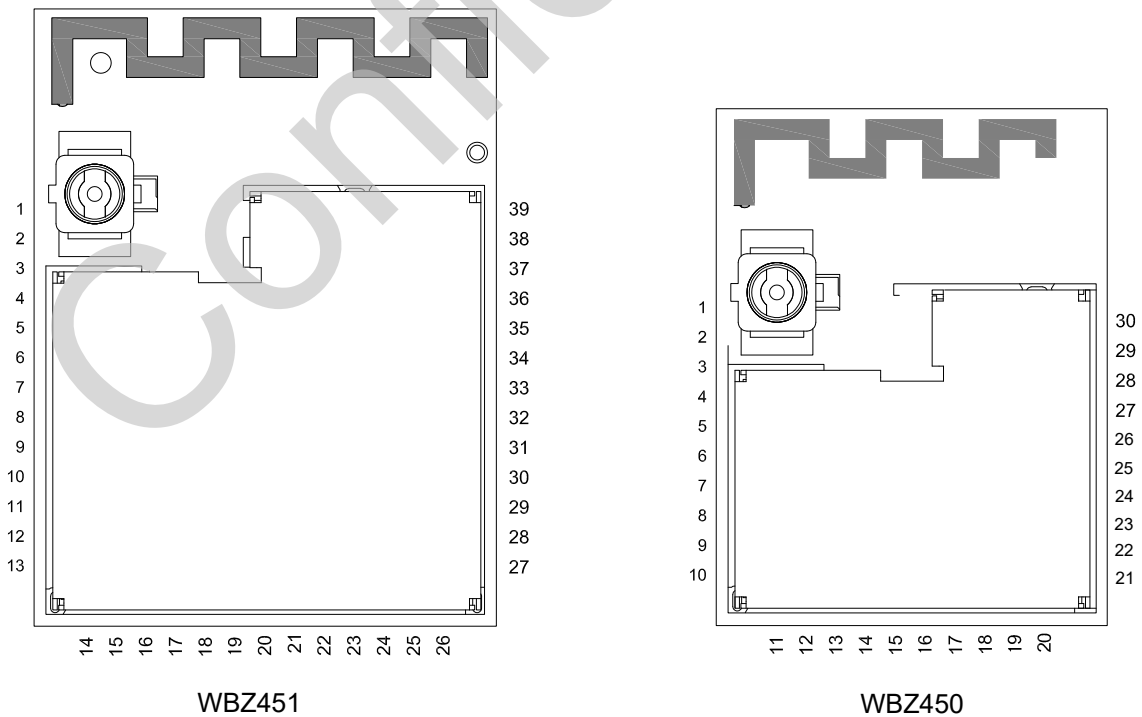
WBZ451

WBZ450

Table 3-1. Pin Details of PIC32CX-BZ2 and WBZ45 Family

SoC			Module		Pin Name[1][2][6]
PIC32CX1012BZ25032	PIC32CX1012BZ24032	PIC32CX1012BZ25048	WBZ450	WBZ451	
—	—	—	1, 5, 8, 18, 21, 27	1, 2, 8,11, 19, 26	GND[3]
32	32	1	—	—	PMU_BK
1	1	2	—	—	VPMU_VDD
2	2	3	—	—	PMU_MLDO
—	—	4	—	20	PA0/RA0/QSPI_DATA2/ RTC_IN3
—	—	5	—	21	PA1/AC_CMP1/RA1/ QSPI_DATA3/RTC_IN2
—	—	6	—	35	PA2/AC_CMP0/RA2/RTC_IN1
3	3	7	19	24	PA5/RA5/SERCOM0_PAD0
4	4	8	16, 17	27, 28	VDD
5	5	9	20	25	PA6/AC_CMP1_ALT/RA6/ SERCOM0_PAD1/ PGC2ENTRY
6	6	10	25	31	PA7/RA7/SERCOM1_PAD0/ TRACECLK
7	7	11	24	29	PA8/RA8/SERCOM1_PAD1/ FECTRL0/PGD2ENTRY
8	8	12	22	30	PA9/RA9/RTC_IN0_ALT/ SERCOM1_PAD2/FECTRL1
9	9	13	23	32	PA10/RA10/RTC_OUT_ALT/ SERCOM1_PAD3/FECTRL2
—	—	14	—	22	PB12/RB12/QSPI_DATA0
—	—	15	—	23	PB13/RB13/QSPI_DATA1/ RTC_EVENT
—	—	16	—	33	PA13/RA13/SERCOM2_PAD0/ COEXCTRL0
—	—	17	—	34	PA14 /RA14/ SERCOM2_PAD1/ COEXCTRL1
10	10	18	—	—	CLDO_O
11	11	19	—	—	BUCK_CLDO

..........continued

SoC			Module		Pin Name[1][2][6]
PIC32CX1012BZ25032	PIC32CX1012BZ24032	PIC32CX1012BZ25048	WBZ450	WBZ451	
12	12	20	—	—	EXTR
13	13	21	—	—	BUCK_BB
14	14	22	—	—	XO_N/XO−
15	15	23	—	—	XO_P/XO+
16	16	24	—	—	BUCK_PLL
17	17	25	—	—	BUCK_LPA
18	18	26	—	—	LPA_OUT/LPA
19	—	27	—	—	MPA_OUT/MPA
20	—	28	—	—	BUCK_MPA
21	—	29	2	3	NMCLR
—	20	30	3	4	PB0/AC_AIN2/AN4/RB0/ COEXCTRL2
—	21	31	10	38	PB1/AC_AIN3/AN5/RB1
—	—	32	—	37	PB2/AC_AIN0/AN6/RB2
—	—	33	—	5	PB3/AC_AIN1/AN7/RB3
22	22	34	11	39	PB4/AN0/INT0/RB4/FECTRL3/ TRACEDATA3, PGC1
23	23	35	9	6	PB5/AN1/RB5/FECTRL4/ TRACEDATA0, PGC4
24	24	36	4	7	AVDD
25	25	37	12	12	PB6/AN0, AN2/RB6/FECTRL5/ TRACEDATA1, PGD1
26	26	38	15	13	PB7/LVDIN/AN3/RB7/ TRACEDATA2, CM4_SWO, PGD4
—	—	39	—	—	VDD
27	27	40	14	15	PB9/RB9/CM4_SWDIO
28	28	41	13	14	PB8/RB8/CM4_SWCLK
29[5]	29[5]	42	6	16	PA4/RA4/RTC_OUT/ SERCOM0_PAD3
—	—	43	—	17	PB10/RB10/QSPI_CS
—	—	44	—	18	PB11/RB11/QSPI_SCK

..........continued

SoC			Module		Pin Name[1][2][6]
PIC32CX1012BZ25032	PIC32CX1012BZ24032	PIC32CX1012BZ25048	WBZ450	WBZ451	
29	29	45	—	9	PA11/RA11[4]/SOSCI
30	30	46	—	10	PA12/ RA12[4]/SOSCO
30[5]	30[5]	47	7	36	PA3/RA3/RTC_IN0/ SERCOM0_PAD2/SCLKI
30[5]	30[5]	48	—	—	VPMU_VDD
—	—	—	26, 28, 29, 30	—	NC

Notes:

1. All GPIOs (RAn and RBn) can be used by remappable peripherals via PPS.

2. All GPIOs (RAn and RBn) can be used as IO Change Notification (IOCAn and IOCBn).

3. The metal paddle at the bottom of the device must be connected to system ground.

4. This pin can be used as Input only pin if not using SOSC.

5. For 25032 and 24032 only, pin 29 and pin 30 act as GPIO PA4/PA3 respectively ONLY if CFGCON0.GPSOSCE = 0. If CFGCON0.GPSOSCE=1, these pins are SOSC 32 kHz crystal inputs OR as digital input only RA11/RA12 respectively.

6. These I/O pins are 5.5V tolerant: NMCLR, PA0, PA1, PA2, PA4, PA5, PA6, PA7, PA8, PA9, PA10, PA13, PA14, PB10, PB11, PB12, PB13. All other I/O pins are 3.3V tolerant.

4. Packaging Information

This chapter provides the information on package markings, dimension and footprint of the PIC32CX-BZ2 and WBZ45 family.

4.1 PIC32CX-BZ2 SoC Packaging Information

Note: For the most current package drawings, please see the Microchip Packaging Specification located at www.microchip.com/en-us/support/package-drawings.

The following images illustrate the packaging information of the PIC32CX1012BZ25048, which has 48-lead very thin quad flat, no lead package (MYX) - 7x7x0.9 mm body [VQFN] with 4.04x4.12 mm exposed pad.
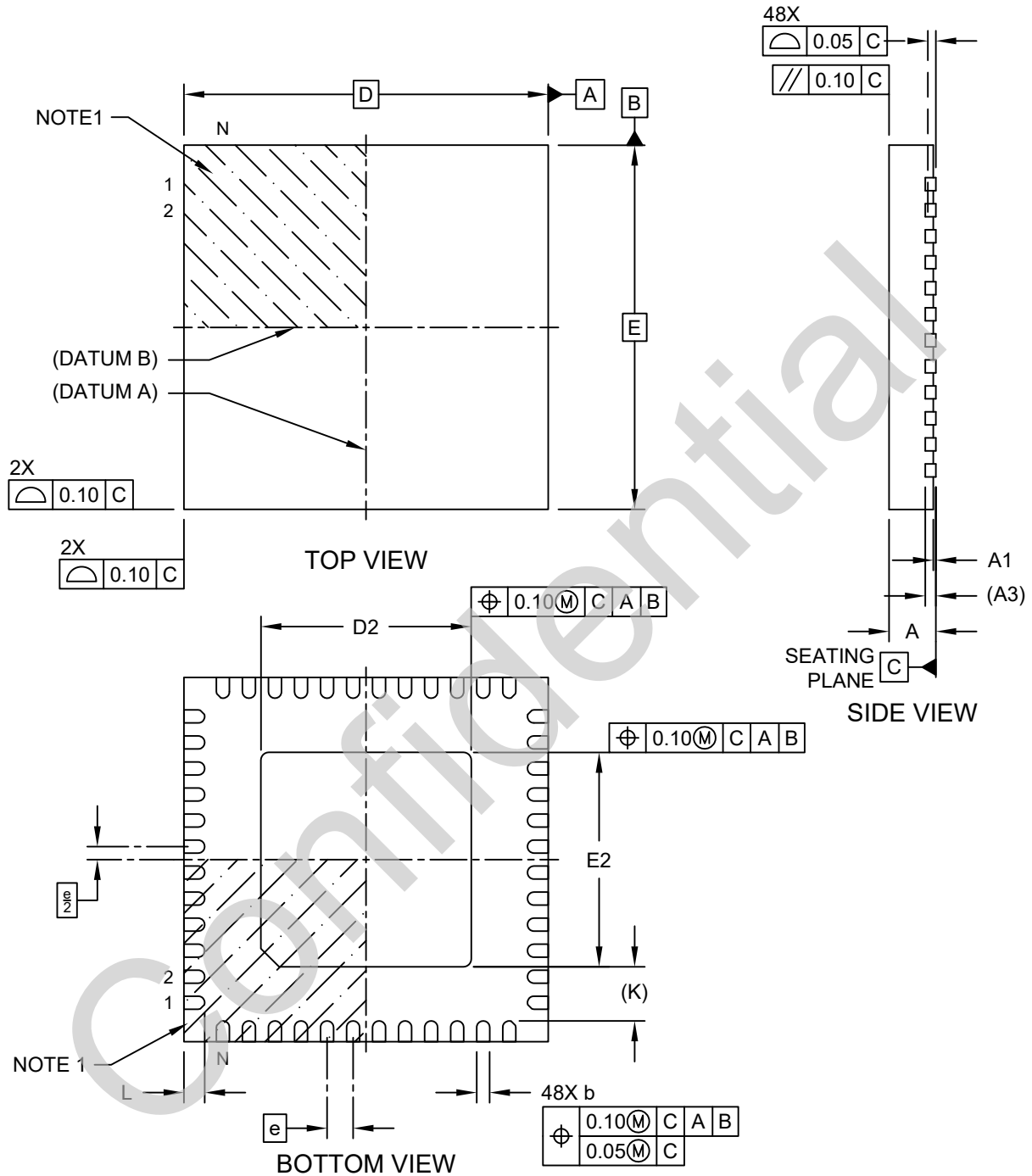
Figure 4-1. PIC32CX1012BZ25048 SoC Packaging Dimension

Figure 4-2. PIC32CX1012BZ25048 SoC Package Outline Drawing
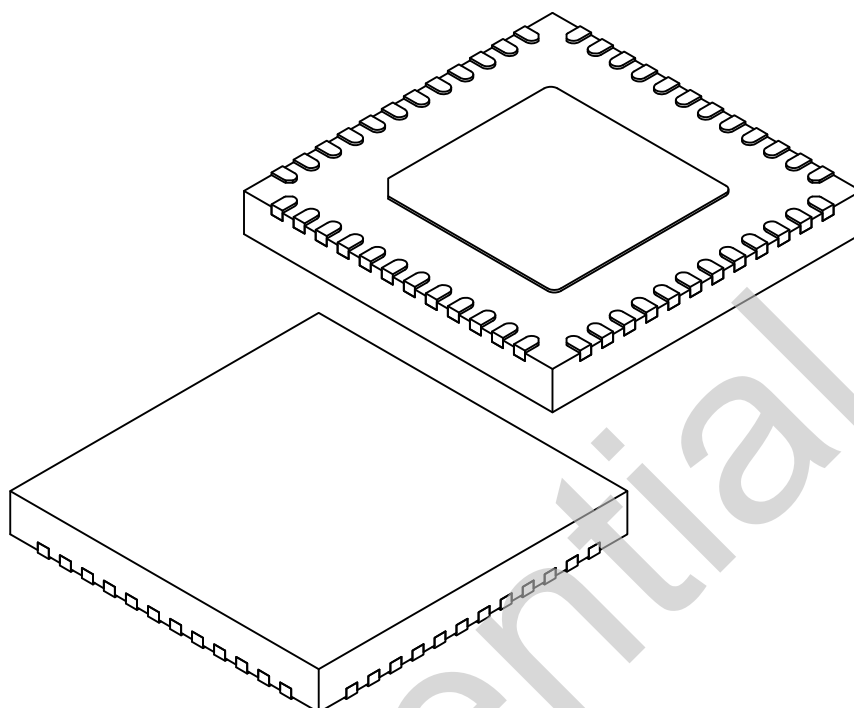
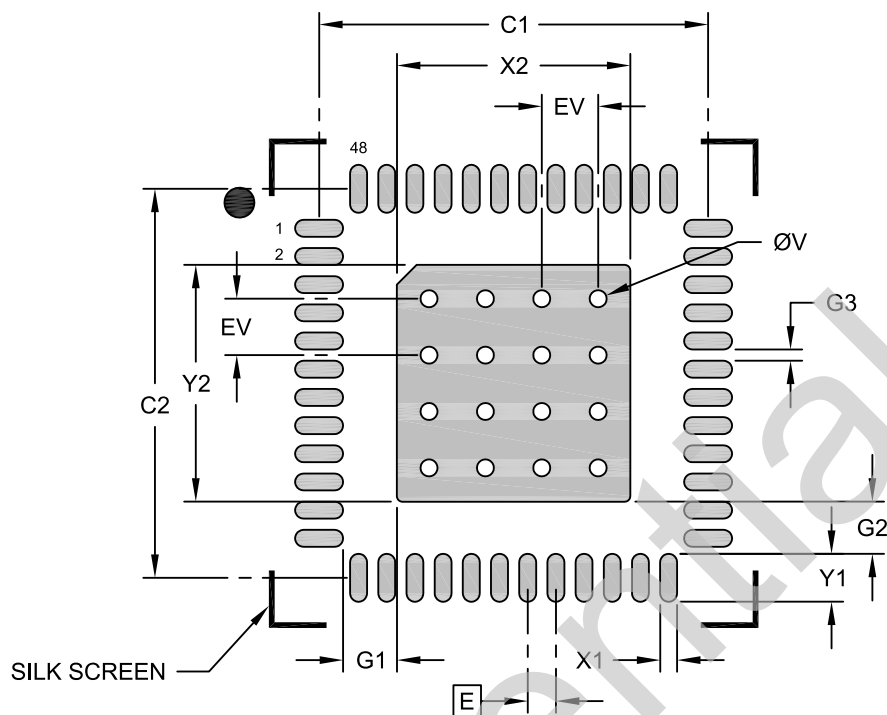|	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		7.00 BSC	
Exposed Pad Length	D2	3.94	4.04	4.14
Overall Width	E		7.00 BSC	
Exposed Pad Width	E2	4.02	4.12	4.22
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		1.04 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Figure 4-3. PIC32CX1012BZ25048 SoC Recommended Land Pattern

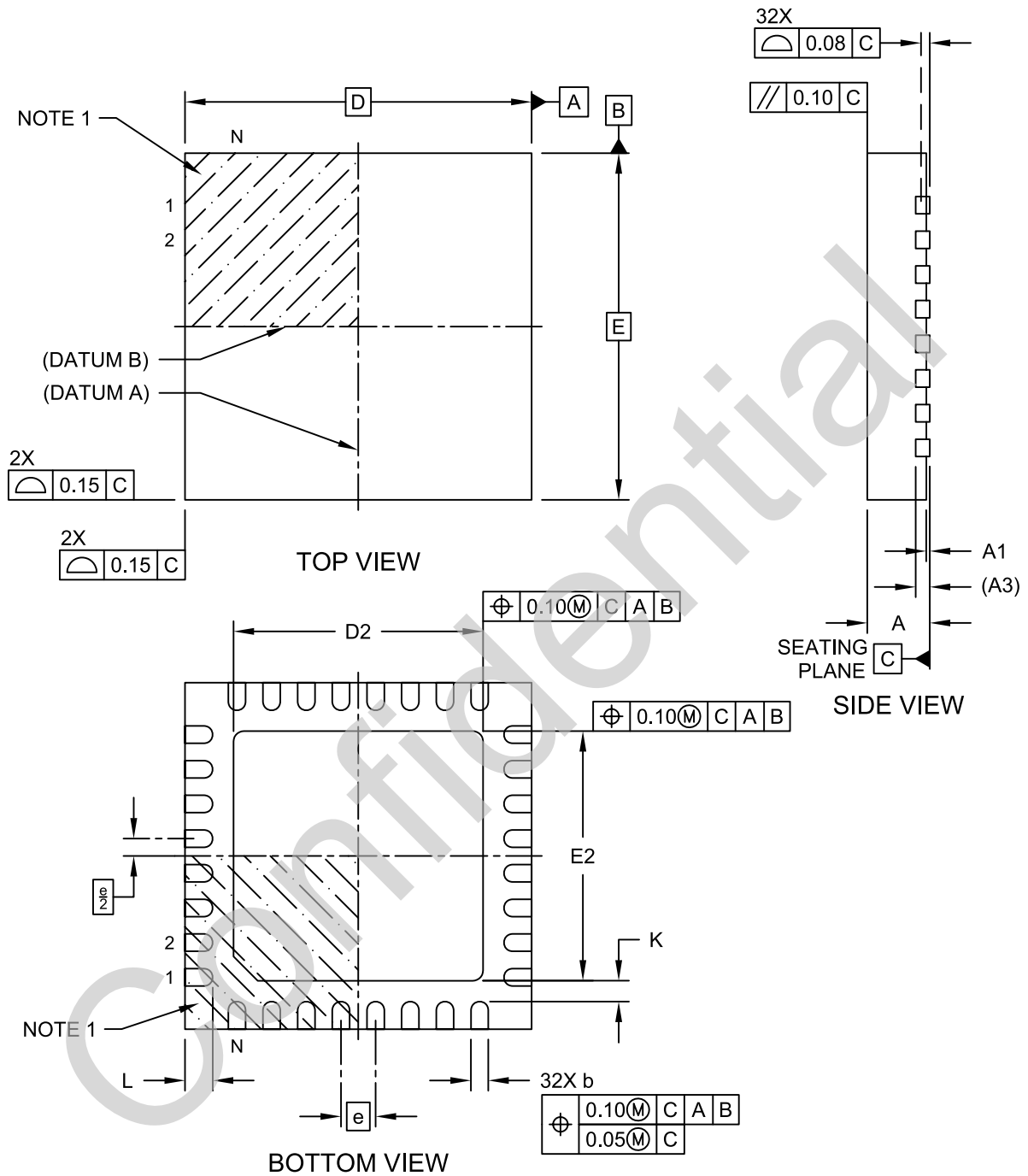|	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			4.14
Optional Center Pad Length	Y2			4.20
Contact Pad Spacing	C1		6.90	
Contact Pad Spacing	C2		6.90	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			0.85
Contact Pad to Center Pad (X24)	G1	0.96		
Contact Pad to Center Pad (X24)	G2	0.93		
Contact Pad to Contact Pad (X44)	G3	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

The following images illustrate the packaging information of the PIC32CX1012BZ25032 and PIC32CX1012BZ24032, which has 32-lead very thin plastic quad flat, no lead package (S8B) - 5x5 mm body [VQFN] with 3.6x3.6 mm exposed pad.

Figure 4-4. PIC32CX1012BZ25032 and PIC32CX1012BZ24032 SoC Packaging Dimension

TOP VIEW

SIDE VIEW

BOTTOM VIEW

Figure 4-5. PIC32CX1012BZ25032 and PIC32CX1012BZ24032 SoC Package Outline Drawing
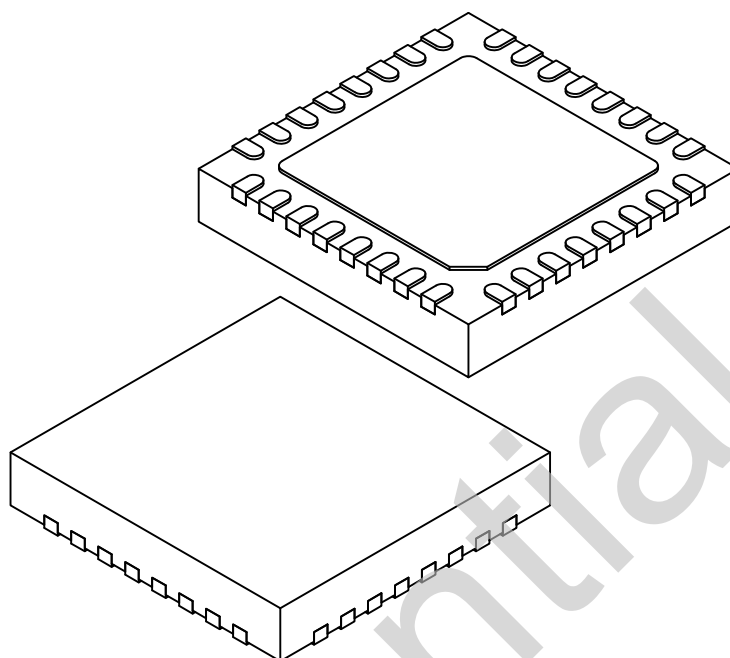
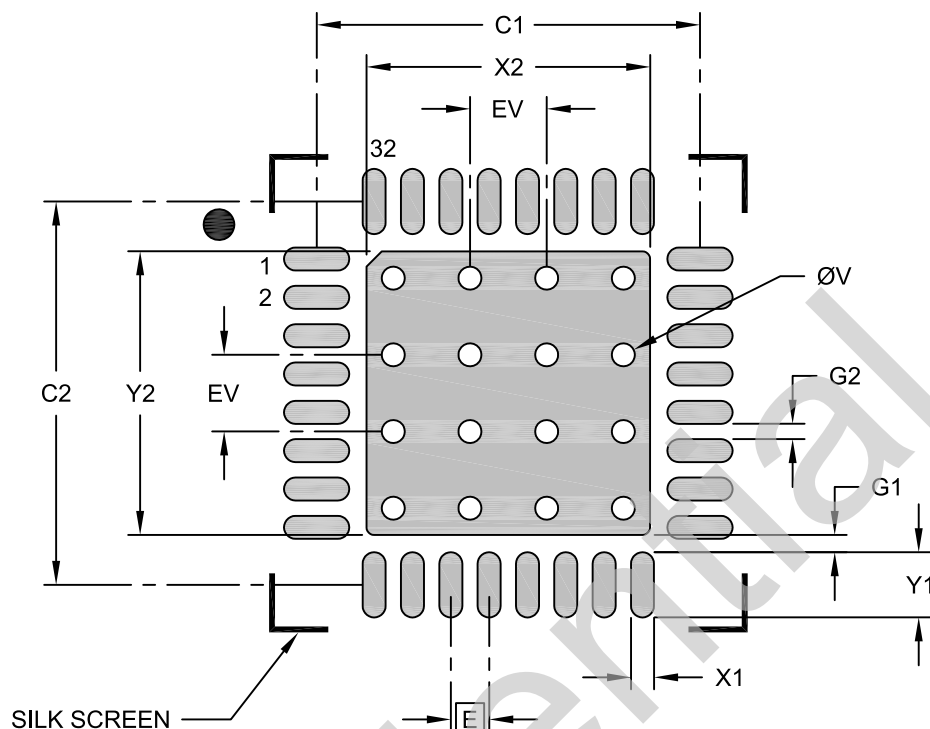|	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.50	3.60	3.70
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.50	3.60	3.70
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Figure 4-6. PIC32CX1012BZ25032 and PIC32CX1012BZ24032 SoC Recommended Land Pattern

RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.70
Optional Center Pad Length	Y2			3.70
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.85
Contact Pad to Center Pad (X32)	G1	0.23		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process
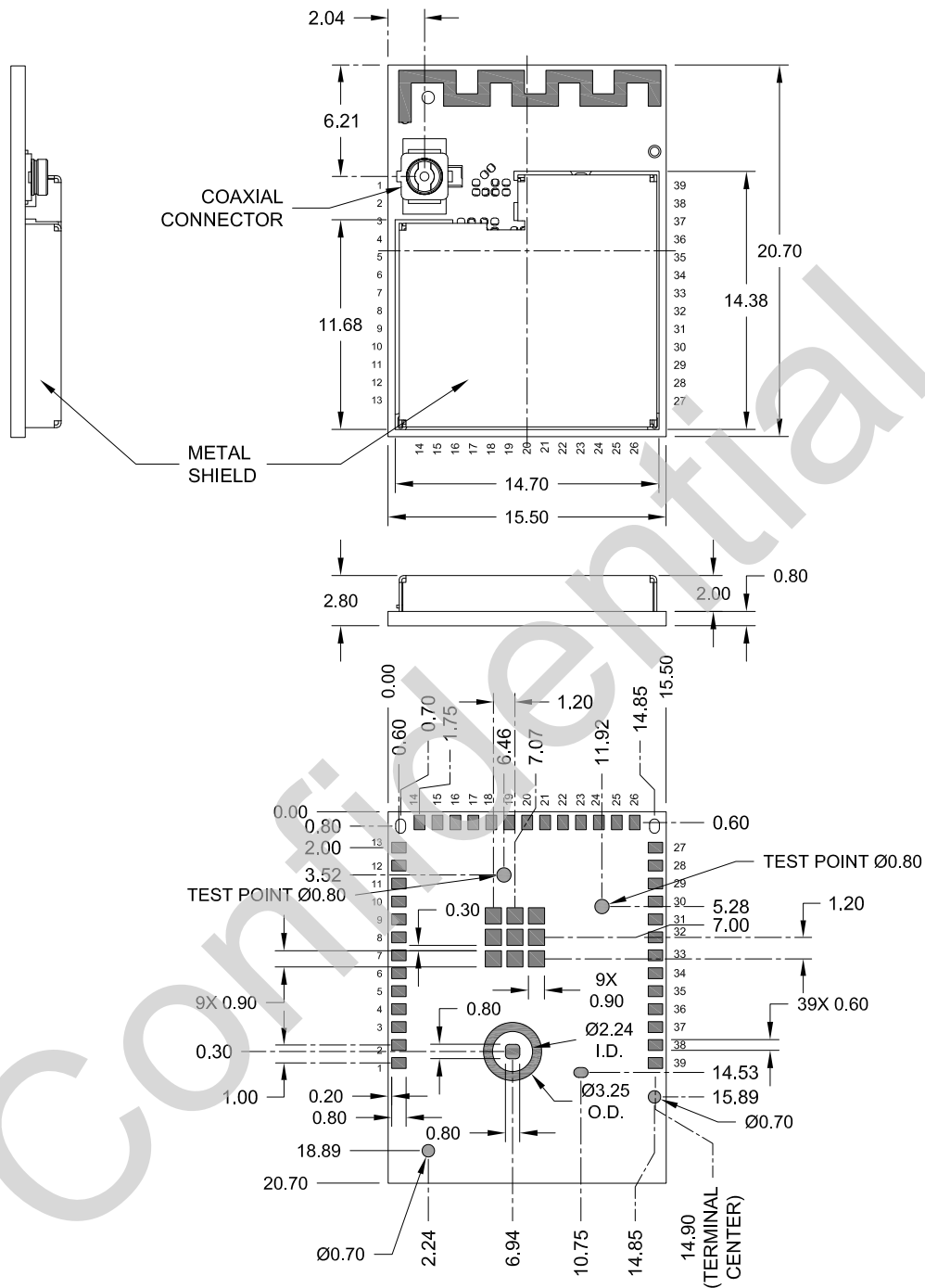
4.2 WBZ45 Module Packaging Information

Note: For the most current package drawings, please see the Microchip Packaging Specification located at www.microchip.com/en-us/support/package-drawings.

The following images illustrate the packaging information of the WBZ451, which has 39-lead PCB module (ZSX) -15.5x20.7x2.8 mm body (module) with metal shield and coaxial connector.

Figure 4-7. Dimensions and Top, Bottom, and Side Views of WBZ451 Module

Figure 4-8. WBZ451 Module Package Outline Drawing
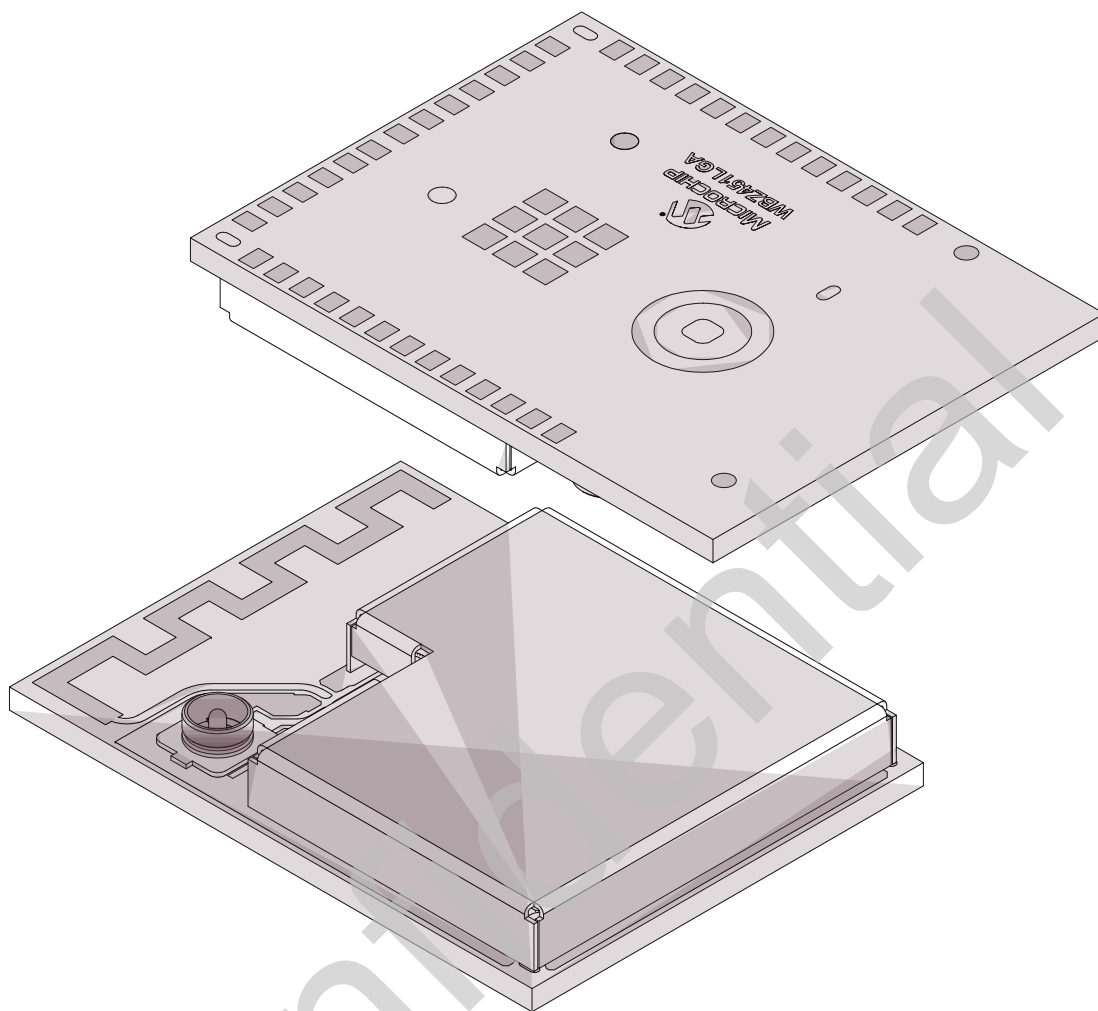
Figure 4-9. Recommended Land Pattern of WBZ451 Module

COPPER KEEPOUT ZONE
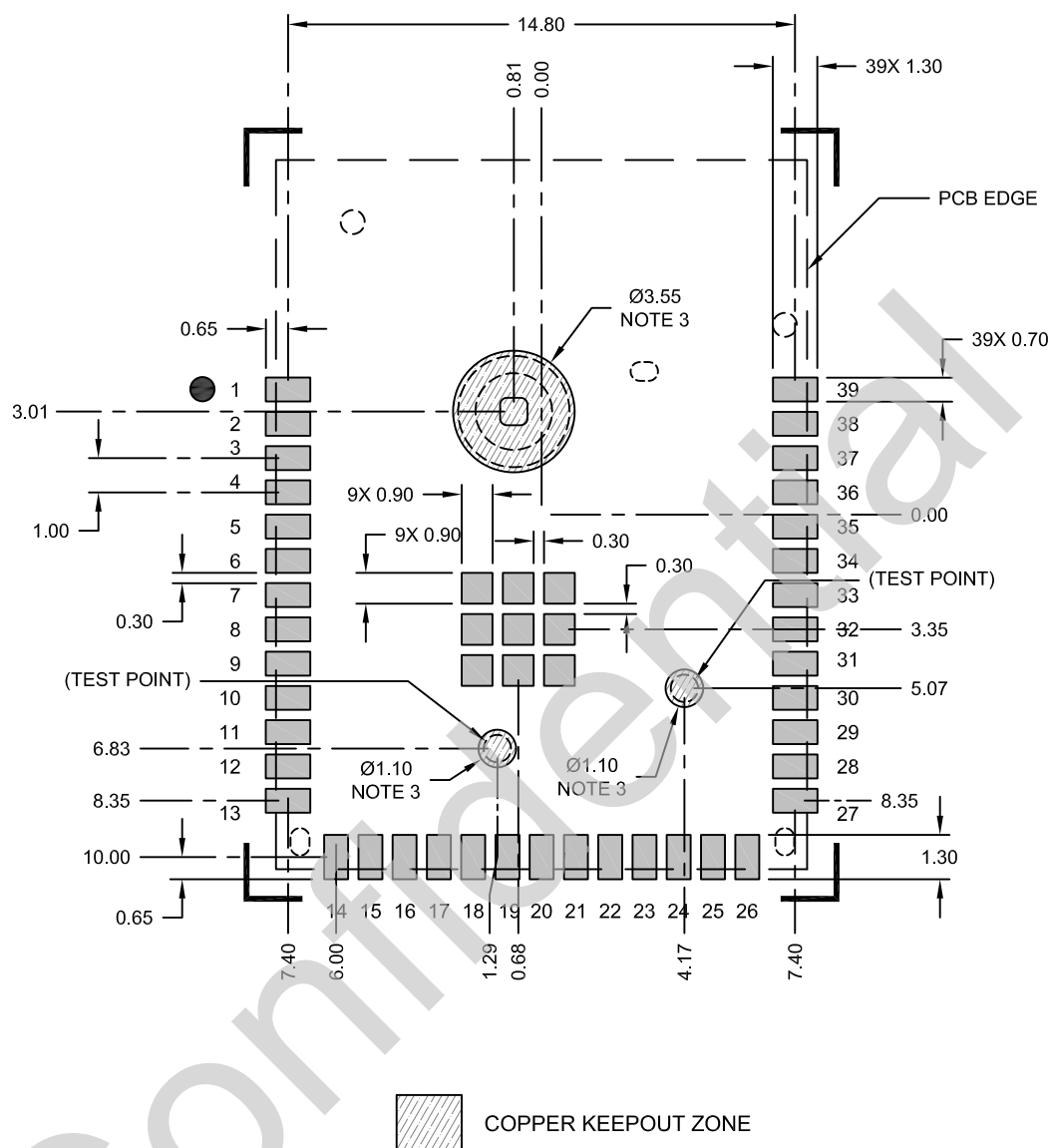
Notes:

1. All dimensions are in millimeters.
2. Keep this area free from all metal, including ground fill.
3. Keep these areas free from routes and exposed copper. Ground fill with solder mask may be placed here.

The following images illustrate the packaging information of the WBZ450, which has 30-lead PCB module (ZRX) -13.4x18.7x2.8 mm body (module).

Figure 4-10. Top, Bottom, End and Side Views of WBZ450 Module

SIDE VIEW

TOP VIEW

END VIEW

BOTTOM VIEW
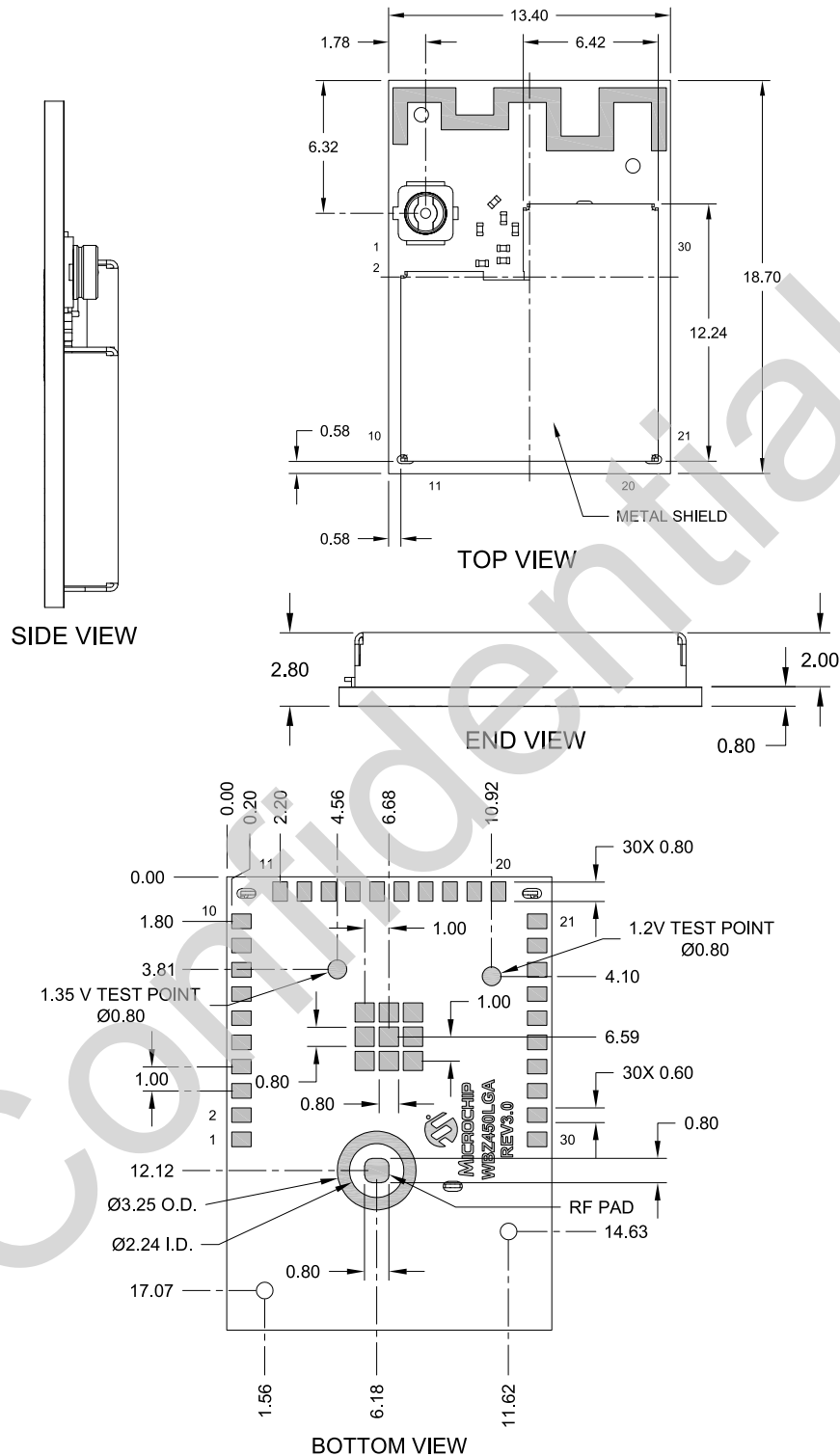
Figure 4-11. WBZ450 Module Package Outline Drawing
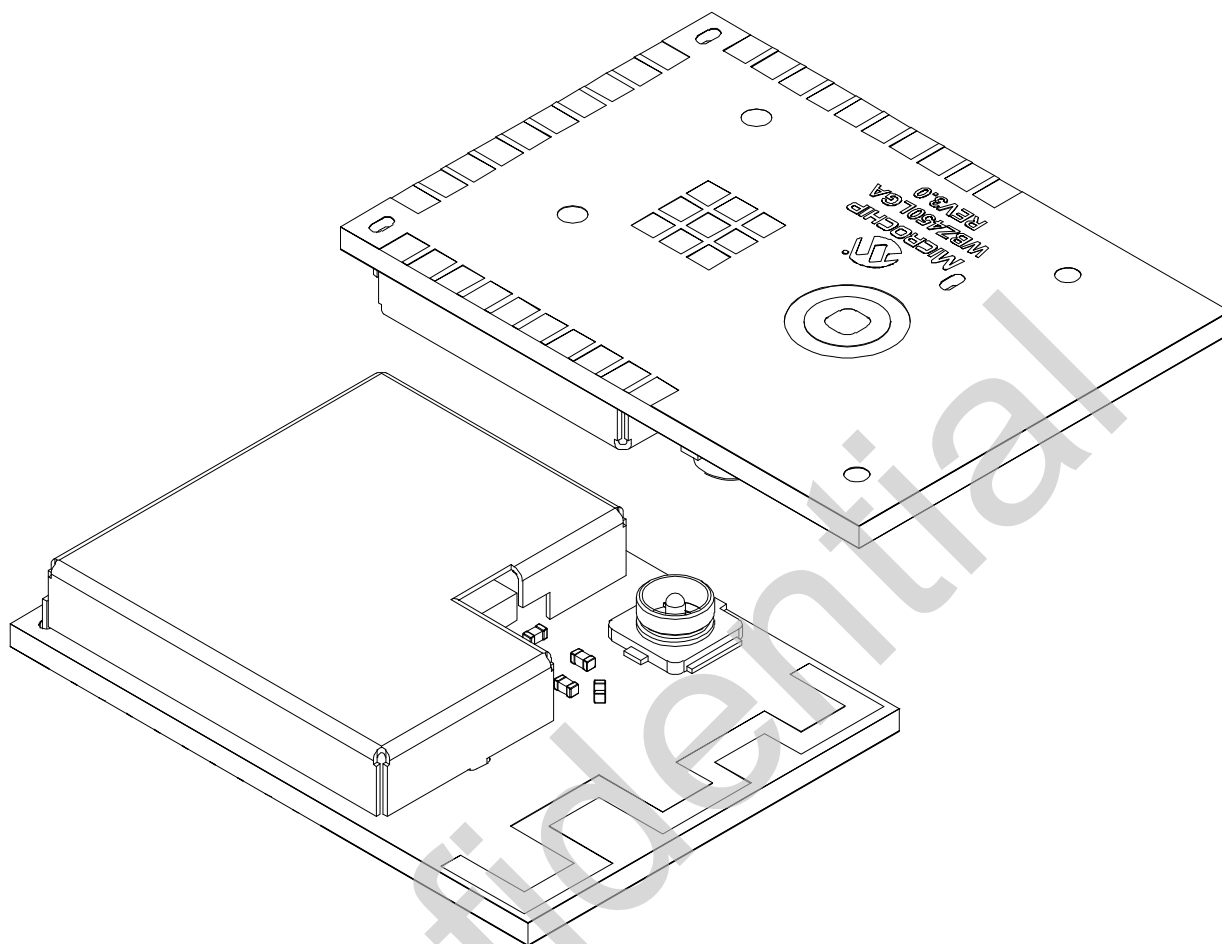
5.   Document Revision History

Revision	Date	Section	Description
A	10/2021	Document	Initial revision

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