PIC32CX-BZ2 Family Silicon Errata and Data Sheet Clarification

PIC32CX-BZ2 Family Errata

The PIC32CX-BZ2 family of devices that you have received conform functionally to the current preliminary Device Data Sheet, except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following table. The silicon issues are summarized in the Table of Contents following this section.

The errata described in this document will be addressed in future revisions of the PIC32CX-BZ2 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. PIC32CX-BZ2 Family Silicon Device Identification

Part Number	Device Identification (DID[31:0])	Revision ID (DID.REVISION[3:0])
		A0
PIC32CX1012BZ25048	0x09B8F053	0x0
PIC32CX1012BZ24032	0x09B0B053	

Note: Refer to the **"Device Service Unit"** chapter in the current advance device data sheet for a detailed information on Device Identification and Revision IDs for your specific device.

Table of Contents

1. Silicon Errata Summary

Table 1-1. Errata Summary

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A0
2.1. Analog-to-Digital Converter (ADC)	Level Trigger	2.1.1	The ADC level trigger does not perform burst conversions in Debug mode.	X
	Scan	2.1.2	The Scan list conversions defined in the ADCCSS1 register will restart without finishing the current scan list and does not generate an EOSRDY bit (ADCCON2[29]) end of scan interrupt status if a new trigger event from the STRGSRC[4:0]bits (ADCCON1[20:16]) trigger source occurs before the scan list completion on the shared ADC2 core.	X
2.2. Clock Reset Unit (CRU)	Peripheral Bus Clocks	2.2.1	The Power-on Reset (POR) value of the PB3 clock is not correct.	X
2.3. Configurable Custom Logic (CCL)	Enable Protected Registers	2.3.1	The SEQCTRLx and LUCTRLx registers are enable-protected by the CTRL.ENABLE bit, whereas they should be enable-protected by the LUTCTRLx.ENABLE bits.	X
	Sequential Logic	2.3.2	LUT output is corrupted after enabling CCL when sequential logic is used.	X
2.4. Device	Vil Input Low Voltage	2.4.1	There is degraded VIL/VIH performance when the GPIO pull-up/pull-down resistors are enabled on PB0, PB1, PB2, PB3,PB4, PB5, PB6, PB8, or PB9. These pins may not be able to recognize a logic low level if the pull-up on that pad is enabled.	X
2.5. Device Service Unit (DSU)	CRC32	2.5.1	DSU CRC32 will not complete when targeting NVM memory space while the NVM cache is disabled.	X
2.6. Direct Memory Access Controller (DMAC)	DMAC in Debug Mode	2.6.1	In debug mode, DMAC does not restart after a debug halt when DBGCTRL.DBGRUN=0.	X
2.7. External Interrupt Controller (EIC)	Edge Detection	2.7.1	When enabling EIC, SYNCBUSY.ENABLE is released before EIC is fully enabled. Edge detection can be done only after three cycles of the selected GCLK (GCLK_EIC or CLK_ULP32K).	X
	Asynchronous Edge Detection	2.7.2	When the asynchronous edge detection is enabled and the system is in Standby mode, only the first edge will be detected. The following edges are ignored until the system wakes up.	X

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Module	Feature	Item Number	Issue Summary	Affected Revisions
				A0
2.8. Event System (EVSYS)	Software Event	2.8.1	BUSYCH flag never resets upon software events in synchronous/resynchronized path modes with event detection on falling edges If a software event occurs when the EVSYS is set in synchronous/resynchronized path modes (CHANNELn.PATH=0x0/0x1) with event detection set on falling edges (CHANNELn.EDGSEL=0x2), the CHSTATUS.BUSYCHn flag will be set but will never come back to 0. It is then impossible to know if the event user for this channel is ready or not to accept new events.	X
	Spurious Overrun	2.8.2	Overrun interrupt flag may be incorrectly set upon software events in synchronous/resynchronized path modes with event detection on both rising and falling edges. If a software event occurs when the EVSYS is set in synchronous/resynchronized path modes (CHANNELn.PATH=0x0/0x1) with event detection set on both rising and falling edges (CHANNELn.EDGSEL=0x3), spurious overrun interrupts may occur (INTFLAG.OVRn).	X
General Purpose Input / Output (GPIO)	GPIO Output Configuration in Deep Sleep and Extreme Deep Sleep	2.9.1	In Deep Sleep and Extreme Deep Sleep Mode GPIO should not be set to output state of pin HIGH. Configuring GPIO state to pin High during Deep Sleep and Extreme Deep Sleep Mode will cause leakage current and potential reliability issues on the Silicon. This issue is only applicable when CPU is in Deep Sleep/ Extreme Deep Sleep Mode and when GPIO is configured as output state pin HIGH	X
2.10. Peripheral Access Controller (PAC)	PAC Protection Error in FREQM	2.101	FREQM reads on the Control B register (FREQM.CTRLB) generate a PAC protection error.	X
	PAC Protection Error in CCL	2.10.2	Writing the Software Reset bit in the Control A register (CTRLASWRST) will trigger a PAC protection error.	X
2.11. Prefetch Cache	CPU Hang Configuration Switch	2.11.1	CPU hang is observed when CHECON.ADRWS configuration switches from1 to 0 and a flash read access. When CHECON.ADRWS is configured to '0' (default is '1'), the cache_adrws will be latched at next clock and if a flash read access happens at the same clock, the system hangs waiting for an internal ack due to the PFM cache miss.	X
2.12. Real-Time Counter (RTC)	Write Corruption	2.12.1	A 8-bit or 16-bit write access for a 32-bit register, or 8-bit write access for a 16-bit register can fail for the following registers: • The COUNT register in COUNT32 mode • The COUNT register in COUNT16 mode • The CLOCK register in CLOCK mode	X
	COUNTSYNC	2.12.2	When COUNTSYNC is enabled, the first COUNT value is not correctly synchronized and therefore it is a wrong value.	X
	Tamper Input Filter	2.12.3	Majority debouncing, as part of RTC tamper detection, does not work, when enabled by setting Debouncer Majority Enable bit CTRLB.DEBMAJ.	X
	Tamper Detection	2.12.4	Upon enabling the RTC, a false tamper detection could be reported by the RTC.	X
	Tamper Detection Timestamp	2.12.5	If an external reset occurs during a tamper detection, the TIMESTAMP register will not be updated when next tamper detection is triggered.	X

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Module	Feature	Item Number	Issue Summary	Affected Revisions
				A0
2.13. Serial Communication Interface (SERCOM)	SERCOM-USART: USART Auto-Baud Mode	2.13.1	In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.	X
	SERCOM-USART: Collision Detection	2.13.2	In USART operating mode with Collision Detection enabled (CTRLB.COLDEN=1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB Clock is lower than the SERCOM Generic Clock.	X
	SERCOM-USART: Debug Mode	2.13.3	In USART operating mode, if DBGCTRL.DBGSTOP=1, data transmission is not halted after entering Debug mode.	X
	SERCOM-USART: 32-bit Extension Mode	2.13.4	When 32-bit Extension mode is enabled and data to be sent is not in multiples of 4 bytes (which means the length counter must be enabled), additional bytes will be sent over the line.	X
	SERCOM-UART: TXINV and RXINV Bits	2.13.5	The TXINV and RXINV bits in the CTRLA register have inverted functionality.	X
	STATUS.CLKHOLD Bit in Master and Slave Modes	2.13.6	The STATUS.CLKHOLD bit in master and slave modes can be written whereas it is a read-only status bit.	X
	SERCOM-I^{2}C: I^{2}C in Slave Mode	2.137	In I^{2}C mode, LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR bits are not cleared when INTFLAG.AMATCH is cleared.	X
	SERCOM-I^{2}C: Slave Mode with DMA	2.13.8	In I^{2}C Slave Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register.	X
	SERCOM-I^{2}C: I^{2}C Slave in DATA32B Mode	2.13.9	When SERCOM is configured as an I^{2}C slave in 32-bit Data Mode (DATA32B=1) and the I^{2}C master reads from the I^{2}C slave (slave transmitter) and outputs its NACK (indicating no more data is needed), the I^{2}C slave still receives a DRDY interrupt.	X
	SERCOM-I^{2}C: Repeated Start	2.13.10	When the Quick command is enabled (CTRLB.QCEN=1), software can issue a repeated Start by writing either CTRLB.CMD or ADDR.ADDR bit fields.	X
	SERCOM-SPI: Data Preload	2.13.11	In SPI Slave mode and with Slave Data Preload Enabled (CTRLB.PLOADEN=1), the first data sent from the slave will be a dummy byte if the master cannot keep the Slave Select (SS) line low until the end of transmission.	X
	SERCOM-SPI: Slave Data Preload	2.13.12	Preloading a new SPI data (CTRLB.PLOADEN = 1) before going into Standby Sleep mode, may lead to extra power consumption.	X
	SERCOM-SPI: Hardware Slave Select Control	2.13.13	When Hardware Slave Select Control is enabled (CTRLB.MSSEN = 1), the Slave Select (SS) pin goes high after.	X
2.14. System Bus	Bus Error Address Checks	2.14.1	When accessing peripherals on the PB-PIC bus, an access beyond the implemented memory region 0x4401_FFFF will cause the CPU to hang waiting for a bus error signal.	X
2.15. System Configuration Registers	CFGCON0 Register	2.15.1	CFGCON0.SWOEN is non-functional, which makes PB7 function as SWO during debugging only.	X
	System Bus QoS	2.15.2	The Power-on Reset values of the CFGPGQOS register sets all bus master QoS values to zero (Background) instead of the required Power-on Reset values.	X

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Module	Feature	Item Number	Issue Summary	Affected Revisions
				A0
2.16. Timer/Counter for Control Applications (TCC)	Re-trigger in RAMP2 Operations	2.16.1	Re-trigger in RAMP2 operations (RAMP2, RAMP2A, RAMP2C) is not supported if a prescaler is used (CTRLA.PRESCALER ! = 0) and the re-trig of the counter is done on the next GCLK (CTRLA.PRESCSYNC = GCLK or CTRLA.PRESCSYNC = RESYNC).	X
	Re-trigger	2.16.2	If a Re-trigger event (EVCTRL.EVACTn = 0x1, RETRIGGER) occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted.	X
	TCC Outputs	2.16.3	TCC0/TCC1 output not working as expected with PPS, output signals not visible on output pins via PPS even though the TCC is working correctly. TCC2 cannot be used to drive external pins.	X
2.17. Timer/Counter (TC)	TC Outputs	2.17.1	TC0/1/2 output not working as expected with PPS, output signals are not visible on output pins via PPS even thought the TC is working correctly. TC3 cannot be used to drive external pins.	X
	ALOCK Feature	2.17.2	ALOCK feature is not functional.	X
2.18. Watchdog Timer (WDT)	Watchdog Counter	2.18.1	When the interval between clearing the watch dog timer (in other words, clearing the Run mode watchdog counter) and the sleep instruction is less than 1 WDT clock cycle, the “Run Mode” watchdog counter is not cleared.	X

Notes:

- Cells with ‘X’ indicates the issue is present in this revision of the silicon.
- Cells with ‘-’ indicates this silicon revision does not exist for this issue.
- The blank cell indicates the issue has been corrected or does not exist in this revision of the silicon.

2. Silicon Errata Issues

The following errata issues apply to the PIC32CX-BZ2 family of devices.

Note:
Cells with an 'X' indicates the issue is present in this revision of the silicon.

Cells with a dash ('-') indicate this silicon revision does not exist for this issue.

Blank cells indicate the issue has been corrected or does not exist in this revision of the silicon.

2.1 Analog-to-Digital Converter (ADC)

2.1.1 Level Trigger

The ADC level trigger does not perform burst conversions in Debug mode.

Workaround:
None.

Affected Silicon Revisions

A0						
X						

2.1.2 Scan

The Scan list conversions defined in the ADCCSS1 register will restart without finishing the current scan list and does not generate an EOSRDY bit (ADCCON2[29]) end of scan interrupt status if a new trigger event from the STRGSRC[4:0]bits (ADCCON1[20:16]) trigger source occurs before the scan list completion on the shared ADC core.

Workaround:
Ensure that the STRGSRC[4:0] bits trigger source repetition rate.

Affected Silicon Revisions

A0						
X						

2.2 Clock Reset Unit (CRU)

2.2.1 Peripheral Bus Clocks

The Power-on Reset value of the PB3 clock is not correct.

Workaround:
Use Microchip provided SDK and boot loader. This software will initialize the CRU.PB3DIV register to the data sheet specified default value. If using third-party tools and other custom developed software, set this register to the data sheet default value of 0x0000_8809.

Affected Silicon Revisions

A0						
X						

2.3 Configurable Custom Logic (CCL)

2.3.1 Enable Protected Registers

The SEQCTRLx and LUCTRLx registers are enable-protected by the CTRL.ENABLE bit, whereas they must be enable-protected by the LUTCTRLx.ENABLE bits.

Workaround:
None.

Affected Silicon Revisions

A0						
X						

2.3.2 Sequential Logic

LUT Output is corrupted after enabling CCL when sequential logic is used.

Workaround:
Write the CTRL register twice when enabling the CCL.

Affected Silicon Revisions

A0						
X						

2.4 Device

2.4.1 Vil Input Low Voltage

There is degraded VIL/VIH performance when the GPIO pull-up/pull-down resistors are enabled on PB0, PB1, PB2, PB3,PB4, PB5, PB6, PB8, or PB9. These pins may not be able to recognize a logic low level if the pull-up on that pad is enabled.

Workaround:
If using PB0, PB1, PB2, PB3,PB4, PB5, PB6, PB8, or PB9 for GPIO, do not enable pull-up or pull-down, use external resistors.

Affected Silicon Revisions

A0						
X						

2.5 Device Service Unit (DSU)

2.5.1 CRC32

The DSU CRC32 will not complete when targeting NVM memory space while the NVM cache is disabled.

Workaround:
Be sure to always enable the NVM cache when performing a DSU CRC32 request targeting the NVM memory space.

Affected Silicon Revisions

A0						
X						

2.6 Direct Memory Access Controller (DMAC)

2.6.1 DMAC in Debug Mode

In Debug mode, DMAC does not restart after a debug halt when DBGCTRL.DBGRUN = 0.

Workaround:
Set DBGCTRL.DBGRUN to one so that the DMAC continues normal operation when the CPU is halted by an external debugger.

Affected Silicon Revisions

A0						
X						

2.7 External Interrupt Controller (EIC)

2.7.1 Edge Detection

When enabling EIC, SYNCBUSY.ENABLE bit resets before EIC is fully enabled. Edge detection can be done only after three cycles of the selected GCLK (GCLK_EIC or CLK_ULP32K).

Workaround:
None.

Affected Silicon Revisions

A0						
X						

2.7.2 Asynchronous Edge Detection

When the asynchronous edge detection is enabled and the system is in Standby mode, only the first edge will be detected. The following edges are ignored until the system wakes up.

Workaround:
Use the asynchronous edge detection with debouncer enabled. It is recommended to set the DPRESCALER.PRESCALER and DPRESCALER.TICKON to have the lowest frequency possible. To reduce the

power consumption, set the EIC GCLK frequency as low as possible or select the ULP32K clock (EIC CTRLA.CKSEL set).

Affected Silicon Revisions

A0						
X						

2.8 Event System (EVSYS)

2.8.1 Software Event

BUSYCH flag never resets upon software events in synchronous/resynchronized path modes with event detection on falling edges

If a software event occurs when the EVSYS is set in synchronous/resynchronized path modes (CHANNELn.PATH=0x0/0x1) with event detection set on falling edges (CHANNELn.EDGSEL=0x2), the CHSTATUS.BUSYCHn flag will be set but will never come back to 0. It is then impossible to know if the event user for this channel is ready or not to accept new events.

Workaround:
Generate software events for this user through a dedicated channel configured with event detection set on rising edges (CHANNELn.EDGSEL=0x1).

Affected Silicon Revisions

A0						
X						

2.8.2 Spurious Overrun

Overrun interrupt flag may be incorrectly set upon software events in synchronous/resynchronized path modes with event detection on both rising and falling edges.

If a software event occurs when the EVSYS is set in synchronous/resynchronized path modes (CHANNELn.PATH=0x0/0x1) with event detection set on both rising and falling edges (CHANNELn.EDGSEL=0x3), spurious overrun interrupts may occur (INTFLAG.OVRn).

Workaround:
Generate software events for the event user through a dedicated channel configured with even detection set on rising edges (CHANNELn.EDGSEL=0x1).

Affected Silicon Revisions

A0						
X						

2.9 General Purpose Input / Output (GPIO)

2.9.1 GPIO Output Configuration in Deep Sleep and Extreme Deep Sleep

In Deep Sleep and Extreme Deep Sleep Mode GPIO should not be set to output state of pin HIGH.

Configuring GPIO state to pin High during Deep Sleep and Extreme Deep Sleep Mode will cause leakage current and potential reliability issues on the Silicon.

This issue is only applicable when CPU is in Deep Sleep/Extreme Deep Sleep Mode and when GPIO is configured as output state pin HIGH

Workaround:
None

Affected Silicon Revisions

A0						
X						

2.10 Peripheral Access Controller (PAC)

2.10.1 PAC Protection Error in FREQM

FREQM reads on the Control B register (FREQM.CTRLB) generate a PAC protection error.

Workaround:
None.

Affected Silicon Revisions

A0						
X						

2.10.2 PAC Protection Error in CCL

Writing the Software Reset bit in the Control A register (CTRLASWRST) will trigger a PAC protection error.

Workaround:
Clear the CCL PAC error each time a CCL software reset is executed.

Affected Silicon Revisions

A0						
X						

2.11 Prefetch Cache

2.11.1 CPU Hang Configuration Switch

CPU hang is observed when CHECON.ADRWS configuration switches from1 to 0 and a flash read access.

When CHECON.ADRWS is configured to '0' (default is '1'), the cache_adrws will be latched at next clock and if a flash read access happens at the same clock, the system hangs waiting for an internal ack due to the PFM cache miss.

Workaround:
Execute the CHECON configuration from SRAM (at the very beginning of System Initialization) until the configuration is done and resume execution from Flash after configuration is set.

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Affected Silicon Revisions

A0						
X						

2.12 Real-Time Counter (RTC)

2.12.1 Write Corruption

A 8-bit or 16-bit write access for a 32-bit register, or 8-bit write access for a 16-bit register can fail for the following registers:

- COUNT register in COUNT32 mode
- COUNT register in COUNT16 mode
- CLOCK register in CLOCK mode

Workaround:
Write the registers with:

- A 32-bit write access for COUNT register in COUNT32 mode, CLOCK register in CLOCK mode
- A 16-bit write access for the COUNT register in COUNT16 mode

Affected Silicon Revisions

A0						
X						

2.12.2 COUNTSYNC

When COUNTSYNC is enabled, the first COUNT value is not correctly synchronized and thus it is a wrong value.

Workaround:
After enabling COUNTSYNC, read the COUNT register until its value is changed when compared to its first value read. After this, all consequent value read from the COUNT register is valid.

Affected Silicon Revisions

A0						
X						

2.12.3 Tamper Input Filter

Majority debouncing, as part of RTC tamper detection, does not work when enabled by setting the Debouncer Majority Enable bit, CTRLB.DEBMAJ.

Workaround:
None.

Affected Silicon Revisions

A0						
X						

2.12.4 Tamper Detection

Upon enabling the RTC tamper detection feature, a false tamper detection can be reported by the RTC.

Workaround:
Use any one of the following workarounds:

- **Workaround 1**: Configure TAMPER detection to ONLY falling edge.
- **Workaround 2**: If the user software has to use TAMPER detection as rising edge, it must ignore the first tamper interrupt generated after enabling the RTC tamper detection.

Affected Silicon Revisions

A0						
X						

2.12.5 Tamper Detection Timestamp

If an external reset occurs during a tamper detection, the TIMESTAMP register will not be updated when next tamper detection is triggered.

Workaround:
Enable RTC tamper interrupt and copy the timestamp from the RTC CLOCK COUNT register to one of the following destinations:

- SRAM
- GPx register in RTC
- BKUPx register in RTC

Affected Silicon Revisions

A0						
X						

2.13 Serial Communication Interface (SERCOM)

2.13.1 SERCOM-USART: Auto-Baud Mode

In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.

Workaround:
None.

Affected Silicon Revisions

A0						
X						

2.13.2 SERCOM-USART: Collision Detection

In USART operating mode with Collision Detection enabled (CTRLB.COLDEN = 1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB Clock is lower than the SERCOM Generic Clock.

Workaround:
The SERCOM APB clock must always be higher than the SERCOM Generic Clock to support collision detection. .

Affected Silicon Revisions

A0						
X						

2.13.3 SERCOM-USART: Debug Mode

In USART operating mode, if DBGCTRL.DBGSTOP = 1, data transmission is not halted after entering Debug mode.

Workaround:
None.

Affected Silicon Revisions

A0						
X						

2.13.4 SERCOM-USART: 32-bit Extension Mode

When 32-bit Extension mode is enabled and data to be sent is not in multiples of 4 bytes, which means the length counter must be enabled, and additional bytes will be sent over the line.

Workaround:
Use any one of the following workarounds:

1. Write the Inter-Character Spacing bits (CTRLC.ICSPACE) to a non-zero-value.
2. Do not use length counter in firmware by keeping the data to be sent is in multiples of 4 bytes.

Affected Silicon Revisions

A0						
X						

2.13.5 SERCOM-UART: TXINV and RXINV Bits

The TXINV and RXINV bits in CTRLA are interchanged. TXINV controls the RX signal inversion and RXINV controls the TX signal inversion.

Workaround:
In software interpret the TXINV bit as a functionality of RXINV, and conversely, interpret the RXINV bit as a functionality of TXINV.

Affected Silicon Revisions

A0						
X						

2.13.6 STATUS.CLKHOLD Bit in Master and Slave Modes

The STATUS.CLKHOLD bit in master and slave modes can be written even though it is specified as a read-only status bit.

Workaround:
Do not clear STATUS.CLKHOLD bit to preserve the current clock hold state.

Affected Silicon Revisions

A0						
X						

2.13.7 SERCOM-I²C: I²C in Slave Mode

In I²C mode, LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR bits are not cleared when INTFLAG.AMATCH is cleared.

Workaround:
Manually clear status bits LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR by writing these bits to 1 when set.

Affected Silicon Revisions

A0						
X						

2.13.8 SERCOM-I²C: Slave Mode with DMA

In I²C Slave Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register. Because a NACK was received, the transfer on the I ²C bus will not occur causing the loss of this data.

Workaround:
Configure the DMA transfer size to the number of data to be received by the I²C master. DMA cannot be used if the number of data to be received by the master is not known..

Affected Silicon Revisions

A0						
X						

2.13.9 SERCOM-I²C: I²C Slave in DATA32B Mode

When SERCOM is configured as an I²C slave in 32-bit Data Mode (DATA32B = 1) and the I²C master reads from the I²C slave (slave transmitter) and outputs its NACK (indicating no more data is needed), the I²C slave still receives a DRDY interrupt.

If the CPU does not write a new data to the I²C slave DATA register, I²C slave will pull SDA line, which will result in stalling the bus permanently.

Workaround:

1. Write a dummy data to data register when a NACK is received from the master.
2. Use command #2 (SERCOMx->I2CS.CTRLB.bit.CMD = 2) when a NACK is received from the master.

Important: Because STATUS.RXNACK always indicates the last received ACK, to determine when a NACK is received from the I²C master, the I²C slave software needs to consider I2CS.STATUS.RXNACK only on the second DRDY interrupt after receiving the AMATCH interrupt.

Affected Silicon Revisions

A0						
X						

2.13.10 SERCOM-I²C: Repeated Start

When the Quick command is enabled (CTRLB.QCEN = 1), software can issue a repeated Start by writing either CTRLB.CMD or ADDR.ADDR bit fields. If in these conditions, SCL Stretch Mode is CTRLA.SCLSM = 1, a bus error will be generated.

Workaround:
Use Quick Command mode (CTRLB.QCEN = 1) only if SCL Stretch Mode is CTRLA.SCLSM = 0.

Affected Silicon Revisions

A0						
X						

2.13.11 SERCOM-SPI: Data Preload

In SPI Slave mode and with Slave Data Preload Enabled (CTRLB.PLOADEN = 1), the first data sent from the slave will be a dummy byte if the master cannot keep the Slave Select (SS) line low until the end of transmission.

Workaround:
In SPI Slave mode, the Slave Select pin (SS) must be kept low by the master until the end of the transmission if the Slave Data Preload feature is used (CTRLB.PLOADEN = 1).

Affected Silicon Revisions

A0						
X						

2.13.12 SERCOM-SPI: Slave Data Preload

Preloading a new SPI data (CTRLB.PLOADEN = 1) before going into Standby Sleep mode, may lead to extra power consumption.

Workaround:
None

Affected Silicon Revisions

A0						
X						

2.13.13 SERCOM-SPI: Hardware Slave Select Control

When Hardware Slave Select Control is enabled (CTRLB.MSSEN = 1), the Slave Select (SS) pin goes high after.

Workaround:
Set CTRLB.MSSEN = 0 and handle the Slave Select (SS) pin by software.

Affected Silicon Revisions

A0						
X						

2.14 System Bus

2.14.1 Bus Error Address Checks

When accessing peripherals on the PB-PIC bus, an access beyond the implemented memory region 0x4401_FFFF causes the CPU to hang waiting for a bus error signal.

Workaround:
Use Microchip provided peripheral drivers from Harmony 3 and Microchip provided SDK. This software will not generate addresses outside the implemented regions. If using third-party tools and other custom developed software, do not create accesses outside this region or an MCU reset will be required to recover.

Affected Silicon Revisions

A0						
X						

2.15 System Configuration Registers

2.15.1 CFGCON0 Registers

CFGCON0.SWOEN is non-functional, which makes PB7 function as SWO during debugging only. PB7 works normally when not doing debug.

Workaround:
Do not use PB7 as GPIO while debugging.

Affected Silicon Revisions

A0						
X						

2.15.2 System Bus QoS

The Power-on Reset values of the CFGPGQOS register sets all bus master QoS values to zero (Background) instead of the required Power-on Reset values.

Workaround:
Use Microchip provided SDK and bootloader. This software will initialize the CFGPGQOS register to the data sheet specified default value. If using third-party tools and other custom developed software, set this register to the data sheet default value of 0xE040_004C.

Affected Silicon Revisions

A0						
X						

2.16 Timer/Counter for Control Applications (TCC)

2.16.1 Re-trigger in RAMP2 Operations

Re-trigger in RAMP2 operations (RAMP2, RAMP2A, RAMP2C) is not supported if a prescaler is used (CTRLA.PRESCALER ! = 0) and the re-trig of the counter is done on the next GCLK (CTRLA.PRESCSYNC = GCLK or CTRLA.PRESCSYNC = RESYNC).

Workaround:
Configure the re-trigger of the counter on the next prescaler clock (CTRLA.PRESCSYNC = PRESC).

Affected Silicon Revisions

A0						
X						

2.16.2 Re-trigger

If a Re-trigger event (EVCTRL.EVACTn = 0x1, RETRIGGER) occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted.

Workaround:
Use two channels to store their two successive (n and n+1) CC register values and combine their related waveform outputs to make signal redundancy.

Affected Silicon Revisions

A0						
X						

2.16.3 TCC Outputs

TCC0/TCC1 output not working as expected with PPS, output signals not visible on output pins via PPS even though the TCC is working correctly. TCC2 cannot be used to drive external pins.

Workaround: Use CCL module to route TCC outputs
Use CCL module to output up to 2 TCCx_WO[n] signals on CCL0_OUT and CCL1_OUT using PPS to the desired pins.

The required configuration in CCL1/2:

- CCL.CTRL.ENABLE = 1, To enable CCL
- CCL.LUTCTRLx.ENABLE = 1, To enable LUT in CCL
- CCL.LUTCTRLx.INSELx = 8, To select TCC as input source
- CCL.LUTCTRLx.TRUTH, To match the toggle of TCC
  - CCL.LUTCTRLx.TRUTH = 0xAA, to match toggle on WO[0]
  - CCL.LUTCTRLx.TRUTH = 0xCC, to match toggle on WO[1]
  - CCL.LUTCTRLx.TRUTH = 0xF0, to match toggle on WO[2]
- CFGCON1.CCL_OE = 1, To enable CCL output onto PADs

Then configure PPS for CCL output to desired pin.
Note: CCL0_OUT allows one instance of TCC0_WO[n] and CCL1_OUT allow one instance of TCC1_WO[n].

Affected Silicon Revisions

A0						
X						

2.17 Timer/Counter (TC)

2.17.1 TC Outputs

TC0/1/2 output not working as expected with PPS, output signals are not visible on output pins via PPS even though the TC is working correctly. TC3 cannot be used to drive external pins.

Workaround: Set COPENx and CAPTENx before enabling/re-enabling the Timer Counter
Set TC.CTRLA.COPENx = 1 and TC.CTRLA.CAPTENx = 1 before enabling/re-enabling the Timer Counter.

- Configure PPS for output to desired pin
- Initialize Timer Counter
- TC.CTRLA.COPENx = 1
- TC.CTRLA.CAPTENx = 1
- Start/Enable Timer Counter

Affected Silicon Revisions

A0						
X						

2.17.2 ALOCK Feature

ALOCK feature is not functional.

Workaround:
None

Affected Silicon Revisions

A0						
X						

2.18 Watchdog Timer (WDT)

2.18.1 Watchdog Counter

When the interval between clearing the watch dog timer (in other words, clearing the Run mode watchdog counter) and the sleep instruction is less than 1 WDT clock cycle, the “Run Mode” watchdog counter is not cleared. When using LPRC as clock source, the interval is 1 LPRC clock. Because watchdog timer is in LPRC domain, which is much slower than CPU clock, the sleep instruction is executed even before the “Run mode” watch dog counter is cleared. Hence, the “Run mode” watchdog counter remains frozen to its last count instead of clearing to 0.

While in sleep mode, the “sleep mode” watchdog counter is incrementing and at the end of the WDTPS, it generates an NMI which causes the CPU to wake up.

After wake up, the user would expect that since they cleared the WDT just before going to sleep, they have an entire WDT period available to them before they have to clear WDT again. But since the “Run mode” counter was not cleared before going into sleep, the WDT reset would occur earlier than expected.

Workaround (either or both can be used):

1. Add a delay of more than 1 WDT Clock (LPRC clock), between clearing of the WDT and execution of sleep instruction.
2. Execute the WDT clear instruction as soon as the CPU wakes up.

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Affected Silicon Revisions

A0						
X						

3. Document Revision History

Revision	Date	Section	Description
A	02/2022	Document	Initial revision

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