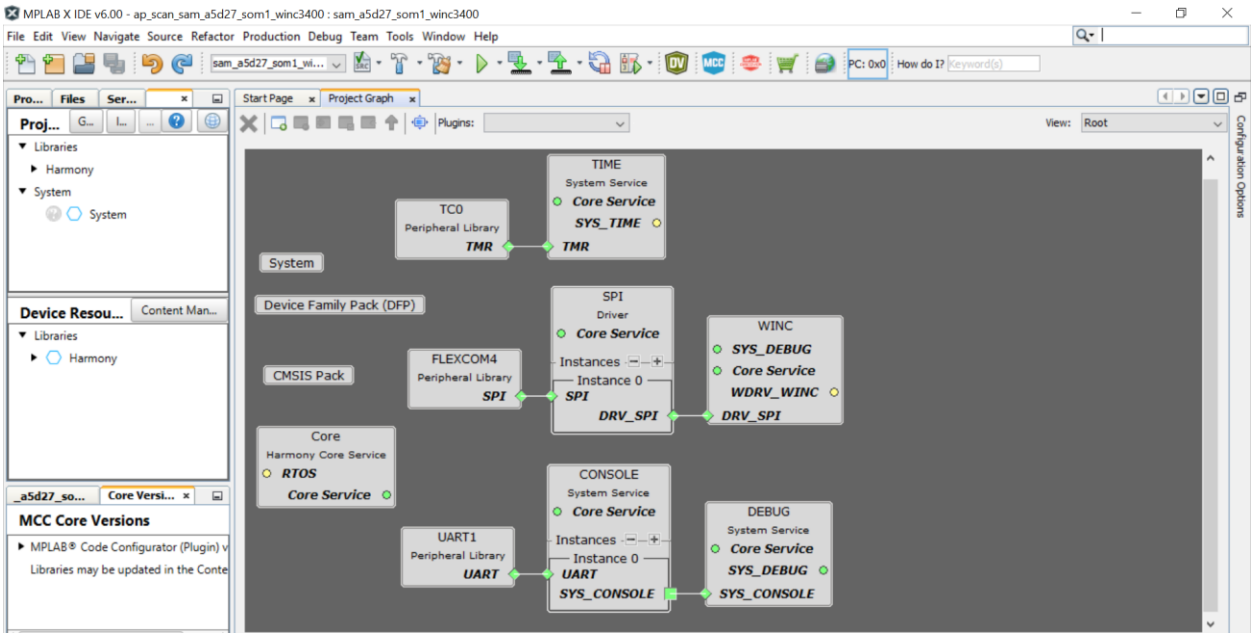
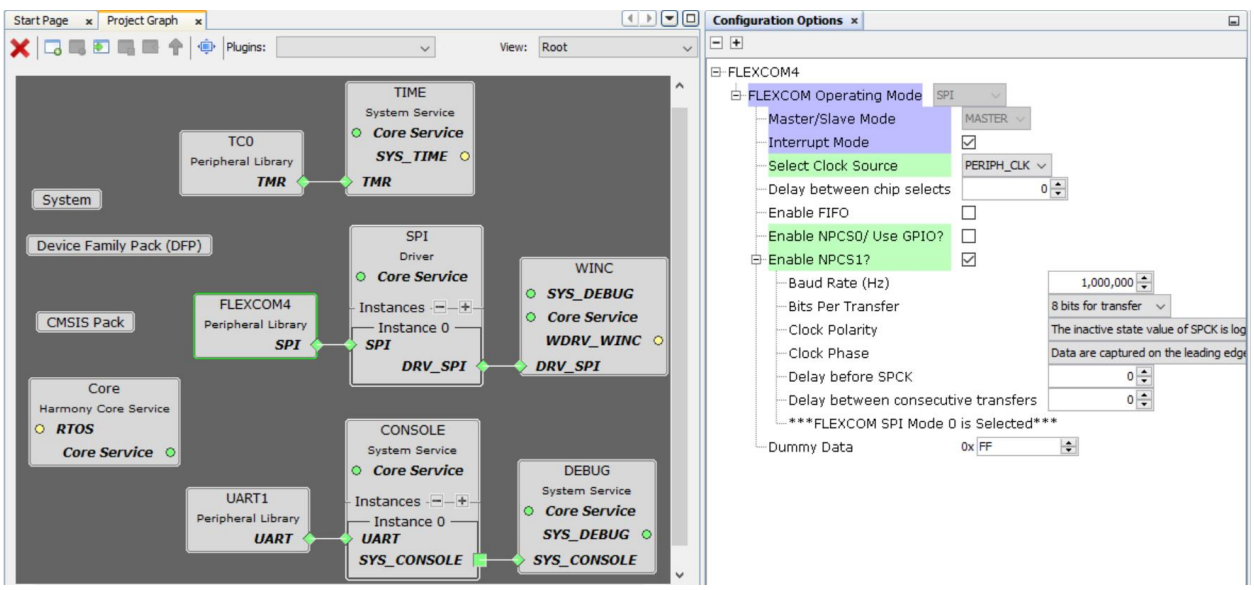
WINC Sample Applications Quick Configurations Guide

1. ap_scan Application MCC Configuration

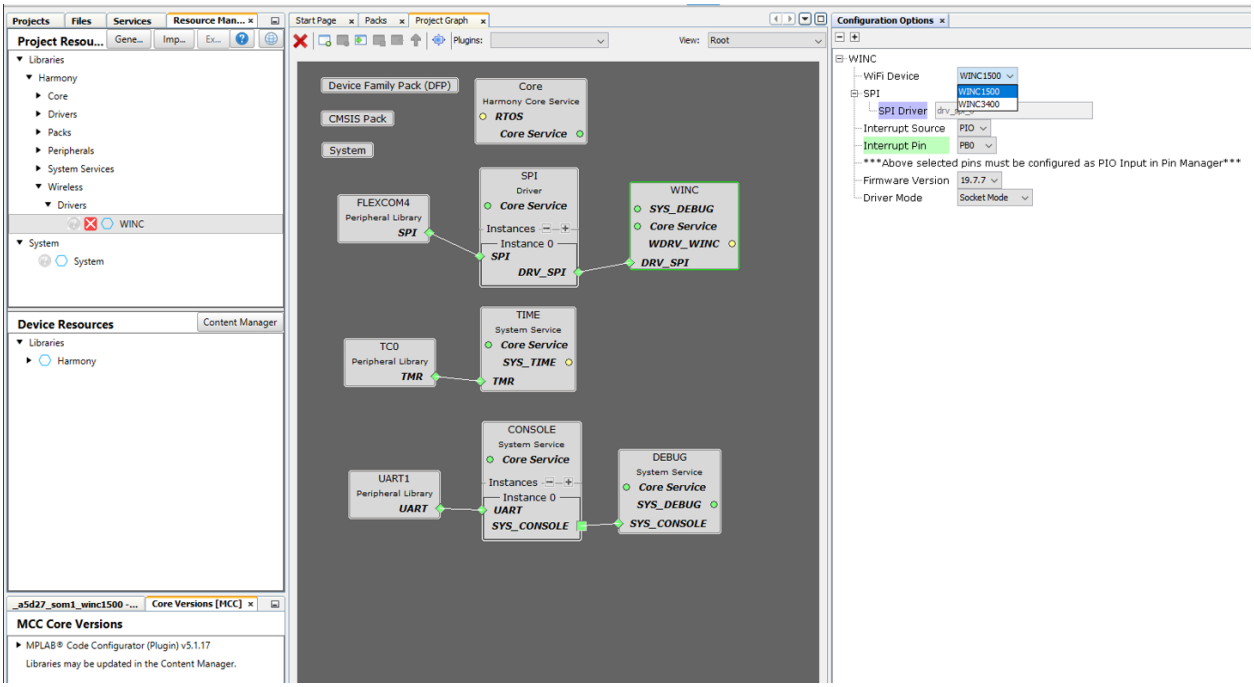
Project Graph

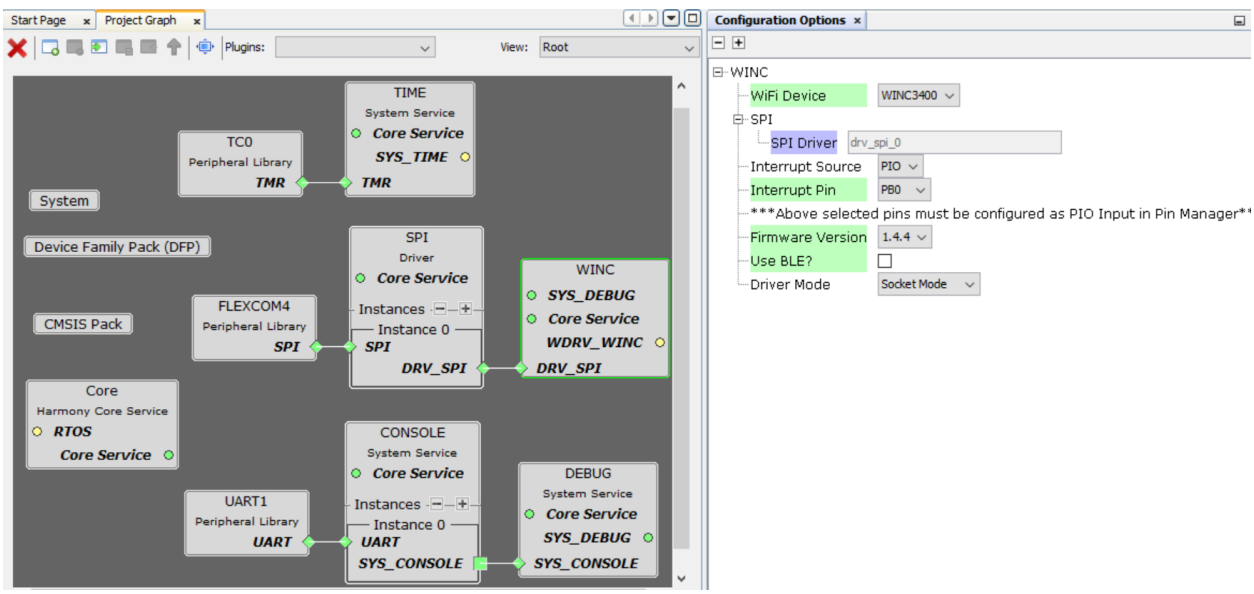


FLEXCOM4_SPI Configuration



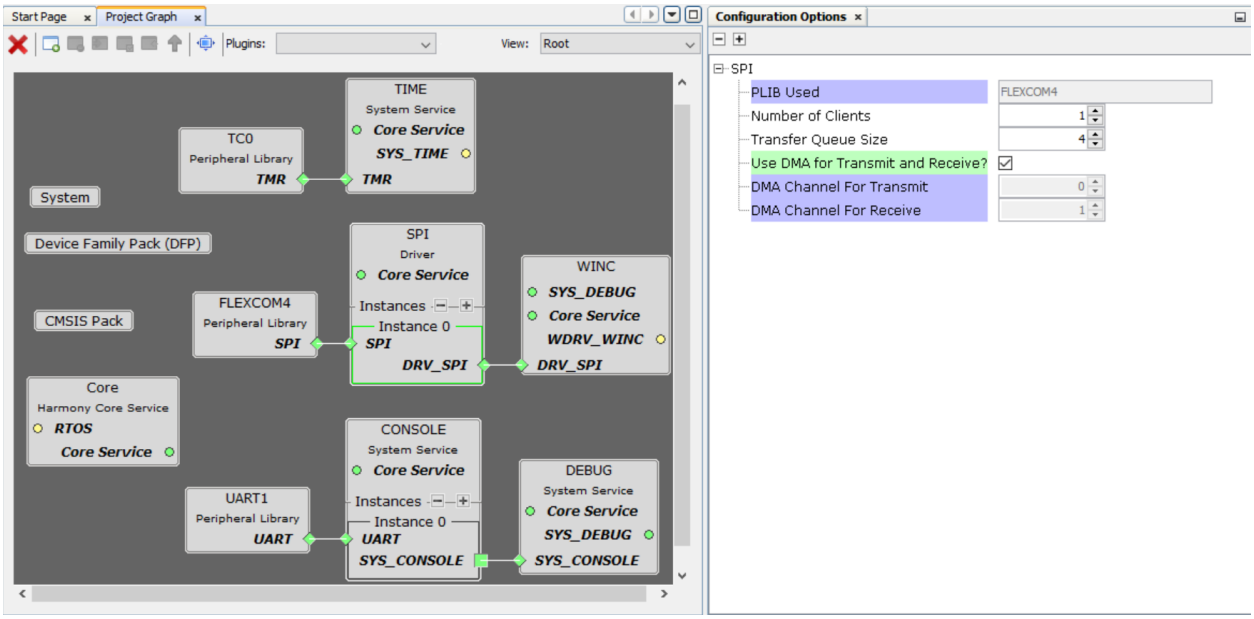
WINC Driver Configuration



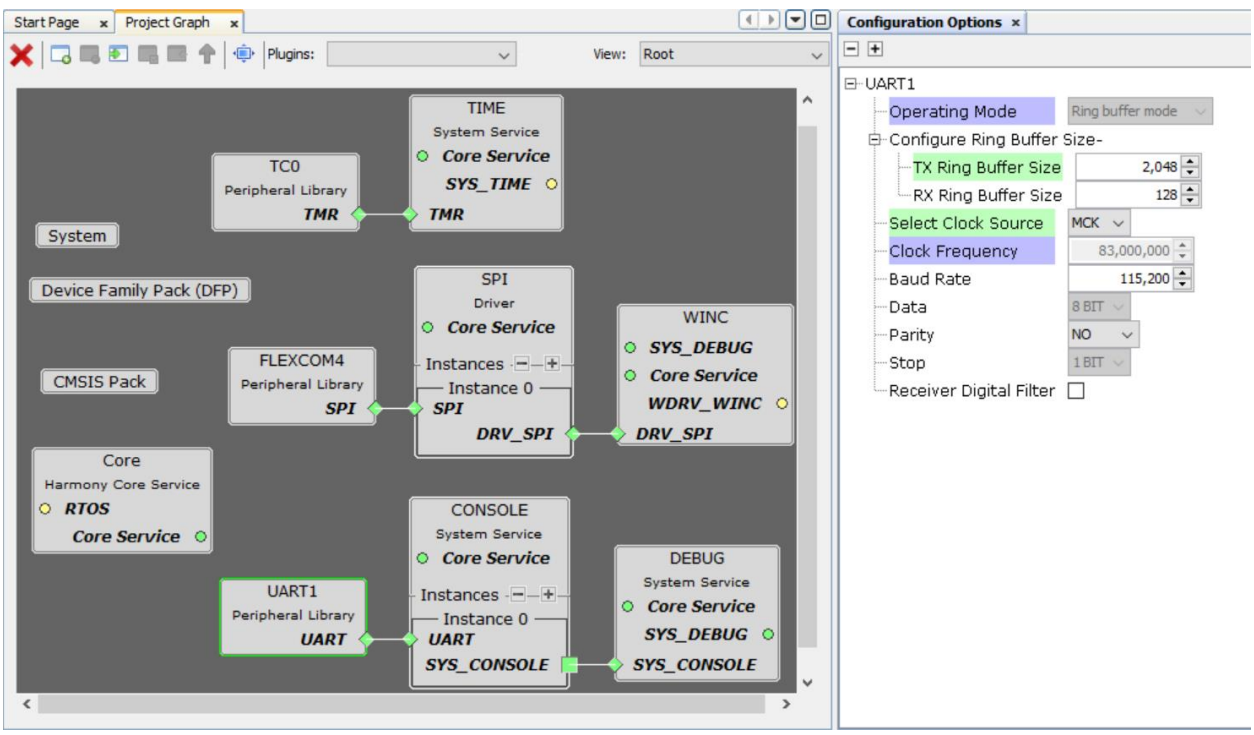


Note: Select WiFi device and its appropriate Firmware version.

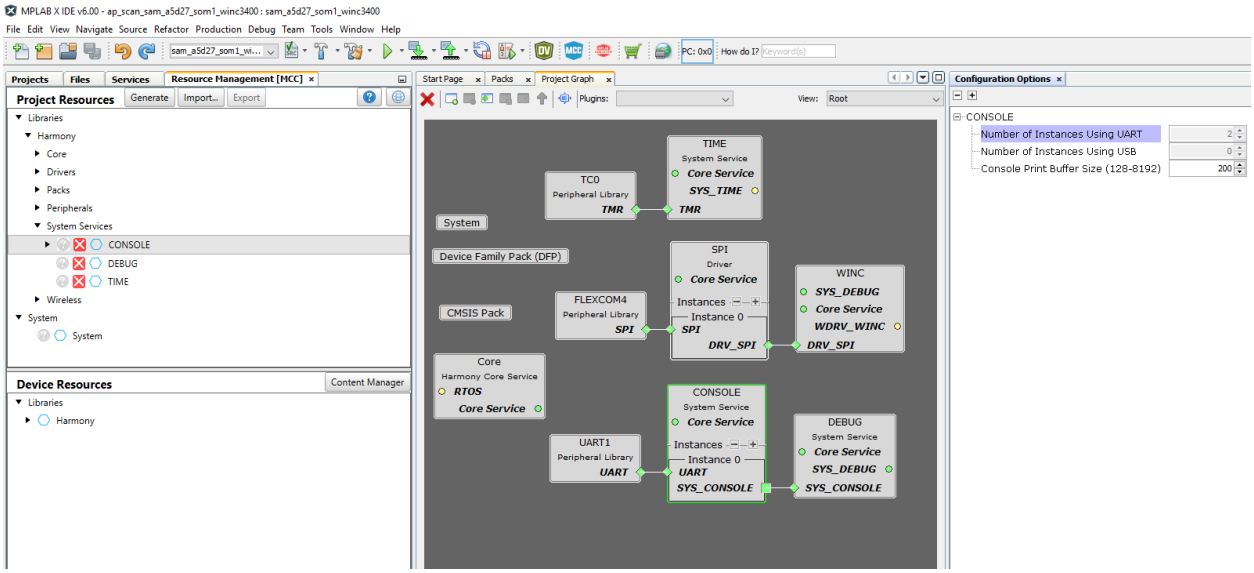
SPI Driver



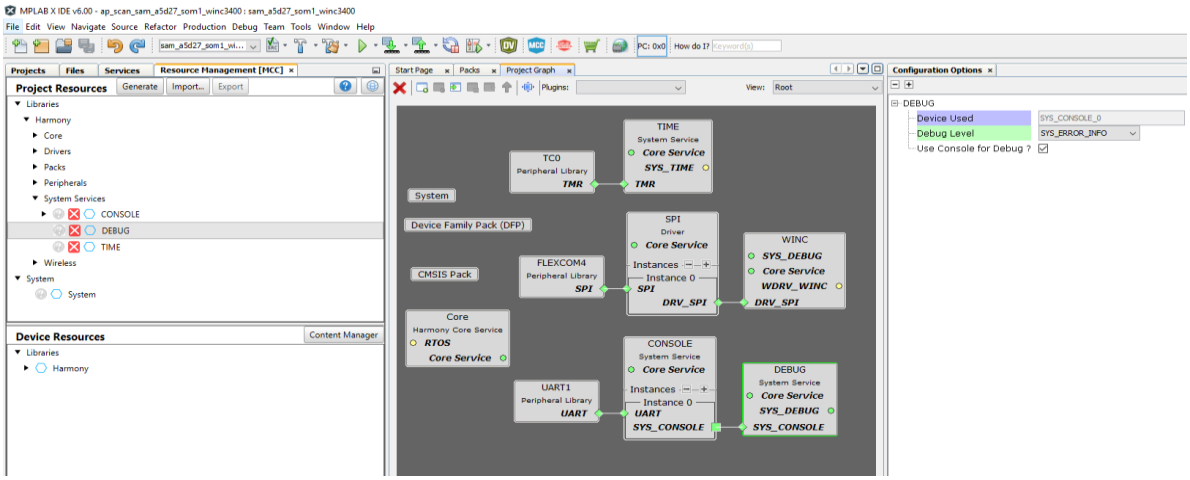
UART(UART1)



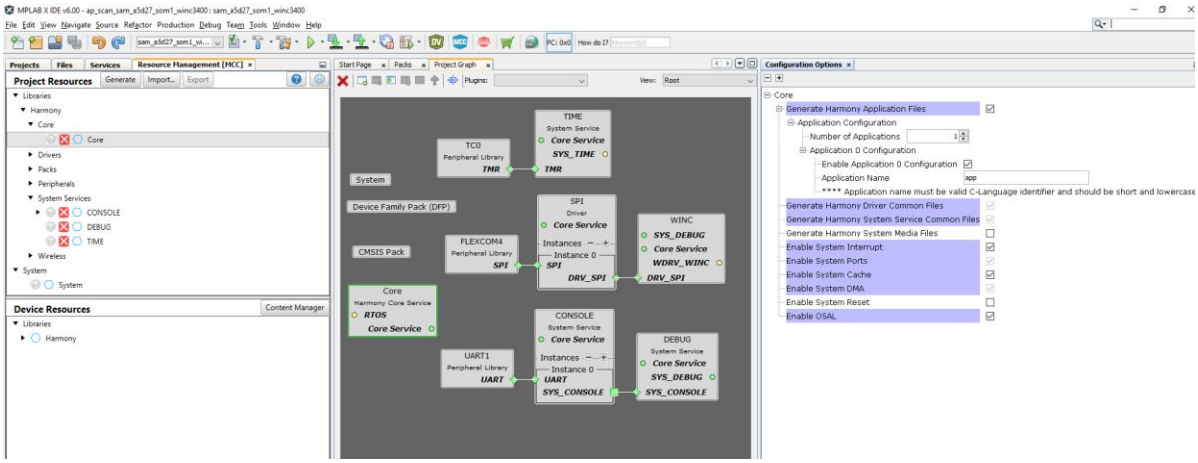
Console



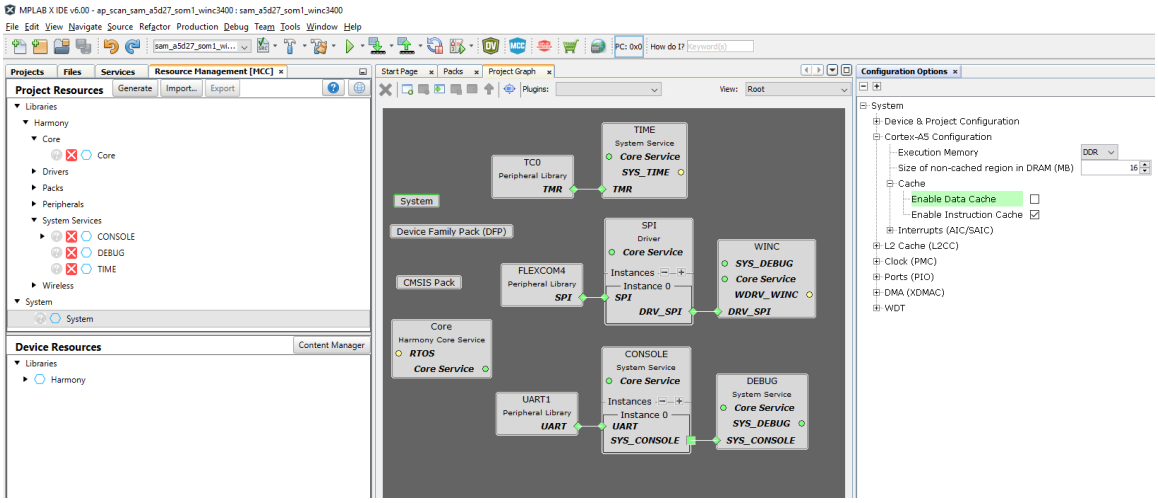
Debug



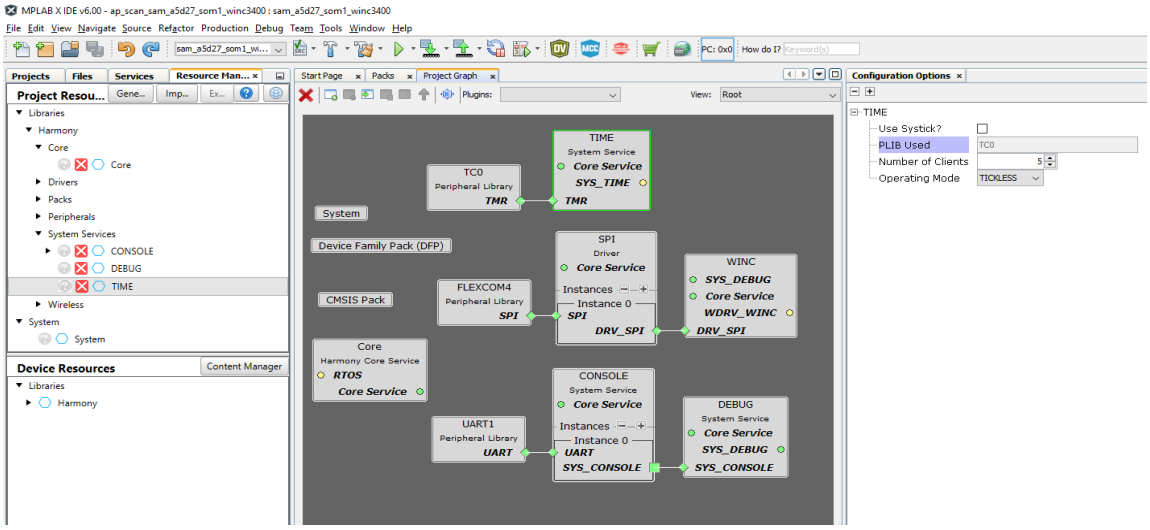
Core



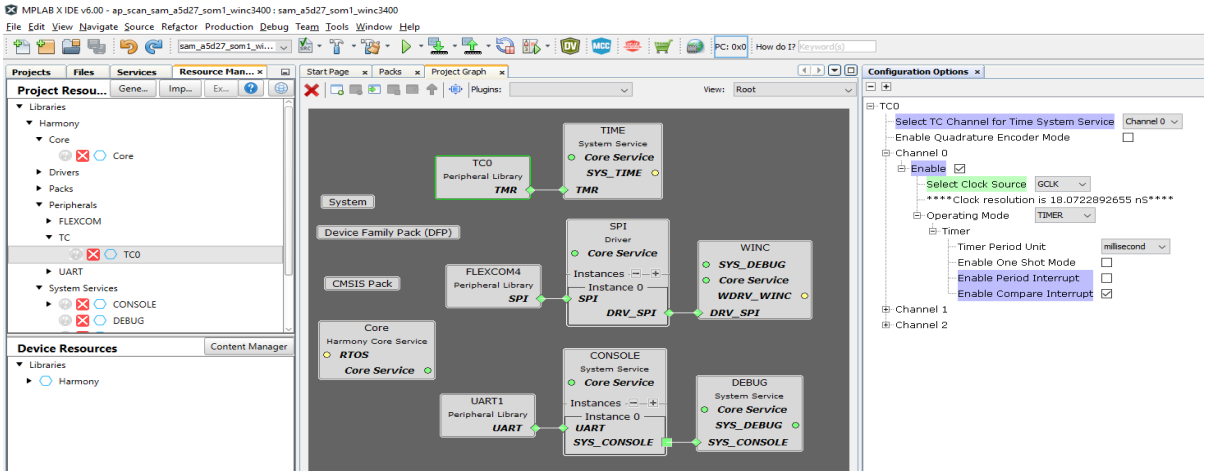
System



Time



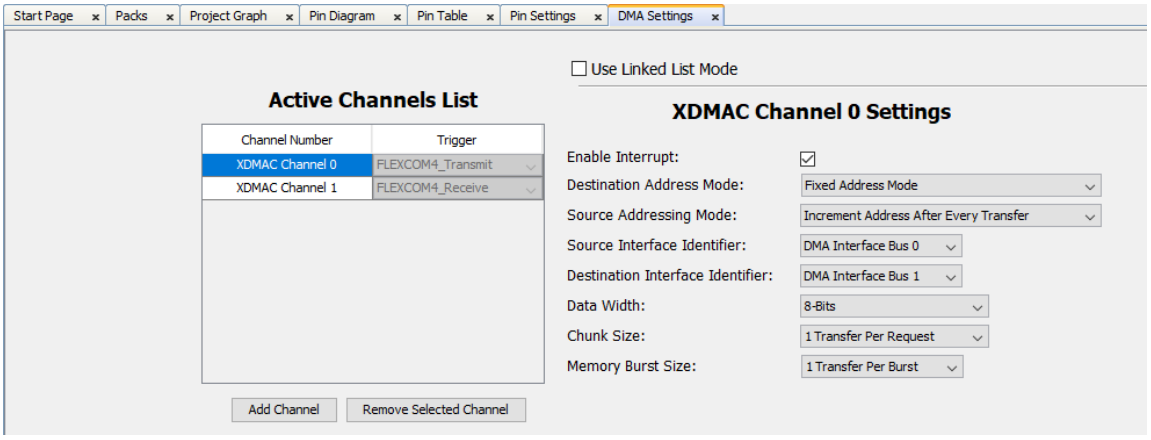
TC0

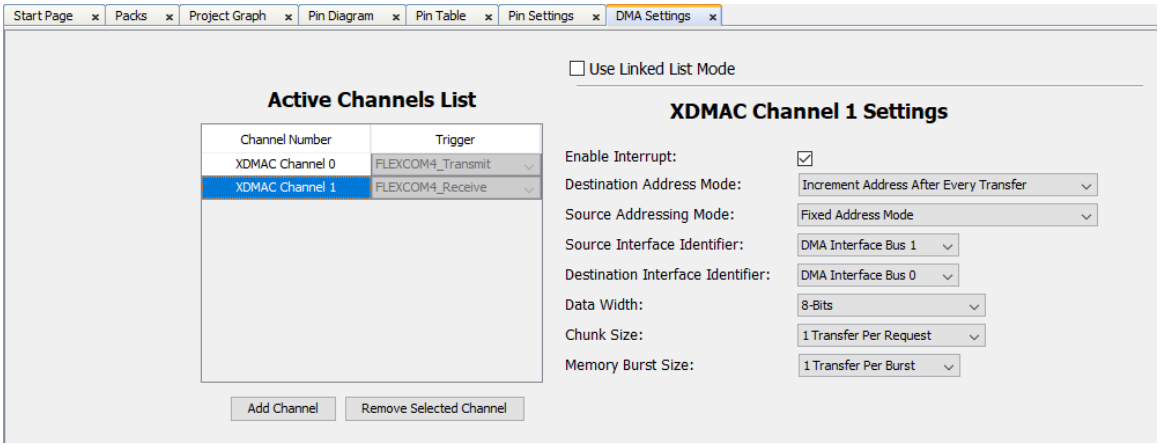


PIN Configuration

Pin Number	Pin ID	Custom Name	Function	Direction	Latch	Open Drain	PIO Interrupt	Pull Up	Pull Down	Drive Strength	Glitch/Debounce Filter
F6	PC28		FLEXCOM4_IO0	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
B9	PC29		FLEXCOM4_IO1	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
E6	PC30		FLEXCOM4_IO2	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
E7	PD0		FLEXCOM4_IO4	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
C7	PB2	WDRV_WINC_RESETN	GPIO	Out	High	☐	Disabled	☐	☐	Low drive	Disabled
F5	PB0	GPIO_PB0	GPIO	In	n/a	☐	Falling Edge	☑	☐	Low drive	Disabled
L5	PD25	WDRV_WINC_CHIP_EN	GPIO	Out	High	☐	Disabled	☐	☐	Low drive	Disabled
J1	PD3		UART1_UTXD1	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
D8	PD2		UART1_URXD1	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled

DMA Configuration





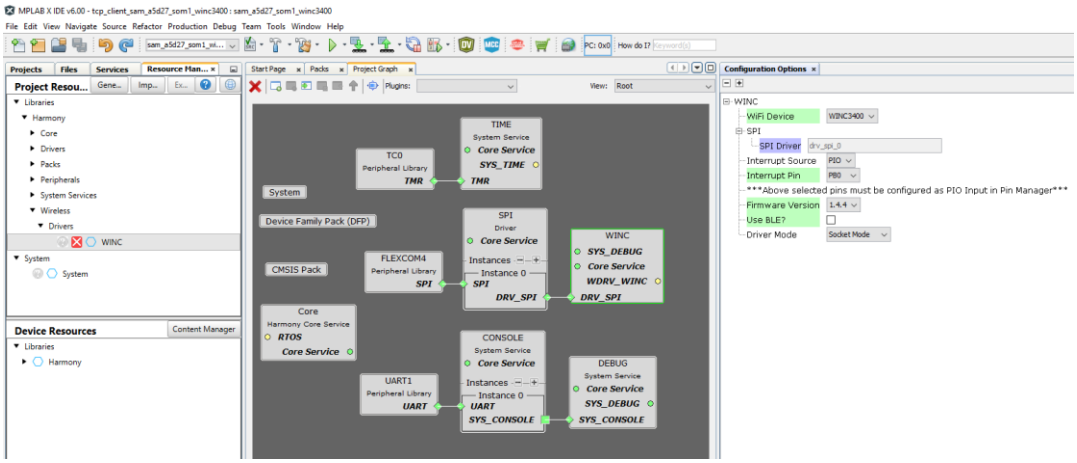
AIC Configuration

Start Page | Packs | Project Graph | Pin Diagram | Pin Table | Pin Settings | AIC Configuration

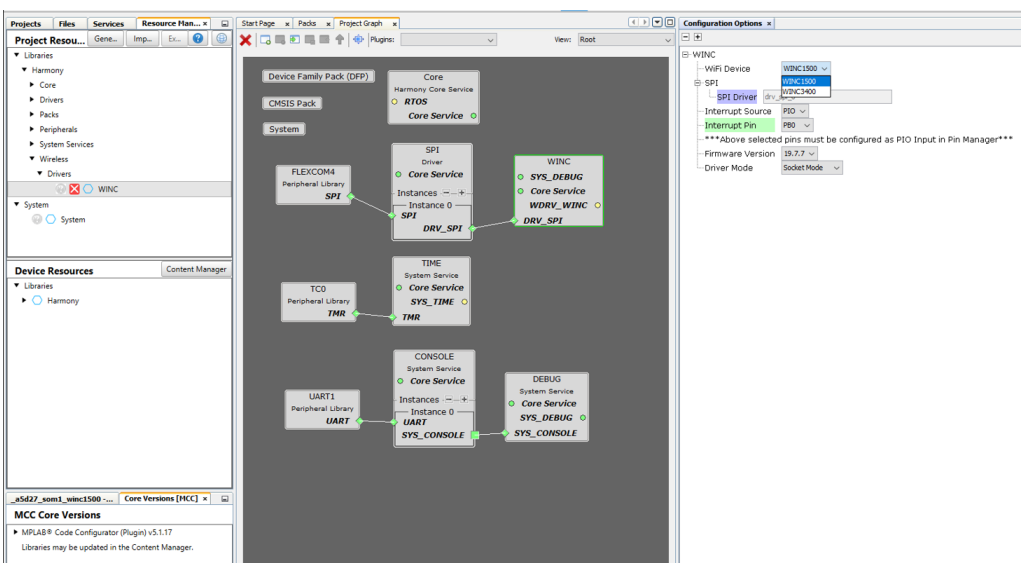
Vector	Enable	Handler Name	Map Type	Source Type	Priority
6) XDMAC0_IRQn - DMA Controller 0	☑	XDMAC0_InterruptHan...	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority
23) FLEXCOM4_IRQn - FLEXCOM 4	☑	FLEXCOM4_InterruptH...	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority
25) UART1_IRQn - UART 1	☑	UART1_InterruptHandler	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority
35) TC0_IRQn - Timer Counter 0 (ch. 0, 1, 2)	☑	TC0_InterruptHandler	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority
68) PIOB_IRQn - Parallel I/O Controller	☑	PIOB_InterruptHandler	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority

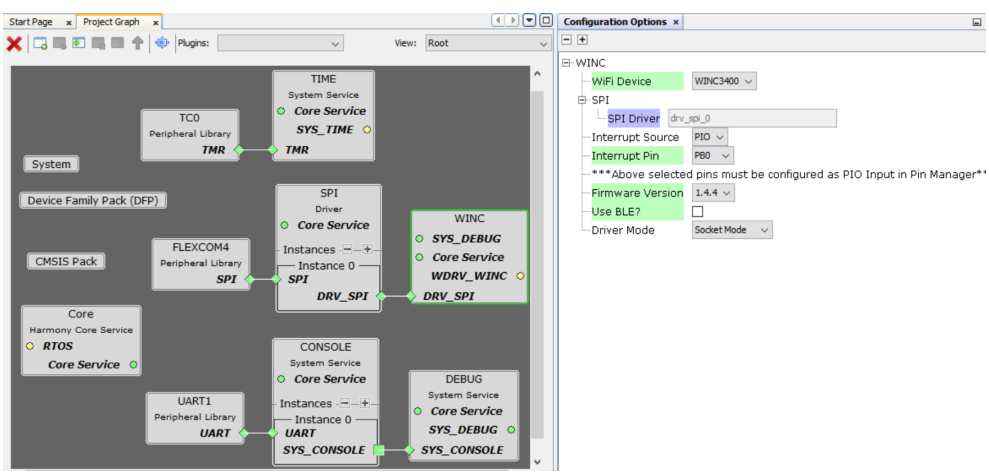
2. tcp_client application MCC Configuration

Project graph

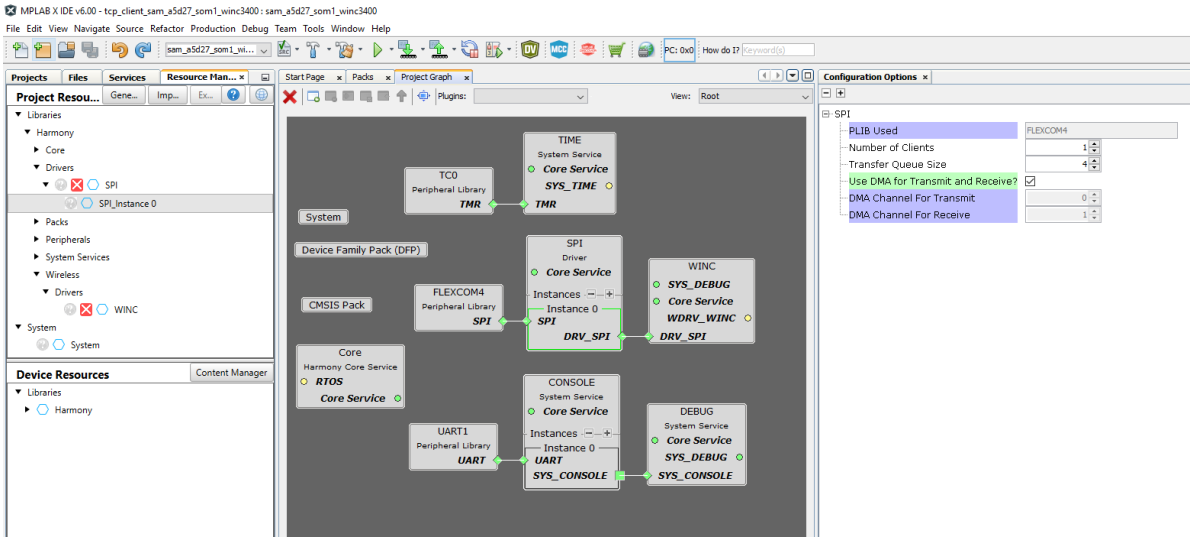


WINC Driver Configuration

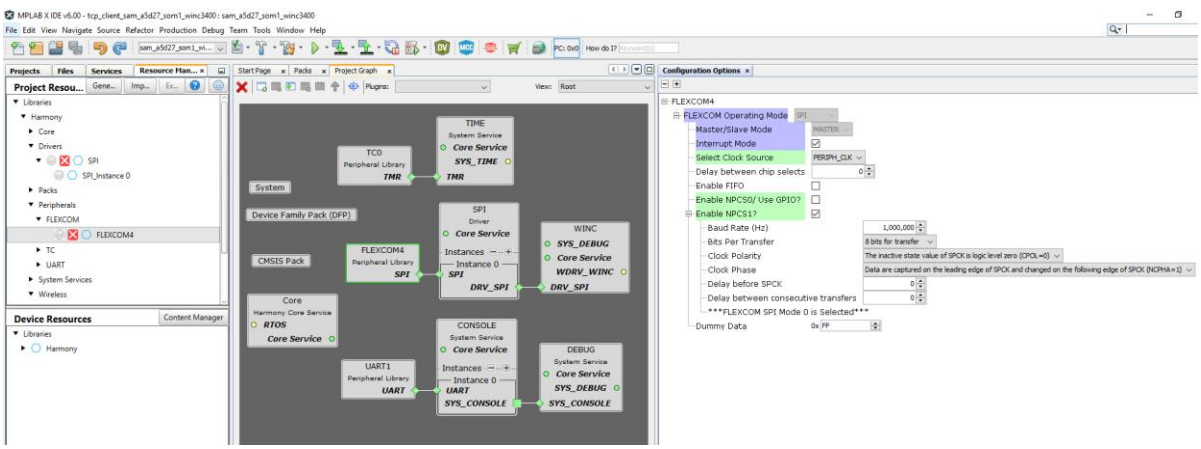




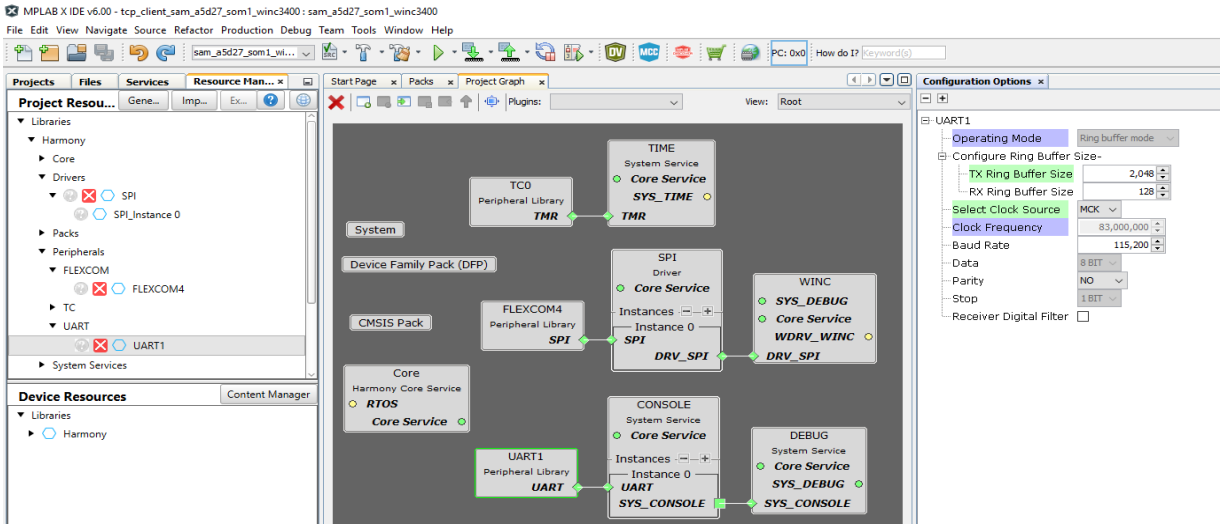
SPI Driver



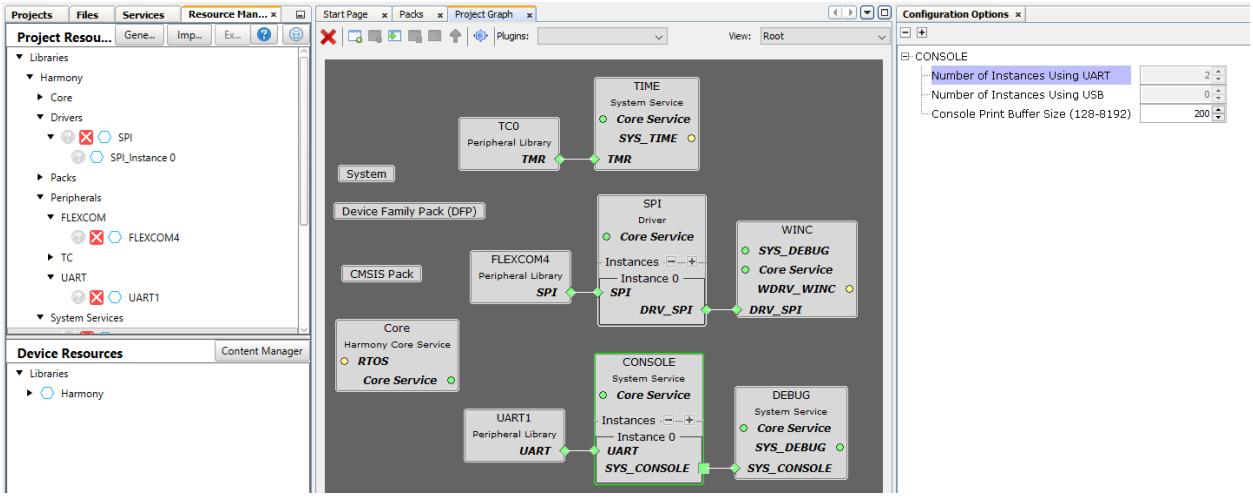
FLEXCOM4_SPI



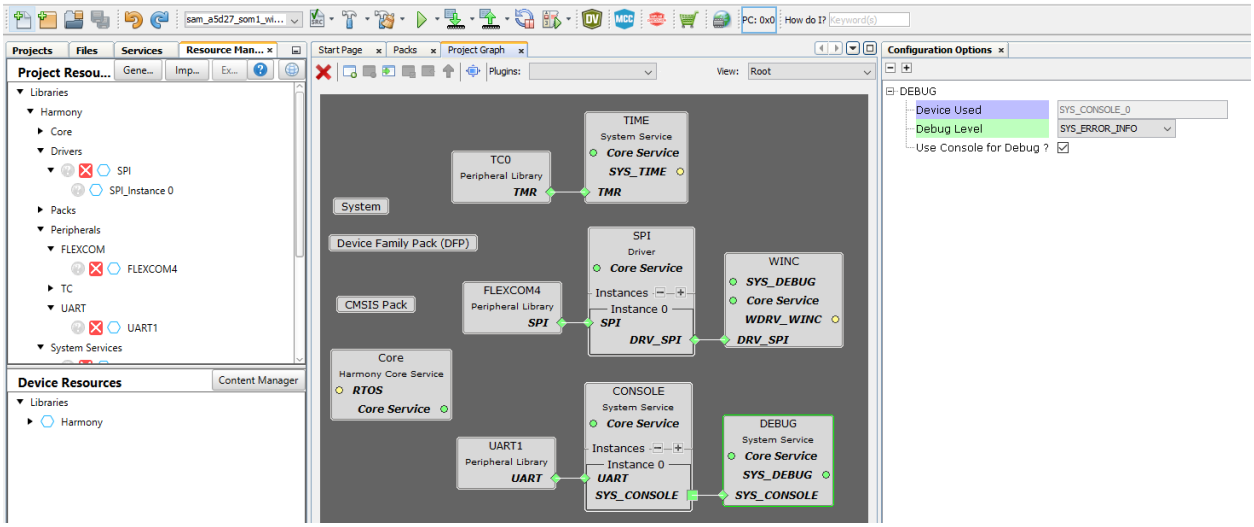
UART(UART1)



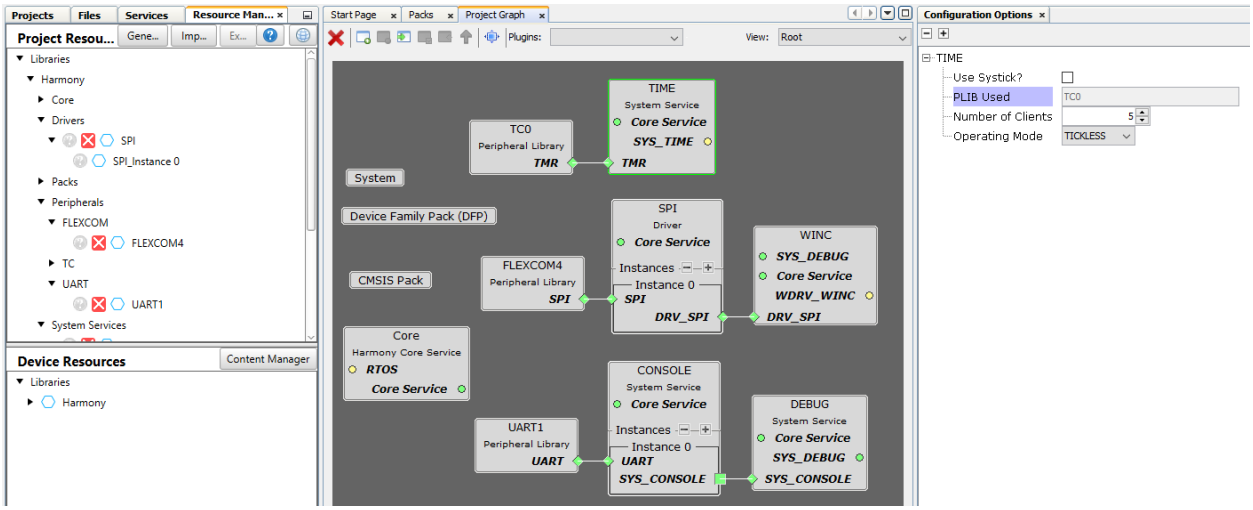
Console



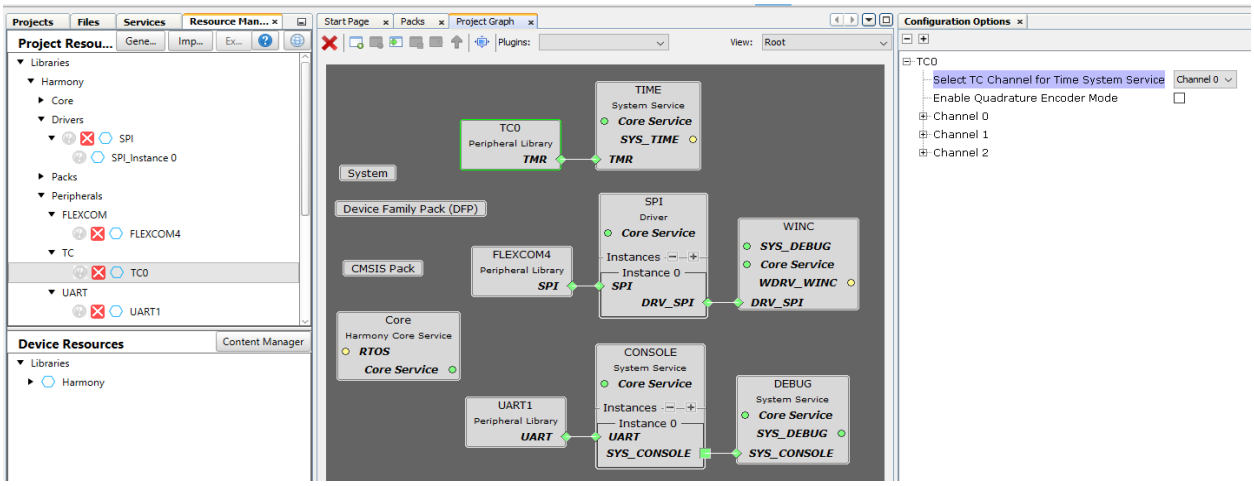
Debug



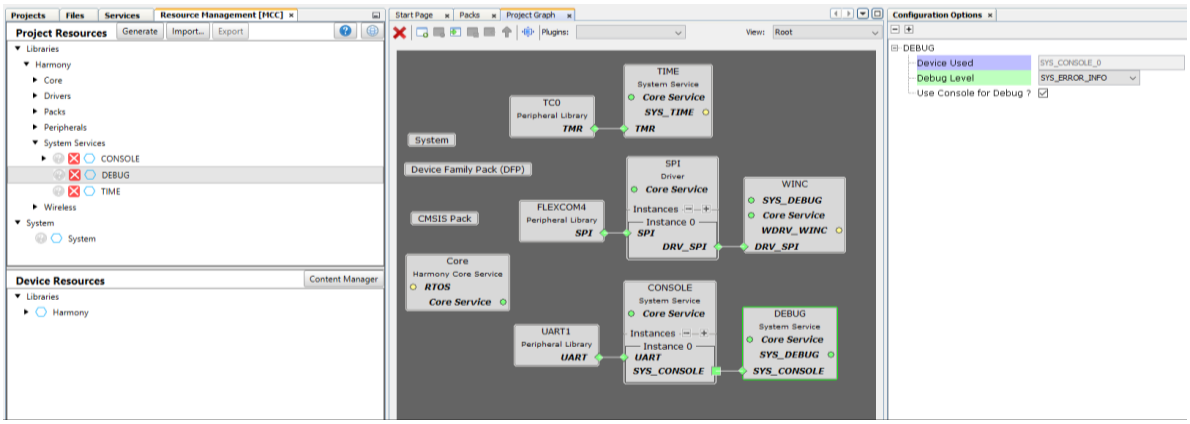
Time



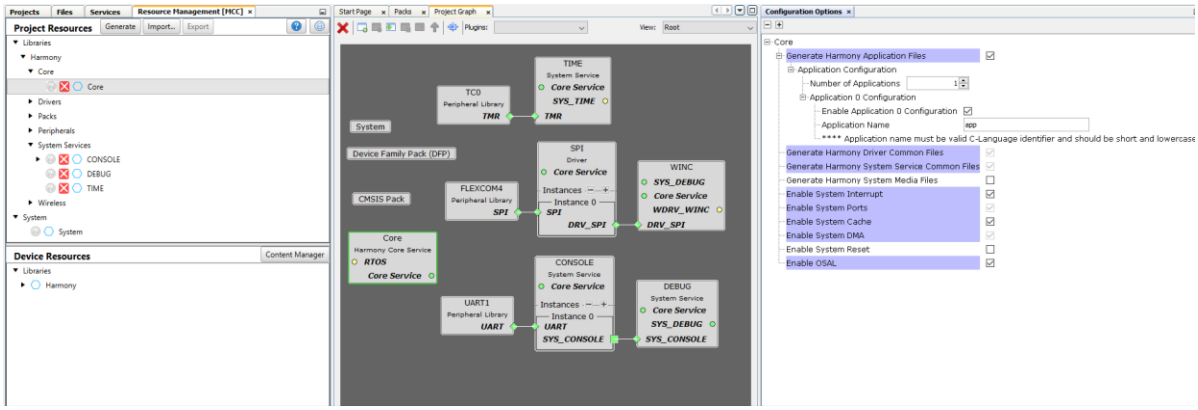
TC0



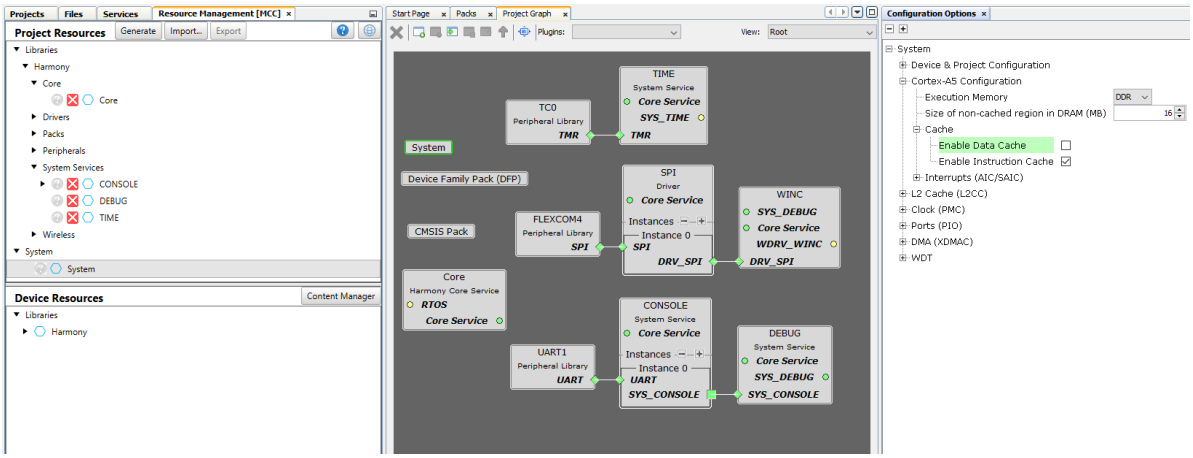
Debug



Core



System



PIN Configuration

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E6	PC30		FLEXCOM4_IO2	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
E7	PD0		FLEXCOM4_IO4	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
C7	PB2	WDRV_WINC_RESETN	GPIO	Out	High	☐	Disabled	☐	☐	Low drive	Disabled
F5	PB0	GPIO_PB0	GPIO	In	n/a	☐	Falling Edge	☑	☐	Low drive	Disabled
L5	PD25	WDRV_WINC_CHIP_EN	GPIO	Out	High	☐	Disabled	☐	☐	Low drive	Disabled
J1	PD3		UART1_UTXD1	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
D8	PD2		UART1_URXD1	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled

DMA Configuration

Start Page | Packs | Project Graph | Pin Diagram | Pin Table | Pin Settings | DMA Settings

☐ Use Linked List Mode

Active Channels List

Channel Number	Trigger
XDMAC Channel 0	FLEXCOM4_Transmit
XDMAC Channel 1	FLEXCOM4_Receive

Add Channel | Remove Selected Channel

XDMAC Channel 0 Settings

Enable Interrupt:	☑
Destination Address Mode:	Fixed Address Mode
Source Addressing Mode:	Increment Address After Every Transfer
Source Interface Identifier:	DMA Interface Bus 0
Destination Interface Identifier:	DMA Interface Bus 1
Data Width:	8-Bits
Chunk Size:	1 Transfer Per Request
Memory Burst Size:	1 Transfer Per Burst

Start Page | Packs | Project Graph | Pin Diagram | Pin Table | Pin Settings | DMA Settings

☐ Use Linked List Mode

Active Channels List

Channel Number	Trigger
XDMAC Channel 0	FLEXCOM4_Transmit
XDMAC Channel 1	FLEXCOM4_Receive

Add Channel | Remove Selected Channel

XDMAC Channel 1 Settings

Enable Interrupt:	☑
Destination Address Mode:	Increment Address After Every Transfer
Source Addressing Mode:	Fixed Address Mode
Source Interface Identifier:	DMA Interface Bus 1
Destination Interface Identifier:	DMA Interface Bus 0
Data Width:	8-Bits
Chunk Size:	1 Transfer Per Request
Memory Burst Size:	1 Transfer Per Burst

AIC Configuration

Start Page | Packs | Project Graph | Pin Diagram | Pin Table | Pin Settings | AIC Configuration

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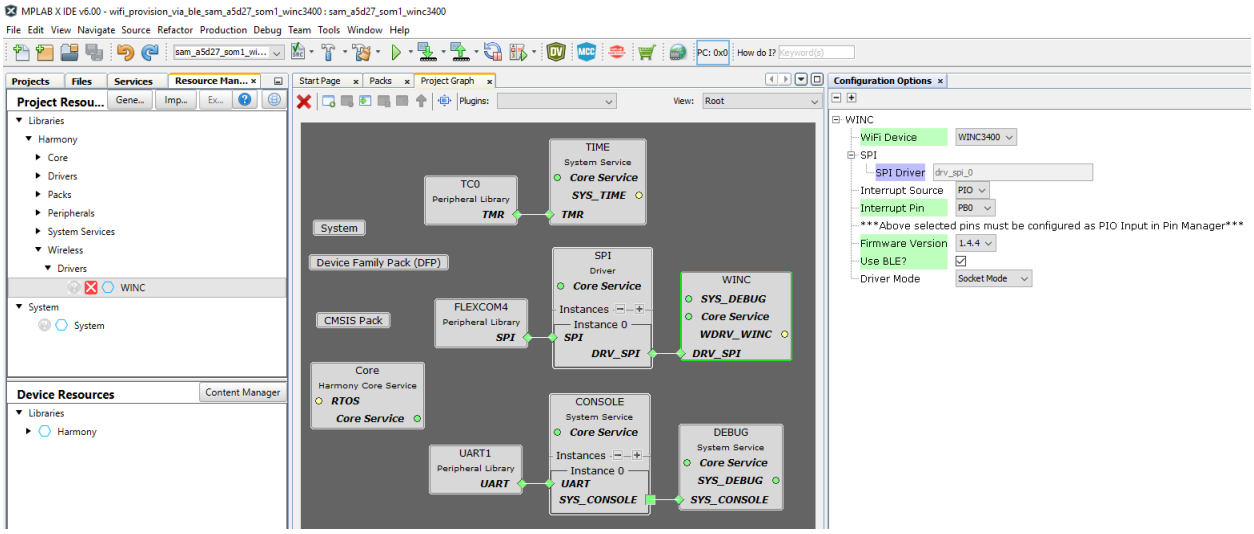
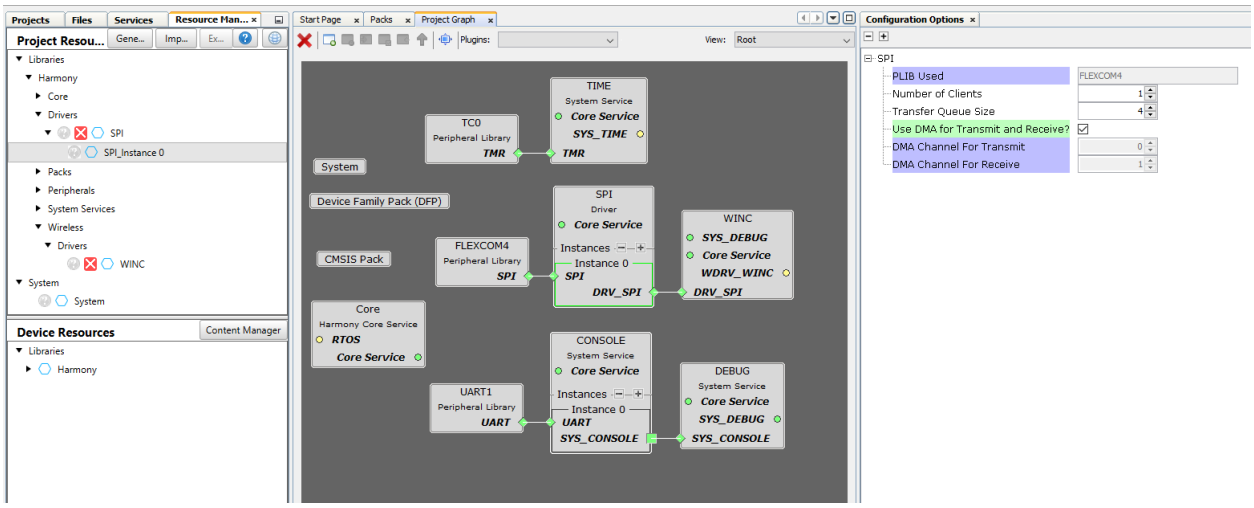
3. wifi_provision_via_ble application MCC Configuration

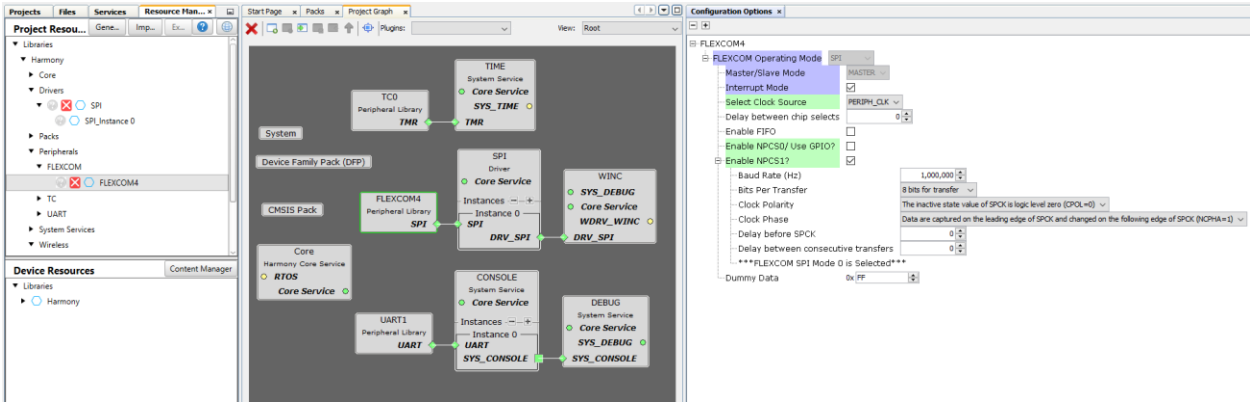
WINC3400 Driver



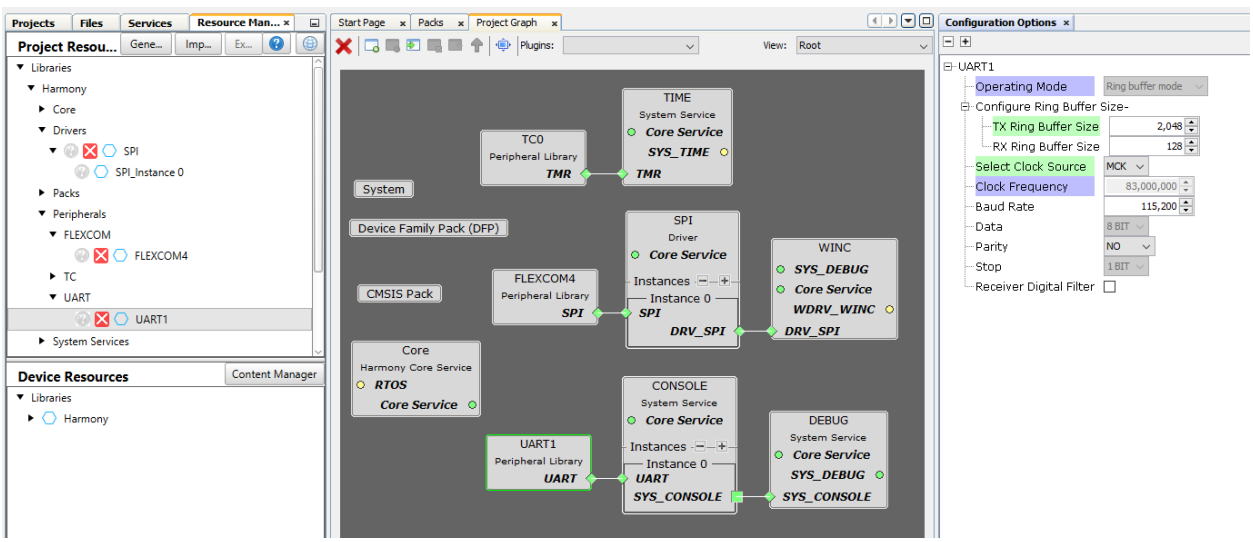
SPI Driver



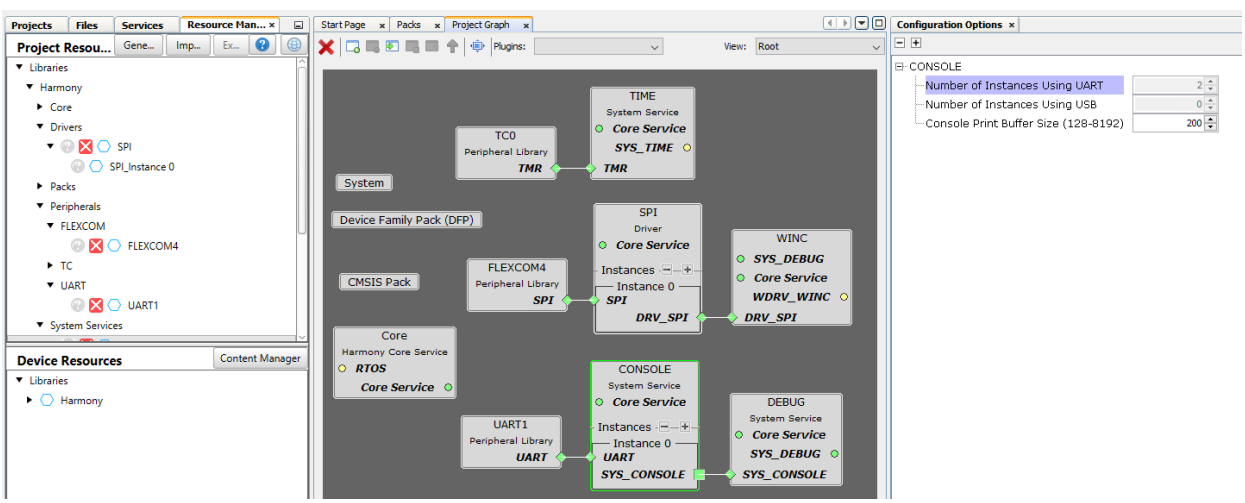
FLEXCOM4_SPI



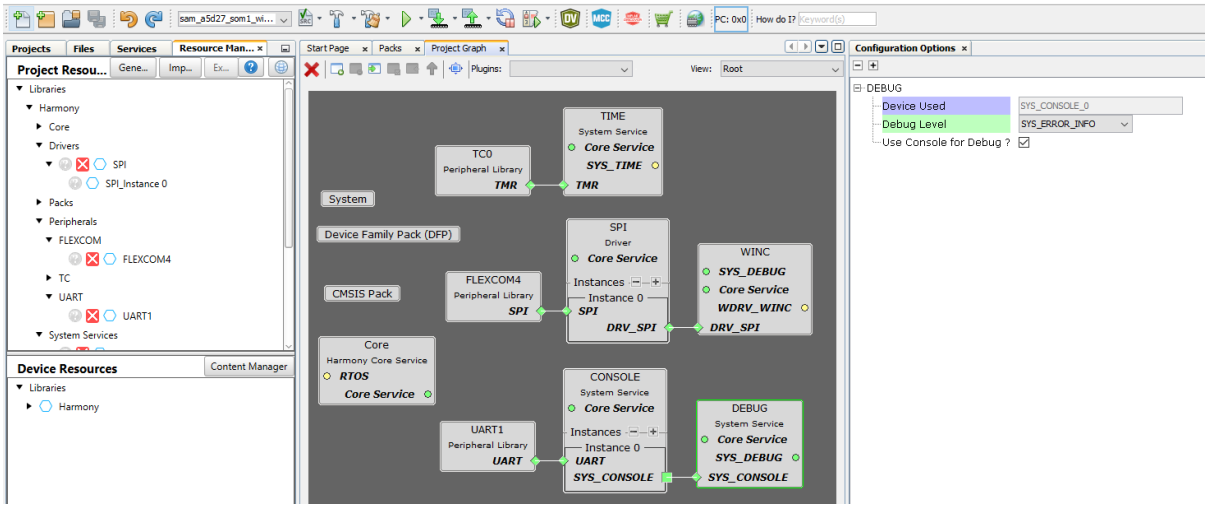
UART(UART1)



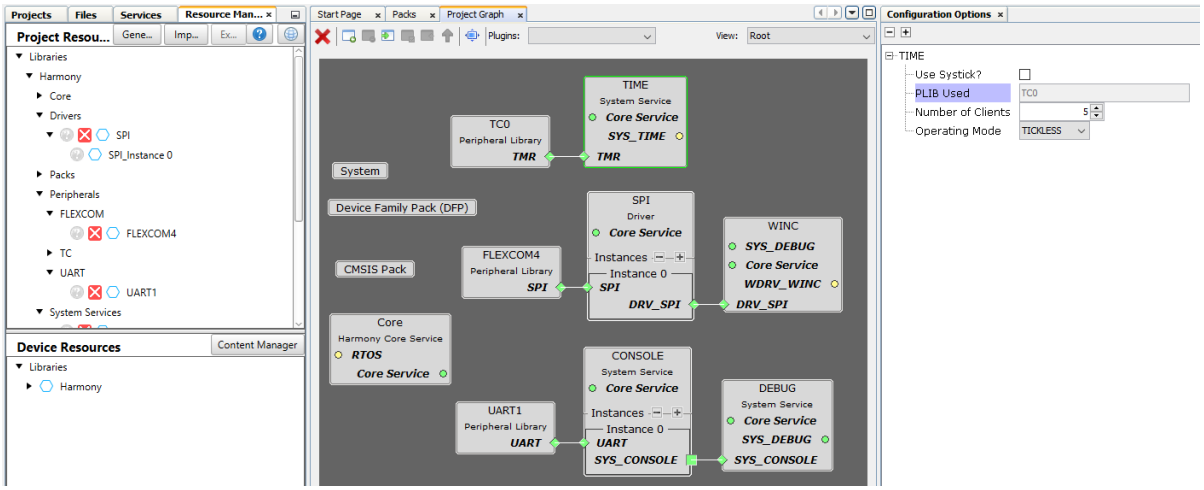
Console



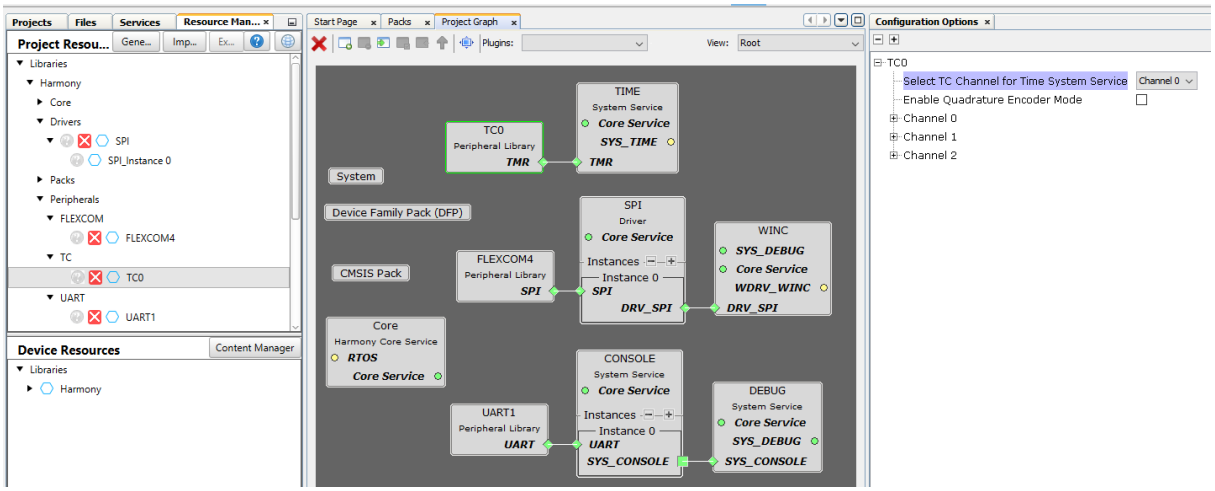
Debug



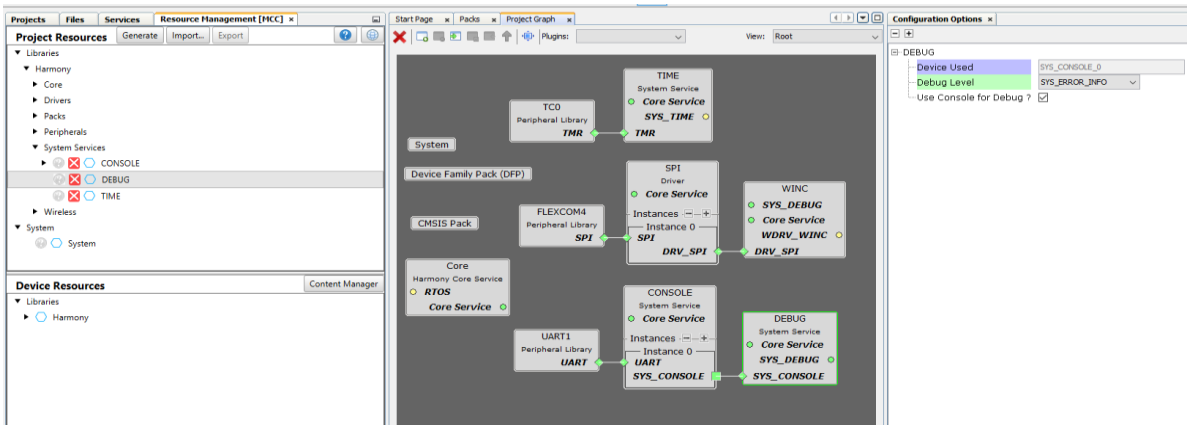
Time



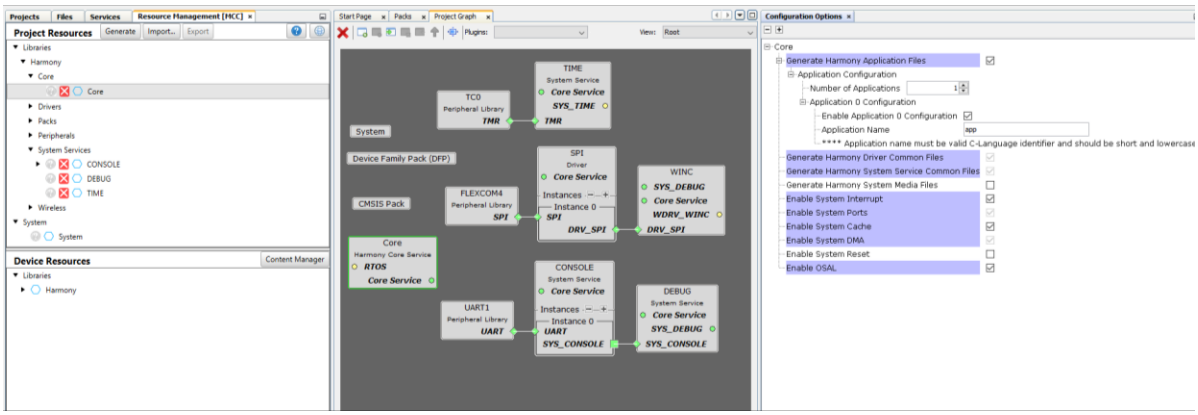
TC0



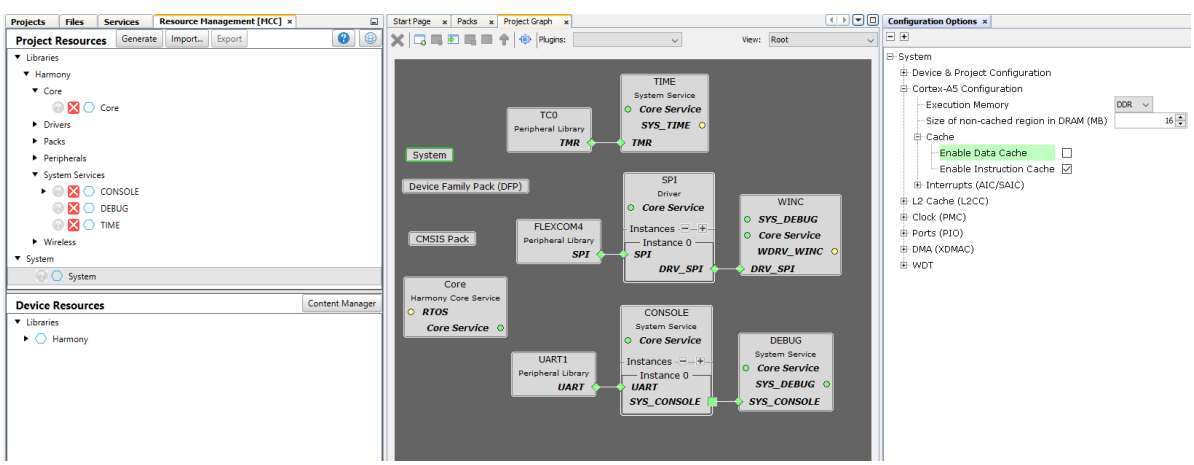
Debug



Core



System



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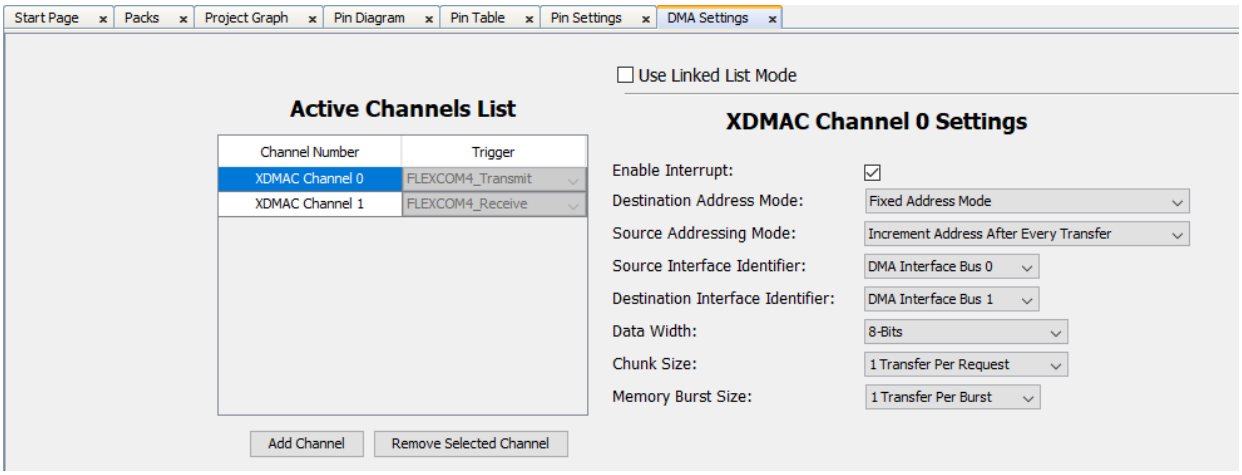
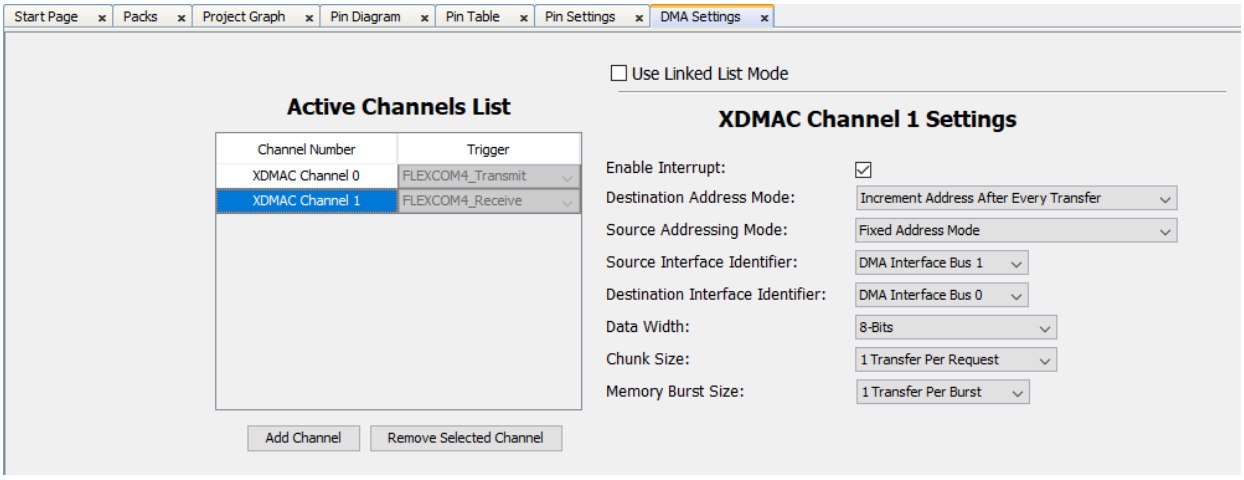
J1	PD3		UART1_UTXD1	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
D8	PD2		UART1_URXD1	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled

DMA Configuration





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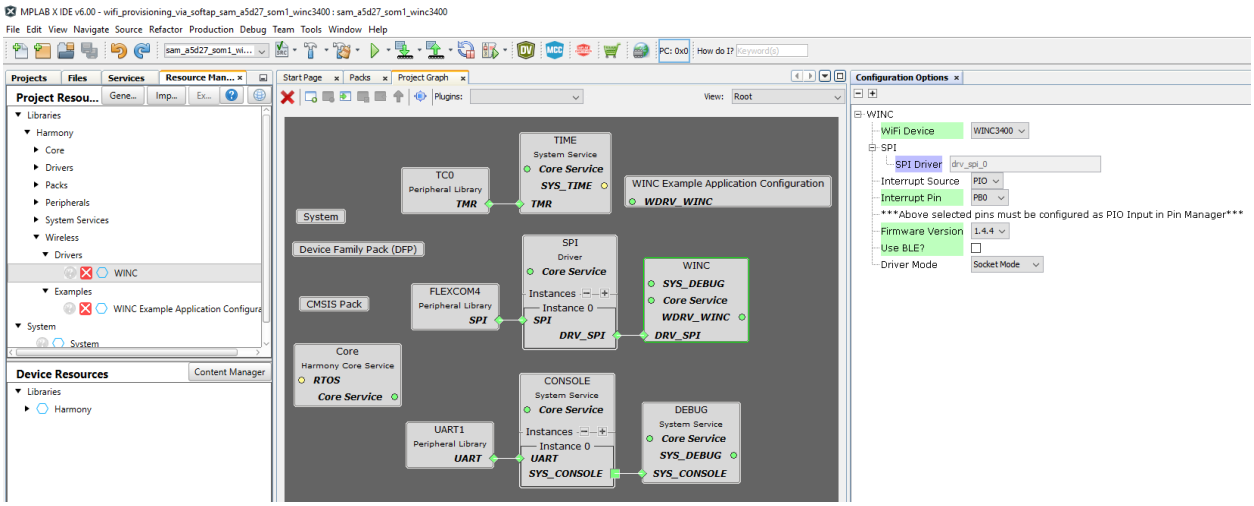
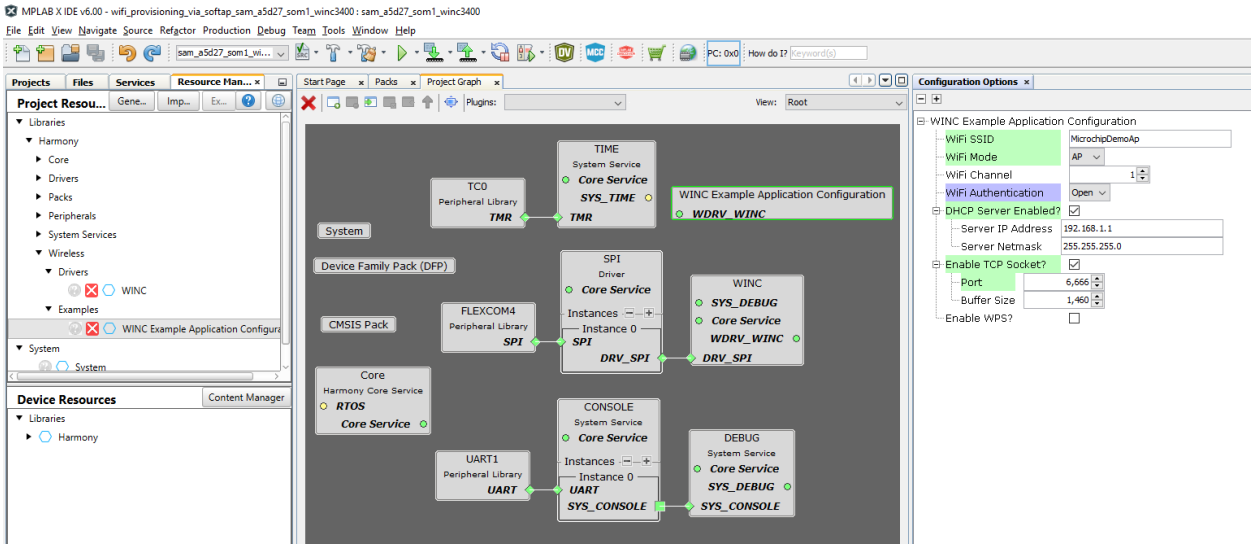
6) XDMAC0_IRQn - DMA Controller 0	☑	XDMAC0_InterruptHan...	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority
23) FLEXCOM4_IRQn - FLEXCOM 4	☑	FLEXCOM4_InterruptH...	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority
25) UART1_IRQn - UART 1	☑	UART1_InterruptHandler	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority
35) TC0_IRQn - Timer Counter 0 (ch. 0, 1, 2)	☑	TC0_InterruptHandler	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority
68) PIOB_IRQn - Parallel I/O Controller	☑	PIOB_InterruptHandler	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority

4. wifi_provisioning_via_softap application MCC Configuration

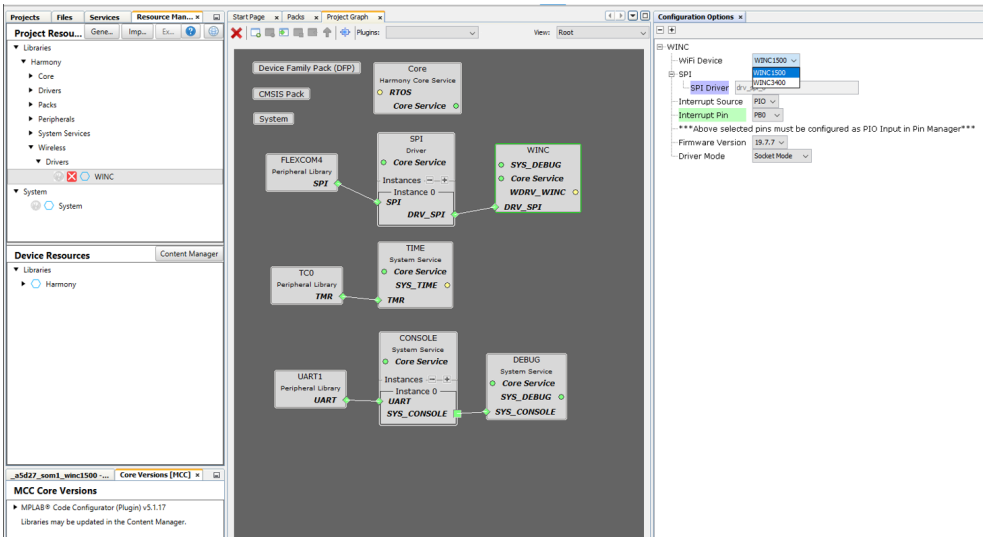
Project graph

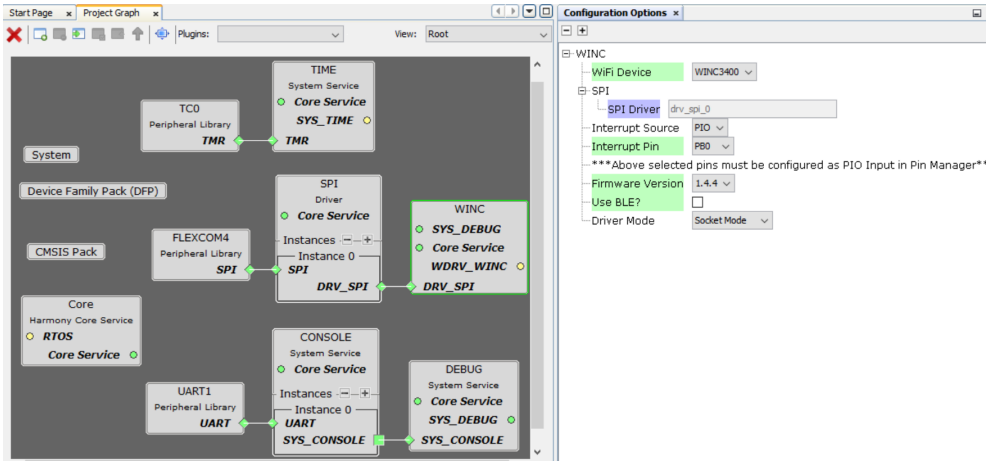


WINC Example application Configuration

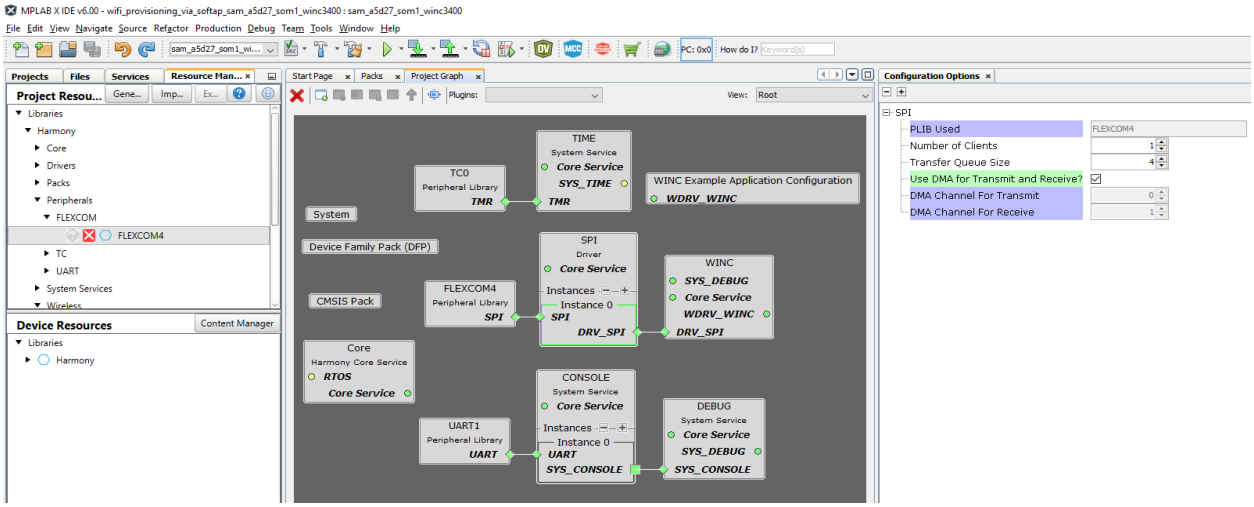


WINC Driver Configuration

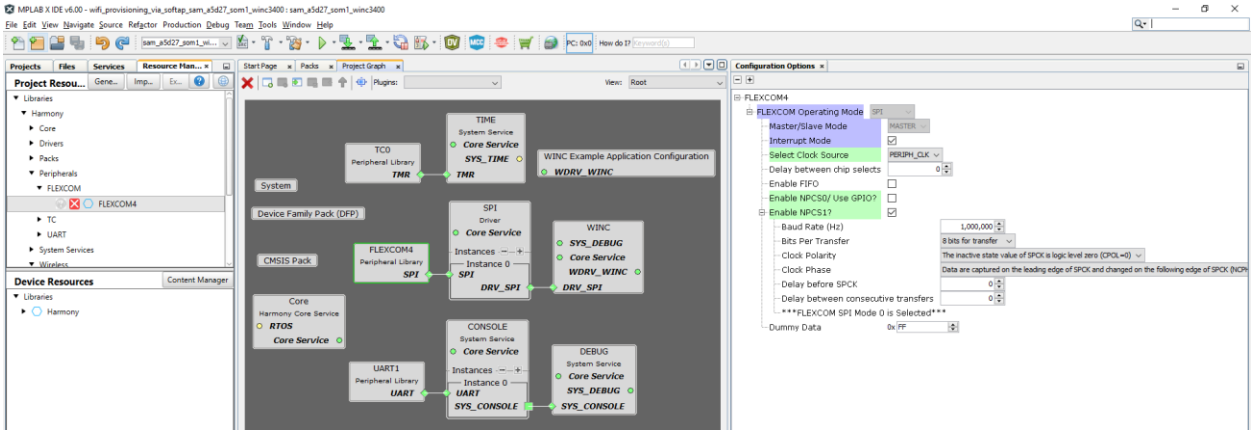




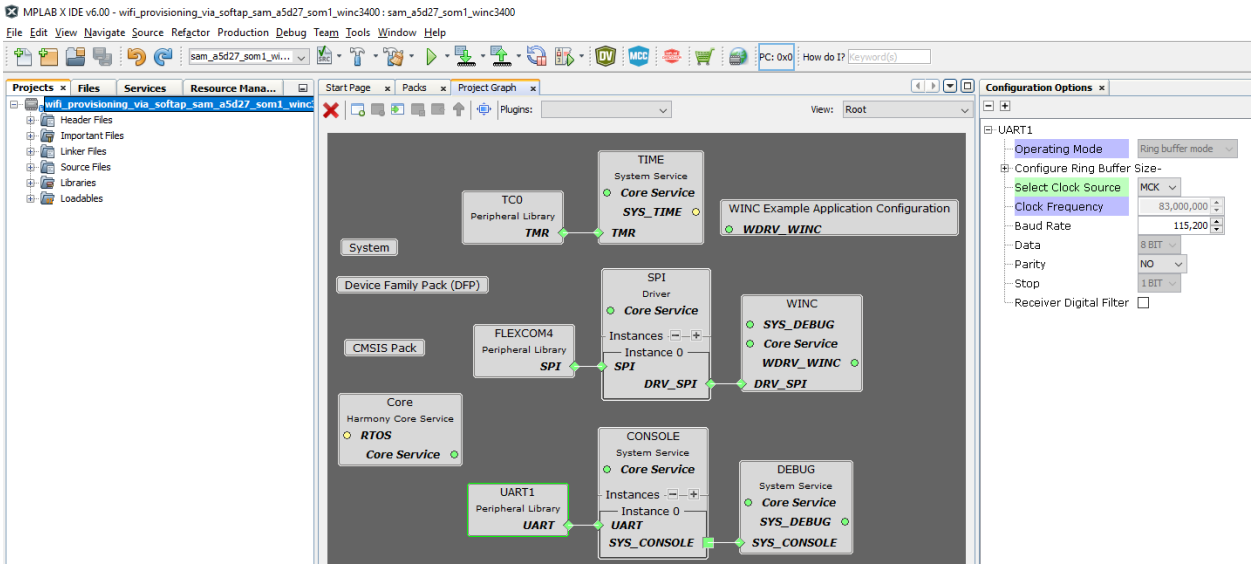
SPI Driver



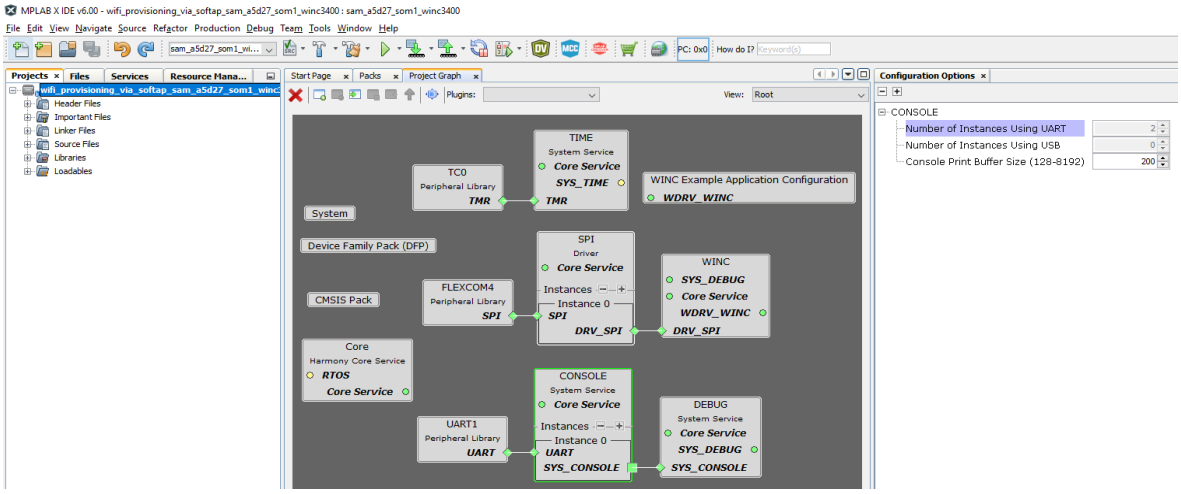
FLEXCOM4_SPI



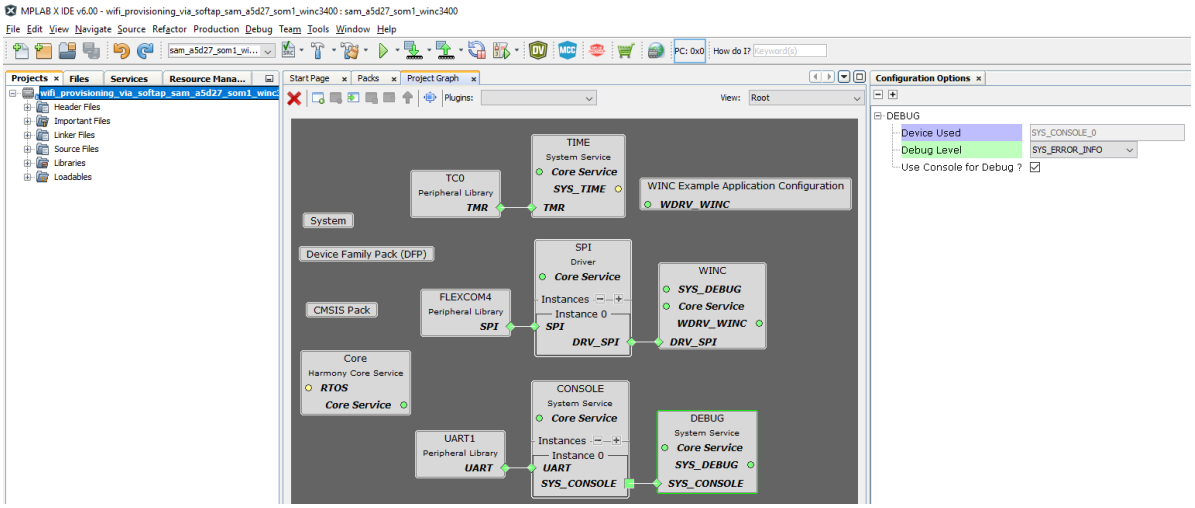
UAR(UART1)



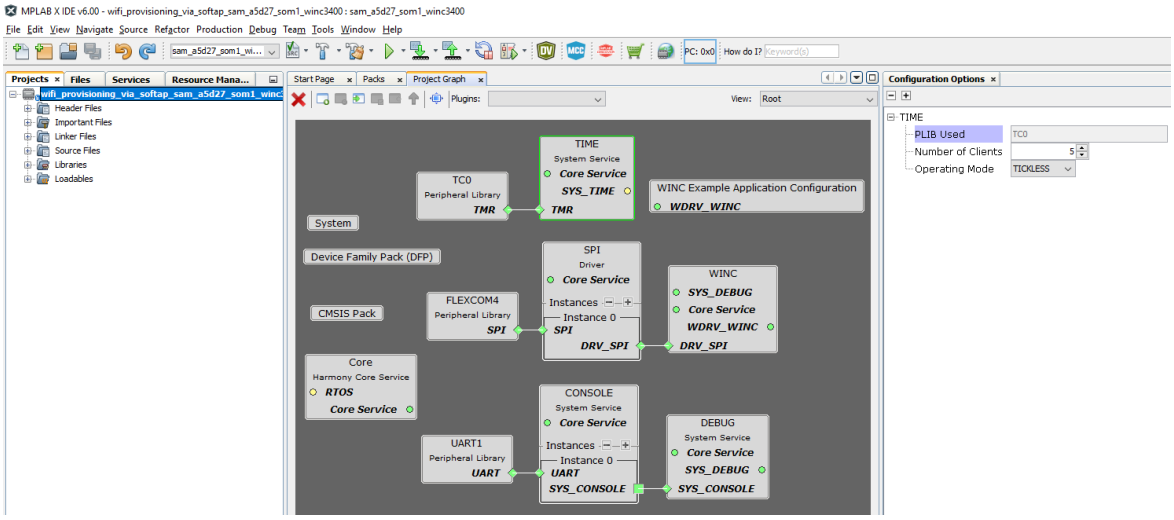
Console



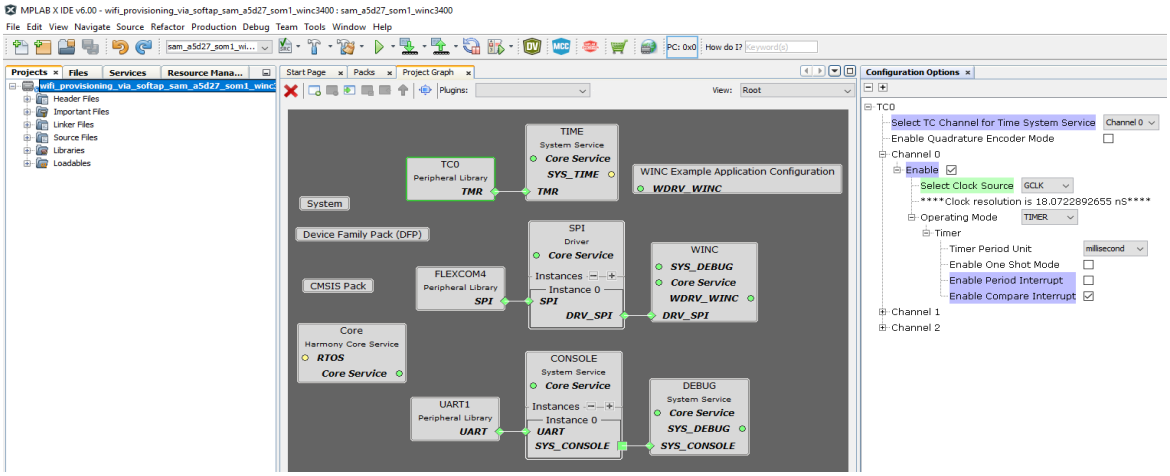
Debug



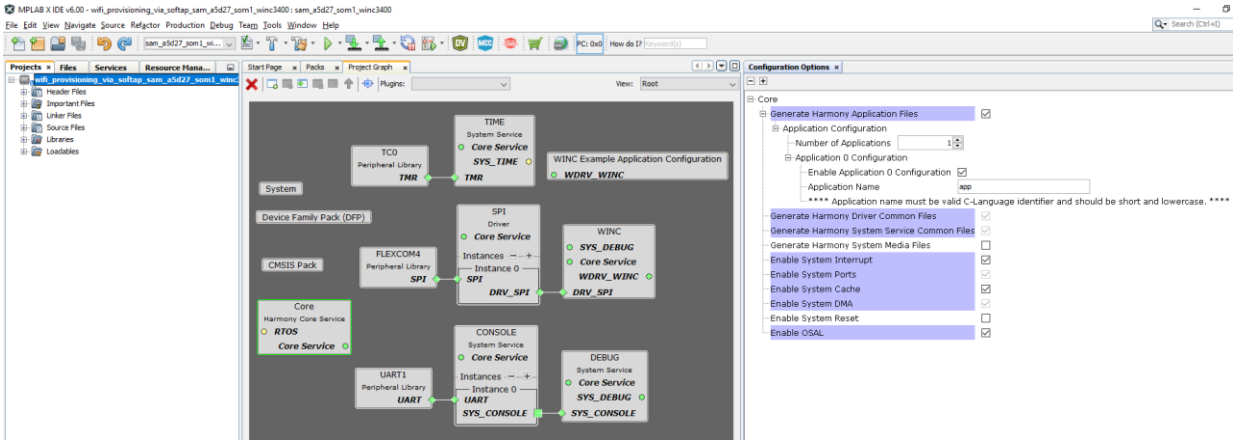
Time



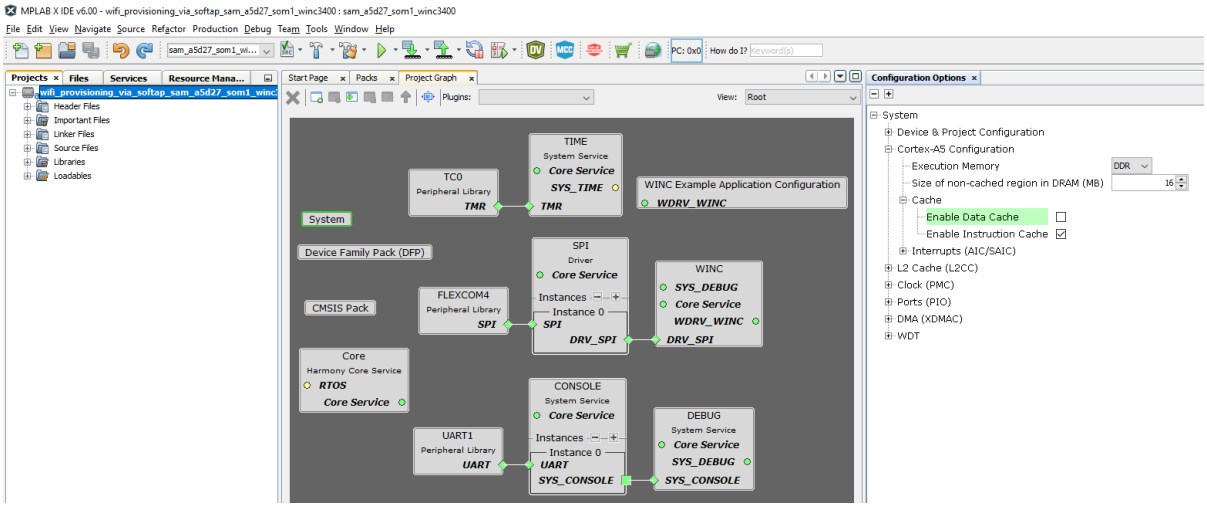
TC0



Core



System



PIN Configuration

Pin Number	Pin ID	Custom Name	Function	Direction	Latch	Open Drain	PIO Interrupt	Pull Up	Pull Down	Drive Strength	Glitch/Debounce Filter
F6	PC28		FLEXCOM4_IO0	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
B9	PC29		FLEXCOM4_IO1	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
E6	PC30		FLEXCOM4_IO2	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
E7	PD0		FLEXCOM4_IO4	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
C7	PB2	WDRV_WINC_RESETN	GPIO	Out	High	☐	Disabled	☐	☐	Low drive	Disabled
F5	PB0	GPIO_PB0	GPIO	In	n/a	☐	Falling Edge	☑	☐	Low drive	Disabled
L5	PD25	WDRV_WINC_CHIP_EN	GPIO	Out	High	☐	Disabled	☐	☐	Low drive	Disabled
J1	PD3		UART1_UTXD1	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
D8	PD2		UART1_URXD1	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled

DMA Configuration

Start Page | Packs | Project Graph | Pin Diagram | Pin Table | Pin Settings | DMA Settings

☐ Use Linked List Mode

Active Channels List

Channel Number	Trigger
XDMAC Channel 0	FLEXCOM4_Transmit
XDMAC Channel 1	FLEXCOM4_Receive

Add Channel | Remove Selected Channel

XDMAC Channel 0 Settings

Enable Interrupt:	☑
Destination Address Mode:	Fixed Address Mode
Source Addressing Mode:	Increment Address After Every Transfer
Source Interface Identifier:	DMA Interface Bus 0
Destination Interface Identifier:	DMA Interface Bus 1
Data Width:	8-Bits
Chunk Size:	1 Transfer Per Request
Memory Burst Size:	1 Transfer Per Burst

Start Page | Packs | Project Graph | Pin Diagram | Pin Table | Pin Settings | DMA Settings

☐ Use Linked List Mode

Active Channels List

Channel Number	Trigger
XDMAC Channel 0	FLEXCOM4_Transmit
XDMAC Channel 1	FLEXCOM4_Receive

Add Channel | Remove Selected Channel

XDMAC Channel 1 Settings

Enable Interrupt:	☑
Destination Address Mode:	Increment Address After Every Transfer
Source Addressing Mode:	Fixed Address Mode
Source Interface Identifier:	DMA Interface Bus 1
Destination Interface Identifier:	DMA Interface Bus 0
Data Width:	8-Bits
Chunk Size:	1 Transfer Per Request
Memory Burst Size:	1 Transfer Per Burst

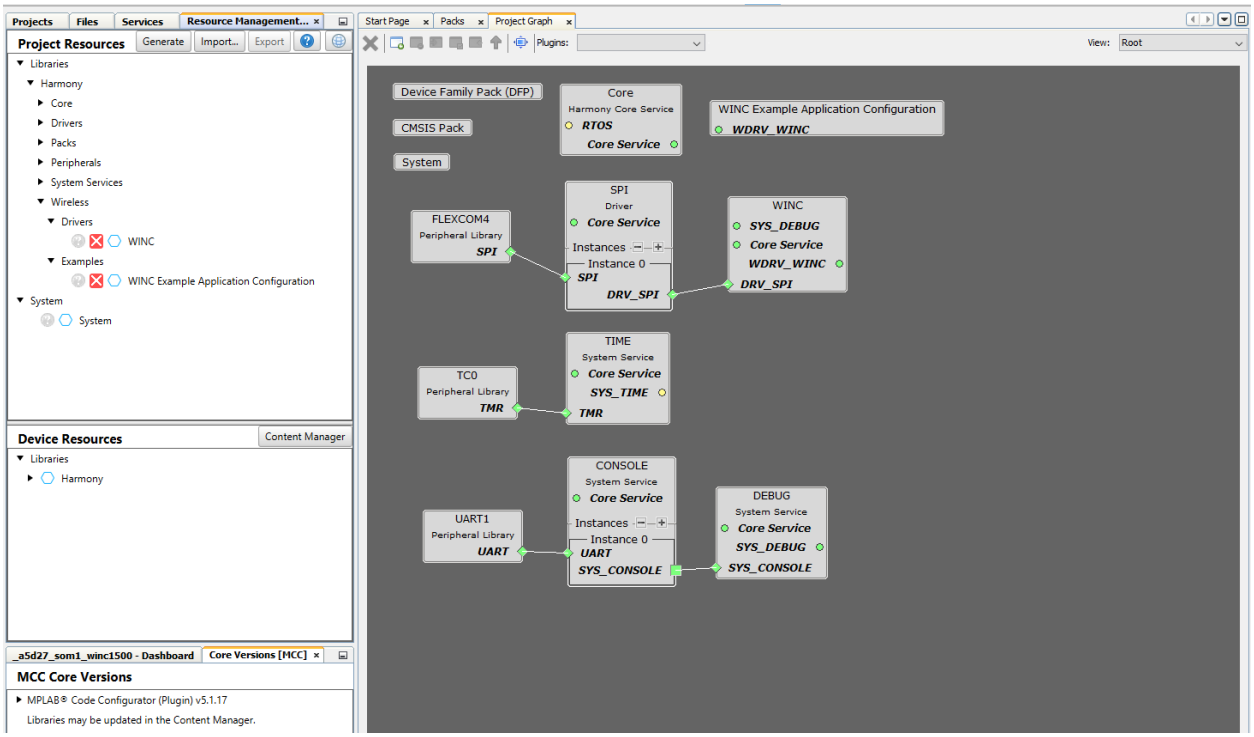
AIC Configuration

Start Page | Packs | Project Graph | Pin Diagram | Pin Table | Pin Settings | AIC Configuration

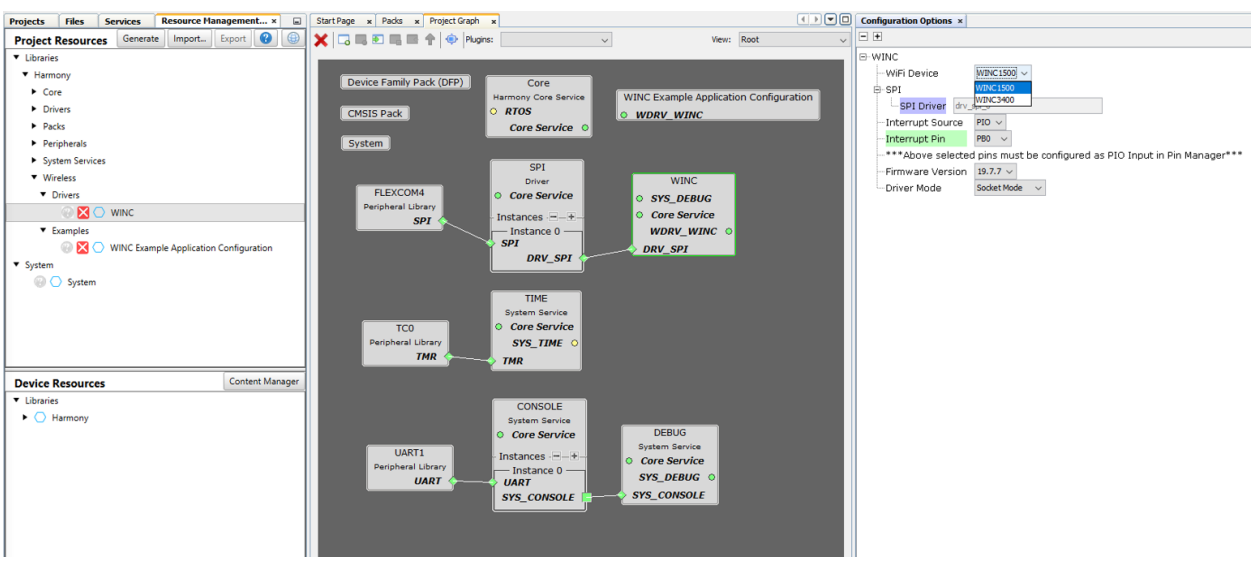
Vector	Enable	Handler Name	Map Type	Source Type	Priority
6) XDMAC0_IRQn - DMA Controller 0	☑	XDMAC0_InterruptHan...	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority
23) FLEXCOM4_IRQn - FLEXCOM 4	☑	FLEXCOM4_InterruptH...	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority
25) UART1_IRQn - UART 1	☑	UART1_InterruptHandler	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority
35) TC0_IRQn - Timer Counter 0 (ch. 0, 1, 2)	☑	TC0_InterruptHandler	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority
68) PIOB_IRQn - Parallel I/O Controller	☑	PIOB_InterruptHandler	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority

5. wifi_provisioning_via_wps

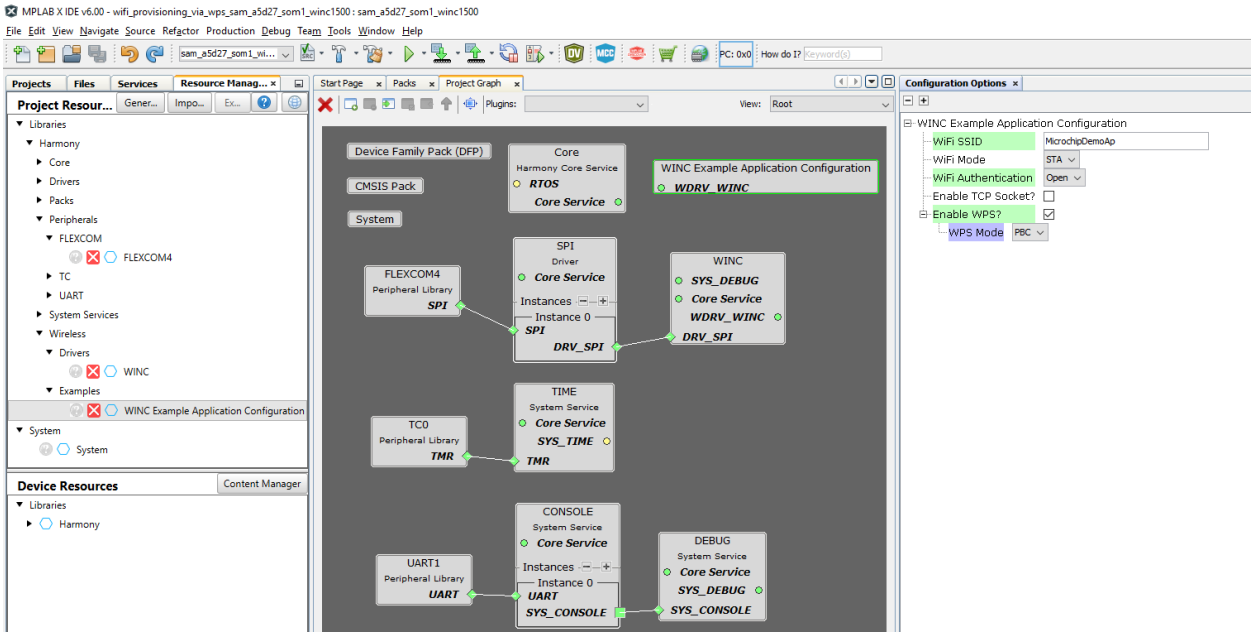
Project graph



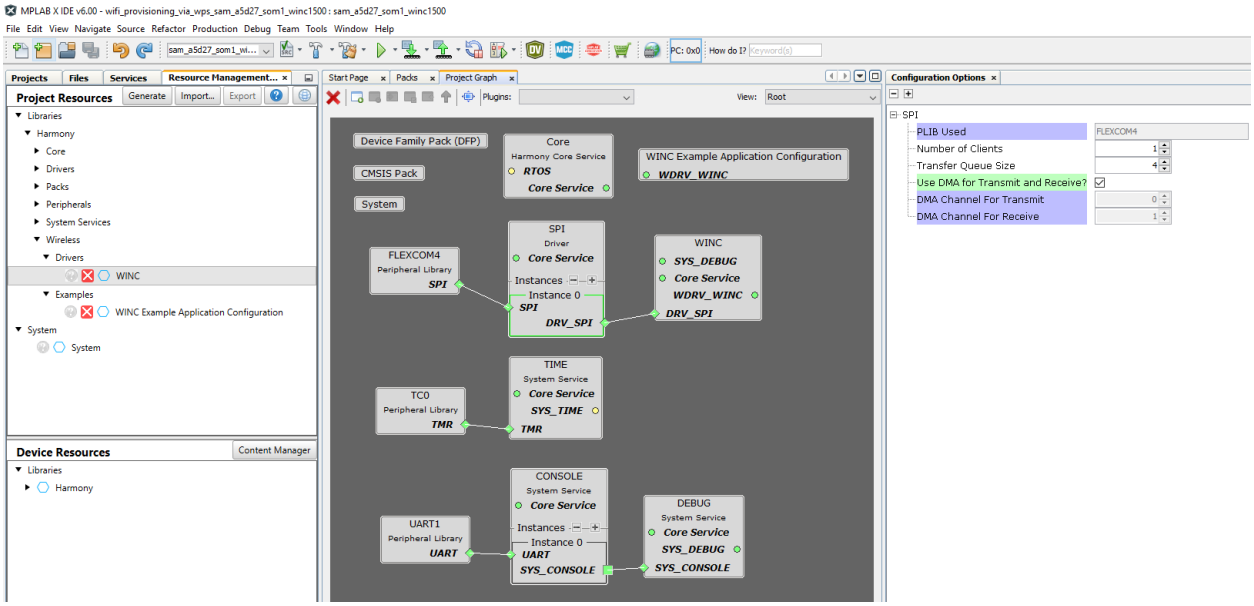
WINC Driver Configuration



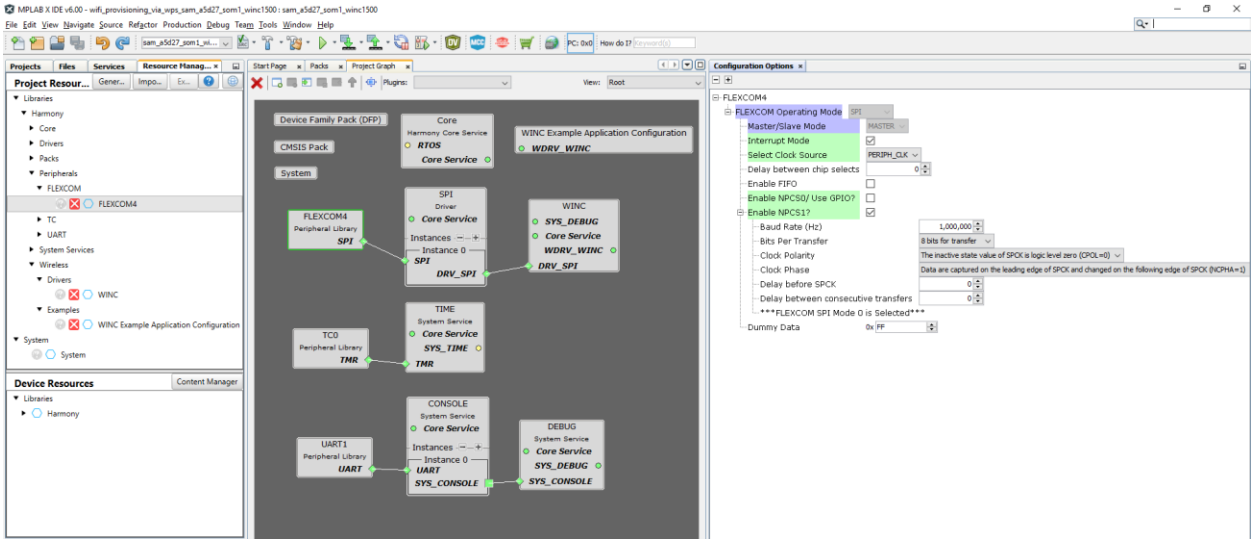
WINC Example application Configuration:



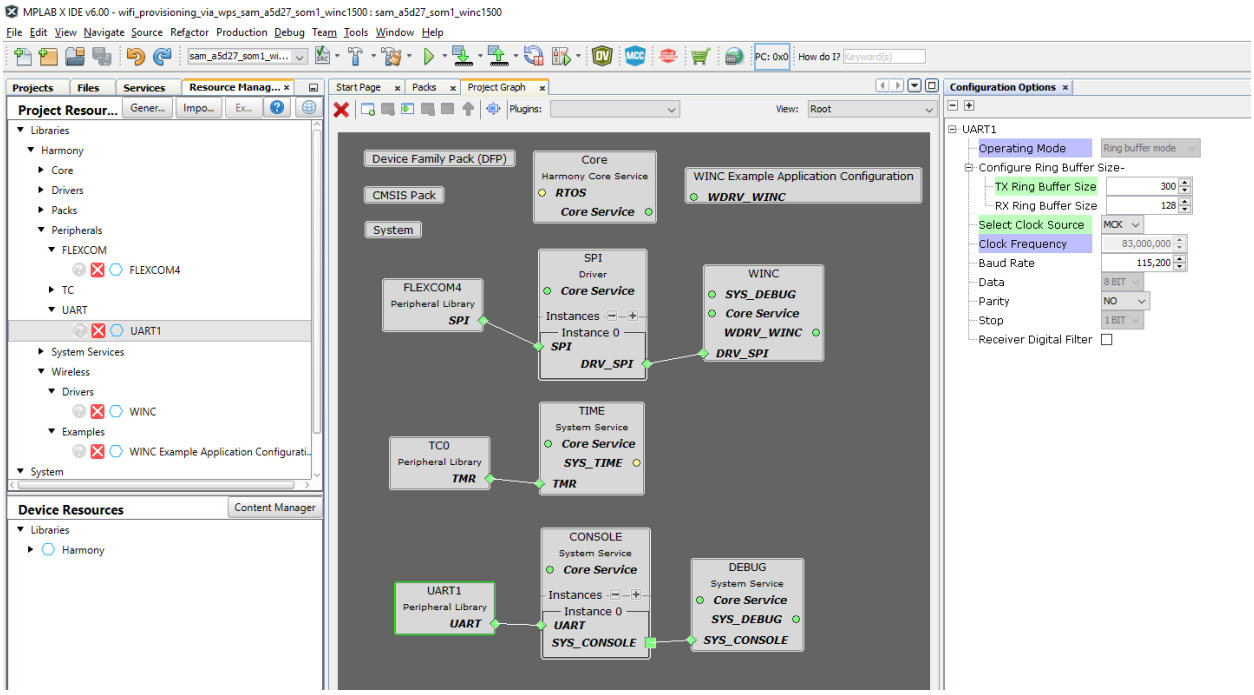
SPI Driver



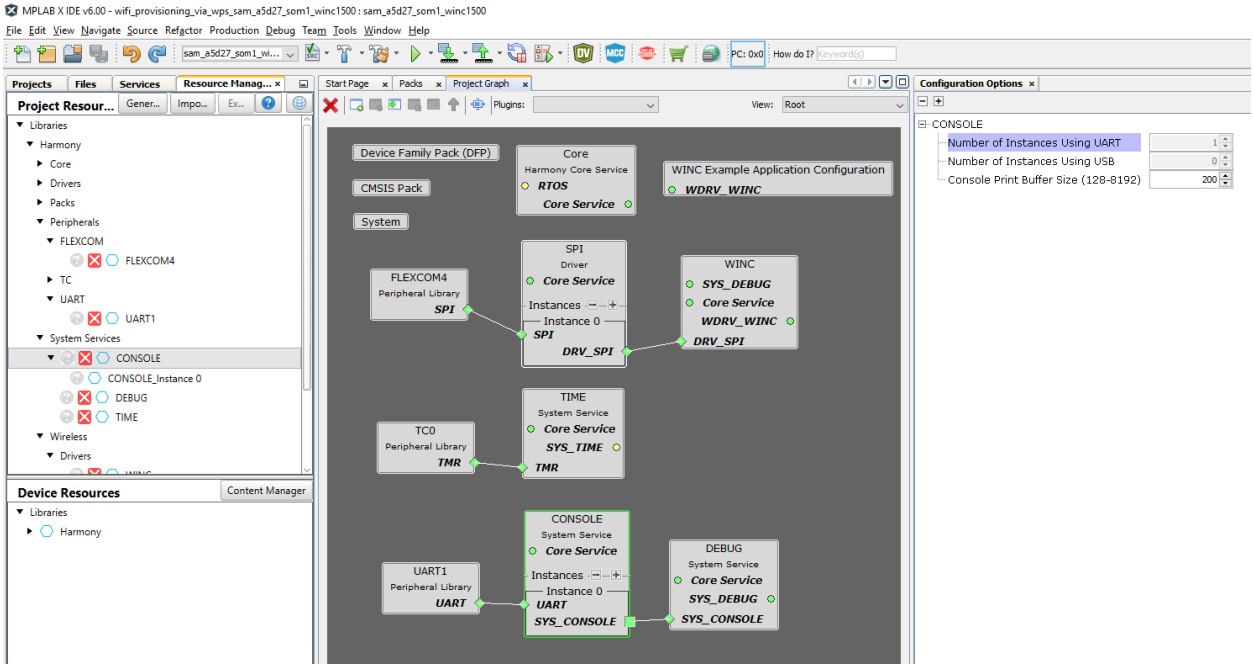
FLEXCOM4_SPI



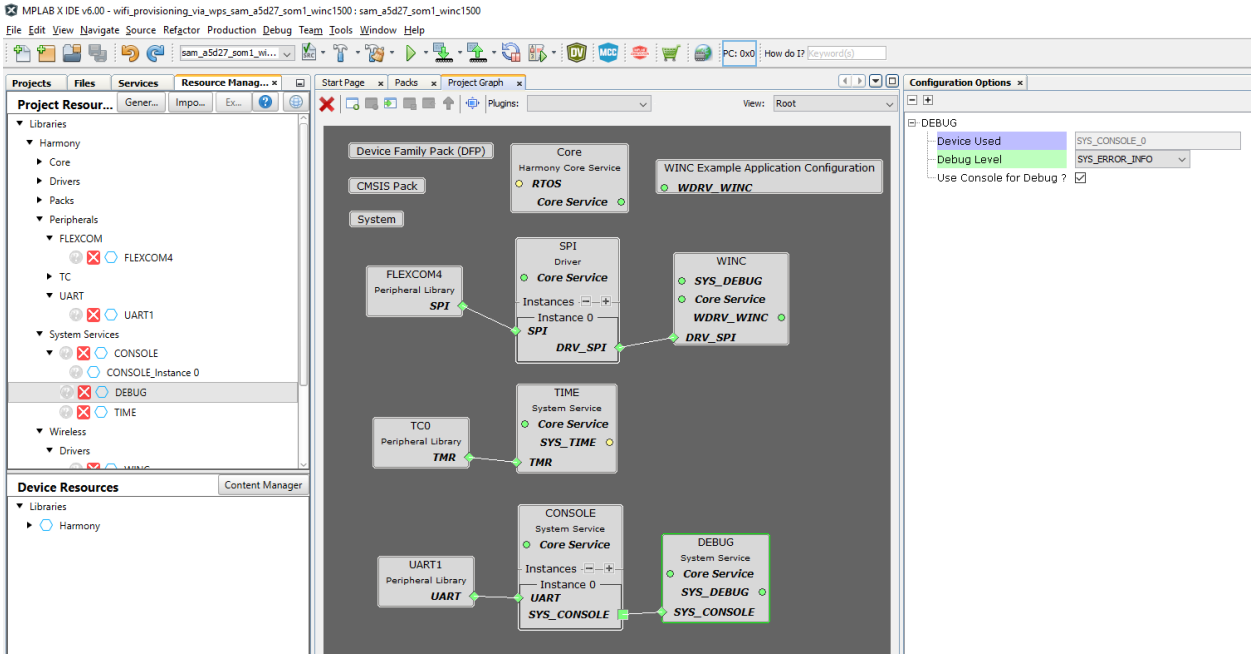
UART(UART1)



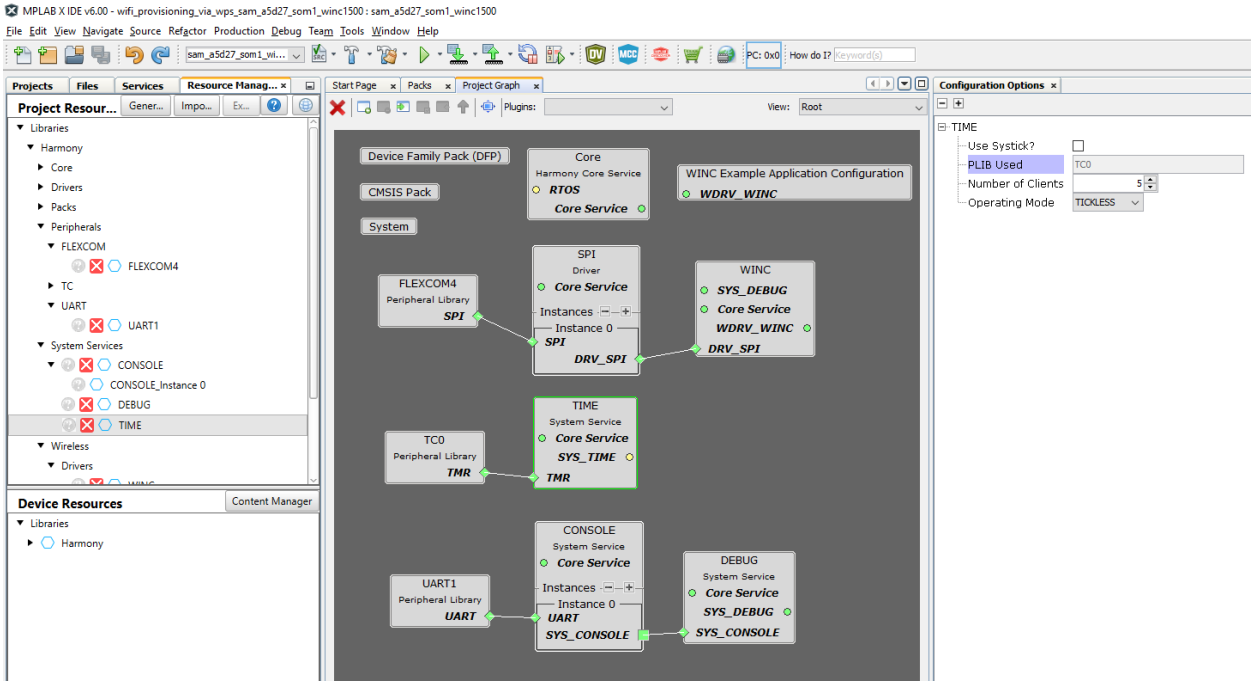
Console



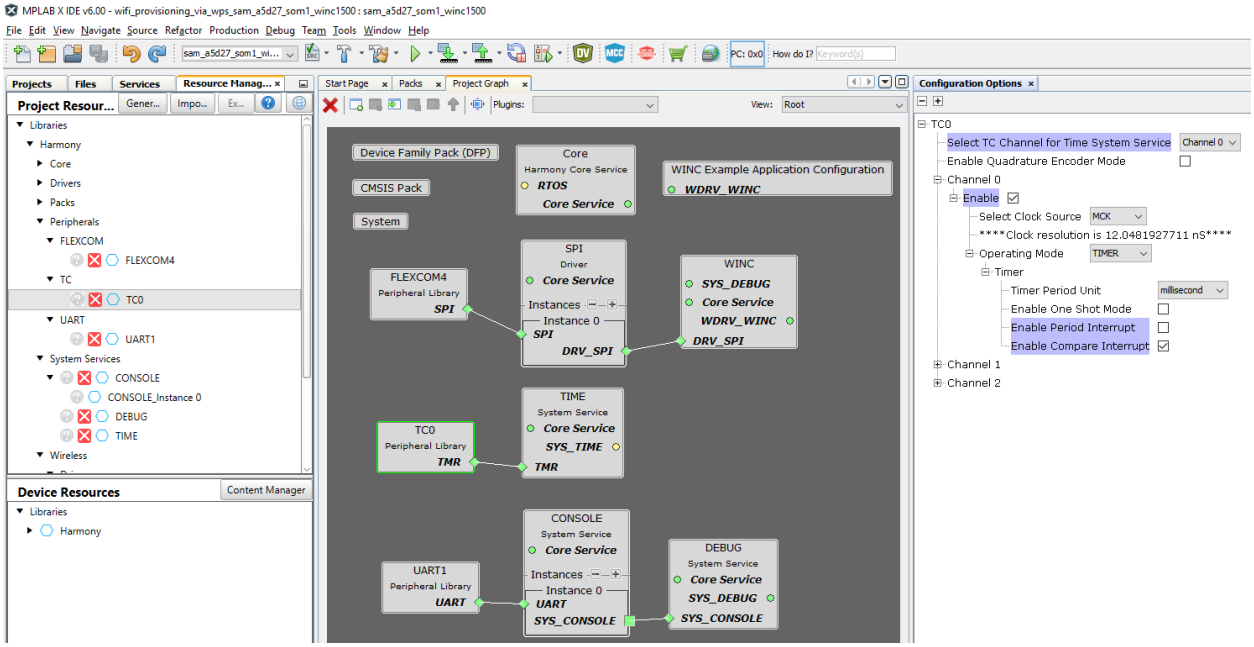
Debug



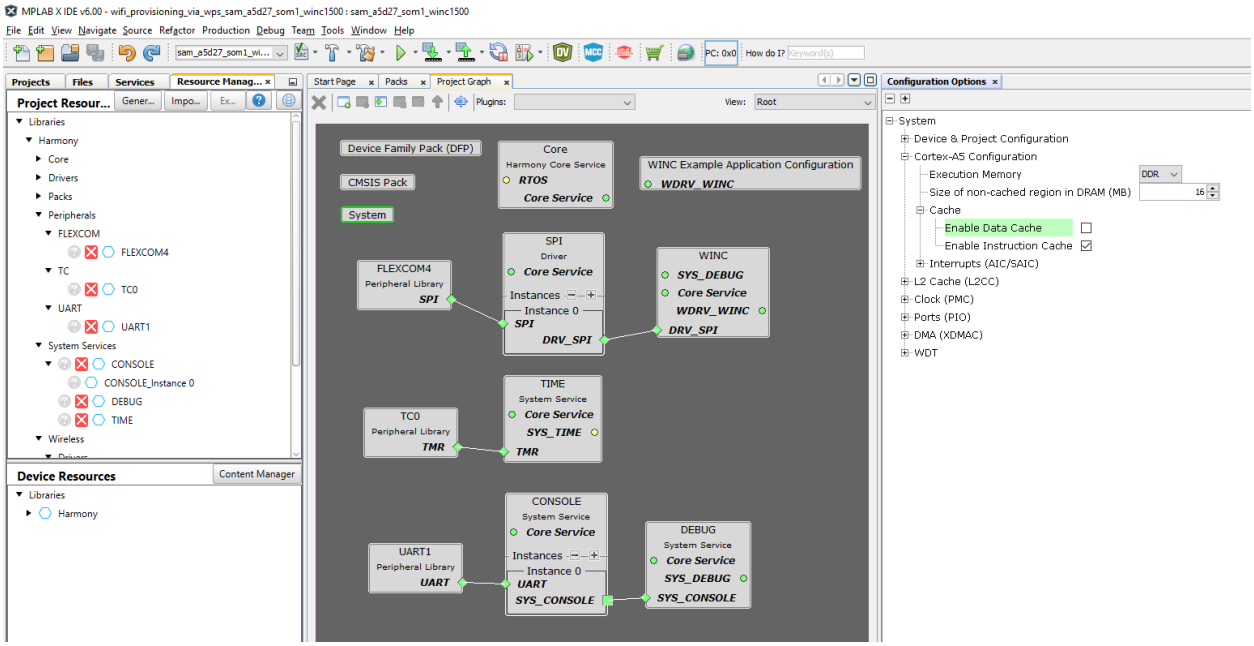
Time


MPLAB X IDE v6.00 - wifi_provisioning_via_wps_sam_a5d27_som1_winc1500 : sam_a5d27_som1_winc1500
File Edit View Navigate Source Refactor Production Debug Team Tools Window Help
Projects Files Services Resource Manag...
Project Resour...
Libraries
Harmony
Core
Drivers
Packs
Peripherals
FLEXCOM
FLEXCOM4
TC
UART
UART1
System Services
CONSOLE
CONSOLE_Instance 0
DEBUG
TIME
Wireless
Drivers
Device Resources
Content Manager
Libraries
Harmony
Start Page
Packs
Project Graph
Plugins:
View: Root
Device Family Pack (DFP)
CMSIS Pack
System
Core
Harmony Core Service
RTOS
Core Service
WINC Example Application Configuration
WDRV_WINC
SPI
Driver
Core Service
Instances
Instance 0
SPI
DRV_SPI
FLEXCOM4
Peripheral Library
SPI
WINC
SYS_DEBUG
Core Service
WDRV_WINC
DRV_SPI
TIME
System Service
Core Service
SYS_TIME
TMR
TC0
Peripheral Library
TMR
CONSOLE
System Service
Core Service
Instances
Instance 0
UART
SYS_CONSOLE
UART1
Peripheral Library
UART
DEBUG
System Service
Core Service
SYS_DEBUG
SYS_CONSOLE
Configuration Options
TIME
Use Systick?
PLIB Used
TC0
Number of Clients
5
Operating Mode
TICKLESS

TC0


MPLAB X IDE v6.00 - wifi_provisioning_via_wps_sam_a5d27_som1_winc1500 : sam_a5d27_som1_winc1500
File Edit View Navigate Source Refactor Production Debug Team Tools Window Help
Projects Files Services Resource Manag...
Project Resour...
Libraries
Harmony
Core
Drivers
Packs
Peripherals
FLEXCOM
FLEXCOM4
TC
TC0
UART
UART1
System Services
CONSOLE
CONSOLE_Instance 0
DEBUG
TIME
Wireless
Device Resources
Content Manager
Libraries
Harmony
Start Page
Packs
Project Graph
Plugins:
View: Root
Device Family Pack (DFP)
CMSIS Pack
System
Core
Harmony Core Service
RTOS
Core Service
WINC Example Application Configuration
WDRV_WINC
SPI
Driver
Core Service
Instances
Instance 0
SPI
DRV_SPI
FLEXCOM4
Peripheral Library
SPI
WINC
SYS_DEBUG
Core Service
WDRV_WINC
DRV_SPI
TIME
System Service
Core Service
SYS_TIME
TMR
TC0
Peripheral Library
TMR
CONSOLE
System Service
Core Service
Instances
Instance 0
UART
SYS_CONSOLE
UART1
Peripheral Library
UART
DEBUG
System Service
Core Service
SYS_DEBUG
SYS_CONSOLE
Configuration Options
TC0
Select TC Channel for Time System Service
Channel 0
Enable Quadrature Encoder Mode
Channel 0
Enable
Select Clock Source
MCK
****Clock resolution is 12.0481927711 nS****
Operating Mode
TIMER
Timer
Timer Period Unit
millisecond
Enable One Shot Mode
Enable Period Interrupt
Enable Compare Interrupt
Channel 1
Channel 2

System


MPLAB X IDE v6.00 - wifi_provisioning_via_wps_sam_a5d27_som1_winc1500 : sam_a5d27_som1_winc1500
File Edit View Navigate Source Refactor Production Debug Team Tools Window Help
Projects Files Services Resource Manag...
Project Resour...
Libraries
Harmony
Core
Drivers
Packs
Peripherals
FLEXCOM
FLEXCOM4
TC
TC0
UART
UART1
System Services
CONSOLE
CONSOLE_Instance 0
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Content Manager
Libraries
Harmony
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CMSIS Pack
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Core Service
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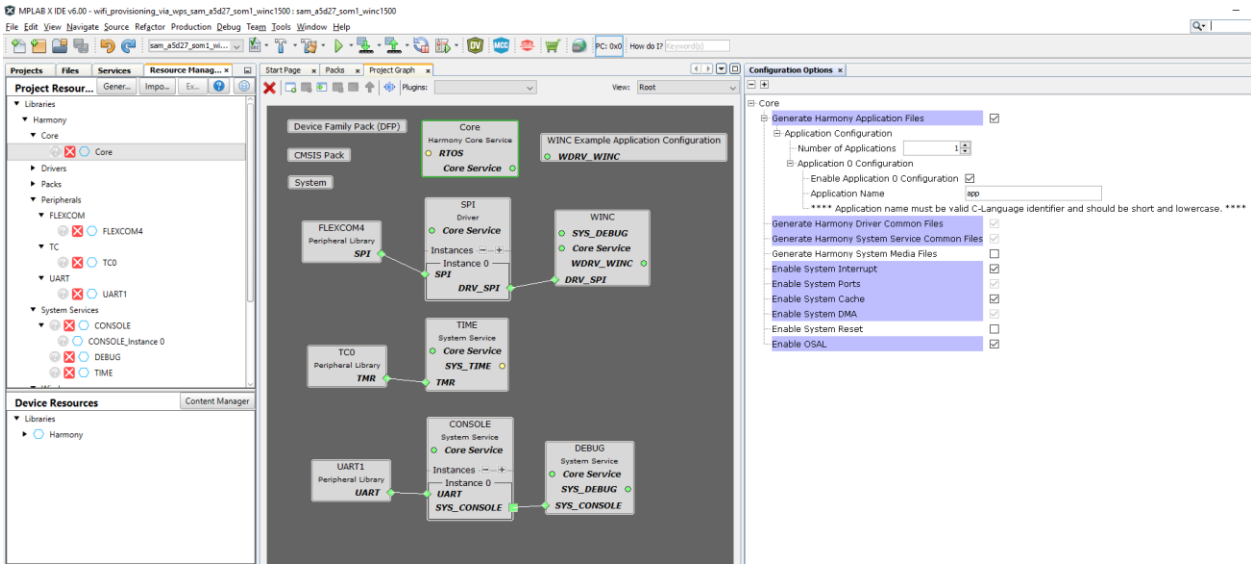
WDRV_WINC
FLEXCOM4
Peripheral Library
SPI
SPI
Driver
Core Service
Instances
Instance 0
SPI
DRV_SPI
WINC
SYS_DEBUG
Core Service
WDRV_WINC
DRV_SPI
TC0
Peripheral Library
TMR
TIME
System Service
Core Service
SYS_TIME
TMR
UART1
Peripheral Library
UART
CONSOLE
System Service
Core Service
Instances
Instance 0
UART
SYS_CONSOLE
DEBUG
System Service
Core Service
SYS_DEBUG
SYS_CONSOLE
Configuration Options
System
Device & Project Configuration
Cortex-A5 Configuration
Execution Memory
DDR
Size of non-cached region in DRAM (MB)
16
Cache
Enable Data Cache
Enable Instruction Cache
Interrupts (AIC/SAIC)
L2 Cache (L2CC)
Clock (PMC)
Ports (PIO)
DMA (XDMAC)
WDT

Core


MPLAB X IDE v6.00 - wifi_provisioning_via_wps_sam_a5d27_som1_winc1500 : sam_a5d27_som1_winc1500
File Edit View Navigate Source Refactor Production Debug Team Tools Window Help
Projects Files Services Resource Manag...
Project Resour...
Libraries
Harmony
Core
Core
Drivers
Packs
Peripherals
FLEXCOM
FLEXCOM4
TC
TC0
UART
UART1
System Services
CONSOLE
CONSOLE_Instance 0
DEBUG
TIME
Device Resources
Content Manager
Libraries
Harmony
Start Page
Packs
Project Graph
Plugins:
View: Root
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CMSIS Pack
System
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Harmony Core Service
RTOS
Core Service
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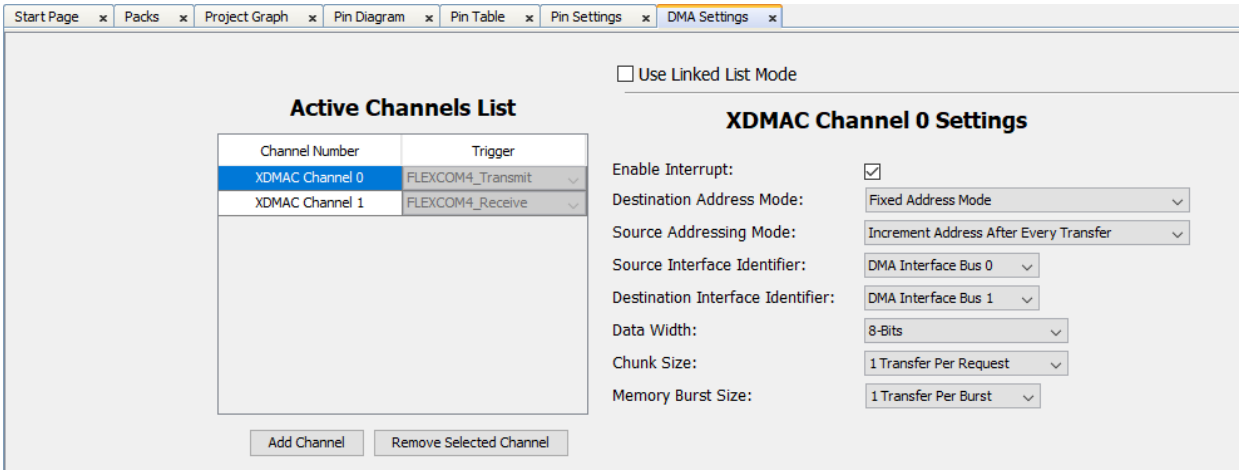
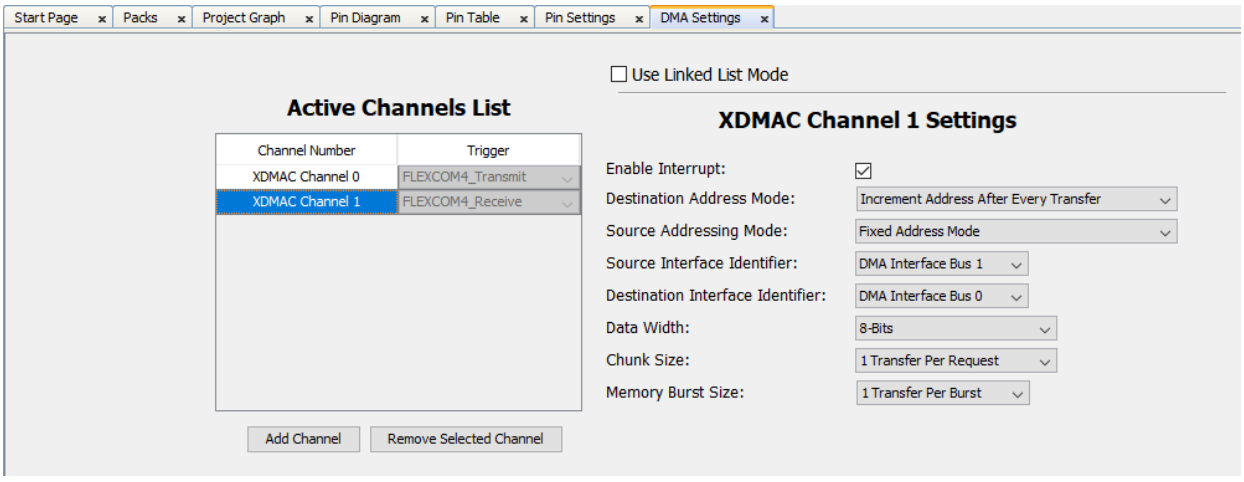
WDRV_WINC
FLEXCOM4
Peripheral Library
SPI
SPI
Driver
Core Service
Instances
Instance 0
SPI
DRV_SPI
WINC
SYS_DEBUG
Core Service
WDRV_WINC
DRV_SPI
TC0
Peripheral Library
TMR
TIME
System Service
Core Service
SYS_TIME
TMR
UART1
Peripheral Library
UART
CONSOLE
System Service
Core Service
Instances
Instance 0
UART
SYS_CONSOLE
DEBUG
System Service
Core Service
SYS_DEBUG
SYS_CONSOLE
Configuration Options
Core
Generate Harmony Application Files
Application Configuration
Number of Applications
1
Application 0 Configuration
Enable Application 0 Configuration
Application Name
app
**** Application name must be valid C-Language identifier and should be short and lowercase. ****
Generate Harmony Driver Common Files
Generate Harmony System Service Common Files
Generate Harmony System Media Files
Enable System Interrupt
Enable System Ports
Enable System Cache
Enable System DMA
Enable System Reset
Enable OSAL

PIN Configuration

Pin Number	Pin ID	Custom Name	Function	Direction	Latch	Open Drain	PIO Interrupt	Pull Up	Pull Down	Drive Strength	Glitch/Debounce Filter
F6	PC28		FLEXCOM4_IO0	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
B9	PC29		FLEXCOM4_IO1	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
E6	PC30		FLEXCOM4_IO2	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
E7	PD0		FLEXCOM4_IO4	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
C7	PB2	WDRV_WINC_RESETN	GPIO	Out	High	☐	Disabled	☐	☐	Low drive	Disabled
F5	PB0	GPIO_PB0	GPIO	In	n/a	☐	Falling Edge	☑	☐	Low drive	Disabled
L5	PD25	WDRV_WINC_CHIP_EN	GPIO	Out	High	☐	Disabled	☐	☐	Low drive	Disabled
J1	PD3		UART1_UTXD1	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
D8	PD2		UART1_URXD1	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled

DMA Configuration





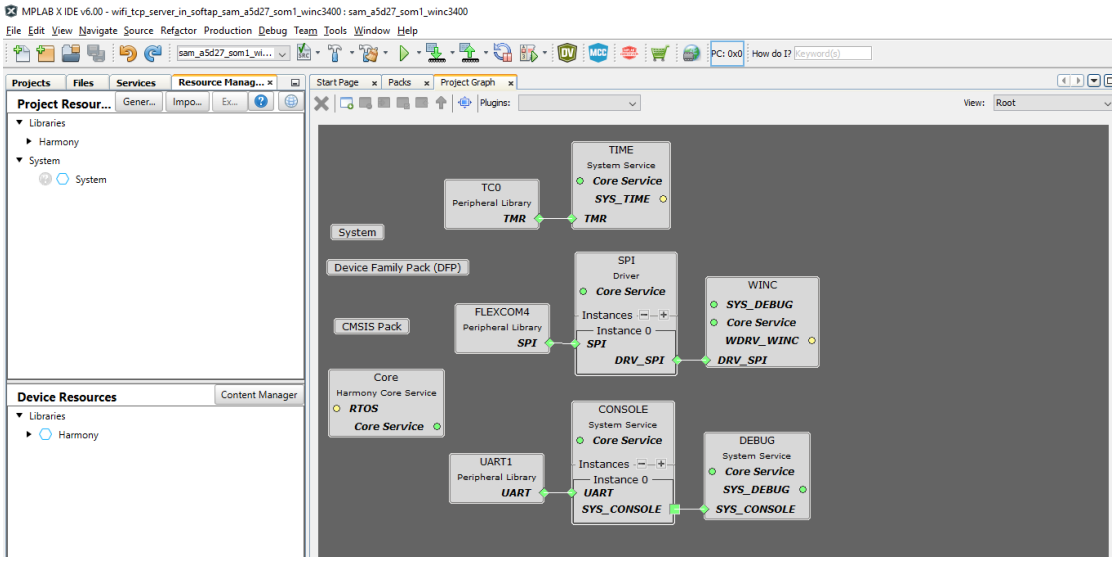
AIC Configuration

Start Page | Packs | Project Graph | Pin Diagram | Pin Table | Pin Settings | AIC Configuration

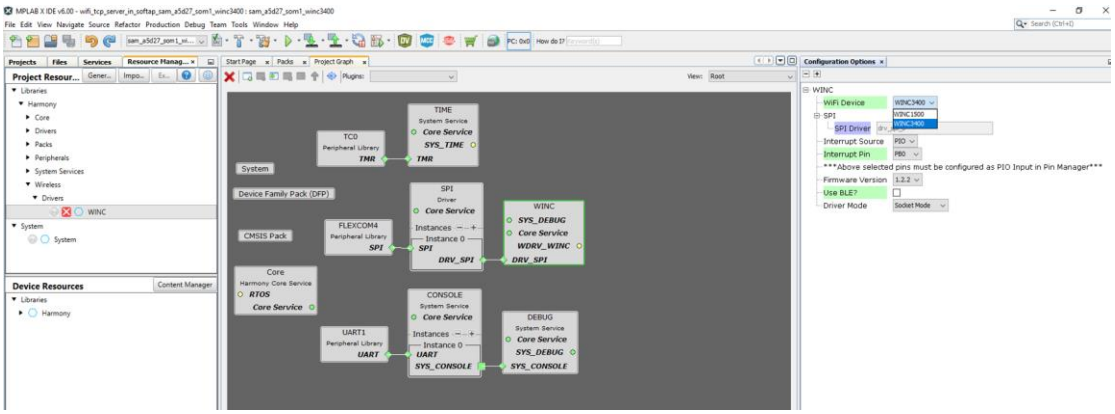
Vector	Enable	Handler Name	Map Type	Source Type	Priority
6) XDMAC0_IRQn - DMA Controller 0	☑	XDMAC0_InterruptHan...	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority
23) FLEXCOM4_IRQn - FLEXCOM 4	☑	FLEXCOM4_InterruptH...	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority
25) UART1_IRQn - UART 1	☑	UART1_InterruptHandler	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority
35) TC0_IRQn - Timer Counter 0 (ch. 0, 1, 2)	☑	TC0_InterruptHandler	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority
68) PIOB_IRQn - Parallel I/O Controller	☑	PIOB_InterruptHandler	NonSecure	High-level sensitive for internal source. Low-level sensitive for external source	Minimum priority

6. wifi_tcp_server_in_softap

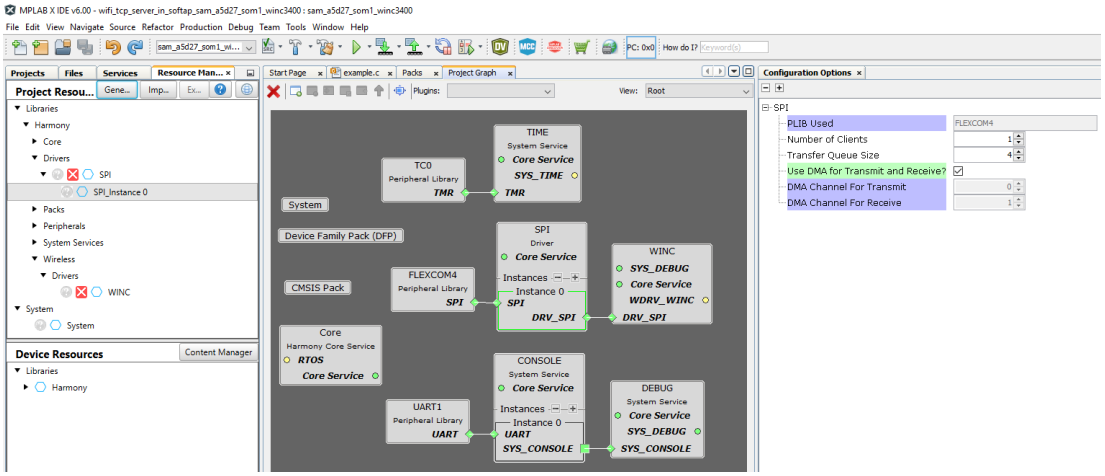
Project graph



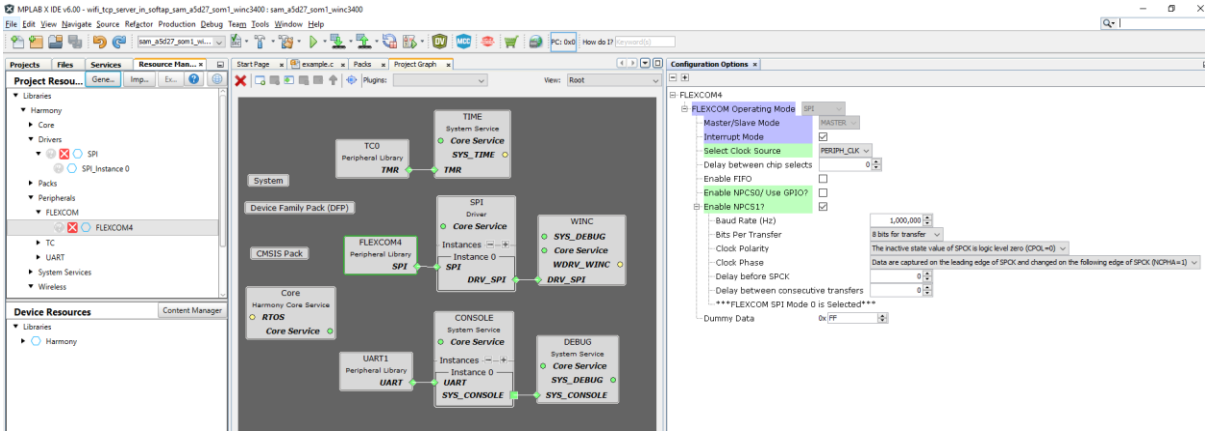
WINC Driver Configuration



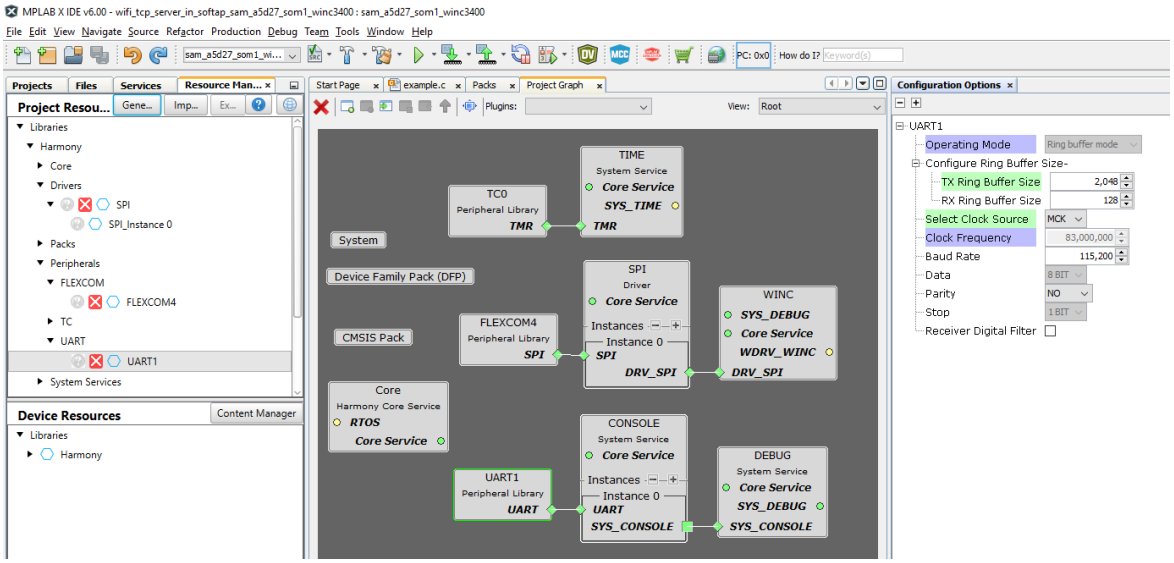
SPI Driver



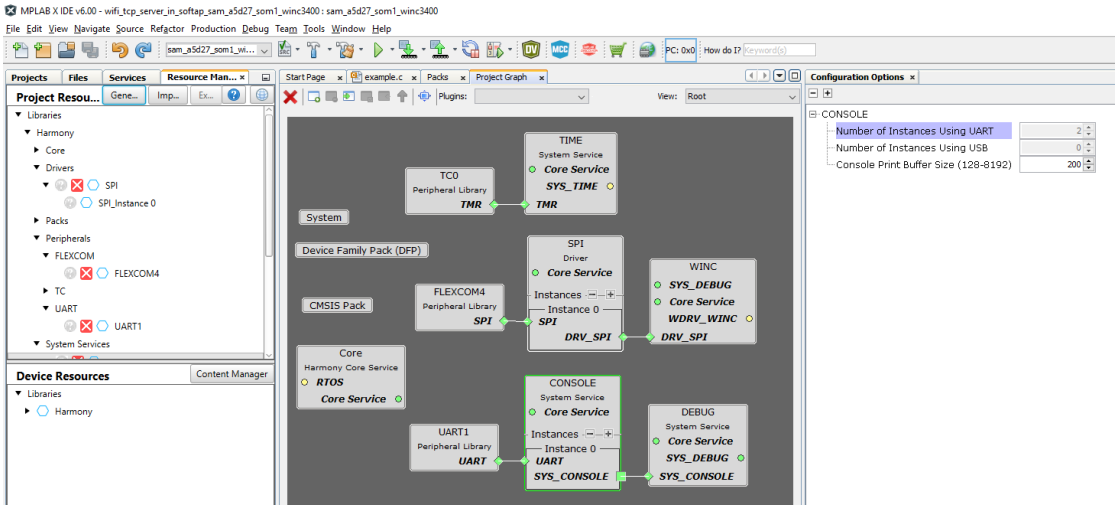
FLEXCOM4_SPI



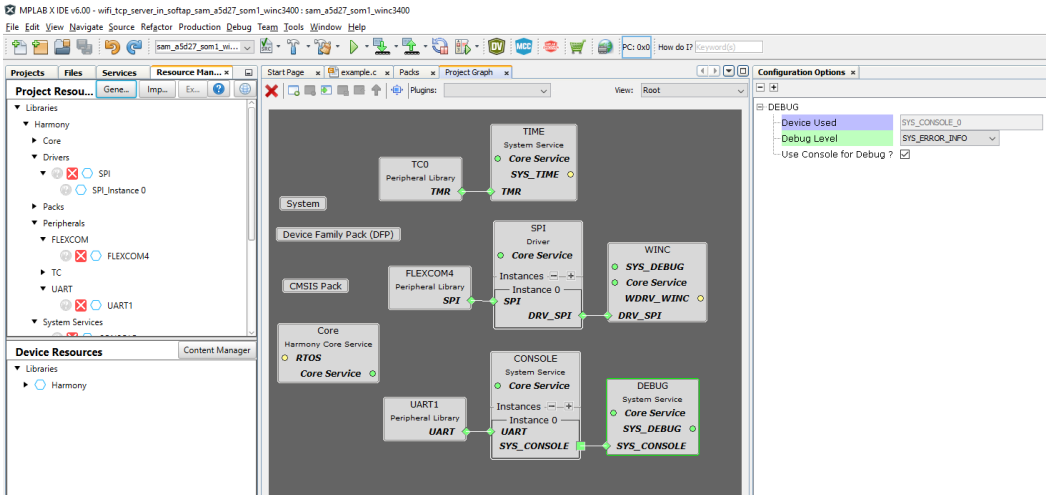
UART(UART1)



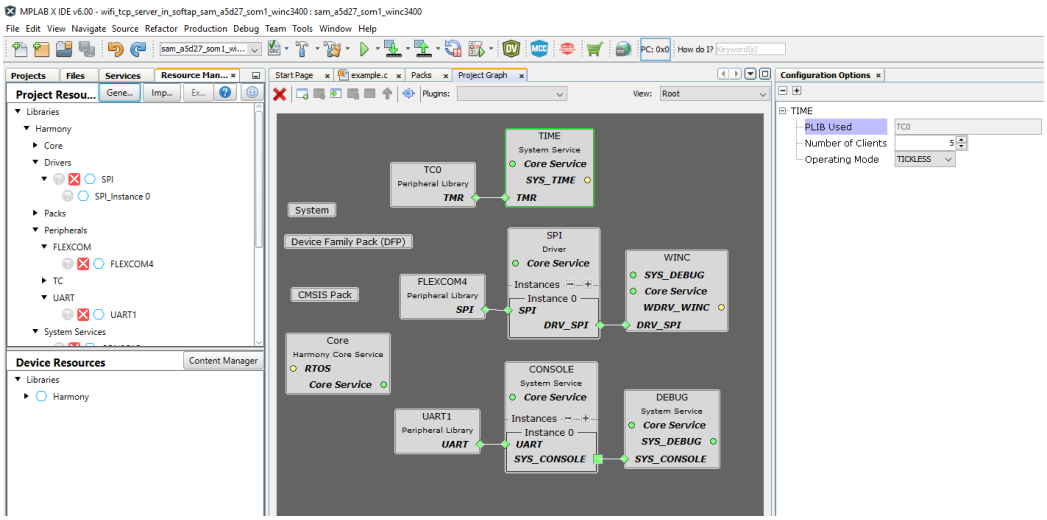
Console



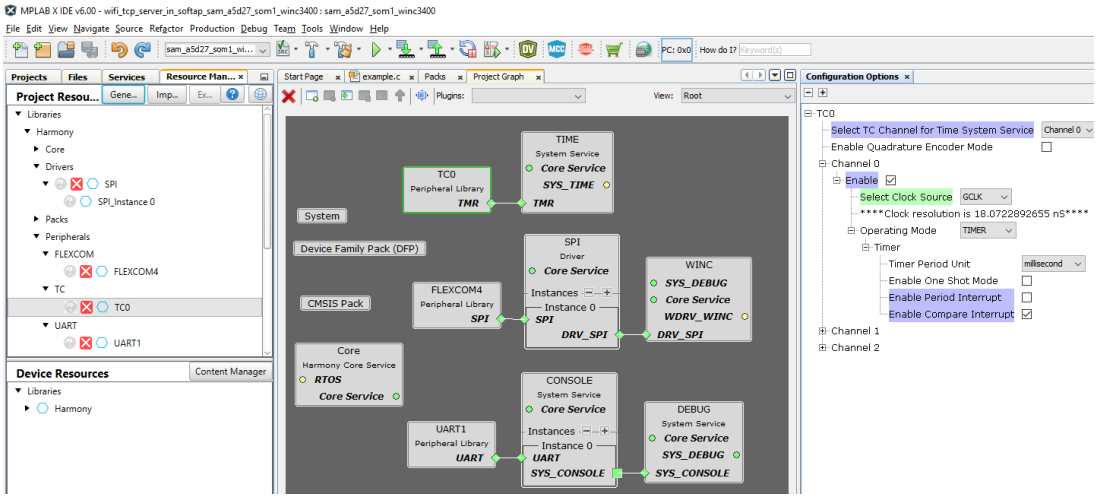
Debug



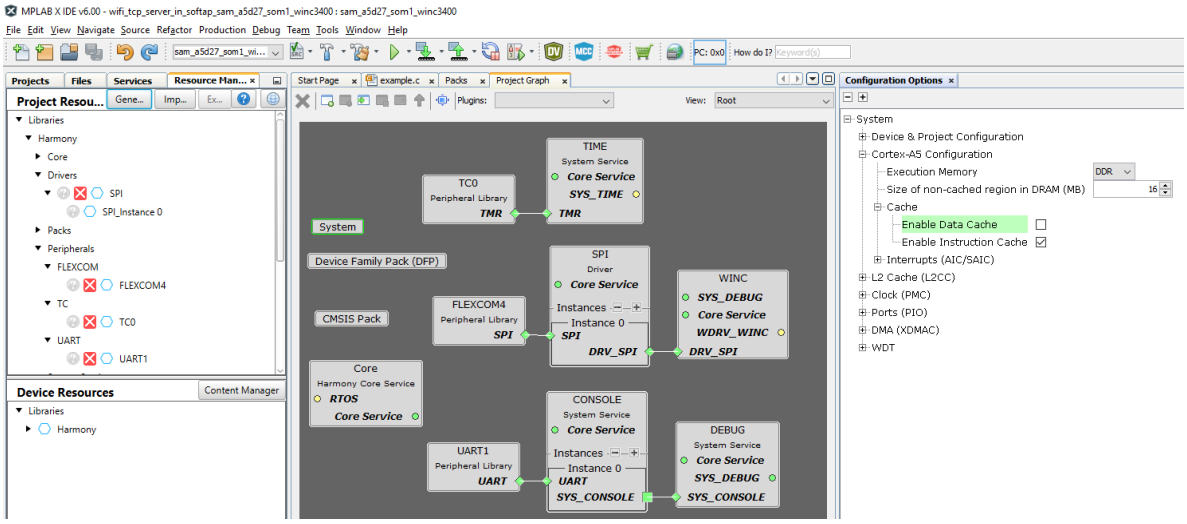
Time



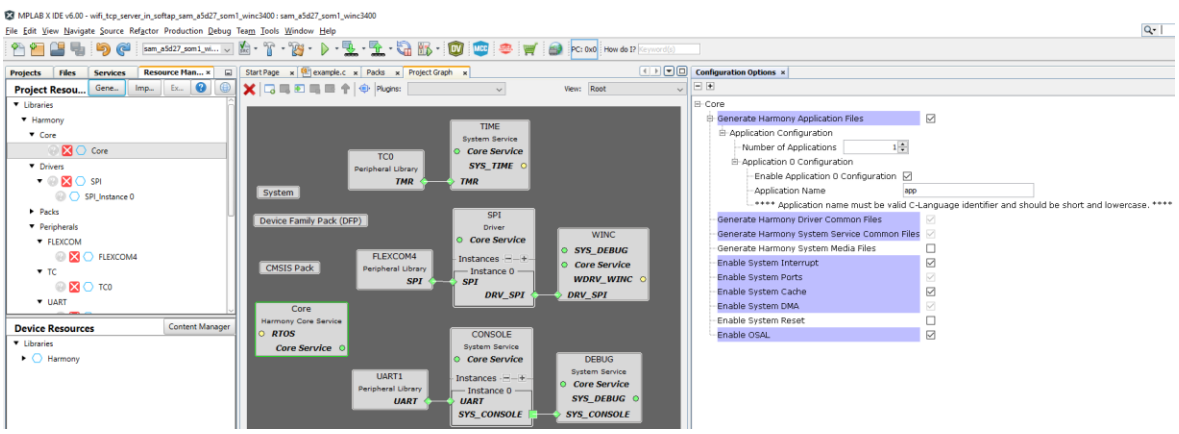
TC0



System



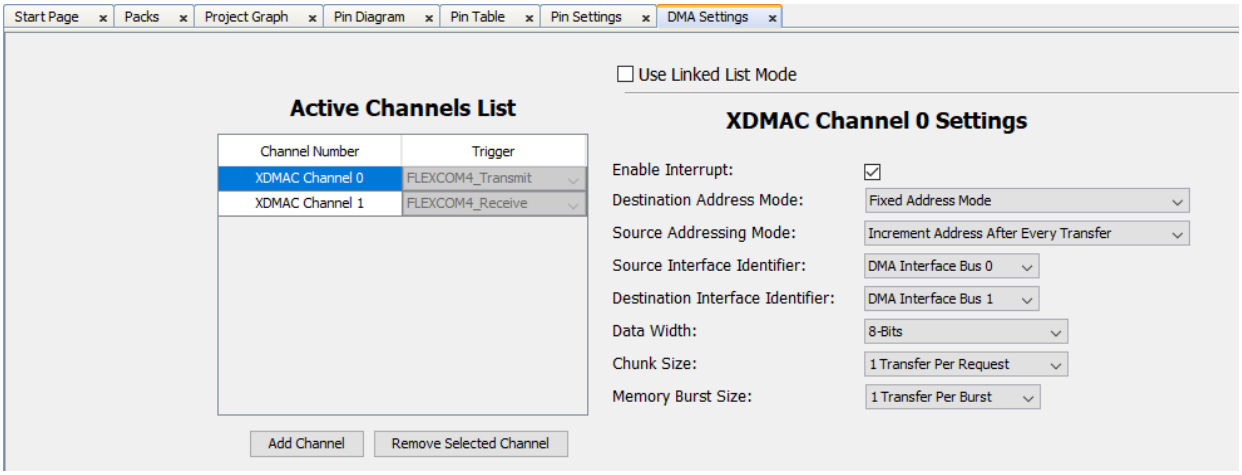
Core

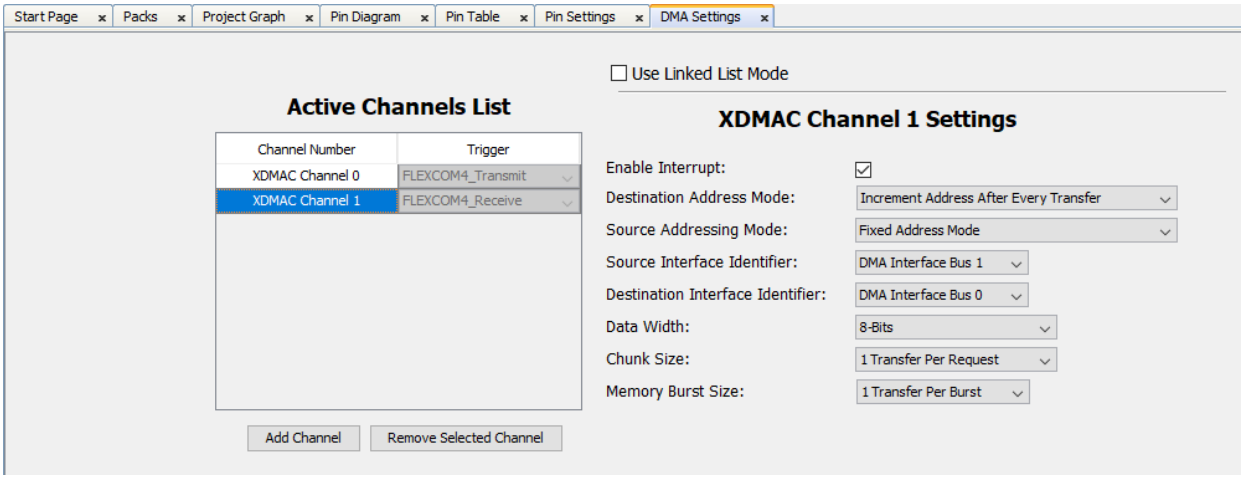
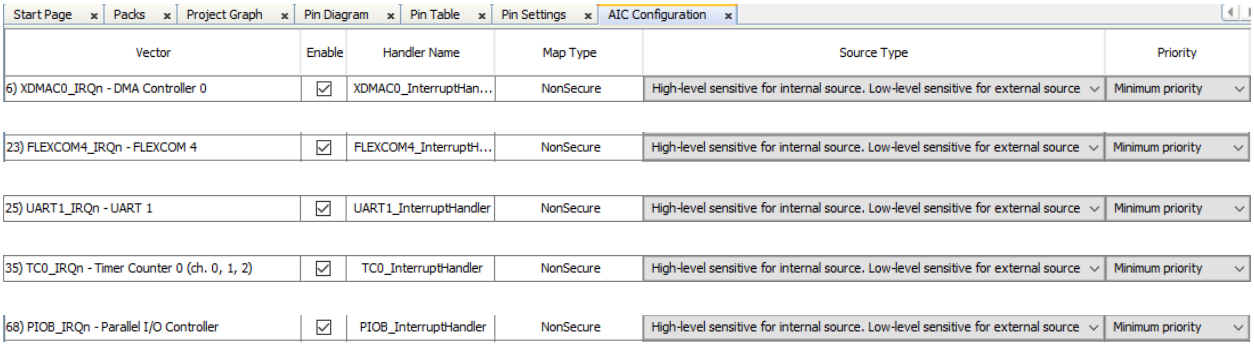


PIN Configuration

Pin Number	Pin ID	Custom Name	Function	Direction	Latch	Open Drain	PIO Interrupt	Pull Up	Pull Down	Drive Strength	Glitch/Debounce Filter
F6	PC28		FLEXCOM4_IO0	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
B9	PC29		FLEXCOM4_IO1	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
E6	PC30		FLEXCOM4_IO2	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
E7	PD0		FLEXCOM4_IO4	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
C7	PB2	WDRV_WINC_RESETN	GPIO	Out	High	☐	Disabled	☐	☐	Low drive	Disabled
F5	PB0	GPIO_PB0	GPIO	In	n/a	☐	Falling Edge	☑	☐	Low drive	Disabled
L5	PD25	WDRV_WINC_CHIP_EN	GPIO	Out	High	☐	Disabled	☐	☐	Low drive	Disabled
J1	PD3		UART1_UTXD1	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled
D8	PD2		UART1_URXD1	n/a	n/a	☐	Disabled	☐	☐	Low drive	Disabled

DMA Configuration





AIC Configuration