

AUTHOR: COLIN O'FLYNN**KEYWORDS:** XRAM, FRAM, EXTERNAL MEMORY

This document is originally distributed by AVRfreaks.net, and may be distributed, reproduced, and modified without restrictions. Updates and additional design notes can be found at: www.AVRfreaks.net

Interfacing Parallel FRAM to AVR Microcontrollers

Introduction

Ferromagnetic Random Access Memory (FRAM for short) is a new type of non-volatile memory that has the speed and durability of RAM, but doesn't lose its data on Power-off. FRAM is manufactured by a company called Ramtron International Corporation, their website is <http://www.ramtron.com>.

Overview

This design note is about interfacing parallel FRAM to AVR's that have a built-in XRAM interface. You cannot just hook up a parallel FRAM chip like it was a normal SRAM chip, using a latch. The problem is that the FRAM chips requires that the \overline{CE} signal be driven high and low, whereas a normal SRAM chip only requires that you connect the \overline{CE} signal to ground when you want to enable the chip (which is normally all the time).

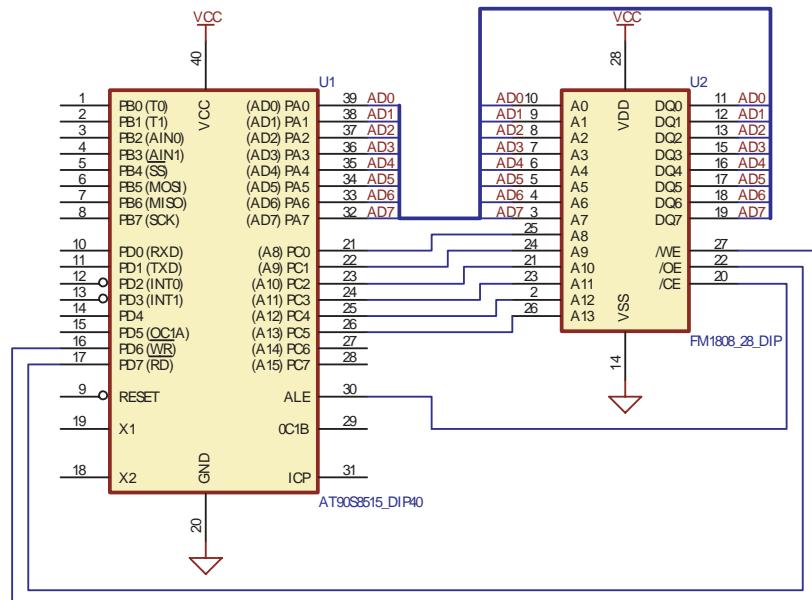
However, because of the way the AVR is made and the way the FRAM chip is made, the process of interfacing an FRAM to an AVR is much easier than a normal SRAM chip. The FRAM chip will latch the address on the falling edge of \overline{CE} , and in a normal SRAM chip the external latch will latch the address of the falling edge of ALE from the AVR, so you can forgo the external latch altogether.

The schematic shows you how to connect the FRAM chip to the AVR. Note that this schematic does not show proper connection of AVR (i.e., crystal is missing), it shows the proper connection of the AVR pins to the FRAM pins.

You can now access the FRAM chip like a normal SRAM chip, setting the appropriate bits as described in the AVR data sheet for your AVR chip. Note that you may need to use wait states though, as the AVR running at higher speeds may outpace the FRAM chip. Consult the timing diagrams of the FRAM chip and the AVR microcontroller XRAM interface to decide if you need wait states or not, making sure that your AVR will satisfy all the minimum timing requirements. Also it would be a good idea to run the "SRAM Tester" available from the AVRfreaks.net academy to test all memory locations.

The Ramtron web site has additional important information on the FRAM chips, and it is highly recommended that you read the entire datasheet for the parallel FRAM you choose.

Figure 1. FRAM Schematics



STK500/STK501

If you wish to use an FRAM chip on the STK501 you cannot just solder it onto the provided pads. The main reason being that the pin-outs of the FRAM chip is not compatible with the pin-out of the STK501 SRAM pad, but also you would need to modify your STK501 to work with the FRAM chip. Instead, simply make an adapter board that plugs into expansion slot 0 on the STK500 or STK501 and connects to the FRAM (the ALE signal and likely the RD and WR are not available on the expansion slots though, so you will need to use wires to connect the \overline{CE} , WR, and RD signals on the FRAM to the STK500).

You will have to be careful of capacitive loading on the lines to the FRAM chip though, you may end up having to use the low-voltage version of the chip (and a lower voltage V_{CC}) to meet the minimum timing requirements. Also adding pull-downs on some of the FRAM lines may help you run the FRAM chip at a higher (i.e., 5) voltage.