Signal	Wire ID	Wire Status	Edge A	Edge B	T-3.25ms	T-2.75ms	T-2.25ms	T-1.75ms	T-1.25ms	T-750us	T-250us , , ,]	T+250us	T+750us
TXdata	DO	Т	Ĺ						1				
RXdata	D1	Т		ı									
+tx to display			•		(63h) 4Eh	(09h (4Fh (0A	h (16h) (16h)—						
+from display				•	1	1	1	 	 	 		06h	

CLK1 Freq: 0Hz

D3 Period: 111.982us

Interval T->C: 255.5us

D1 Transitions A->R: 0

UART.LPF

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This diagram is a screenshot of the logic analyzer monitoring the TXdata command to shift a block (micro to uOLED module) and the ACK response from the uOLED module on RXdata.

The command begins with 63h followed by the starting (x,y) coordinates, the destination (x,y) coordinates, and the size of the bock (16h wide and 16h high).

The ACK response (06h) from the uOLED module arrives after approximately 2 msec.