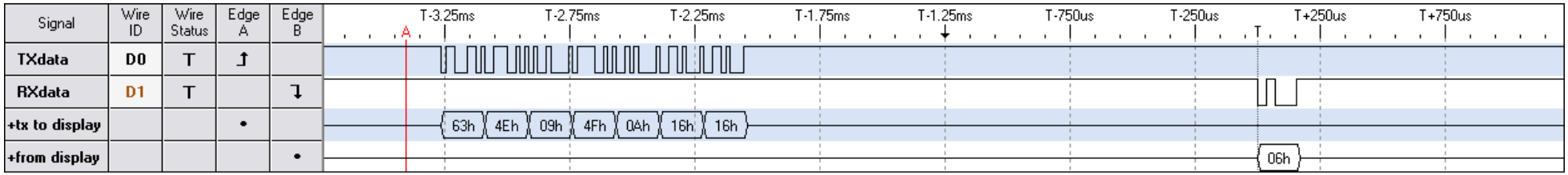

CLK1 Freq: 0Hz **D3 Period: 111.982us** **Interval T->C: 255.5us** **D1 Transitions A->R: 0**

UART.LPF **4/9/2008 10:05:05 AM**

This diagram is a screenshot of the logic analyzer monitoring the TXdata command to shift a block (micro to uOLED module) and the ACK response from the uOLED module on RXdata.
The command begins with 63h followed by the starting (x,y) coordinates, the destination (x,y) coordinates, and the size of the bock (16h wide and 16h high).
The ACK response (06h) from the uOLED module arrives after approximately 2 msec.