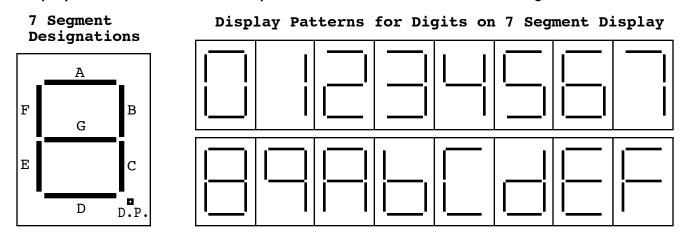
ATMega8 Hexadecimal Display Decoder/Driver/Latch for Dual 7/10/14 Segment L.E.D Displays

/RESET(Display Blank)——— D0—————————————————————————————————	1 ATMega8 2 3	28 — Digit 2 CC (High Order) 27 — Digit 1 CC (Low Order) 26 — J
D2 — — — — — — — — — — — — — — — — — — —	456	25 H 24 G2 23 G/G1
B VCC C GND H 7/10 Segment Select ∞ LATCH D5	7 8 9 10 11	22 —— GND 21 —— N/C 20 —— Vcc 19 —— F 18 —— E 17 —— D
D7 — A ——	13 14	16 ————————————————————————————————————

Application Description:

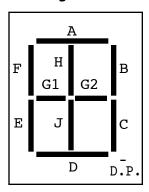
This program allows the AVR ATMega8 microcontroller to act as a dual digit display driver for a hexadecimal display. The microcontroller can drive either two seven segment LED displays (or a dual 7-segment LED display), or two 10 segment LED displays (or a dual 10 segment LED display.) 14 or 15 segment displays may be used in place of a 10 segment display, but only 10 segments are used.

One data byte is decoded to two hexadecimal digits, and the appropriate LED segments are driven for each digit. Output follows input when LATCH is low. When LATCH is high, the output reflects the last input received while LATCH was low. Display will be blanked at start up, and will remain blank until LATCH goes low.

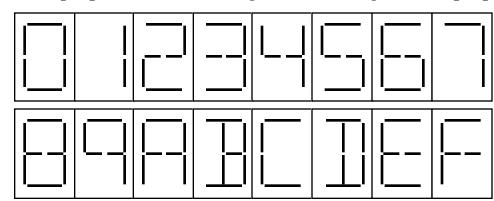


For use with M8DualHexDisplayDriver programs. Mark Graybill 10Apr2009

10 Segment Designations



Display Patterns for Digits on 10 Segment Display



Input Signal Descriptions:

D0-D3: Latched Data Inputs. D0=LSb, D3=MSb.

LATCH: When low, outputs follow inputs. When high, last data value obtained when low is retained on outputs.

7/10 Segment Select: Tie line high for 7 segment displays or low for 10 segment displays. This line is sampled only at startup, perform a /RESET or power cycle to change the character set used.

/RESET: Tie high for most applications, can be used for display blanking if uC startup time is not a problem for the application.

Output Signal Descriptions:

A-J: LED Segment driver outputs. Active high for use with common cathode displays. To use common anode displays, invert the signals or modify the program data for the character patterns. For 7 segment displays only A through G are used. To ease the use of 10 segment displays with the 7 segment character set, the G2 output will mirror that of G. When 7 segments are selected.

Digit 1 CC: Common cathode digit driver for low order digit (D0..3). Active low. For common anode displays, invert the signal or modify the program.

Digit 2 CC: Common cathode digit driver for high order digit (D4..7). Active low. For common anode displays, invert the signal or modify the program.

Timing: With the internal oscillator programmed to run at 8MHz, the sample rate is nominally 400K samples per second. The actual sample rate will depend on the variance of the actual oscillator frequency from 8MHz. The program provides for an oscillator calibration value to be programmed into flash at location \$13 (decimal 19.)

The means the minimum pulse width on the latch going low is 250mS to be sure of the data value being sampled. This is far slower than, for example, a TIL311 display which is capable of ~7.3M samples/sec. Therefore, if faster response is required an octal latch should be placed on the data lines between the ATMega8 and the data source, e.g. a 74HC373, with the 373's gate used to latch the data.

Full details of the operation of the program are included in the comments in the M8DualHexDisplayDriver.asm file, including pinouts, wiring diagrams, timing details, suggestions for use and extension, etc.

For use with M8DualHexDisplayDriver programs. Mark Graybill 10Apr2009