CN1

Pin	Signal
1	MOSI_PB0
2	MISO_PB1
3	SCK_PB2
4	PB3
5	PB4
6	+5V
7	GND
8	GND

GND

+5V

C3

GND

JP1

VTG	2	1	MISO
RST	5	4	MOSI
GND	6	3	SCK

AVR ISP

GND

RESET

JP2

JP3

Q1

XTAL1_PB3

XTAL2_PB4

C1

C2

GND

GND

IC1
ATTINY45-20P

(MOSI/DI/SDA/AIN0/OC0A/OC1A/AREF/PCINT0)PB0 — 5
(MISO/DO/AIN1/OC0B/OC1A/PCINT1)PB1 — 6
(SCK/USCK/SCL/ADC1/T0/INT0/PCINT2)PB2 — 7
(XTAL1/CLKI/OC1B/ADC3/PCINT3)PB3 — 2
(XTAL2/CLKO/OC1B/ADC2/PCINT4)PB4 — 3
(RESET/DW/ADC0/PCINT5)PB5 — 1

8 — VCC
4 — GND

R1

+5V

H1
MOUNT-PAD-ROUND3.0

H2
MOUNT-PAD-ROUND3.0

H3
MOUNT-PAD-ROUND3.0

H4
MOUNT-PAD-ROUND3.0

C1, C2=22p
C3=100n
R1=4K7
Q1=crystal 4-20MHZ
JP1=2X3 pin header
JP2, JP3=3-pin header
CN1=8-pin header

Dselec   http://dselec.wordpress.com

TITLE: ATtiny45 development board

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GND
+5V
PB4
PB3
PB2
PB1
PB0

CN1

1

JP1

1

C3

IC1

R1

JP2

3 2 1

Q1

C1

JP3

3 2 1

C2