# Class B Library Help

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# 1 Introduction



**Introduction**

This document describes the Class B Safety Software Library routines that detect the occurrence of Faults in a single channel CPU. These routines have been developed in accordance with the IEC 60730 standard to support the Class B certification process. These routines can be directly integrated with the end user's application to test and verify the critical functionalities of a controller without affecting the end

user's application. The Class B safety software routines can be called periodically at start-up or run time to test the following components:

• CPU Registers

• CPU Program Counter

• Invariable Memory

• Variable Memory

• Clock

**Hardware Setup :**

The Explorer 16 Development Board and two PIC24F and dsPIC33 plug-in modules are used for demonstrating the Class B Library functionality.

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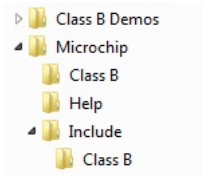
# 3 Getting Started

The folder structure of Class B Software Library is shown below:




The library specific folders are the following:

• The ...\Class B Demo folder will contain the library demo projects.

• The ...\Microchip folder will contain the library components.

• The ...\Help sub-folder under ..\Microchip folder will contain this document (Class B Library Help.chm file).

• The ...\Class B sub-folder under the ..\Microchip folder is where the C files related to the Class B library are located.

• The ...\Class B sub-folder under the Include folder is where the Header files related to the Class B library located.



## 3.1 Class B Library Files

The following files should be included in the project:

| | |
|---|---|
| **Common** | |
| classb.h | This file joins all definitions, macros and functions prototypes related to Class B library. To use the library API only this header can be included in the application code. |
| classb_config.h | Class B library configurations. |
| **RAM Tests** | |
| classb_marchc_.s | March C and March C Minus test routines. |
| classb_marchb_.s | March B test routines. |
| classb_checkerboard_.s | Checker Board test routines. |
| **CRC Checksum Calculation** | |
| classb_crc.c | CRC checksum calculation routines for Flash and EEPROM. |
| **MCU Registers Tests** | |
| classb_registers_.s | MCU registers test routines. |
| classb_pc.c | MCU program counter test routines. |
| **Clock Tests** | |
| classb_clock.c,<br>classb_clock_.s | Clock source test routines. |

# 3.2 Class B Library Configuration

The following Class B Library settings should be defined in classb_config.h file:

| | |
|---|---|
| **CLASSB_DEVICE_FLASH_SIZE_KB** | Device flash memory size in KBytes. This option is used by the program counter test. |
| **CLASSB_CLOCK_TEST_TIME_MS** | Clock test time in mS. Can be about 20 mS if clock is between 1-32MHz and the reference clock is 50Hz-33kHz. |
| **CLASSB_CLOCK_TEST_TIMER_ADDRESS** | Clock test hardware timer SFR address. The timer is used to count the reference clock pulses. |



# 3.3 Using API

The Class B Library doesn't require modifications of the linker script (.gld file). To use the library functions one header file "classb.h" must be included in the application source file. Also the library configuration "classb_config.h" file must exist in the application project. The interrupts must be disabled during the Class B library tests. The memory regions (start address and length) can be retrieved form the map file ("Generate map file" option in the "Diagnostic" group of the linker settings must be enabled). Or the basic memory map information can be found in "Build" window if the "Display memory usage" option is selected in "Diagnostic" group of the linker settings. The following code explains the Class B library test functions usage:

```
-------------------------------------------------------------------------------------------------------------
// CPU Registers test.
// Interrupts must be disabled during the test.
DisableInterrupts();
if (CLASSB_CPURegistersTest())
{
// ERROR IS DETECTED
while (1);
}
EnableInterrupts();

-------------------------------------------------------------------------------------------------------------
// CPU Program Counter test.
if(CLASSB_CPUPCTest())
{
// ERROR IS DETECTED
```

```
while (1);
}

-------------------------------------------------------------------------------------------------------------
// Checker board test.
// RAM tests memory of the .nbss section
// The linker has generated the following map information:
// Data Memory [Origin = 0x800, Length = 0x7800]
//
// section address alignment gaps total length (dec)
// ------- ------- -------------- -------------------
// .nbss 0x800 0 0xfa2 (4002)
//
// Total data memory used (bytes): 0xfa2 (4002) 13%

// Interrupts must be disabled during the test.
DisableInterrupts();
if (CLASSB_RAMCheckerboardTest(0x0800, // start address (must be aligned by word (2 bytes))
0x0fa2)) // length in bytes (must be even)
{
// ERROR IS DETECTED
while (1);
}
EnableInterrupts();

-------------------------------------------------------------------------------------------------------------
// March C test.
// !!!The selected memory region must not cross the buffer!!!
// Interrupts must be disabled during the test.
DisableInterrupts();
if (CLASSB_RAMMarchCTest(0x0850,  // start address (must be aligned by word (2 bytes))
sizeof(marchTestBuffer), // byte length (must be even number)
marchTestBuffer,  // buffer to store the tested memory content
false))
{
// ERROR IS DETECTED
while(1);
}
```

```
EnableInterrupts();


-------------------------------------------------------------------------------------------------------------
// March C Minus test.
// !!!The selected memory region must not cross the buffer!!!
// Interrupts must be disabled during the test.
DisableInterrupts();
if (CLASSB_RAMMarchCTest(0x0850,  // start address (must be aligned by word (2 bytes))
sizeof(marchTestBuffer), // byte length (must be even number)
marchTestBuffer,  // buffer to store the tested memory content
true))
{
// ERROR IS DETECTED
while(1);
}
EnableInterrupts();


-------------------------------------------------------------------------------------------------------------
//  March B test.
// !!!The selected memory region must not cross the buffer!!!
// Interrupts must be disabled during the test.
DisableInterrupts();
if(CLASSB_RAMMarchBTest((0x0850,  // start address (must be aligned by word (2 bytes))
sizeof(marchTestBuffer), // byte length (must be even number)
marchTestBuffer))  // buffer to store the tested memory content
{
// ERROR IS DETECTED
while(1);
}
EnableInterrupts();


-------------------------------------------------------------------------------------------------------------
//  Flash memory CRC.
// Calculate the check sum for interrupt vectors table and .text section.
// The linker has generated the following map information:
// Program Memory [Origin = 0x200, Length = 0x2a9fe]
//
// section address length (PC units) length (bytes) (dec)
```

```
// ------- ------- ----------------- --------------------
// .text 0x200 0xc0 0x120 (288)
// .text 0x2c0 0xa80 0xfc0 (4032)
// .dinit 0xd40 0x8 0xc (12)
// _03F32480_at_address_0000AAAA 0xaaaa 0x6 0x9 (9)
// _03F32400_at_address_00015554 0x15554 0x6 0x9 (9)
//
// Total program memory used (bytes): 0x10fe (4350) 1%

checkSum = CLASSB_CRCFlashTest(0x000000, // interrupt vectors table start address
0x000100, // 256 PC units (addressable bytes)
-1);  // initial seed is 0xffff

checkSum = CLASSB_CRCFlashTest(0x000200, // the first part of the .text
0x0000c0, // length in PC units (addressable bytes)
checkSum); // seed is the previous check sum


checkSum = CLASSB_CRCFlashTest(0x0002c0,  // the second part of the .text
0x000a80,  // length in PC units (addressable bytes)
checkSum); // seed is the previous check sum

-----------------------------------------------------------------------------------------------------------
// Clock test.
// Interrupts must be disabled during the test.
// The reference clock should be connected to the timer.The timer must be initialized by the application code
// to count the reference clock pulses. The period register must be set to the maximum value. The address of
// the timer counter register must be specified in classb_config.h using the compile time option
// CLASSB_CLOCK_TEST_TIMER_ADDRESS. There's a second compile option CLASSB_CLOCK_TEST_TIME_MS
// in the classb_config.h. It defines the test time and can be about 20 mS if clock is between 1-32MHz and the
// reference clock is 50Hz-33kHz.
DisableInterrupts();
if(CLASSB_ClockTest(32000000, // clock is 32 MHz
32768, // secondary oscillator frequency as reference
5)) // 0.5% tolerance limit
{
// ERROR IS DETECTED
while(1);
```

```
}
EnableInterrupts();
```

# 4 Tests Execution Time

The time was measured for clock source 32 MHz (16MIPS) and "S" code optimization option.

| Test Name | Test Function Name | Time |
|---|---|---|
| March C | CLASSB_RAMMarchCTest | 7.2 mS/KByte |
| March C Minus | CLASSB_RAMMarchCTest | 7.6 mS/KByte |
| March B | CLASSB_RAMMarchBTest | 12 mS/KByte |
| Checker Board | CLASSB_RAMCheckerboardTest | 110uS/KByte |
| Flash CRC | CLASSB_CRCFlashTest | 10 mS/KByte |
| EEPROM CRC | CLASSB_CRCEEPROMTest | 8 mS/KByte |
| MCU Registers | CLASSB_CPURegistersTest | 15 uS |
| MCU Program Counter | CLASSB_CPUPCTest | 2 uS |
| Clock Source | CLASSB_ClockTest | 10-40 mS |

# 5 API Reference

This section describes Class B library API.

## 5.1 Structures and Enumerations

In this section the library structures and enumerations are described.

### 5.1.1 CLASSBRESULT

**Description:** this enumeration is used by the class B test functions to return the result.

**Values:**

- **CLASSB_TEST_PASS** - the test finished successfully (**zero**).
- **CLASSB_TEST_FAIL** - the test is failed.
- **CLASSB_TEST_TIMEOUT** - the test is failed because a timeout was detected.

## 5.2 CLASSBRESULT CLASSB_RAMMarchBTest(startAddress, length, bufferAddress)

**Description:** This function tests the RAM region using march B algorithm. The interrupts must be disabled during the test.

**Parameters:**

- **startAddress** - the first address of the tested RAM memory (must be even number),
- **length** - the byte length of the tested RAM memory (must be even number),
- **bufferAddress** - the first address of the buffer to store the tested memory content (must be even number), if this parameter is NULL then tested memory will be cleared.

**Returns:**

- The test result (zero if successful).

# 5.3 CLASSBRESULT CLASSB_RAMMarchCTest(startAddress, length, bufferAddress, minus)

**Description:** This macro tests the RAM region using march C or march C minus algorithms. The interrupts must be disabled during the test.

**Parameters:**

- **startAddress** - the first address of the tested RAM memory (must be even number),
- **length** - the byte length of the tested RAM memory (must be even number),
- **bufferAddress** - the first address of the buffer to store the tested memory content (must be even number), if this parameter is NULL then tested memory will be cleared,
- **minus** - if the parameter is TRUE the "minus" algorithm is used.

**Returns:**

- The test result (zero if successful).

# 5.4 CLASSBRESULT CLASSB_RAMCheckerboardTest(startAddress, length)

**Description:** This function tests the RAM region using the checker board pattern. The interrupts must be disabled during the test.

**Parameters:**

- **startAddress** - the first address of the tested RAM memory (must be even number),
- **length** - the byte length of the tested RAM memory (must be even number).

**Returns:**

- Returns zero if successful. Non zero means - failed.

# 5.5 CLASSBRESULT CLASSB_CPURegistersTest()

**Description:** This function tests CPU registers. The interrupts must be disabled during the test.

**Returns:**

- The test result (zero if successful).

## 5.6 CLASSBRESULT CLASSB_CPUPCTest()

**Description:** This function tests the CPU program counter. The device flash memory size must be set using parameter CLASSB_DEVICE_FLASH_SIZE in classb_conig.h.

**Returns:**

- The test result (zero if successful).

## 5.7 uint16_t CLASSB_CRCFlashTest(startAddress, length, crcSeed)

**Description:** The function calculates the CRC check sum for the flash memory region. The start address and length must be even numbers (aligned by 2). The "length" parameter must be specified in PC units (addressable bytes, the PC units are used in map files).

**Parameters:**

- **startAddress** - the first address of the tested flash memory in bytes (must be even number),
- **length** - the length of the tested flash memory in PC units (must be even number),
- **crcSeed** - initial value of the CRC check sum.

**Returns:**

- The function returns the standard 16-bit CRC.

## 5.8 uint16_t CLASSB_CRCEEPROMTest(startAddress, length, crcSeed)

**Description:** The function calculates the CRC check sum for the EEPROM memory region. The start address and length must be even numbers (aligned by 2).

**Parameters:**

- **startAddress** - the first address of the tested EEPROM memory in bytes (must be even number),
- **length** - the byte length of the tested EEPROM memory (must be even number),
- **crcSeed** - initial value of the CRC check sum.

**Returns:**

- The function returns the standard 16-bit CRC.

# 5.9 CLASSBRESULT CLASSB_ClockTest(uint32_t clockFrequency, uint32_t referenceFrequency, uint16_t tolerance)

**Description:** The function tests the CPU clock source. The interrupts must be disabled during the test. The reference clock should be connected to the timer. The timer must be initialized by the application code to count the reference clock pulses. The period register must be set to the maximum value. The address of the timer counter register must be specified in classb_config.h using the compile time option CLASSB_CLOCK_TEST_TIMER_ADDRESS. There's another compile option CLASSB_CLOCK_TEST_TIME_MS in the classb_config.h. It defines the test time and can be about 20 mS if clock is between 1-32MHz and the reference clock is 50Hz-33kHz.

**Parameters:**

- **clockFrequency** - frequency of the clock source,
- **referenceFrequency** - frequency of the reference clock (such as power line or secondary oscillator),
- **tolerance** - maximum valid frequency tolerance, can be from 1(0.1%) to 10(1%).

**Returns:**

- Returns zero if successful. Non zero means - failed. See CLASSBRESULT enumeration for details.

# 6 Known Limitations

The limitations of Class B software library are listed below:

- The address and length of the tested memory are required by some test procedures. These parameters MUST be even numbers (aligned by 2).
- The interrupts must be disabled during the RAM, clock and CPU registers tests.

# 7 Resources

To get more information about Class B Library visit http://www.microchip.com/classb and read the following articles:

- AN1229 - Class B Safety Software Library for PIC® MCUs and dsPIC® DSCs

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