PIC32CXMTC MULTICHANNEL METROLOGY LIBRARY REFERENCE GUIDE – BETA VERSION

Author	Rev.	Date	Modification
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1 DEFINITIONS, ACRONYMS AND ABBREVIATIONS

Table 1-1. Abbreviations and Acronyms

Abbreviation	Description
ADC	Analog-to-Digital Converter of the AFE, consisting of a PGA, a Δ/Σ modulator, and followed by an integrated sinc decimation filter.
AFE	Analog Front End
BAMS	Binary Angular Measurement System. Angles are normalized to the binary range [-1.0000, +0.9999] k, where k may represent any convenient scale, such as 180°, or π-radians. In this metering discussion, all angles are drawn as if vectors starting to 0° (3 o'clock position) and rotating counter-clockwise for positive phase increases. Using BAMS allows for graceful rollover from ±180° to ∓180° without edge-effects.
CT	Current Transformer
Δ/Σ ADC	Delta-Sigma Analog-to-Digital Converter, an over-sampled converter with noise shaping
DSP	Digital Signal Processing
G_{PGA}	Gain selected for use in the ADC front end, G_{PGA}.
Kh	Watt-hour meter constant for electro-mechanical meters, defines an amount of energy indicated by one (1) pulse generated by the meter and does not usually apply to solid-state meters.
Kt	Watt-hour meter test constant for solid-state meters, defines an amount of energy indicated by one (1) optical pulse generated by the meter and does not usually apply to electro-mechanical meters.
MSB	Most Significant Bit, the left-most bit of a binary number.
N	The number of samples in any one measurement interval. This number may vary for each measurement interval.
OSR	Over Sample Rate
Qformat	To prevent ambiguity, this document uses the following definition of Qformat numbers, being a fixed-point number format representing both integer and fractional numbers, and may be unsigned (uQm.n) or signed (sQm.n). Unsigned Qformat numbers: An (m+n)-bit unsigned number is designated uQm.n. It occupies (m+n) bits and is stored as an unsigned fixed-point binary number. An unsigned uQm.n number may represent numbers in the range: $[0, +(2^m - 2^{-n})]$. Signed Qformat numbers: An (m+n+1)-bit signed number is designated sQm.n. It occupies (m+n+1) bits and is stored as a signed fixed-point binary number, where the MSB is used as a sign bit. A signed sQm.n number may represent numbers in the range: $[-(2^m), +(2^m - 2^{-n})]$. For example, an 8-bit sQ4.3 format number has one (1) sign bit, four (4) bits to the left of the binary point and three (3) bits to the right of the binary point and may be used to represent numbers in the range: $[-(2^4), +(2^4 - 2^{-3})]$ = [-16, +15.875]. To convert a sQm.n format number to a decimal equivalent, divide the equivalent twos-complement binary number by 2^n. For example: an 8-bit signed sQ2.5 number: [0b0100 0001] = $65/(2^5)$ = 2.03125, an 8-bit [0b1100 0001] = $-63/(2^5)$ = -1.96875. To convert a decimal number into a sQm.n format number, multiply by 2^n and convert to a signed two's-complement (m+n+1)-bit number. For example: -7.33 => sQ3.4: $(-7.33)*(2^4)$ = -117 => -[0b0111 0101] => [0b1000 1011]. Example-1: sQ1.14 A signed 16-bit number, having 1 sign bit, 1 integer bit to the left of the binary point, and 14 mantissa bits to the right of the binary point that can represent numbers in the range: [-2.0, +1.999938965]. Example-2: uQ2.14 An unsigned 16-bit number, having no sign bit, 2 integer bits to the left of the binary point and 14 mantissa bits to the right of the binary point that can represent numbers in the range: [0, +3.999938965].
PGA	Programmable Gain Amplifier: The ADC channels could have an internal, selectable, programmable gain amplifier that can provide an additional analog gain equal to GPGA.
V_P, V_{P-M}	Voltage potential: VP is the voltage measured from node P to an implied neutral reference voltage. VP-M is the voltage measured from node P to node M, where a positive voltage is indicative of a voltage rise from node M to node P.

	All phase diagrams are drawn as if mathematical vectors starting at 0° (3 o'clock) and rotating counter-clockwise for positive phase increases, with 90° being at 12 o'clock, 180° at 9 o'clock and 270° at 6 o'clock.

2 Overall Description

2.1 Power Quantities Definition Perspective

The quantities available in the Metrology module make observable all basic components required to completely define or derive all power system measurement quantities for most currently used definitions of power. All per-phase voltages, currents and power for fundamental and fundamental+ harmonics are available, allowing computation of all modern system or poly-phase power quantities.

Quantities labeled as “ACC_Tx” are totals accumulated energy since power-up, they are the same with those energy calculated with pulse x.

2.2 User Characteristics

Measurement data from one measurement interval is short-lived and does not persist longer than one measurement interval. At the end of a measurement interval, the user will be informed by a software interrupt, at which point, the user must read all pertinent quantities before the next measurement period ends.

2.3 Constraints

All computed quantities available through the Metrology module are integrated over a time interval equivalent to an integral number of periods of the fundamental frequency. All integration periods are approximated by the final output sample rate of the DSP filters, 4000 Hz; so, measurement accuracy will increase using longer integration periods. One second is the recommended minimum integration period (50 cycles of 50 Hz or 60 cycles of 60 Hz), but fewer numbers of samples may still yield acceptable results.

DSP filters require a settling time before accurate measurements may be used for revenue-quality metering. It is recommended to wait at least 250 ms after start-up before testing to revenue-grade accuracy.

2.4 Assumptions and Dependencies

The Smart Meter DSP module is specifically designed to accept samples from an Δ/Σ ADC at an input sample rate of 16000 kHz. This input data stream is further filtered to an internal sample rate of 4000 kHz for generation of metrology quantities. All computed metrology quantities are available at a rate of approximately 1 Hz when using recommended settings.

2.5 Channels and Powers

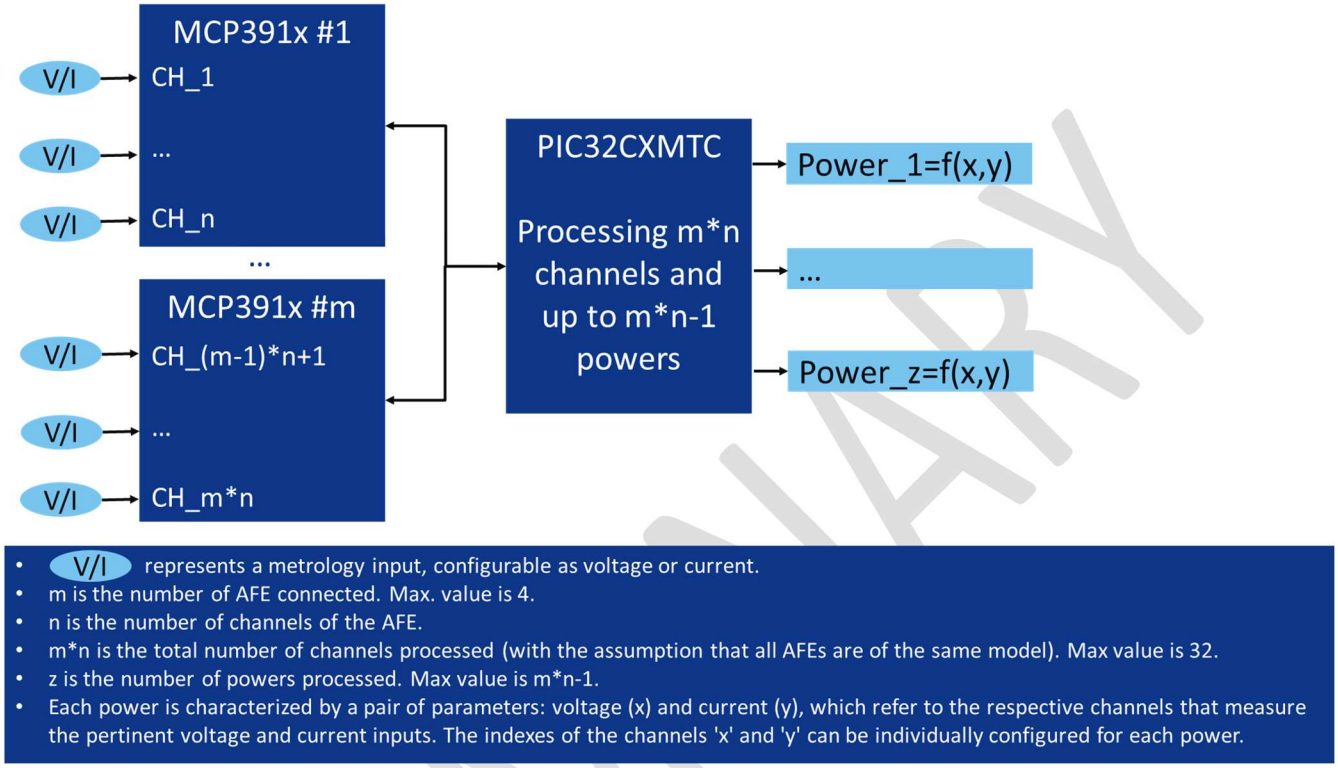
The metrology library systematically acquires data from the signals connected to the MCP391x devices, designating each signal as a "channel" for the purpose of measuring electrical currents or voltages.

A "power" is defined as a pair of one voltage and one current channel.

The library's control registers offer users the capability to tailor the configuration of both channels and powers, ensuring an outstanding degree of adaptability. Standard configuration procedures include:

- Selection of the MCP391x devices connected to the PIC32CXMTC MCU.
- Configuring each channel to function as either a voltage or current measurement channel.
- Determining the specific voltage and current channels that constitute each power

measurement.



- V/I represents a metrology input, configurable as voltage or current.
- m is the number of AFE connected. Max. value is 4.
- n is the number of channels of the AFE.
- m*n is the total number of channels processed (with the assumption that all AFEs are of the same model). Max value is 32.
- z is the number of powers processed. Max value is m*n-1.
- Each power is characterized by a pair of parameters: voltage (x) and current (y), which refer to the respective channels that measure the pertinent voltage and current inputs. The indexes of the channels 'x' and 'y' can be individually configured for each power.

2.6 DSP Channel and Computed Quantity Description

The metrology library computes quantities for each channel and for each power defined.

Values further labeled as '_F' indicate values associated with the fundamental frequency component only, while values without the '_F' indicate values associated with fundamental + harmonics.

3 Metrology Interface Definition

The metrology module provides the following control registers and status registers; it also provides different kinds of accumulated quantities. Control registers are introduced in 3.1. Metrology Control Registers. Status registers are introduced in 3.2. Metrology Status Registers. Accumulated quantities are introduced in 3.3. Accumulated Output Quantities. Harmonic analysis quantities are introduced in 3.4. Harmonic Analysis Output Quantities.

3.1 Metrology Control Registers

All 32-bit metrology input control registers are prefixed “Metrology_Reg_In”. The start address is 0x20086000.

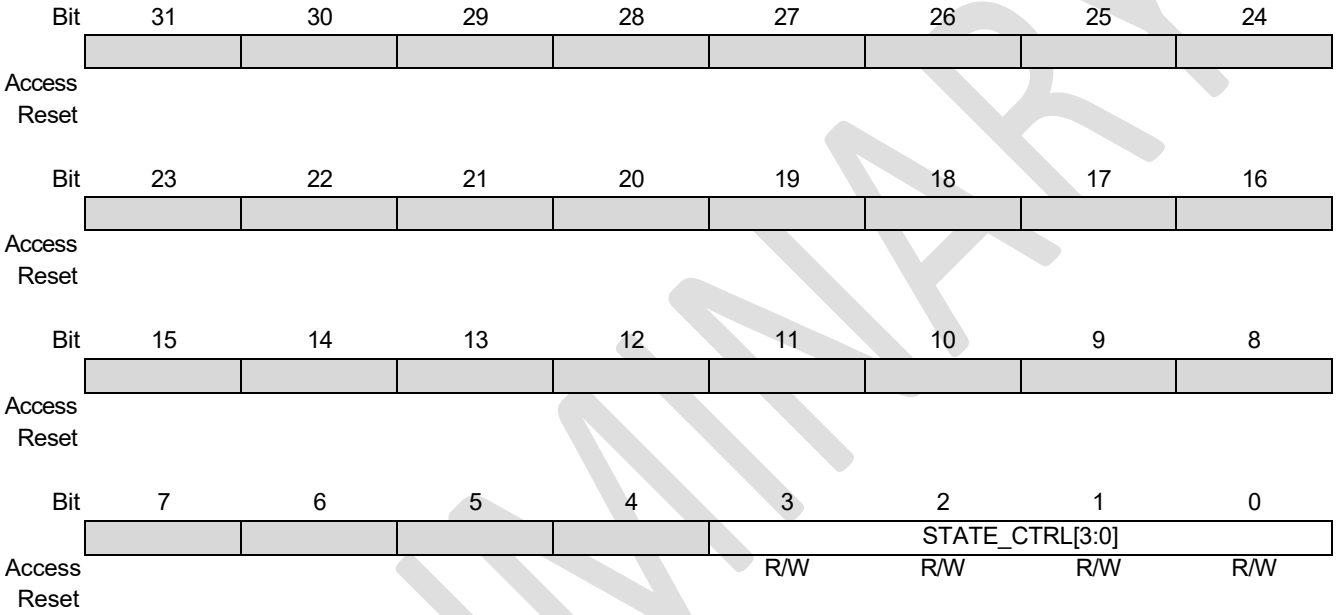
Offset	Variable	Access Mode	Name	Format	# Bytes	Min Value	Max Value	Default	Unit
0	STATE_CTRL	R/W	Metrology state control register	uQ32.0	4	—	—	—	integer
1	FEATURE_CTRL0	R/W	Metrology feature setting register 0	uQ32.0	4	—	—	—	integer
2	FEATURE_CTRL1	R/W	Metrology feature setting register 1	uQ32.0	4	—	—	—	integer
3	RESERVED	—	—	—	4	—	—	—	—
4	POWER SOURCE	R/W	Power source configuration	uQ32.0	16x4	—	—	—	integer
20	METER_TYPE	R/W	Sensor type and service type settings register	uQ32.0	4	—	—	—	integer
21	SENSOR_TYPE	R/W	Sensor type selection	uQ32.0	2x4	—	—	—	integer
23	M	R/W	Number of line cycles for integration period	uQ32.0	4	0	1980	0	integer
24	N_MAX	R/W	Maximum number of samples in an integration period	uQ32.0	4	—	132000	4400	integer
25	PULSE0_CTRL	R/W	Pulse 0 control: enable/disable, polarity, quantity type selection	uQ32.0	4	—	—	—	integer
26	PULSE1_CTRL	R/W	Pulse 1 control: enable/disable, polarity, quantity type selection	uQ32.0	4	—	—	—	integer
27	PULSE2_CTRL	R/W	Pulse 2 control: enable/disable, polarity, quantity type selection	uQ32.0	4	—	—	—	integer
28	RESERVED	—	—	—	4	—	—	—	—
29	PULSE_CONTRIBUTION_PW	R/W	Selection of power sources contributing to pulse, for pulses configured to pulse P or Q	uQ32.0	4	—	—	—	integer
30	PULSE_CONTRIBUTION_I	R/W	Selection of current sources contributing to pulse, for pulses configured to pulse I^2	uQ32.0	4	—	—	—	integer
31	RESERVED	—	—	—	4	—	—	—	—
32	P_K_t	R/W	Watt-hour meter constant for pulse output	uQ8.24	4	—	—	0.3125	Wh/imp
33	Q_K_t	R/W	Var-hour meter constant for pulse output	uQ8.24	4	—	—	0.3125	VARh/imp
34	I_K_t	R/W	Amp-squared-hour meter constant for pulse output	uQ8.24	4	—	—	0.3125	Amp^2h/imp
35	CREEP_THRESHOLD_P	R/W	Starting per-cycle total Active Energy for pulse and pulse accumulation	uQ2.30	4	—	—	—	Wh
36	CREEP_THRESHOLD_Q	R/W	Starting per-cycle total Reactive Quadergy for pulse and pulse accumulation	uQ2.30	4	—	—	—	VARh
37	CREEP_THRESHOLD_I	R/W	Starting per-phase current for both Energy and Quadergy pulse and pulse accumulation	uQ12.20	4	—	—	—	mArms scaled
38	P_POWER_OFFSET_CTRL	R/W	Active power offset control	uQ32.0	4	—	—	—	integer
39	Q_POWER_OFFSET_CTRL	R/W	Reactive power offset control	uQ32.0	4	—	—	—	integer
40	POWER_OFFSET_P	R/W	Pulse computation active power offset compensation used to eliminate voltage effects to small current (cross talk). Affects only pulse measurements.	sQ1.30	4	-2.000	1.9999…	0	Wh/cycle
41	POWER_OFFSET_Q	R/W	Pulse computation reactive power offset compensation used to eliminate voltage effects to small current (cross talk). Affects only pulse measurements.	sQ1.30	4	-2.000	1.9999…	0	VARh/cycle
42	SWELL_OVERCURRENT_THRESHOLD_CHx	R/W	Voltage swells or overcurrent threshold for each half cycle of CHx channel	uQ0.32	32x4	0	0.9999…	—	—
74	SAG_THRESHOLD_CHx	R/W	Voltage sag threshold for each half cycle of CHx voltage	uQ0.32	32x4	0	0.9999…	—	—
106	K_CH_x	R/W	ADC input channel conversion factor (I_A(rms)/Vadc(rms) or V_A(rms)/Vadc(rms))	uQ22.10	32x4	—	2,000.00	—	A_{RMS}/ $VADC_{RMS}$ or V_{RMS}/ $VADC_{RMS}$
138	CAL_M_CHx	R/W	Magnitude calibration constant for channel CHx	sQ2.29	32x4	-4.0000	+3.9999	+1.0000	—
170	CAL_PH_CHx	R/W	Phase calibration constant for channel CHx	sQ0.31	32x4	-1.000	+0.999	0	BAMS
202	CAPTURE_CTRL	R/W	Waveform capture control register	uQ32.0	4	—	—	—	integer
203	CAPTURE_CH_SEL	R/W	Waveform capture channel selection	uQ32.0	4	—	—	—	integer

204	CAPTURE_BUFF_SIZE	R/W	Waveform capture buffer size	uQ32.0	4	1	8000000	—	integer
205	CAPTURE_ADDR	R/W	Waveform capture buffer address pointer	uQ32.0	4	—	—	—	pointer
206∼208	RESERVED	—	—	—	4	—	—	—	—
209	MCP3914_GAIN	R/W	MCP3914 GAIN register	uQ32.0	4x4	—	—	—	integer
213	MCP3914_CONFIG0	R/W	MCP3914 CONFIG0 register	uQ32.0	4x4	—	—	—	integer
217	RESERVED	—	—	—	4	—	—	—	—
218	POWER_OFFSET_P_x	R/W	Phase-x accumulation active power offset compensation used to eliminate voltage effects at small current (cross talk). Affects accumulator and pulse measurement.	sQ-9.40	31x4	-2.000	1.9999…	0.0	W-samp scaled
249	RESERVED	—	—	—	4	—	—	—	—
250	POWER_OFFSET_Q_x	R/W	Phase-x accumulation reactive power offset compensation used to eliminate voltage effects at small current (cross talk). Affects accumulator and pulse measurement.	sQ-9.40	31x4	-2.000	1.9999…	0.0	VAR-samp scaled
281	RESERVED	—	—	—	4	—	—	—	—

3.1.1 Metrology State Control

Name: STATE_CTRL
Offset: Metrology_Reg_In[0]
Property: Read-Write

State control bits input to Metrology module from application code.



Bits 3:0 – STATE_CTRL[3:0] State control bits input to Metrology module from application code. Refer to Interface in Initialization Stage for a detailed description.

Notes: Before entering in a Low-Power mode the Core 0 application should reset the metrology to enable the proper low power mode in the AFEs connected. This action reduces the consumption in Low-Power mode. The Core 0 appplication should follow these steps:

1. Write a '0' in the "STATE_CTRL" control register.
2. Wait until the "STATUS" status register changes to "RESET".
3. Continue with the procedure to switch to a Low-Power mode.

3.1.2 Metrology Feature Control Register 0

Name: FEATURE_CTRL0
Offset: Metrology_Reg_In[1]
Property: Read-Write

The metrology feature control register contains the main control bits for overall metrology feature

Bit	31	30	29	28	27	26	25	24
	AFE_SELECTION							
Access	R/W				R/W			
Reset								

Bit	23	22	21	20	19	18	17	16
	RZC_DIR	RZC_CHAN_SELECT[6:0]						
Access	R/W	R/W						
Reset								

Bit	15	14	13	12	11	10	9	8
	MAX_INT_SELECT			POWER_NUMBER				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	RZC_THRESH_DIS	SYNCH[1:0]						
Access	R/W	R/W						
Reset								

Bits 28-31 – AFE SELECTION Selection of the AFEs connected to the host MCU. The changes in this field are applied after re-initializing the metrology library.

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Value	Description
0	1 x MCP3914. (Default). 8 channels and up to 7 powers are allowed. Not tested.
1	2 x MCP3914. 16 channels and up to 15 powers are allowed. Not tested
2	3 x MCP3914. 24 channels and up to 23 powers are allowed. Not supported in this version.
3	4 x MCP3914. 32 channels and up to 31 powers are allowed. Not supported in this version.
4	1 x MCP3913. 6 channels and up to 5 powers are allowed.
5	2 x MCP3913. 12 channels and up to 11 powers are allowed
6	3 x MCP3913. 18 channels and up to 17 powers are allowed. Not supported in this version.
7	4 x MCP3913. 24 channels and up to 23 powers are allowed. Not supported in this version.
8-15	Reserved for future uses

Bit 8-12 – POWER_NUMBER Number of powers computed.
It configures the number of powers computed by the metrology library. A power is defined as a pair of voltage and current channels, so the maximum number of powers is equal to the maximum number of channels minus one.

. The metrology library will compute the active and reactive power associated with each one of the powers enabled.
The changes in this field are applied after re-initializing the metrology library.

Value	Name	Description
0	POWER_NUMBER	Number of powers supported

Bit 23 – RZC_DIR Raw Zero-Crossing Direction Selection
Raw Zero-Crossing Direction selects either positive-going or negative-going raw zero-crossings trigger the IPC interrupt: IPC_RAW_ZERO_CROSSING.

Value	Name	Description
0	POSITIVE	Positive-going raw zero-crossings selected
1	NEGATIVE	Negative-going raw zero-crossings selected

Bits 22:16 – RZC_CHAN_SELECT[6:0] Raw Zero-Crossing Channel Select and Enable
Raw Zero-Crossing allows detection of zero-crossings using the raw 16 KHz input voltage channel samples. Unlike the zero-crossing detection used for timing decisions that use a 4 KHz fundamental-only filtered data stream, the Raw Zero-Crossing detection feature has no frequency-dependent group delay nor any appreciable bulk filter delay.

Value	Description
0x0	Raw Zero-Crossing detection is disabled
0x1-0x20	Raw Zero-Crossing detection based on input voltage channel Vx (V_0 if value is 1, V_1 if value is 2, … $V_3$1 if value is 32)
Other	Reserved

Bit15 - MAX_INT_SELECT Max Integration Period Select.
Only applies if control word M = 0 (M = Number of cycles for integration period) and affects rounding when determining number of cycles closest to 1 sec.

Value	Description
0	Metrology DSP will integrate for an integral number of cycles closest to 1 second. Due to line frequency drift, the integration period may be slightly longer or shorter than 1 sec, bounded approximately by [0.99, 1.01] sec.
1	Metrology DSP will integrate for an integral number of cycles no greater than 1 second. Due to line frequency drift, the integration period will always be ≤ 1 sec, bounded by approximately by [0.98, 1.00] sec.

Bit 7 – RZC_THRESH_DIS Raw Zero-Crossing Threshold Disable.
Selects the raw Zero-Crossing detection algorithm threshold.

Value	Description
0	Threshold set to the average value computed in the last integration period.
1	Threshold set to 0.

Bits 5:4 – SYNCH[5:0] Active Voltage Channel Selection
The energy integration period is determined by counting zero-crossings of a narrow-band filtered version of the active voltage channel. SYNCH is used to allow the metrology module to dynamically determine which voltage channel is the active voltage channel or to statically choose one particular channel for zero-crossing counting. In all cases of active channel cycle counting, measurement quantities are integrated over M-number of (negative-to-positive) zero-crossings. We recommend the sync channel is appointed, especially for a single phase application.

Value	Description
0x0	Measurement interval based on active channel, determined dynamically
0x1-0x20	Measurement interval based on channel x (x= value-1). If value is 1 channel 0, if value is 2 channel 1, …, if value is 32 channel 31

3.1.3 Metrology Feature Control Register 1

Name: FEATURE_CTRL1
Offset: Metrology_Reg_In[2]
Property: Read-Write

The metrology feature control register contains the main control bits for the overall metrology feature.

Bit	31	30	29	28	27	26	25	24
	NUM_CHANNELS							
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	V_MAX_RESET				I_MAX_RESET			
Access	R/W				R/W			
Reset								

Bit	15	14	13	12	11	10	9	8
	HARMONIC_EN		HARMONIC_m_REQ[5:0]					
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
						CREEP_P_EN	CREEP_Q_EN	CREEP_I_EN
Access						R/W	R/W	R/W
Reset								

Bit 31 – 24 NUM CHANNELS Number of channels

Reserved for future use. Not implemented in this version.

Bit 23 – V_MAX_RESET Reset All V_x_MAX values in Metrology Status Registers

This bit will be cleared by the metrology firmware automatically.

Value	Description
1	Reset all V_x_MAX values in Metrology Status Registers

Bit 19 – I_MAX_RESET Reset All I_x_MAX values in Metrology Status Registers

This bit will be cleared by the metrology firmware automatically.

Value	Description
1	Reset all I_x_MAX values in Metrology Status Registers

Bit 15 – HARMONIC_EN Enable Harmonic Analysis

Value	Name	Description

0	DISABLED	Disable harmonic analysis
1	ENABLED	Enable harmonic analysis

Bits 13:8 – HARMONIC_m_REQ[5:0] Request number of harmonic for analysis

Power analysis may be computed for one additional harmonic during any one integration period. Set this value to the number harmonic analysis is to be computed. Analysis must be computed over an entire integration period, so set this number prior to the start of the integration period to be analyzed. After a harmonic analysis measurement is completed, the number of harmonics analyzed is confirmed in the HARMONIC_m_CONF register

Bit 2 – CREEP_P_EN Active Power Creep Threshold Feature Enable

Used to enable/disable metrology creep function of active power pulse generation and any associated ACC_Tx total energy pulse value accumulators. Refer to CREEP_THRESHOLD_P for more information.

Value	Name	Description
0	DISABLED	Disable active power creep threshold feature.
1	ENABLED	Enable active power creep threshold feature.

Bit 1 – CREEP_Q_EN Reactive Power Creep Threshold Feature Enable

Used to enable/disable metrology creep function of reactive power pulse generation and any associated ACC_Tx total quadergy pulse value accumulators. Refer to CREEP_THRESHOLD_Q for more information.

Value	Name	Description
0	DISABLED	Disable reactive power creep threshold feature.
1	ENABLED	Enable reactive power creep threshold feature.

Bit 0 – CREEP_I_EN Current Creep Threshold Feature Enable

Used to enable/disable creep function of metrology, both for pulse generation and any associated ACC_Tx total pulse value accumulators. Current creep thresholding is used to kill pulse contribution from any or all powers having currents below the current threshold and affects all enabled [P, Q, and I^2] pulsing.

Refer to CREEP_THRESHOLD_I for more information.

Value	Name	Description
0	DISABLED	Disable current creep threshold feature.
1	ENABLED	Enable current creep threshold feature.

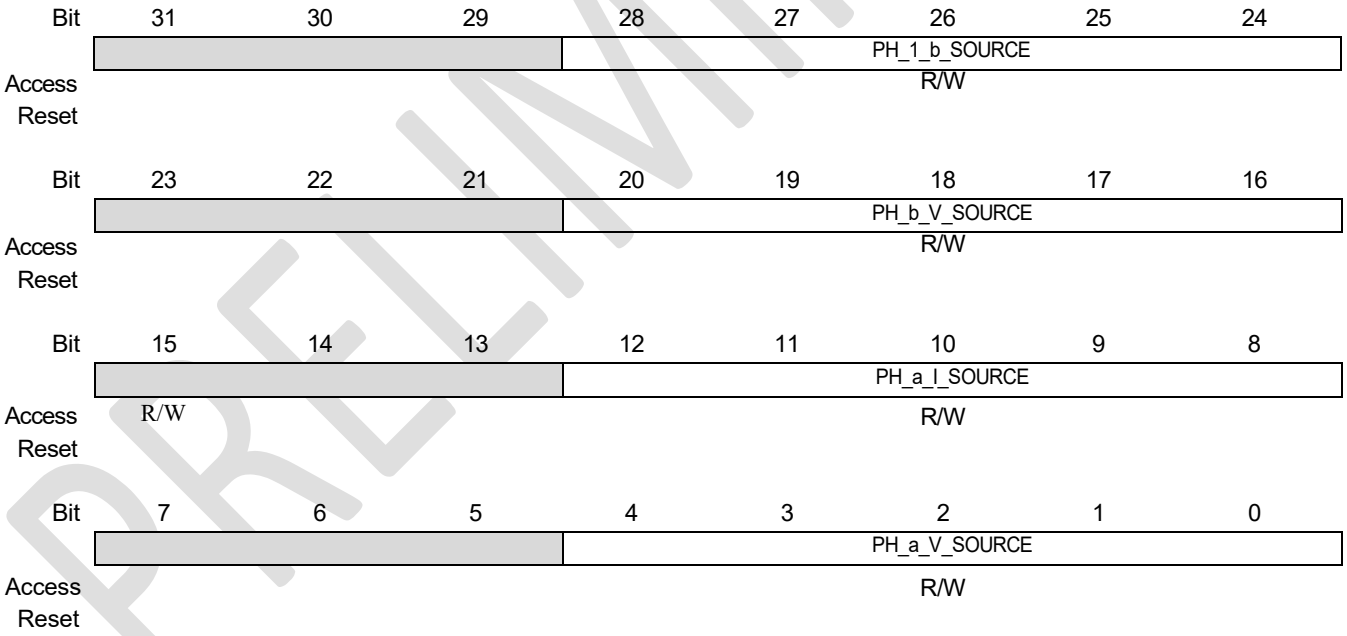
3.1.4 Power Source

Name: Power_Source
Offset: Metrology_Reg_In[4-19]
Property: Read-Write

This group of registers selects the voltage and current indexes composing the power x. Each register allows to configure 2 powers, so 16 registers are needed for the maximum number of powers allowed (31 powers):

- Metrology_Reg_In[4] configures powers 0 and 1.
- Metrology_Reg_In[5] configures powers 2 and 3.
- …
- Metrology_Reg_In[18] configures powers 28 and 29.
- Metrology_Reg_In[19] configures power 30.

The number of active powers is defined in FEATURE_CTRL0.POWER_NUMBER. The powers should be configured in ascendant order. For example, if FEATURE_CTRL0.POWER_NUMBER=6, just the three first registers (Metrology_Reg_In[4-6]) will be used for the configuration.
The changes in these registers are applied after re-initializing the metrology library.



Bits 0-4, 16-20 – PH_x_V_SOURCE Selects the channels with the voltage source of each power x (x = 0, … , 30).

Value	Name	Description
0-31	Voltage channel index	Channel 0-31 is the voltage source for the power x (x= 0, …, 30): • For the register Metrology_Reg_In[4] “a” corresponds to power 0 and “b” to power 1. • For the register Metrology_Reg_In[5] “a” corresponds to power 2 and “b” to power 3. • …. • For the register Metrology_Reg_In[18] “a” corresponds to power 28 and “b” to power 29. • For the register Metrology_Reg_In[19] “a” corresponds to power 30 and “b” does not exist.

Bits 8-12, 24-28 – PH_x_I_SOURCE Selects the channels with the current source of each power x (x = 0, … , 30).

Value	Name	Description
0-31	Current channel index	Channel 0-31 is the current source for the power x (x= 0, …, 30): • For the register Metrology_Reg_In[4] “a” corresponds to power 0 and “b” to power 1. • For the register Metrology_Reg_In[5] “a” corresponds to power 2 and “b” to power 3. • …. • For the register Metrology_Reg_In[18] “a” corresponds to power 28 and “b” to power 29. • For the register Metrology_Reg_In[19] “a” corresponds to power 30 and “b” does not exist.

3.1.5 Meter Type Settings Register

Name: METER_TYPE
Offset: Metrology_Reg_In[20]
Property: Read-Write

Not implemented in this version.

3.1.6 Channel type and Sensor Configuration Register 0

Name: SENSOR_TYPE0
Offset: Metrology_Reg_In[21]
Property: Read-Write

This register configures the sensor connected in channels 0 to 15 and, consequently, the channel type (voltage or current channel).

The changes in this register are applied after re-initializing the metrology library.

The number of channels depends on the AFE model connected to the host MCU (FEATURE_CTRL0.AFE_SELECTION). Channel index corresponds to the channel index of the first AFE connected to the host MCU. In the case of having several AFEs connected, the index increments. Example with 2 MCP3914 connected:

- Channels 0 to 7 correspond to channels 0 to 7 of the first MCP3914.
- Channels 8 to 15 correspond to channels 0 to 7 of the second MCP3914.

The index of the AFEs corresponds to the index of the chip select signal connecting the host MCU with the AFE:

- CS0 → Index 0 (first AFE).
- CS1 → Index 1 (second AFE).
- CS2 → Index 2 (third AFE).
- CS3 → Index 3 (fourth AFE).

Bit	31	30	29	28	27	26	25	24
	SENSOR_TYPE_CH15[1:0]		SENSOR_TYPE_CH14[1:0]		SENSOR_TYPE_CH13[1:0]		SENSOR_TYPE_CH12[1:0]	
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	SENSOR_TYPE_CH11[1:0]		SENSOR_TYPE_CH10[1:0]		SENSOR_TYPE_CH9[1:0]		SENSOR_TYPE_CH8[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	SENSOR_TYPE_CH7[1:0]		SENSOR_TYPE_CH6[1:0]		SENSOR_TYPE_CH5[1:0]		SENSOR_TYPE_CH4[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	SENSOR_TYPE_CH3[1:0]		SENSOR_TYPE_CH2[1:0]		SENSOR_TYPE_CH1[1:0]		SENSOR_TYPE_CH0[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 31:0 – SENSOR_TYPE_CH_x[1:0] Sensor Type on Channel x

Selects the types of current and voltage sensor used. For each channel selected as using a Rogowski sensor, the Metrology DSP implements a digital integrator filter to normalize the effects of the sensor's di/dt behavior.

Value	Name	Description
0x0	CURRENT TRANSFORMER	When this type of sensor is selected, the channel is considered as a current channel.
0x1	RESISTIVE SHUNT	May only be used with phase-to-neutral voltage measurement applications. When this type of sensor is selected, the channel is considered as a current channel.
0x2	ROGOWSKI COIL (CRC) CURRENT SENSOR	A digital integrator function is added to the DSP of all current channels selected as using Rogowski Coils. When SENSOR_TYPE_CH_x = 2, an additional phase correction is internally added to each channel with a Rogowski sensor in the amount of -0.3704° (@ 60 Hz) to correct for a linear phase response introduced by the digital integrator filter. This is taken into account during the internal calculation of actual phase-correction filter coefficients, when a new set of phase calibration settings are loaded, and must not be added by the user in the phase-correction entries. When SENSOR_TYPE_CH_x is set to other values, it takes no effect. When this type of sensor is selected, the channel is considered as a current channel.
0x3	RESISTIVE DIVIDER (VRD) VOLTAGE SENSOR	Normally, this is the typical option selected for voltage sensors. When this type of sensor is selected, the channel is considered as a voltage channel.

3.1.7 Channel type and Sensor Configuration Register 1

Name: SENSOR_TYPE1
Offset: Metrology_Reg_In[22]
Property: Read-Write

This register configures the sensor connected in channels 16 to 31 and, consequently, the channel type (voltage or current channel).

The changes in this register are applied after re-initializing the metrology library.

The number of channels depends on the AFE model connected to the host MCU (FEATURE_CTRL0.AFE_SELECTION). Channel index corresponds to the channel index of the first AFE connected to the host MCU. In the case of having several AFEs connected, the index increments. Example with 2 MCP3914 connected:

- Channels 0 to 7 correspond to channels 0 to 7 of the first MCP3914.
- Channels 8 to 15 correspond to channels 0 to 7 of the second MCP3914.

The index of the AFEs corresponds to the index of the chip select signal connecting the host MCU with the AFE:

- CS0 → Index 0 (first AFE).
- CS1 → Index 1 (second AFE).
- CS2 → Index 2 (third AFE).
- CS3 → Index 3 (fourth AFE).

Bit	31	30	29	28	27	26	25	24
	SENSOR_TYPE_CH31[1:0]		SENSOR_TYPE_CH30[1:0]		SENSOR_TYPE_CH29[1:0]		SENSOR_TYPE_CH28[1:0]	
Access	R/W		R/W		R/W		R/W	
Reset								

Bit	23	22	21	20	19	18	17	16
	SENSOR_TYPE_CH27[1:0]		SENSOR_TYPE_CH26 [1:0]		SENSOR_TYPE_CH25[1:0]		SENSOR_TYPE_CH24[1:0]	
Access	R/W		R/W		R/W		R/W	
Reset								

Bit	15	14	13	12	11	10	9	8
	SENSOR_TYPE_CH23[1:0]		SENSOR_TYPE_CH22[1:0]		SENSOR_TYPE_CH21[1:0]		SENSOR_TYPE_CH20[1:0]	
Access	R/W		R/W		R/W		R/W	
Reset								

Bit	7	6	5	4	3	2	1	0
	SENSOR_TYPE_CH19[1:0]		SENSOR_TYPE_CH18[1:0]		SENSOR_TYPE_CH17[1:0]		SENSOR_TYPE_CH16[1:0]	
Access	R/W		R/W		R/W		R/W	
Reset								

Bits 31:0 – SENSOR_TYPE_CH_x[1:0] Sensor Type on Channel x

Selects the types of current and voltage sensor used. For each channel selected as using a Rogowski sensor, the Metrology DSP implements a digital integrator filter to normalize the effects of the sensor's di/dt behavior.

Value	Name	Description
0x0	CURRENT TRANSFORMER	When this type of sensor is selected, the channel is considered as a current channel.
0x1	RESISTIVE SHUNT	May only be used with phase-to-neutral voltage measurement applications. When this type of sensor is selected, the channel is considered as a current channel.
0x2	ROGOWSKI COIL (CRC) CURRENT SENSOR	A digital integrator function is added to the DSP of all current channels selected as using Rogowski Coils. When SENSOR_TYPE_CH_x = 2, an additional phase correction is internally added to each channel with a Rogowski sensor in the amount of -0.3704º (@ 60 Hz) to correct for a linear phase response introduced by the digital integrator filter. This is taken into account during the internal calculation of actual phase-correction filter coefficients, when a new set of phase calibration settings are loaded, and must not be added by the user in the phase-correction entries. When SENSOR_TYPE_CH_x is set to other values, it takes no effect. When this type of sensor is selected, the channel is considered as a current channel.
0x3	RESISTIVE DIVIDER (VRD) VOLTAGE SENSOR	Normally, this is the typical option selected for voltage sensors. When this type of sensor is selected, the channel is considered as a voltage channel.

3.1.8 Number of Line Cycles for Integration Period

Name: M
Offset: Metrology_Reg_In[23]
Property: Read-Write

The measurement time unit, t_M, or integration period, is delineated by M-number of negative-to-positive zero-crossings of the fundamental frequency using a selected voltage signal. All primary output quantities are computed for this many number of cycles of the fundamental frequency.

M, the number of cycles of the integration period, are provided as input into the metrology module.

Note: After changing this register, please check the value of "N_MAX" register.

Note: If the phase voltage for frequency determination is not present, defined as >= 1/32 of max range, then the metrology module transitions to a default integration period of "N_MAX" samples. If phase voltage loss occurs before the expected number, then that specific integration period may end with some intermediate number of samples. In all cases, the number of samples used in an integration period is available in the output Register N, at the end of an integration period.

Presently, fixed-precision accumulation is scaled for a maximum integration period of 30 seconds (given max V & I inputs). This has to be changed if a one-minute integration period is desired.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access					R/W	R/W	R/W	R/W
Reset					M[11:8]			

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	M[7:0]							

Bits 11:0 – M[11:0] (uQ12.0)

Value	Description
0	Number of cycles for the measurement period will be determined automatically as the number of cycles closest to 1.0 second of integration time. The number of cycles is variable and the measurement period, t_M, will closely track 1.0 sec of measurement time, regardless of line frequency.
Other	Number of cycles is fixed and the measurement period, t_M, will vary with line frequency.

3.1.9 Max Number of Samples in an Integration Period

Name: N_MAX
Offset: Metrology_Reg_In[24]
Property: Read-Write

The maximum number of samples in a measurement time period must be defined, in case of loss of active voltage phase detection and zero-crossing cycle synchronization. "N_MAX" and "M" must be chosen in such a way that "N_MAX" is large enough to consider the expected number samples in the number of line cycles for the integration period.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	N_MAX[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	N_MAX[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	N_MAX[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 23:0 – N_MAX[23:0] (uQ24.0)

3.1.10 Pulse Control Register x (x = 0, 1, 2)

Name: PULSEx_CTRL
Offset: Metrology_Reg_In[25-27]
Property: Read-Write

Three pulses can be generated at the same time. PULSE0_CTRL is used to control the pulse output from PD17. PULSE1_CTRL is used to control the pulse output from PD18. PULSE2_CTRL is used to control the pulse output from PD19. IPC interrupts are triggered at each pulse: IPC_PULSEx.

Bit	31	30	29	28	27	26	25	24
	PCx_ENABLE	PU_ENABLE	PCx_DETENT[1:0]		OPD_ENABLE	PCx_ACC_HOLD	PCx_OVERRIDE	PCx_POLARITY
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
					PCx_TYPE[3:0]			
Access					R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	PCx_WIDTH[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	PCx_WIDTH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit 31 – PCx_ENABLE Output Pulse Enable
Used to enable or disable pulse functionality. For short-term disable of pulses, use the PC_OVERRIDE control bit.

Value	Description
0x0	Pulse output disabled, inactive level determined by PULSE_POLARITY
0x1	Pulse output enabled

Bit 30 – PU_ENABLE Pull-Up Enable
Used to enable or disable an optional pull-up on the pulse output pin.

Value	Description
0x0	Pull-Up disabled
0x1	Pull-Up enabled

Bits 29:28 – PCx_DETENT[1:0] Total Absolute Values for P and Q values
When creating P and Q accumulator totals of multiple powers, this option allows taking the absolute values of each power before adding to make the total. This is used to primarily ignore direction of energy delivered/generated for pulse generation.

Value	Name	Description
0x0	NET	Pulses generated based on (energy delivered – energy generated): Individual sign of each channel's P and Q is taken into account when creating total P and Q accumulator sums.
0x1	ABSOLUTE	Pulses generated based on (energy delivered + energy generated): The absolute value of each power's P and Q is used when creating the total P and Q accumulator sums.
0x2	DELIVERED	Pulses generated based on (delivered only): Only positive values (energy delivered) of each power's P and Q are used when creating the total P and Q accumulator sums, with negative values (energy generated) being ignored.
0x3	GENERATED	Pulses generated based on (generated only): Only negative values (energy generated) of each power's P and Q are used when creating the total P and Q accumulator sums, with positive values (energy delivered) being ignored.

Bit 27 – OPD_ENABLE Open Drain Enable

Used to enable or disable open-drain drive on the pulse output pin.

Value	Description
0x0	The open drain is disabled. Pulse pin is driven at high- and low-level
0x1	The open drain is enabled. Pulse pin is driven at low-level only

Bit 26 – PCx_ACC_HOLD Pulse Accumulation Hold Control

Value	Description
0x0	Pulse accumulation registers continue to increment even if pulse generation is temporarily disabled.
0x1	Pulse accumulation is held static. All incremental quantities normally used for pulse determination are discarded.

Bit 25 – PCx_OVERRIDE Pulse Override Control

Use to temporarily disable pulse generation. While disabled, pulse accumulation functions as selected with the PC_ACC_HOLD control bit.

Value	Description
0x0	Pulse generation functions as normal
0x1	Pulse generation is temporarily disabled

Bit 24 – PCx_POLARITY Pulse Polarity

Value	Description
0x0	Output pulse is low with width set by K_WIDTH, followed by an inactive level of high
0x1	Output pulse is high with width set by K_WIDTH, followed by an inactive level of low

Bits 19:16 – PCx_TYPE[3:0] Pulse Type Selection

Types described as "all powers" are based on all active powers.

Value	Name	Description
0x0	P_T	Watt-hours, total all powers, fundamental + harmonics
0x1	P_T_F	Watt-hours, total all powers, fundamental only
0x2	Q_T	Var-hours, total all powers, fundamental + harmonics
0x3	Q_T_F	Var-hours, total all powers, fundamental only
0x4	I_T	Amp-squared-hours, total all currents, fundamental + harmonics
0x5	I_T_F	Amp-squared-hours, total all currents, fundamental only
0x6-0xF	RESERVED	—

Bits 15:0 – PCx_WIDTH[15:0] Pulse Width

The granularity for pulse width is in units of 2.1552 µs.

.

PCx_WIDTH = PULSE_WIDTH[sec] x 464000
For example, for a desired pulse width of 750 µs, the computation for the value PCx_WIDTH would be:

$$PCx\_WIDTH = 750 \times 10^{-6} \times 464000 = 348 = 0x015C$$

There is a limitation on the maximum frequency of pulse occurrence: the pulse period duration cannot exceed the sum of the pulse width plus an additional 500 microseconds.
For example, if the pulse width is set at 500 microseconds, the maximum pulse frequency that can be attained is 1 kHz. On the other hand, if the pulse width is reduced to 50 microseconds, the pulse frequency can increase to a maximum of 1.818 kHz.

3.1.11 Pulse Contribution Power

Name: PULSE_CONTRIBUTION_PW
Offset: Metrology_Reg_In[29]
Property: Read-Write

Bit	31	30	29	28	27	26	25	24
		POWER_30_EN	POWER_29_EN	POWER_28_EN	POWER_27_EN	POWER_26_EN	POWER_25_EN	POWER_24_EN
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	POWER_23_EN	POWER_22_EN	POWER_21_EN	POWER_20_EN	POWER_19_EN	POWER_18_EN	POWER_17_EN	POWER_16_EN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	POWER_15_EN	POWER_14_EN	POWER_13_EN	POWER_12_EN	POWER_11_EN	POWER_10_EN	POWER_9_EN	POWER_8_EN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	POWER_7_EN	POWER_6_EN	POWER_5_EN	POWER_4_EN	POWER_3_EN	POWER_2_EN	POWER_1_EN	POWER_0_EN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 0-30 – POWER_x_EN Enable Power x (x = 0, … , 30) for pulse computation.
Selects the powers used for pulse computation, for all the pulses configured to pulse active or reactive energy. At least one power must be enabled for pulsing to function. This feature may be used to temporarily disable or exclude powers from pulse computation.

Value	Name	Description
0	DISABLED	Disable power
1	ENABLED	Enable power

3.1.12 Pulse Contribution Current

Name: PULSE_CONTRIBUTION_I
Offset: Metrology_Reg_In[30]
Property: Read-Write

Bit	31	30	29	28	27	26	25	24
	CURRENT_31_EN	CURRENT_30_EN	CURRENT_29_EN	CURRENT_28_EN	CURRENT_27_EN	CURRENT_26_EN	CURRENT_25_EN	CURRENT_24_EN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	CURRENT_23_EN	CURRENT_22_EN	CURRENT_21_EN	CURRENT_20_EN	CURRENT_19_EN	CURRENT_18_EN	CURRENT_17_EN	CURRENT_16_EN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	CURRENT_15_EN	CURRENT_14_EN	CURRENT_13_EN	CURRENT_12_EN	CURRENT_11_EN	CURRENT_10_EN	CURRENT_9_EN	CURRENT_8_EN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	CURRENT_7_EN	CURRENT_6_EN	CURRENT_5_EN	CURRENT_4_EN	CURRENT_3_EN	CURRENT_2_EN	CURRENT_1_EN	CURRENT_0_EN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 0-30 – CURRENT_x_EN Enable current x (x = 0, … , 30) for pulse computation.
Selects the currents used for pulse computation, for all the pulses configured to pulse I^2. At least one current must be enabled for pulsing to function. This feature may be used to temporarily disable or exclude currents from pulse computation.

Value	Name	Description
0	DISABLED	Disable current
1	ENABLED	Enable current

3.1.13 Meter Active Power Pulse Constant

Name: P_K_t
Offset: Metrology_Reg_In[32]
Property: Read-Write

P_K_t register defines the meter test constant, which is the amount of active energy signified by one output pulse. P_K_t is in units of [Wh/pulse]. P_K_t is stored in uQ8.24 format.

In Europe and Asia, the pulse constant, MC, is used where MC is in units of [pulses/kWh]. First, convert from units of MC to units of P_K_t (P_K_t = 1000/MC), then convert into uQ8.24 format by multiplying by 2^24.

For example, if MC=800 pulses/kWh, then P_K_t = 1000/800 = 1.25 Wh/pulse, and:

P_K_t = round[1.25 x 2^24] = 20971520 = 0x01400000

The frequency of pulse output generated depends on the quantity of energy measured and the defined pulse constants (P_K_t, Q_K_t, and I_K_t). It is important to note that there is a limitation on the maximum frequency of pulse occurrence: the pulse period duration cannot exceed the sum of the pulse width plus an additional 500 microseconds.

For example, if the pulse width is set at 500 microseconds, the maximum pulse frequency that can be attained is 1 kHz. On the other hand, if the pulse width is reduced to 50 microseconds, the pulse frequency can increase to a maximum of 1.818 kHz.

Updates to P_K_t take effect at the next negative zero-crossing (narrow-band filtered version) of the present control phase voltage channel.

Bit	31	30	29	28	27	26	25	24
	P_K_t[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	P_K_t[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	P_K_t[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	P_K_t[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 31:0 – P_K_t[31:0] (uQ8.24)

3.1.14 Meter Reactive Power Pulse Constant

Name: Q_K_t
Offset: Metrology_Reg_In[33]
Property: Read-Write

Q_K_t defines the meter test constant, which is the amount of reactive energy signified by one output pulse. Q_K_t is in units of [VARh/pulse].

Q_K_t is stored in uQ8.24 format.

In Europe and Asia, the pulse constant, MC, is used where MC is in units of [pulses/kVARh]. First, convert from units of MC to units of Q_K_t (Q_K_t = 1000/MC), then convert into uQ8.24 format by multiplying by 2^24.

For example, if MC=800 pulses/kVARh, then Q_K_t = 1000/800 = 1.25 VARh/pulse, and:

Q_K_t = round[1.25 x 2^24] = 20971520 = 0x01400000

The frequency of pulse output generated depends on the quantity of energy measured and the defined pulse constants (P_K_t, Q_K_t, and I_K_t). It is important to note that there is a limitation on the maximum frequency of pulse occurrence: the pulse period duration cannot exceed the sum of the pulse width plus an additional 500 microseconds.

For example, if the pulse width is set at 500 microseconds, the maximum pulse frequency that can be attained is 1 kHz. On the other hand, if the pulse width is reduced to 50 microseconds, the pulse frequency can increase to a maximum of 1.818 kHz.

Updates to Q_K_t take effect at the next negative zero-crossing (narrow-band filtered version) of the present control phase voltage channel.

Bit	31	30	29	28	27	26	25	24
	Q_K_t[1:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	Q_K_t[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	Q_K_t[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	Q_K_t[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 31:0 – Q_K_t[31:0] (uQ8.24)

3.1.15 Meter Current Pulse Constant

Name: I_K_t
Offset: Metrology_Reg_In[34]
Property: Read-Write

I_K_t defines the meter test constant, which is the amount of Amp^2-h signified by one output pulse. I_K_t is in units of [Amp^2-h/pulse].

I_K_t is stored in uQ8.24 format.

In Europe and Asia, the pulse constant, MC, is used where MC is in units of [pulses/$kAmp^2$-h]. First, convert from units of MC to units of I_K_t

(I_K_t = 1000/MC), then convert into uQ8.24 format by multiplying by 2^24.

For example, if MC=800 pulses/$kAmp^2$-h, then I_K_t = 1000/800 = 1.25 $kAmp^2$-h /pulse, and:

I_K_t = round[1.25 x 2^24] = 20971520 = 0x01400000

The frequency of pulse output generated depends on the quantity of energy measured and the defined pulse constants (P_K_t, Q_K_t, and I_K_t). It is important to note that there is a limitation on the maximum frequency of pulse occurrence: the pulse period duration cannot exceed the sum of the pulse width plus an additional 500 microseconds.

For example, if the pulse width is set at 500 microseconds, the maximum pulse frequency that can be attained is 1 kHz. On the other hand, if the pulse width is reduced to 50 microseconds, the pulse frequency can increase to a maximum of 1.818 kHz.

Updates to I_K_t take effect at the next negative zero-crossing (narrow-band filtered version) of the present control phase voltage channel.

Bit	31	30	29	28	27	26	25	24
	I_K_t[31:24]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset								

Bit	23	22	21	20	19	18	17	16
	I_K_t[23:16]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset								

Bit	15	14	13	12	11	10	9	8
	I_K_t[15:8]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset								

Bit	7	6	5	4	3	2	1	0
	I_K_t[7:0]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset								

Bits 31:0 – I_K_t[31:0] (uQ8.24)

3.1.16 Creep Threshold for Active Energy

Name: CREEP_THRESHOLD_P
Offset: Metrology_Reg_In[35]
Property: Read-Write

Total active energy pulse quantities in any one line cycle interval less than the creep threshold are reset to zero and are not accumulated.

CREEP_THRESHOLD_P is the creep active energy (Watt-hour) in a full cycle (20 ms for 50 Hz, 16.667 ms for 60 Hz).

CREEP_THRESHOLD_P is stored in uQ2.30 format.

If the creep active power is set to 11 Watt, and the system frequency is 60 Hz, then:

CREEP_THRESHOLD_P = round[11/(60*3600)*2^30] = 54681 = 0x0000D599

Bit	31	30	29	28	27	26	25	24
	CREEP_THRESHOLD_P[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	CREEP_THRESHOLD_P[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	CREEP_THRESHOLD_P[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	CREEP_THRESHOLD_P[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 31:0 – CREEP_THRESHOLD_P[31:0] (uQ2.30)

3.1.17 Creep Threshold for Quadergy

Name: CREEP_THRESHOLD_Q
Offset: Metrology_Reg_In[36]
Property: Read-Write

Total reactive energy pulse quantities in any one line cycle interval less than the creep threshold are reset to zero and are not accumulated.

CREEP_THRESHOLD_Q is the creep reactive energy (Var-hour) in a full cycle (20 ms for 50 Hz, 16.667 ms for 60 Hz).

CREEP_THRESHOLD_Q is stored in uQ2.30 format.

If the creep active power is set to 11 VAR, and the system frequency is 60 Hz, then:

CREEP_THRESHOLD_Q = round[11/(60*3600)*2^30] = 54681 = 0x0000D599

Bit	31	30	29	28	27	26	25	24
	CREEP_THRESHOLD_Q[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	CREEP_THRESHOLD_Q[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	CREEP_THRESHOLD_Q[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	CREEP_THRESHOLD_Q[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 31:0 – CREEP_THRESHOLD_Q[31:0] (uQ2.30)

3.1.18 Creep Threshold of Phase Current

Name: CREEP_THRESHOLD_I
Offset: Metrology_Reg_In[37]
Property: Read-Write

For each power with a current less than threshold CREEP_THRESHOLD_I in any one line cycle interval, any contributions to a selected pulse are zeroed out, and quantities from that power make no contribution toward any selected pulse and its associated pulse accumulator.

CREEP_THRESHOLD_I is stored in uQ12.20 format and the unit is mArms-scaled (normalized by a common K_I). A single common K_I is used for all phases for CREEP_THRESHOLD_I determination.

$$CREEP\_THRESHOLD\_I = \frac{I_{CREEP-RMS}}{K\_I} \times 2\text{^}20$$

EXAMPLE: For a desired creep threshold of 10mA, K_I = 617.28396, then:

CREEP_THRESHOLD_I = round[(10/617.28396)*2^20] = 16987 = 0x0000425B

Bit	31	30	29	28	27	26	25	24
	CREEP_THRESHOLD_I[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	CREEP_THRESHOLD_I[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	CREEP_THRESHOLD_I[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	CREEP_THRESHOLD_I[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 31:0 – CREEP_THRESHOLD_I[31:0] (uQ12.20)

3.1.19 Active Power Offset Control Register

Name: P_POWER_OFFSET_CTRL
Offset: Metrology_Reg_In[38]
Property: Read-Write

Bit	31	30	29	28	27	26	25	24
	P_OFFSET_PUL	P_OFFSET_ACC_PW30	P_OFFSET_ACC_PW29	P_OFFSET_ACC_PW28	P_OFFSET_ACC_PW27	P_OFFSET_ACC_PW26	P_OFFSET_ACC_PW25	P_OFFSET_ACC_PW24
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	P_OFFSET_ACC_PW23	P_OFFSET_ACC_PW22	P_OFFSET_ACC_PW21	P_OFFSET_ACC_PW20	P_OFFSET_ACC_PW19	P_OFFSET_ACC_PW18	P_OFFSET_ACC_PW17	P_OFFSET_ACC_PW16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	P_OFFSET_ACC_PW15	P_OFFSET_ACC_PW14	P_OFFSET_ACC_PW13	P_OFFSET_ACC_PW12	P_OFFSET_ACC_PW11	P_OFFSET_ACC_PW10	P_OFFSET_ACC_PW9	P_OFFSET_ACC_PW8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	P_OFFSET_ACC_PW7	P_OFFSET_ACC_PW6	P_OFFSET_ACC_PW5	P_OFFSET_ACC_PW4	P_OFFSET_ACC_PW3	P_OFFSET_ACC_PW2	P_OFFSET_ACC_PW1	P_OFFSET_ACC_PW0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit 31 – P_OFFSET_PUL Active Power Offset for Pulse Quantities Enable

P_OFFSET_PUL is used to enable active power offset functionality for pulse quantities only. P_OFFSET_PUL uses register POWER_OFFSET_P affecting: active energy pulse generation and TX pulse accumulation registers.

Value	Name	Description
0x0	DISABLE	Disables offset
0x1	ENABLE	Enables offset

Bits 30:0 – P_OFFSET_ACC_PWx Active Power Offset for Accumulator Quantities Enable

P_OFFSET_ACC_PWx is used to enable per-channel active power offset added to the 64-bit processing stream. P_OFFSET_ACC_PWx uses registers POWER_OFFSET_P_x affecting: ACC_P_x 64-bit accumulators, active energy pulse generation and TX pulse accumulation registers.

Value	Name	Description
0x0	DISABLE	Disable offset
0x1	ENABLE	Enable offset

3.1.20 Reactive Power Offset Control Register

Name: Q_POWER_OFFSET_CTRL
Offset: Metrology_Reg_In[39]
Property: Read-Write

Bit	31	30	29	28	27	26	25	24
	Q_OFFSET_PUL	Q_OFFSET_ACC_PW30	Q_OFFSET_ACC_PW29	Q_OFFSET_ACC_PW28	Q_OFFSET_ACC_PW27	Q_OFFSET_ACC_PW26	Q_OFFSET_ACC_PW25	Q_OFFSET_ACC_PW24
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	Q_OFFSET_ACC_PW23	Q_OFFSET_ACC_PW22	Q_OFFSET_ACC_PW21	Q_OFFSET_ACC_PW20	Q_OFFSET_ACC_PW19	Q_OFFSET_ACC_PW18	Q_OFFSET_ACC_PW17	Q_OFFSET_ACC_PW16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	Q_OFFSET_ACC_PW15	Q_OFFSET_ACC_PW14	Q_OFFSET_ACC_PW13	Q_OFFSET_ACC_PW12	Q_OFFSET_ACC_PW11	Q_OFFSET_ACC_PW10	Q_OFFSET_ACC_PW9	Q_OFFSET_ACC_PW8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	Q_OFFSET_ACC_PW7	Q_OFFSET_ACC_PW6	Q_OFFSET_ACC_PW5	Q_OFFSET_ACC_PW4	Q_OFFSET_ACC_PW3	Q_OFFSET_ACC_PW2	Q_OFFSET_ACC_PW1	Q_OFFSET_ACC_PW0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit 31 – Q_OFFSET_PUL Reactive Power Offset for Pulse Quantities Enable
Q_OFFSET_PUL is used to enable active power offset functionality for pulse quantities only. Q_OFFSET_PUL uses register POWER_OFFSET_Q affecting: active energy pulse generation and TX pulse accumulation registers.

Value	Name	Description
0x0	DISABLE	Disables offset
0x1	ENABLE	Enables offset

Bits 30:0 – Q_OFFSET_ACC_PWx Reactive Power Offset for Accumulator Quantities Enable
Q_OFFSET_ACC_PWx is used to enable per-channel reactive power offset added to the 64-bit processing stream. Q_OFFSET_ACC_PWx uses registers POWER_OFFSET_Q_x affecting: ACC_Q_x 64-bit accumulators, reactive energy pulse generation and TX pulse accumulation registers.

Value	Name	Description
0x0	DISABLE	Disable offset
0x1	ENABLE	Enable offset

3.1.21 Active Power Offset Register

Name: POWER_OFFSET_P
Offset: Metrology_Reg_In[40]
Property: Read-Write

This value indicates the active power offset of appointed pulse.

The physical significance of POWER_OFFSET_P is total active energy (W-hour) offset per full cycle (20 ms for 50 Hz, 16.667 ms for 60 Hz).

POWER_OFFSET_P is stored in sQ1.30 format and is subtracted each full cycle.

POWER_OFFSET_P affects only P and P_F pulse generation and ACC_Tx pulse accumulators.

Refer to “PIC32CXMTx Metrology User Guide” for a more detailed description.

Bit	31	30	29	28	27	26	25	24
	POWER_OFFSET_P[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	POWER_OFFSET_P[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	POWER_OFFSET_P[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	POWER_OFFSET_P[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 31:0 – POWER_OFFSET_P[31:0] (sQ1.30)

3.1.22 Reactive Power Offset Register

Name: POWER_OFFSET_Q
Offset: Metrology_Reg_In[41]
Property: Read-Write

This value indicates the reactive power offset of appointed pulse.

The physical significance of POWER_OFFSET_Q is total reactive energy (VAR-hour) offset per full cycle (20 ms for 50 Hz, 16.667 ms for 60 Hz).

POWER_OFFSET_Q is stored in sQ1.30 format and is subtracted each full cycle.

POWER_OFFSET_Q affects only Q and Q_F pulse generation and ACC_Tx pulse accumulators.

Refer to “PIC32CXMTx Metrology User Guide” for a more detailed description.

Bit	31	30	29	28	27	26	25	24
	POWER_OFFSET_Q[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	POWER_OFFSET_Q[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	POWER_OFFSET_Q[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	POWER_OFFSET_Q[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 31:0 – POWER_OFFSET_Q[31:0] (sQ1.30)

3.1.23 Voltage Swell and Overcurrent Threshold

Name: SWELL_OVERCURRENT_THRESHOLD_CHx
Offset: Metrology_Reg_In[42-73]
Property: Read-Write

For each half cycle of the fundamental period, Vx_{RMS} (for voltage channels) or Ix_{RMS} (for current channels) is calculated, per channel, and compared to the value set in SWELL_OVERCURRENT_THRESHOLD_CHx, where x = [0, …, 31], to determine if a voltage swell or overcurrent condition exists. For each half cycle that a voltage swell or overcurrent exists, the associated flag, SWELL_OVERCURRENT_DET_CHx is set to 1.

Warning: Overcurrent is not supported in this version.

A threshold is allowed for each channel and is computed using the native phase voltages before transformation to implied 4WY service. This allows setting different thresholds for non-balanced service types.

SWELL_OVERCURRENT_THRESHOLD_CHx is stored in uQ0.32 format. So, set the threshold value as follows:

$$Vx_{SWELL\_THRESHOLD}=(V_{SWELL(RMS)}/K\_CHx)^2 \times 2^{32}$$

$$Ix_{OVERCURRENT\_THRESHOLD}=(I_{OVERCURRENT(RMS)}/K\_CHx)^2 \times 2^{32}$$

Bit	31	30	29	28	27	26	25	24
	SWELL_OVERCURRENT_THRESHOLD_CHx[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	SWELL_OVERCURRENT_THRESHOLD_CHx[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	SWELL_OVERCURRENT_THRESHOLD_CHx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	SWELL_OVERCURRENT_THRESHOLD_CHx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 31:0 – SWELL_OVERCURRENT_THRESHOLD_CHx[31:0] (uQ0.32)

3.1.24 Voltage Sag Threshold

Name: SAG_THRESHOLD_Vx
Offset: Metrology_Reg_In[74-105]
Property: Read-Write

For each half cycle of the fundamental period, VxRMS is calculated, per channel, and compared to the value set in SAG_THRESHOLD_Vx: where x = [1, …, 30], to determine if a voltage sag condition exists. For each half cycle that a voltage sag exists, the associated flag, SWAG_DET_Vx is set to 1.

A threshold is allowed for each channel and is computed using the native phase voltages, before transformation to implied 4WY service. This allows setting different thresholds for non-balanced service types.

SAG_THRESHOLD_Vx is stored in uQ0.32 format. So, set the threshold value as follows:

$$V_{x\ SAG\ THRESHOLD} = \left(\frac{V_{SAG-RMS}}{K\_Vx}\right)^2 \times 2\text{^}32$$

Bit	31	30	29	28	27	26	25	24
	SAG_THRESHOLD_Vx[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	SAG_THRESHOLD_Vx[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	SAG_THRESHOLD_Vx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	SAG_THRESHOLD_Vx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 31:0 – SAG_THRESHOLD_Vx[31:0] (uQ0.32)

3.1.25 Voltage and Current Conversion Factor

Name: K_CH_x
Offset: Metrology_Reg_In[106-137]
Property: Read-Write

The current/voltage conversion factor is used when converting an internal current quantity to an external equivalent RMS current/voltage quantity.

Current channels:

K_CH_x corresponds to K_Ix. For proper ADC function the differential input voltage proportional to current must be provided by the current sensor (typically a CT in conjunction with a burden resistor). This differential input voltage ($V_{diff} = V_+ - V_-$) must be scaled so that its peak input value is limited to the max acceptable ADC input voltage:

$$V_{diff\_max} = \frac{V_{ADCmax}}{G_{PGA}}$$

For example, 0.6V for an ADC PGA gain of G_{PGA} = 1 or 75mV for an ADC PGA gain of G_{PGA} = 8.

The maximum differential input voltage must typically not exceed 0.6V (V_+ = 0.3V, V_- = -0.3V). When using single-ended inputs the highest accuracy will be achieved by limiting single-ended input voltages to 0.3V. Reduced input voltage range signal on current input channels may use the programmable gain amplifier to recover input range. In typical applications, external scaling allows for an appropriate over-current factor to maintain linearity during over-current events.

CT Sensors (Current Transformers)

For example, it is desired to have a max measurement current of $240A_{RMS}$ ($200A_{RMS}$ + 20% over-current). The following three steps must be taken (this example assumes use of a CT turns ratio, T_e= 2500:1 ($200A_{RMS}$: 80 mA_{RMS}) and a G_{PGA}=4):

1. Determine total current burden resistor value, as if it were one single-ended input, then divide by 2 for differential burden resistors:

$$R_{burden\_total} = \frac{V_{diff\_max}}{I_{CTmax}} = \frac{\frac{V_{ADCmax}}{G_{PGA}}}{\sqrt{2}\times\frac{240A_{RMS}}{T_e}} = \frac{\frac{0.6V}{4}}{\sqrt{2}\times 96mA_{RMS}} = \frac{0.15}{\sqrt{2}\times 96mA_{RMS}} = 1.1048\,\Omega_{se} = 2\times\left(0.5524\,\Omega_{diff}\right)$$

   Each one of the two burden resistors (for differential inputs) would be selected as 0.5524Ω.

2. Next, determine the current conversion factor (the equation shown, first, is the long-form definition):

$$K\_I_x = \frac{I_{CTmax}}{V_{diff\_max}\times G_{PGA}} = \frac{\sqrt{2}\times 240A_{RMS}}{0.15V\times G_{PGA}} = \frac{339.411A}{0.15V\times 4} = 565.685$$

   When using CTs with a burden resistor, the equation for K_I_x simplifies to (the preferred equivalent short-form):

$$K\_I_x = \frac{T_e}{R_{burden\_total}\times G_{PGA}} = \frac{2500}{1.1048\Omega\times 4} = 565.685$$

Where, T_e= CT equivalent turns ratio.

3. Finally, to compute an equivalent external current, multiply an internal Qformat number, $I_{INTERNAL}$, in the following fashion:

$$I_{LINE\,RMS} = K\_I_x \times I_{INTERNAL}$$

Rogowski Coil Current Sensors

Rogowski coils produce an output voltage proportional to the time derivative of the current being measured and exhibit a gain proportional to the frequency being measured, f, as well as a 90° phase shift relative to the input signal. A 50 Hz signal would have 5/6 the gain as an equivalent 60 Hz signal in addition to the phase shift. The metrology DSP includes a selectable DI (Digital Integrator) to process all current channels using Rogowski coil sensors and introduces a 1/f gain response and an ideal -90° phase shift to compensate for derivative nature of Rogowski coil sensors. The DI (Digital Integrator) filter is adjusted for unity gain at 60 Hz.

For example, it is preferable to have a max measurement current of 240A_{RMS} (200A_{RMS} + 20% over-current). The following steps must be taken (this example assumes use of a Rogowski coil with an output of 500 uV/A at 60 Hz (or 416.6$\bar{6}$ uV/A at 50 Hz) and a G_{PGA} = 4 but operating at a frequency of 50 Hz):

When using Rogowski coils, the equation for K_I_x simplifies to (the preferred equivalent short-form):

$K\_I_x = \frac{k_{sf}(60Hz)}{G_{PGA}} = \frac{2000}{4} = 500$, where, k_{sf} = Rogowski coil scale factor.

For this discussion, the scale factor, k_{sf}, is defined at the reference frequency, f_r = 60 Hz because the DI (Digital Integrator) filter was designed for unity gain at 60 Hz. If it is preferred to use k_{sf} defined at another frequency, the gain of the DI filter must be accounted for in the computation as follows:

$$k_{di}(f) = \frac{60Hz}{f}$$

$$K\_I_x = \frac{k_{sf}(f)}{G_{PGA} \times k_{di}(f)} = \frac{\left(\frac{I_{pr}(f)}{V_{sr}(f)}\right)}{G_{PGA}\left(\frac{60Hz}{50Hz}\right)} = \frac{\left(\frac{1A}{0.000416\bar{6}V}\right)}{4\left(\frac{6}{5}\right)} = 500$$

where, I_{pr} = primary rated current, V_{sr} = secondary rated voltage, f = frequency of operation [Hz].

Refer to “PIC32CXMTx Metrology User Guide” for a more detailed description.

Resistive Shunt Current Sensors

A resistive shunt current sensor produces an output voltage proportional to the current passing through it. Generally, if a shunt is used for measuring the active phase current, then the voltages of the shunt are at the high voltage of line phase being measured and the relative metering ground reference is usually connected directly to that line phase voltage to keep all voltages going into the measuring device at the same relative voltage level. This means the voltage of the neutral line is divided down to a fraction of a volt, also relative to the line phase voltage.

$$K_{Ix} = \frac{1}{G_{PGA} \times R_{shunt}}$$

Example:

If R_{shunt} =100u ohm = 0.0001 ohm and G_{PGA} = 8, then we can get:

K_{Ix} = 1000000 / (8 * 100) = 1250

The metrology firmware uses uQ22.10 to represent both integer and fractional numbers, so set:

K_Ix = ROUND(1250 * 2^10) = 0x00138800

Voltage channels:

K_CH_x corresponds to K_Vx. For proper ADC function, voltage divider circuitry must be provided to reduce each high-voltage input channel from its peak input value to the max peak acceptable ADC differential input voltage.

Typically, voltage channel inputs use single-ended input voltages (in some cases could be interesting to use differential inputs, of course if the measuring device allows it). While the maximum differential input voltage must not exceed 0.6V (V+ = 0. 3V, V- = -0.3V), it is recommended that the single-ended inputs be limited to ±0.3V. In typical applications, external scaling allows for any over-voltage factor (typically 20%). In some applications the over-voltage is increased to be able to measure the phase to phase voltage value (plus the typical 20%), to detect improper connection of the wires to the meter.

For example, it is preferable to have a max measurement voltage of $288V_{RMS}$ ($240V_{RMS}$ + 20% over-voltage). The following three steps must be taken:

1. Determine external voltage divider ratio (single-ended input):

$$K_{divider} = \frac{V_{ADCmax\,pk}}{V_{LINEmax\,RMS}} = \frac{0.3V_{pk}}{\sqrt{2} \times 288V_{RMS}} = 0.000736569$$

2. Internal scaling within the DSP takes care of the multiplication factor, V_{REF}, to renormalize the ADC gain, when the channel calibration constant, CAL_M_Vx, is used.
3. Next, determine voltage conversion factor:

$$K\_V_x = \frac{V_{LINEmax}}{V_{diff\_max}} = \frac{\sqrt{2} \times 288V_{RMS}}{0.3V_{pk}} = 1357.645$$

When using a simple resistive voltage divider, the equation for K_V_x simplifies to the equivalent short-form:

$$K\_V_x = \frac{1}{G_{resistor\_divider\_ratio}} = 1657.645$$

K_Vx is stored in uQ22.10 format.

4. Finally, to compute an equivalent external voltage, multiply an internal Qformat number, $V_{INTERNAL}$, in the following fashion:

$$V_{LINE\ RMS} = K\_V_x \times V_{INTERNAL}$$

Refer to “PIC32CXMTx Metrology User Guide” for a more detailed description.

Bit	31	30	29	28	27	26	25	24
	K_CHx[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	K_CHx[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	K_CHx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	K_CHx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 31:0 – K_CHx[31:0] (uQ22.10)

3.1.26 Channel Magnitude Calibration Constants

Name: CAL_M_CHx
Offset: Metrology_Reg_In[138-169]
Property: Read-Write

Multiplicative magnitude calibration constants are provided for each channel to equalize gain across all channels after an appropriate calibration procedure was exercised. All active input channels, both voltage and current, require final calibration to ensure full accuracy.

CAL_M_CHx: where x=[1, …, 31] is used to calibrate the channels.

$$CAL\_M\_CHx = \frac{CHx\_RMS}{K\_CHx \times \sqrt{\frac{ACC\_CH\_x}{N \times 2^{40}}}} \times 2^{29}$$

CHx_RMS is the ideal RMS value of input calibration channel. ACC_CH_x is the 64-bit accumulated I^2 or V^2- scaled quantities provided by metrology firmware. The value of N is the number of samples in the integration period provided in Metrology Status Registers.

Refer to “PIC32CXMTx Metrology User Guide” for a more detailed description.

Bit	31	30	29	28	27	26	25	24
	CAL_M_CHx[31:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	CAL_M_CHx[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	CAL_M_CHx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	CAL_M_CHx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 31:0 – CAL_M_CHx[31:0] (sQ2.29)

3.1.27 Per-Channel Phase Calibration Constants

Name: CAL_PH_CHx
Offset: Metrology_Reg_In[170-201]
Property: Read-Write

Phase calibration constants are provided for each channel to equalize relative phase differences across all channels after an appropriate calibration procedure was exercised. All active input channels, both voltage and current, require final calibration to ensure full accuracy. All phase-correction amounts are in BAMS units.

In cases where neither phase-phase vector transformation nor optimal phase-phase voltage measurement are not required, phase correction values may be set for only current channel, and voltage phase correction values are set to zero. However, if phase-phase equalization is also desired, voltage channel phase correction values may be used.

Input requested phase correction values are relative values that may be internally adjusted with an internally computed offset to achieve proper phase shifts for use within the phase correction DSP filters. Any internal offset adjustment made by the DSP is available in the PH_OFFSET status register (see PH_OFFSET). This internal offset phase adjustment is made to shift all requested phase correction values to ≤ -1.35° (at 60 Hz). The maximum phase correction capability among the different channels is 32.39º (at 60Hz) or 26.99º (at 50Hz).

The requested input phase correction values may change dynamically and will be used to compute new phase correction filter coefficients at the start of each integration period. If phase correction values do change dynamically and, if it is preferable to keep coefficients as stationary as possible (change as little as possible), then set the phase correction value of an unused channel to a value slightly larger (more positive) than the expected maximum value of the range of allowable phase correction values. Otherwise, all unused channel's phase correction values must be set to zero.

For example, the top row of hex values represents the phase corrections as input into the phase correction registers:

Table 3-2.

	CAL_PH_IA	CAL_PH_VA
Input phase corr. values (hex)	0xFFEDCBAA	0x00000000
Input phase corr. values (dec)	-0.10º	-0.00º
Internally computed offset	-1.35º	—
Actual internal phase delays	-1.45º	-1.35º

If it is preferable to correlate the phase delays of internal signals with the phase delays of outside world signals, simply compute the actual phase delay values by adding the value of PH_OFFSET to the raw input phase correction values.

All phase correction angles entered must be normalized to 60 Hz. For example, if a phase correction factor of -0.31° is measured at 50 Hz, the value at 60 Hz is easily calculated as:

$$\angle angle_{60Hz} = \frac{60}{50}\angle angle_{50Hz} = \frac{60}{50}(-0.31°)_{50Hz} = -0.372°_{60Hz}$$

and to convert to the proper BAMS input format:

$$-0.372°_{60Hz} = \frac{-0.372°}{180°} \times 2^{31} = 0xFFBC478B$$

At the start of every integration period, the input phase calibration constants are used to compute the proper phase correction filter coefficients. If a requested set of phase-corrections is not possible, an error will be returned in the status register STATE_FLAG: PC_OUT_OF_RANGE.

Note: Both sensor type and phase-correction inputs are used to properly compute a new set of phase-correction coefficients because an additional built-in phase shift is used for compensation when the digital integrator is automatically selected when selecting Rogowski coils.

Refer to “PIC32CXMTx Metrology User Guide” for a more detailed description.

Bit	31	30	29	28	27	26	25	24
	CAL_PH_CHx[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	CAL_PH_CHx[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	CAL_PH_CHx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	CAL_PH_CHx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

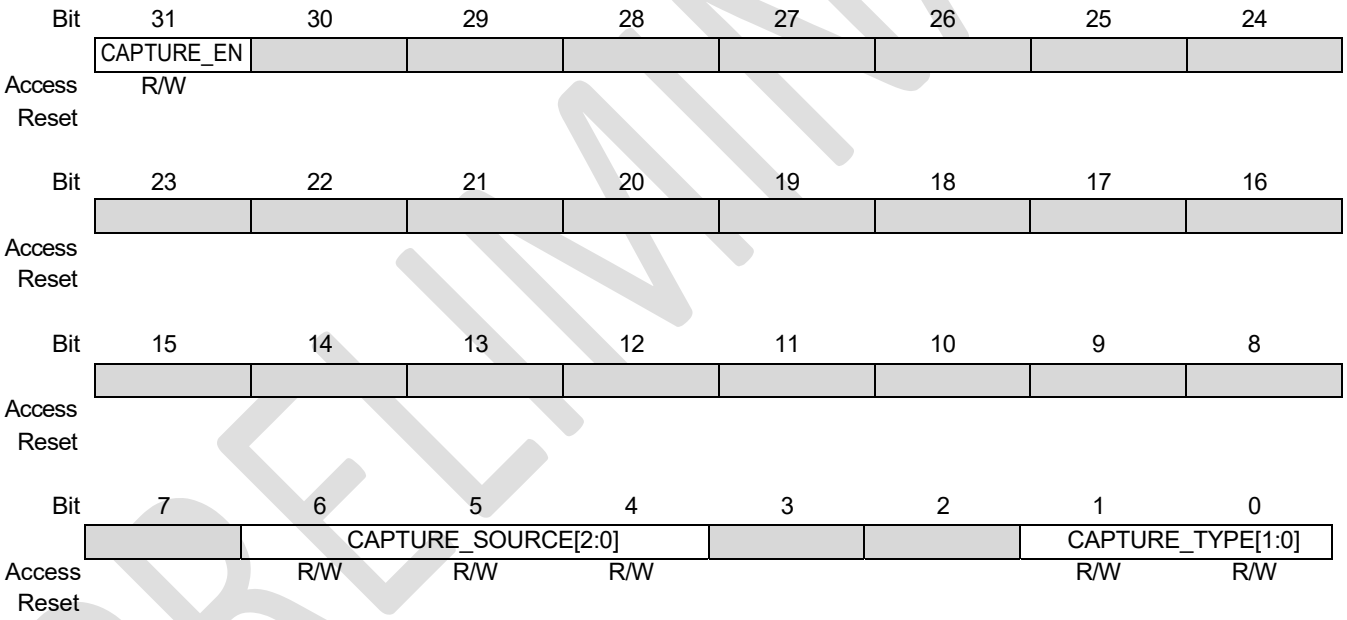
Bits 31:0 – CAL_PH_CHx[31:0] sQ0.31

3.1.28 Waveform Capture Control Register

Name: CAPTURE_CTRL
Offset: Metrology_Reg_In[202]
Property: Read-Write

Waveform capture of 32-bit samples may be accomplished through exercise of these control bits, to select the capture mode, which type of samples are to be captured and how many samples are captured. Capture data are written to the buffer starting at the address pointer stored in the CAPTURE_ADDR register. After each set of samples are captured, the number of the last sample set captured is stored in the CAPTURE_STATUS output register.

Upon completion of a one-shot capture sequence, the CAPTURE_STATE bits in the CAPTURE_STATUS register will be updated to COMPLETE, then, after the application code resets the CAPTURE_ENABLE bit to DISABLED, the CAPTURE_STATE bits will, then, be reset to DISABLED.



Bit 31 – CAPTURE_EN Enable Waveform Capture

Value	Description
0x0	Waveform capture is disabled
0x1	Waveform capture is enabled

Bits 6:4 – CAPTURE_SOURCE[2:0] Capture Source Select

All captured data is after Vref compensation was applied and are scaled values (normalized by the appropriate K_CHx). In the case of 16 kHz sampling data, the calibration constants were not applied. Vref compensation factor is 1.6 for the MCP391x.

Value	Description
0x0	Capture 16 kHz data [sQ1.30] before DSP filtering
0x1	Capture 4 kHz FBW data [sQ2.29] (Full Bandwidth = fundamental + harmonics)
0x2	Capture 4 kHz NBW data [sQ2.29] (Narrow Bandwidth = fundamental only)
0x3	Capture 8 kHz FBW data [sQ2.29] (Full Bandwidth = fundamental + harmonics)
Other	RESERVED

Bits 1:0 – CAPTURE_TYPE[1:0] Selects whether capture is one-shot in nature (no samples captured prior to being enabled) or continuous capturing.

Capture must be enabled to initiate a capture process. Once enabled, capture occurs based on the requested capture mode. If enabled and a continuous capture mode is selected, capture continues until it is disabled. If enabled and a one-shot capture mode is selected, capture continues until appointed number of samples is captured.

Value	Name	Description
0x0	One-Shot Capture Mode	Capture total CAPTURE_BUFF_SIZE of future data; capture will stop after capture finishes or is disabled.
0x1	Continuous Capture Mode	Continuous capture of waveform data in circular-buffer fashion; capture will stop immediately after capture is disabled. CAPTURE_OFFSET indicates the offset of latest sample in capture buffer.

3.1.29 Waveform Capture Channel Selection Register

Name: CAPTURE_CH_SEL
Offset: Metrology_Reg_In[203]
Property: Read-Write

Waveform capture of 32-bit samples may be accomplished through exercise of these control bits, to select the channels to be captured. Capture data are written to the buffer starting at the address pointer stored in the CAPTURE_ADDR register. After each set of samples are captured, the number of the last sample set captured is stored in the CAPTURE_STATUS output register.

Upon completion of a one-shot capture sequence, the CAPTURE_STATE bits in the CAPTURE_STATUS register will be updated to COMPLETE, then, after the application code resets the CAPTURE_ENABLE bit to DISABLED, the CAPTURE_STATE bits will, then, be reset to DISABLED.

Bit	31	30	29	28	27	26	25	24
	CH_SEL_CH31	CH_SEL_CH30	CH_SEL_CH29	CH_SEL_CH28	CH_SEL_CH27	CH_SEL_CH26	CH_SEL_CH25	CH_SEL_CH24
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	CH_SEL_CH23	CH_SEL_CH22	CH_SEL_CH21	CH_SEL_CH20	CH_SEL_CH19	CH_SEL_CH18	CH_SEL_CH17	CH_SEL_CH16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	CH_SEL_CH15	CH_SEL_CH14	CH_SEL_CH13	CH_SEL_CH12	CH_SEL_CH11	CH_SEL_CH10	CH_SEL_CH9	CH_SEL_CH8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	CH_SEL_CH7	CH_SEL_CH6	CH_SEL_CH5	CH_SEL_CH4	CH_SEL_CH3	CH_SEL_CH2	CH_SEL_CH1	CH_SEL_CH0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 31:0 – CH_SEL_x Capture Channel Select
Only selected channels are captured.

Value	Description
0x0	Waveform capture is disabled for channel x
0x1	Waveform capture is enabled for channel x

3.1.30 Capture Buffer Size

Name: CAPTURE_BUFF_SIZE
Offset: Metrology_Reg_In[204]
Property: Read-Write

CAPTURE_BUFF_SIZE specifies buffer size used for the capture function in units of 32-bit values. It must be divisible by the number of channels selected.

For example, to capture exactly 8,000 sets of samples of only the three voltage channels, set buffer size to:

CAPTURE_BUFF_SIZE = 8000[sample sets]×3[samples/set] = 24000[samples]= 0x5DC0

Note: A buffer of 24,000 samples is equal in size to 96,000 bytes.

Table 3-3. Capture Buffer Distribution Samples:

Channel CH0 is selected	Channels CH0 to CH5 are selected	Channels CH0 & CH5 are selected
...	...	...
CH0_0	CH0_0	CH0_0
CH0_1	CH1_0	CH5_0
CH0_2	CH2_0	CH0_1
CH0_3	CH3_0	CH5_1
CH0_4	CH4_0	CH0_2
CH0_5	CH5_0	CH5_2
CH0_6	CH0_1	CH0_3
CH0_7	CH1_1	CH5_3
CH0_8	CH2_1	CH0_4
—	CH3_1	CH5_4
—	CH4_1	—
—	CH5_1	—
—	CH0_2	—
—	CH1_2	—
—	CH2_2	—
—	CH3_2	—
—	CH4_2	—
—	CH5_2	—
—	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CAPTURE_BUFF_SIZE[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	CAPTURE_BUFF_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	CAPTURE_BUFF_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 23:0 – CAPTURE_BUFF_SIZE[23:0] (uQ24.0)

3.1.31 Waveform Capture Destination Buffer Address

Name: CAPTURE_ADDR
Offset: Metrology_Reg_In[205]
Property: Read-Write

This entry is used as the starting address of the waveform capture buffer and is interpreted as a pointer to a 32-bit unsigned integer.

The capture address must be set at least one sample period (250 µs) prior to enabling capture to ensure proper registration of the address.

Bit	31	30	29	28	27	26	25	24
	CAPTURE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	CAPTURE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	CAPTURE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	CAPTURE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 31:0 – CAPTURE_ADDR[31:0] (uQ32.0)

3.1.32 MCP391x Control Register 1

Name: MCP391x_GAIN
Offset: Metrology_Reg_In[209-212]
Property: Read-Write

Use these registers to configure the internal PGA of each one of the channels.

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
PGA_CH7			PGA_CH6			PGA_CH5	

15	14	13	12	11	10	9	8
PGA_CH5	PGA_CH4			PGA_CH3			PGA_CH2

7	6	5	4	3	2	1	0
PGA_CH2		PGA_CH1			PGA_CH0		

Bits 23:0 – PGA_CHx[] PGA setting for channel n.

000	Gain is 1 (default)
001	Gain is 2
010	Gain is 4
011	Gain is 8
100	Gain is 16
101	Gain is 32
110	Reserved (Gain =1)
111	Reserved (Gain =1)

3.1.33 MCP391x Control Register 2

Name: MCP391x_CONFIG0
Offset: Metrology_Reg_In[213-216]
Property: Read-Write

Only Dither and boost can be changed in this version.

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
EN_OFFCAL	EN_GAINCAL	DITHER[1:0]		BOOST[1:0]		PRE[1:0]	
bit 23							bit 16

R/W-0	R/W-1	R/W-1	U-0	U-0	U-0	U-0	U-0
OSR[2:0]			—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
VREFCAL[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23 **EN_OFFCAL:** 24-Bit Digital Offset Error Calibration on All Channels Enable bit
1 = Enabled; this mode does not add any group delay to the ADC data
0 = Disabled (default)

bit 22 **EN_GAINCAL:** 24-Bit Digital Gain Error Calibration on All Channels Enable/Disable bit
1 = Enabled; this mode adds a group delay on all channels of 24 DMCLK periods, all data ready pulses are delayed by 24 DMCLK clock periods compared to the mode with EN_GAINCAL = 0.
0 = Disabled (default)

bit 21-20 **DITHER[1:0]:** Dithering Circuit for Idle Tone's Cancellation and Improved THD on All Channels Control bits
11 = Dithering on, Strength = Maximum (default)
10 = Dithering on, Strength = Medium
01 = Dithering on, Strength = Minimum
00 = Dithering turned off

bit 19-18 **BOOST[1:0]:** Bias Current Selection for all ADCs bits
(impacts achievable maximum sampling speed, see Table 5-2)
11 = All channels have current x 2
10 = All channels have current x 1 (default)
01 = All channels have current x 0.66
00 = All channels have current x 0.5

bit 17-16 **PRE[1:0]:** Analog Master Clock (AMCLK) Prescaler Value bits
11 = AMCLK = MCLK/8
10 = AMCLK = MCLK/4
01 = AMCLK = MCLK/2
00 = AMCLK = MCLK (default)

REGISTER 8-7: CONFIG0 REGISTER (CONTINUED)

bit 15-13	**OSR[2:0]:** Oversampling Ratio for Delta-Sigma A/D Conversion bits (all channels, f_d/f_S) 111 = 4096 (f_d = 244 sps for MCLK = 4 MHz, f_s = AMCLK = 1 MHz) 110 = 2048 (f_d = 488 sps for MCLK = 4 MHz, f_s = AMCLK = 1 MHz) 101 = 1024 (f_d = 976 sps for MCLK = 4 MHz, f_s = AMCLK = 1 MHz) 100 = 512 (f_d = 1.953 ksps for MCLK = 4 MHz, f_s = AMCLK = 1 MHz) 011 = 256 (f_d = 3.90625 ksps for MCLK = 4 MHz, f_s = AMCLK = 1 MHz) (default) 010 = 128 (f_d = 7.8125 ksps for MCLK = 4 MHz, f_s = AMCLK = 1 MHz) 001 = 64 (f_d = 15.625 ksps for MCLK = 4 MHz, f_s = AMCLK = 1 MHz) 000 = 32 (f_d = 31.25 ksps for MCLK = 4 MHz, f_s = AMCLK = 1 MHz)
bit 12-8	**Unimplemented:** Read as '0'
bit 7-0	**VREFCAL[7:0]:** Internal Voltage Temperature Coefficient VREFCAL[7:0] Value bits

3.1.34 Per-Power Active Power Offset Register

Name: POWER_OFFSET_P_x
Offset: Metrology_Reg_In[218-248]
Property: RW, Format sQ-9.40 (same format as the lsb 32-bits of 64-bit P_x accumulators)

This value indicates the per-power active power offset, POWER_OFFSET_P_x: where x = [0, …, 30]. The units of POWER_OFFSET_P_x is [W samp-scaled].

For a fixed voltage, this offset may be computed by applying voltage phase(s), setting zero current(s) and reading the power's active power accumulator, P_x. Averaging over many readings or a longer integration period may provide a more statistically accurate estimate.

$$POWER\_OFFSET\_P\_x = \frac{ACC\_P\_x}{N}$$

Where N = number of samples in integration period.

Bit	31	30	29	28	27	26	25	24
	POWER_OFFSET_P_x[31:24]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset								

Bit	23	22	21	20	19	18	17	16
	POWER_OFFSET_P_x[23:16]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset								

Bit	15	14	13	12	11	10	9	8
	POWER_OFFSET_P_x[15:8]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset								

Bit	7	6	5	4	3	2	1	0
	POWER_OFFSET_P_x[7:0]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset								

Bits 31:0 – POWER_OFFSET_P_x[31:0] Per-Power Active Power Offset Register
POWER_OFFSET_P is stored in sQ1.30 format, and its value is subtracted each sample at a 4 kHz rate.

3.1.35 Per-Power Reactive Power Offset Register

Name: POWER_OFFSET_Q_x
Offset: Metrology_Reg_In[250-280]
Property: RW, Format sQ-9.40 (same format as the lsb 32-bits of 64-bit Q_x accumulators)

This value indicates the per-power reactive power offset, POWER_OFFSET_Q_x: where x = [0, …, 30]. The units of POWER_OFFSET_Q_x is [VAR samp-scaled].

For a fixed voltage, this offset may be computed by applying voltage phase(s), setting zero current(s) and reading the power's reactive power accumulator, Q_x. Averaging over many readings or a longer integration period may provide a more statistically accurate estimate.

$$POWER\_OFFSET\_Q\_x = \frac{ACC\_Q\_x}{N}$$

where N = number of samples in integration period.

Bit	31	30	29	28	27	26	25	24
	POWER_OFFSET_Q_x[31:24]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset								

Bit	23	22	21	20	19	18	17	16
	POWER_OFFSET_Q_x[23:16]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset								

Bit	15	14	13	12	11	10	9	8
	POWER_OFFSET_Q_x[15:8]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset								

Bit	7	6	5	4	3	2	1	0
	POWER_OFFSET_Q_x[7:0]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset								

Bits 31:0 – POWER_OFFSET_Q_x[31:0] Per-Power Reactive Power Offset Register
POWER_OFFSET_Q is stored in sQ1.30 format and its value is subtracted each sample at a 4 kHz rate.

3.2 Metrology Status Registers

The Metrology module generates primary 32-bit output measurement quantities for each measurement interval, per-channel and power quantities with each current or power designated by the subscript “_x”. The start address is 0x20086468

Note: I & V max values will need to be changed to accommodate functionality of recording max values for each half cycle

Offset	Variable	Access Mode	Name	Format	# Bytes	Min Value	Max Value	Default	Unit
0	VERSION	R	Metrology firmware version	—	4	—	—	—	integer
1	STATUS	R	Metrology status register	—	4	—	—	—	integer
2	STATE_FLAG	R	Metrology version and state flags register	—	4	—	—	—	integer
3	SWELL_OVERCURRENT_FLAG	R	Swell (voltage channels) or overcurrent (current channels) flag	—	4	—	—	—	integer
4	SAG_FLAG	R	Sag (voltage channels) flag	—	4	—	—	—	integer
5	CREEP_FLAG	R	Creep (current channels) flag	—	4	—	—	—	integer
6	PH_ACTIVE_FLAG	R	Phase x Active flag	—	4	—	—	—	integer
7	CAPTURE_STATUS	R	Waveform capture status	—	4	—	—	—	integer
8	INTERVAL_NUM	R	Interval number	—	4	0	—	—	integer
9	N	R	Number samples in measurement interval	uQ16.0	4	1	3960	0	integer
10	PH_OFFSET	R	Phase calibration offset	sQ0.31	4	-1.000	+0.9999	—	BAMS
11	FREQ	R	Frequency of fundamental harmonic	uQ20.12	4	45.000	135.000	—	Hz
12-43	FREQ_CHx	R	Frequency of fundamental harmonic, channel x	uQ20.12	32x4	45.000	124.000	—	Hz
44~45	RESERVED	—	—	—	—	—	—	—	—
46~77	CHx_MAX	R	Max current (current channels) or voltage (voltage channels) of channel x during measurement interval	sQ2.29	32x4	—	—	—	Apk scaled or Vpk scaled
78	FEATURES	R	Compiled feature indicator bits	uQ32.0	4	—	—	—	—
79	MPC_CRC_ERRORS	R	CRC errors in the MCP391x MCSPI communication	uQ32.0	4	—	—	—	integer
80~81	RESERVED	—	—	—	—	—	—	—	—
82	PULSE0_COUNTER	R	Number of pulses issued (Pulse 0)	uQ32.0	4	—	—	0	integer
83	PULSE1_COUNTER	R	Number of pulses issued (Pulse 1)	uQ32.0	4	—	—	0	integer
84	PULSE2_COUNTER	R	Number of pulses issued (Pulse 2)	uQ32.0	4	—	—	0	integer
85~86	RESERVED	—	—	—	—	—	—	—	—
87~118	ZC_N_CHx	R	Zero-crossing sample number of channel x. Just for voltage channels.	uQ20.12	32x4	—	—	—	real number
0	VERSION	R	Metrology firmware version	—	4	—	—	—	integer
1	STATUS	R	Metrology status register	—	4	—	—	—	integer
2	STATE_FLAG	R	Metrology version and state flags register	—	4	—	—	—	integer
3	SWELL_OVERCURRENT_FLAG	R	Swell (voltage channels) or overcurrent (current channels) flag	—	4	—	—	—	integer
4	SAG_FLAG	R	Sag (voltage channels) flag	—	4	—	—	—	integer
5	CREEP_FLAG	R	Creep (current channels) flag	—	4	—	—	—	integer
6	PH_ACTIVE_FLAG	R	Phase x Active flag	—	4	—	—	—	integer
7	CAPTURE_STATUS	R	Waveform capture status	—	4	—	—	—	integer
8	INTERVAL_NUM	R	Interval number	—	4	0	—	—	integer
9	N	R	Number samples in measurement interval	uQ16.0	4	1	3960	0	integer
10	PH_OFFSET	R	Phase calibration offset	sQ0.31	4	-1.000	+0.9999	—	BAMS
11	FREQ	R	Frequency of fundamental harmonic	uQ20.12	4	45.000	135.000	—	Hz
12-43	FREQ_CHx	R	Frequency of fundamental harmonic, channel x	uQ20.12	32x4	45.000	124.000	—	Hz
44~45	RESERVED	—	—	—	—	—	—	—	—
46~77	CHx_MAX	R	Max current (current channels) or voltage (voltage channels) of channel x during measurement interval	sQ2.29	32x4	—	—	—	Apk scaled or Vpk scaled
78	FEATURES	R	Compiled feature indicator bits	uQ32.0	4	—	—	—	—
79	MPC_CRC_ERRORS	R	CRC errors in the MCP391x MCSPI communication	uQ32.0	4	—	—	—	integer
80~81	RESERVED	—	—	—	—	—	—	—	—
85~86	RESERVED	—	—	—	—	—	—	—	—
87~118	ZC_N_CHx	R	Zero-crossing sample number of channel x. Just for voltage channels.	uQ20.12	32x4	—	—	—	real number
119~121	RESERVED	—	—	—	—	—	—	—	—

3.2.1 Metrology Firmware Version

Name: VERSION
Offset: Metrology_Reg_Out[0]
Property: Read

This register indicates the metrology version. It is recommended that the application code check this register to make sure that correct metrology version is used.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	FIRMWARE_MA JOR_VER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	FIRMWARE_MINOR_VER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	FIRMWARE_REV[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 23:16 – FIRMWARE_MA JOR_VER[7:0] Major Firmware Version
It indicates the major version number of metrology firmware.

Bits 15:8 – FIRMWARE_MINOR_VER[7:0] Minor Firmware Version
It indicates the minor version number of metrology firmware.

Bits 7:0 – FIRMWARE_REV[7:0] Firmware Revision
It indicates the revision number of metrology firmware.

3.2.2 Metrology Status Register

Name: STATUS
Offset: Metrology_Reg_Out[1]
Property: Read

This register provides status information about the metrology.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

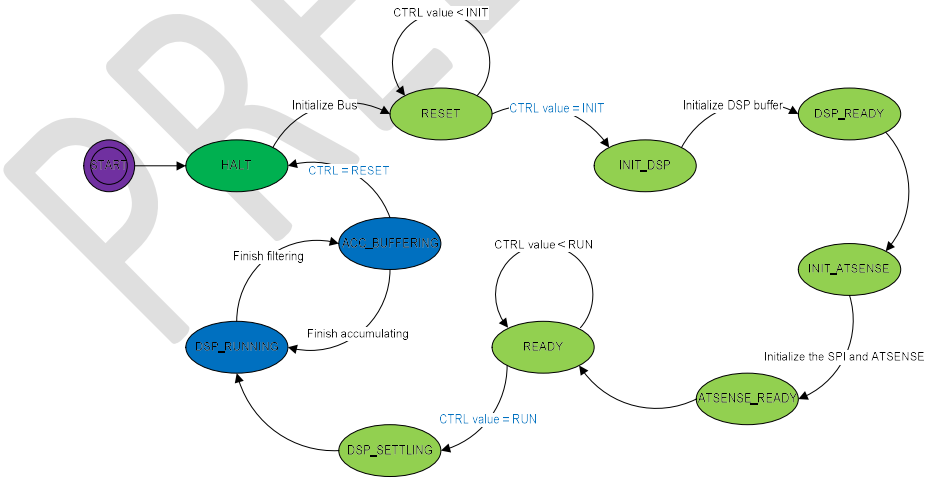
Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					STATUS[3:0]			
Access					R	R	R	R
Reset								

Bits 3:0 – STATUS[3:0] Metrology Function State
You can refer to the metrology state diagram for a more detailed description.

Figure 3-1. Metrology State Diagram



Value	Name	Description
0x0	HALT	Metrology module is halted
0x1	RESET	Resetting metrology module
0x2	INIT_DSP	Initializing DSP filters
0x3	DSP_READY	DSP filters were initialized
0x4	INIT_ATSENSE	Initializing AFE
0x5	ATSENSE_READY	AFE was initialized
0x6	READY	AFE calibration data were copied into output registers
0x7	DSP_SETTLING	Waiting for DSP filters to stabilize to full accuracy
0x8	DSP_RUNNING	DSP filters have stabilized to full accuracy
0x9 and above	RESERVED	—

3.2.3 Metrology State Flags Register

Name: STATE_FLAG
Offset: Metrology_Reg_Out[2]
Property: Read

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		PC_OUT_OF_RANGE	ARCH_DETECT_FAIL	CREEP_DET_P	CREEP_DET_Q			
Access		R	R	R	R			
Reset								

Bit	15	14	13	13	12	11	10	9
	HOST_ID_FAIL	HARMONIC_m_CONGIF[7:0]						
Access	R		R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	AFE_FAIL		FREQ_LOCKED	TIMING_Vx[5:0]				
Access	R		R	R	R	R	R	R
Reset								

Bit 22 – PC_OUT_OF_RANGE Phase Corrector Out of Range
Indicates if a set of requested phase correction values are out of range.

Value	Description
0	Requested phase correction values in range
1	Requested phase correction values out of range

Bit 21 – ARCH_DETECT_FAIL Architecture Detect Failure
Indicates that a proper device architecture was not detected (”SH” or “C”).

Value	Description
0	A proper device (”SH” or “C”) was detected
1	An improper device (not ”SH” nor “C”) was detected

Bit 20 – CREEP_DET_P Total Active Power Creep Detected Flag
CREEP_DET_P status flag only updated when enabled (CREEP_P_EN = 1).

Value	Description
0	Active power creep is not detected in the current full line cycle
1	Active power creep is detected in the current full line cycle

Bit 19 – CREEP_DET_Q Total Reactive Power Creep Detected Flag

CREEP_DET_Q status flag only updated when enabled (CREEP_Q_EN = 1).

Value	Description
0	Reactive power creep is not detected in the current full line cycle
1	Reactive power creep is detected in the current full line cycle

Bit 15 – HOST_ID_FAIL Host Identification Failure Indication

The detection process determines if the host corresponds to a PIC32CXMTC. If a proper ID is not made, this bit is used to show this status.

Value	Description
0	Proper PIC32CXMTC part successfully identified
1	Failed to identify proper PIC32CXMTC part

Bits 15:8 – HARMONIC_m_CONF[7:0] Harmonic Analysis Result Indication

When requested, the metrology module will generate the RMS value for one additional harmonic. There is delay between a particular request and the associated analysis output results; therefore, HARMONIC_m_CONF is used to indicate which harmonic the present analysis results are indicative of.

Bit 7 – ATFE_FAIL AFE State

Value	Description
0	AFE initialization is successful
1	AFE initialization is failed

Bit 5 – FREQ_LOCKED Frequency Locked Flag

Value	Description
0	Line frequency is not determined. Using sample count limit for metrology integration period.
1	Line frequency was determined

Bits 4:3 – TIMING_Vx[5:0] Active Voltage Channel

Indicates which active voltage channel is used for frequency determination and cycle timing. If no voltage phases are active, phase V0 is selected by default.

Value	Description
n (0-31)	Voltage phase Vn is used for timing extraction purposes

3.2.4 Metrology Swell/Overcurrent Flags Register

Name: SWELL_OVERCURRENT_FLAG
Offset: Metrology_Reg_Out[3]
Property: Read

Bit	31	30	29	28	27	26	25	24
	SWELL_OV_DET_CHx[31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	SWELL_OV_DET_CHx[23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	SWELL_OV_DET_CHx[15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	SWELL_OV_DET_CHx[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 0:31 – SWELL_OV_DET_CHx Voltage Swell (for voltage channels) or Overcurrent (for current channels) Detected Flag for Channel x.

Overcurrent is not supported in this version.

Value	Description
0	Voltage swell or overcurrent is not detected for the current half line cycle
1	Voltage swell or overcurrent is detected for the current half line cycle

3.2.5 Metrology Sag Flags Register

Name: SAG_FLAG
Offset: Metrology_Reg_Out[4]
Property: Read

Bit	31	30	29	28	27	26	25	24
	SAG_DET_CHx[31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	SAG_DET_CHx[23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	SAG_DET_CHx[15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	SAG_DET_CHx[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 0:31 – SAG_DET_CHx Voltage Sag Detected Flag for Channel x. The result is updated just for the channels configured as voltage.

Value	Description
0	Voltage sag is not detected in the current half line cycle
1	Voltage sag is detected in the current half line cycle

3.2.6 Metrology Creep Flags Register

Name: CREEP_FLAG
Offset: Metrology_Reg_Out[5]
Property: Read

Bit	31	30	29	28	27	26	25	24
	CREEP_DET_CHx[31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	CREEP_DET_CHx[23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	CREEP_DET_CHx[15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	CREEP_DET_CHx[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 0:31 – CREEP_DET_CHx Channel x Current Creep Detected.

Flag CREEP_DET_CH_x status flag only updated when enabled (CREEP_I_EN = 1) and when the channel is configured as current.

Value	Description
0	Channel x current creep is not detected in the current full line cycle
1	Channel x current creep is detected in the current full line cycle

Bits 0, 1, 2 – PH_x_ACTIVE Phase x is active

Value	Description
0	Voltage phase x is inactive
1	Voltage phase x is active

3.2.7 Metrology Phase Active Flags Register

Name: PHASE_ACTIVE_FLAG
Offset: Metrology_Reg_Out[6]
Property: Read

Bit	31	30	29	28	27	26	25	24
	PHx_ACTIVE[31:24]							
Access		R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	PHx_ACTIVE [23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	PHx_ACTIVE [15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	PHx_ACTIVE [7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 0:30 – PH_ACTIVE Phase x is active

Value	Description
0	Phase x is inactive (the channel x, if configured as voltage, is inactive)
1	Phase x is active (the channel x, if configured as voltage, is active)

3.2.8 Waveform Capture Function Status

Name: CAPTURE_STATUS
Offset: Metrology_Reg_Out[7]
Property: Read

Bit	31	30	29	28	27	26	25	24
	CAPTURE_WRAP			INVALID_ADDR	CAPTURE_STATE[3:0]			
Access	R			R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	CAPTURE_OFFSET[23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	CAPTURE_OFFSET[15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	CAPTURE_OFFSET[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit 31 – CAPTURE_WRAP Capture Buffer Wrapped

Value	Name	Description
0	NOT WRAPPED	Buffer has not wrapped
1	WRAPPED	Buffer has wrapped at least once (in circular buffer fashion, as used in continuous capture modes)

Bit 28 – INVALID_ADDR Invalid Capture Address

Value	Name	Description
0	0	Capture address within valid range [0x20000000, 0x20080000)
1	1	Capture address outside valid range

Bits 27:24 – CAPTURE_STATE[3:0] Waveform Capture Status

Status will be meaningful only when CAPTURE_EN is set to '1'.

Value	Name	Description
0x0	DISABLED	Capture disabled
0x1	ACTIVE	Capture in progress
0x2	COMPLETE	Capture completed
0x3	RESERVED	—

Bits 23:0 – CAPTURE_OFFSET[23:0] Capture Offset

Offset within the buffer indicating the position of the last sample stored.

3.2.9 Measurement Interval Number

Name: INTERVAL_NUM
Offset: Metrology_Reg_Out[8]
Property: Read

The measurement interval number associated with the present set of Metrology output data.

Bit	31	30	29	28	27	26	25	24
	INTERVAL_NUM[15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	INTERVAL_NUM[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	HALFCYCLE_COUNT[15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

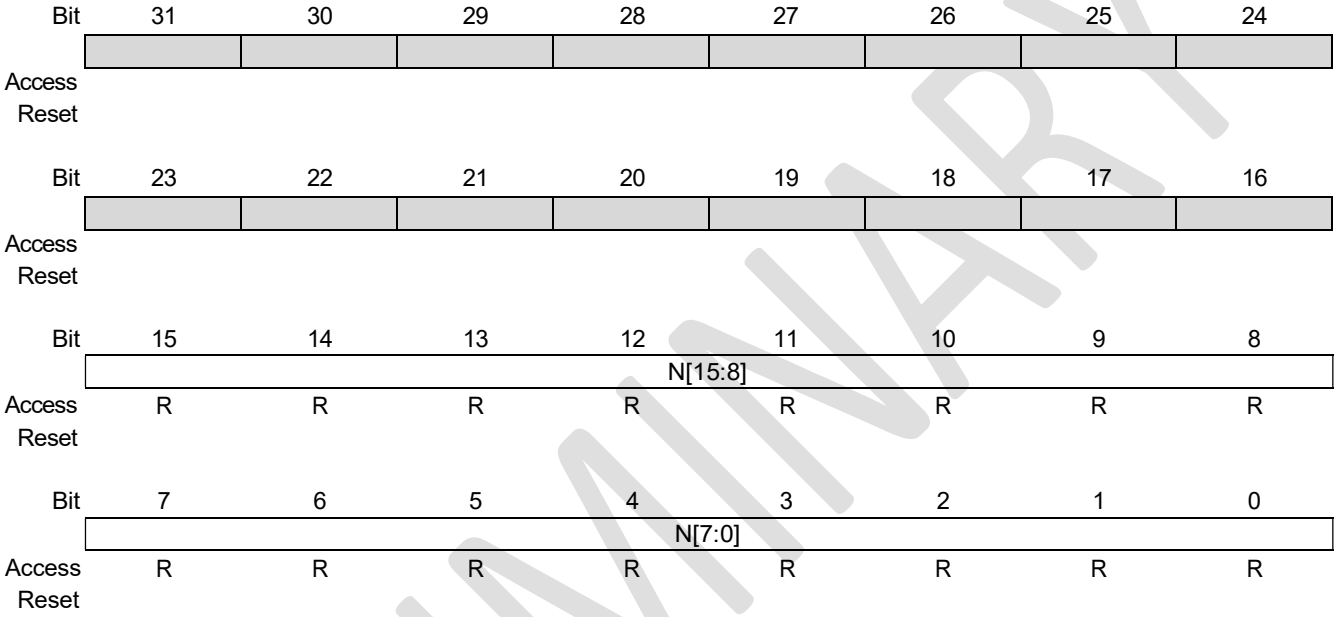
Bit	7	6	5	4	3	2	1	0
	HALFCYCLE_ OUNT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 31:16 – INTERVAL_NUM[15:0] Interval number (uQ16.0)
The number of the present integration interval. This count rolls over from max count to 0.

Bits 15:0 – HALFCYCLE_COUNT[15:0] Sub-interval number (uQ16.0)
The sub-interval number is the number of half-cycles that have occurred in the present integration interval; depending on how often interrupts are selected. This count resets each new integration interval.

3.2.10 Number of Samples in the Last Measurement Interval

Name: N
Offset: Metrology_Reg_Out[9]
Property: Read



Bits 15:0 – N[15:0] Number of Samples in the Last Measurement Interval (uQ16.0)
The number of samples, N, in the last measurement interval based on zero-crossings of the selected voltage channel.
Note: It is recommended that this value be used to calculate the RMS value or power.

3.2.11 Phase Correction Filter Offset

Name: PH_OFFSET
Offset: Metrology_Reg_Out[10]
Property: Read

Bit	31	30	29	28	27	26	25	24
	PH_OFFSET[31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	PH_OFFSET[23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	PH_OFFSET[15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	PH_OFFSET[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 31:0 – PH_OFFSET[31:0] Phase Correction Filter Offset (sQ0.31)

All voltage and current channels may be phase corrected by setting the requested relative phase adjustment values in registers: CAL_PH_Vx & CAL_PH_Iy. The actual phase adjustment angles implemented will be offset by this amount, the minimum required, such that all phase corrections are ≤ -1.35° @ 60 Hz (-1.125° @ 50 Hz). To determine the actual phase correction angle for each channel, add this offset to each requested phase correction amount. See “CAL_PH_Ix, CAL_PH_Vx” description for detailed example.

3.2.12 Active Line Voltage Fundamental Harmonic Frequency

Name: FREQ
Offset: Metrology_Reg_Out[11]
Property: Read

Bit	31	30	29	28	27	26	25	24
	FREQ[31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	FREQ[23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	FREQ[15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	FREQ[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 31:0 – FREQ[31:0] Frequency of Fundamental Harmonic (uQ20.12)
Frequency of the line voltage fundamental harmonic component is determined by the Metrology module and provided in the variable FREQ, using the dominant phase. In addition, a separate frequency is determined for each individual voltage phase, for each phases x = [0, …, 31].

3.2.13 Active Line Voltage Fundamental Harmonic Frequency

Name: FREQ_CHx
Offset: Metrology_Reg_Out[12-43]
Property: Read

Bit	31	30	29	28	27	26	25	24
	FREQ_CHx[31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	FREQ_CHx [23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	FREQ_CHx [15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	FREQ_CHx [7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 31:0 – FREQ[31:0] Frequency of Fundamental Harmonic (uQ20.12)
Frequency of the line voltage fundamental harmonic component is determined by the Metrology module and provided in the variable FREQ, using the dominant phase. In addition, a separate frequency is determined for each individual voltage phase, for each phase x = [0, …, 31]. The register is updated only if the channel CHx is configured as voltage.

3.2.14 Channel Peak Registers

Name: CHx_MAX
Offset: Metrology_Reg_Out[46-77]
Property: Read

There are 32 registers, one for each channel. The value in each register indicates the maximum value of the channel.
For the current channels CHx_MAX corresponds to Ix_MAX, and it is the maximum current peak absolute value of channel x in units of [Amp_{pk} scaled].

They can be reset by setting I_MAX_RESET to '1'.

The peak current may be calculated by the following formula:

$$I_{x_{peak}} = \frac{I_{x_{MAX}}}{2^{29}} \times K_{I_x} = \frac{I_{x_{MAX}}}{2^{29}} \times \frac{K\_Ix}{2^{10}}$$

Where K_I_x is the current conversion factor in float format, or K_Ix is the current conversion register value, and I_x_peak is the peak current of channel x, in unit of Amp.

Current max values, Ix_MAX are determined using FBW (Full Band-Width) baseband DSP-filtered data.

For the voltage channels CHx_MAX corresponds to V_x_MAX, and it is the maximum voltage peak absolute value of channel x in units of [$Volt_{pk}$ scaled].

They can be reset by setting V_MAX_RESET to '1'.

The peak voltage may be calculated by following formula:

$$V\_x\_peak = \frac{V\_x\_MAX}{2^{29}} \times K\_V_x$$

Where K_V_x is the voltage conversion factor in float format; V_x_peak is the peak voltage of channel x, in unit of Volt.

Voltage max values, V_x_MAX are determined using FBW (Full Band-Width) baseband filtered data.

Bit	31	30	29	28	27	26	25	24
	CH_x_MAX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	CH_x_MAX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	CH_x_MAX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	CH_x_MAX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 31:0 – CH_x_MAX[31:0] Max Current or voltage During Measurement Interval (sQ2.29)

3.2.15 Compiled Feature Indicator Bits

Name: FEATURES
Offset: Metrology_Reg_Out[78]

Property: Read

Bit	31	30	29	28	27	26	25	24
	POLY_PHASE	SINGLE_PHASE				RCZ_OUT		Fs_SAMPLE_RATE
Access	R	R				R		R
Reset								

Bit	23	22	21	20	19	18	17	16
		ATSense_LOC	NUM_PULSES[1:0]		ROGOWSKI_DC_REMOVE	CAPTURE	CREEP	DFT_ENABLED
Access		R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	CORE_CLK_SPEED[3:0]				RZC_DETECT	PQ_OFFSET_X	I_N_MUXING	HALF_COPROC_CLK
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
								DEBUG_MODES
Access								R
Reset								

Bit 31 – POLY_PHASE Flag

Value	Description
1	Compiled: Poly-phase metering enabled.

Bit 30 – SINGLE_PHASE Flag

Value	Description
1	Compiled: Single-phase metering enabled.

Bit 26 – RCZ_OUT Flag

Value	Description
1	Compiled: Detect independent V_A raw zero-crossings and output signal on pin PD19 **Note:** Not compatible with NUM_PULSES = 3

Bit 24 – Fs_SAMPLE_RATE

Metrology baseband sample rate

Value	Description
0	Baseband sample rate FS = 4000 KHz

1	Baseband sample rate FS = 8000 KHz

Bit 22 – ATSense_LOC

Value	Description
0	PIC32CXMTSH, Internal ATSense detected (ATsense203)
1	PIC32CXMTC, External ATSense detected (ATSense301)

Bits 21:20 – NUM_PULSES[1:0]

Metrology may be compiled with different number of pulses enabled, [0-3].
NUM_PULSES equals the number of pulses enabled during compile time.

Bit 19 – ROGOWSKI_DC_REMOVE Flag

Value	Description
1	Compiled for DC-removal before integrator filter when using Rogowski coil current sensors

Bit 18 – CAPTURE Flag

Value	Description
1	Compiled for waveform capture

Bit 17 – CREEP Flag

Value	Description
1	Compiled for CREEP thresholding

Bit 16 – DFT_ENABLED Flag

Value	Description
1	Compiled for DFT harmonic analysis

Bits 15:12 – CORE_CLK_SPEED[3:0]

Core-1 (Metrology core) clock fixed at 237.568 MHz in PIC32CXMTxx metrology

Value	Description
0x0	Compiled to be used with Core-0 clock = undefined
0x1	Compiled to be used with Core-0 clock = 102.400 MHz
0x2	Compiled to be used with Core-0 clock = 106.496 MHz
0x3	Compiled to be used with Core-0 clock = 110.592 MHz
0x4	Compiled to be used with Core-0 clock = 114.688 MHz
0x5	Compiled to be used with Core-0 clock = 118.784 MHz
0x6	Compiled to be used with Core-0 clock = 237.568 MHz
0x7	Reserved

Bit 11 – RZC_DETECT Flag

Value	Description
1	Compiled for raw zero-cross detect

Bit 10 – PQ_OFFSET_X Flag

Value	Description
1	Compiled for use of PQ per-phase offsets

Bit 9 – I_N_MUXING Flag

Value	Description
1	Compiled for near-full bandwidth I_Neutral metrology

Bit 8 – HALF_COPROC_CLK Flag

Value	Description
1	Compiled for Core1 coprocessor to run at half speed of Core0

Bit 0 – DEBUG_MODES

Value	Description
0	Unless specifically compiled for a debug mode, this bit is always = 0
1	Metrology FW compiled in a DEBUG mode

3.2.16 CRC error counter

Name: MCP_CRC_ERRORS
Offset: Metrology_Reg_Out[79]
Property: Read

Bit	31	30	29	28	27	26	25	24
	MCP_CRC_ERRORS[31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	MCP_CRC_ERRORS[23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	MCP_CRC_ERRORS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	MCP_CRC_ERRORS[7:0]							

Bits 31:0 – MCP_CRC_ERRORS[31:0] CRC error counter (uQ32.0)

The register counts the number of CRC errors in the MCSPI frames transmitting the raw data samples from the MCSPI to the host MCU.

3.2.17 Pulse counters

Name: PULSEx_COUNTER
Offset: Metrology_Reg_Out[82-84]
Property: Read

Bit	31	30	29	28	27	26	25	24
	PULSEx_COUNTER[31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	PULSEx_COUNTER[23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	PULSEx_COUNTER[15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	PULSEx_COUNTER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 31:0 – PULSEx_COUNTER[31:0] Pulse counters (uQ32.0)
The registers count the number of pulses generated by the available pulse outputs.

3.2.18 Zero-Crossing Sample Number of Channel x Voltage

Name: ZC_N_CHx
Offset: Metrology_Reg_Out[87-118]
Property: Read

There are 32 registers, one per each channel. The registers are only updated if the channel is configured as voltage.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	ZC_COUNT_CHx[23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	ZC_COUNT_CHx[15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	ZC_COUNT_CHx[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 23:0 – ZC_COUNT_CHx[23:0] Zero Crossing Count (uQ20.12)
Zero-crossing sample count of last positive-going zero-crossing of the CH_x voltage channel, in units of the 4K Hz sample rate. Use this to compare with other voltage channels to determine relative phase order.

3.3 Accumulated Output Quantities

All Metrology 64-bit output accumulator registers are prefixed “Metrology_Acc_Out_”. The start address is 0x20086650. All values are integrated at an equivalent sampling rate of 4000 KHz. The Metrology module generates the following primary output measurement quantities for each measurement interval, per-phase quantities with each voltage or current channel, as well as powers (understood as a pair of voltage/current) designated by the subscript “_x”.

The number of channels depends on the number of AFEs connected to the host MCU, and its type. A channel can be configured as current or voltage channel. The powers are configured with the control registers, defining the pair of voltage and current channels generating power quantities. The maximum number of powers is equal to the number of channels minus one. Example: 2 units of MCP3914 have 16 channels. User can configure the channels and define the powers according to their application. Several options are possible:

- Example 1: 1 voltage channel and 15 current channels, so 15 powers.
- Example 2: 3 voltage channels and 13 currents (4 currents for each voltage and the last one for neutral current measurement). In this case there are 12 powers.

Offset	Variable	Access Mode	Name	Format	# Bytes	Min Value	Max Value	Default	Unit
0	CH_x	R	For channels configured as current inputs, it returns Amp-squared-samples, channel x, fundamental + harmonics For channels configured as voltage inputs, it returns Volt-squared-samples, channel x, fundamental + harmonics	uQ24.40	32x8	—	—	—	Amp^2samp scaled or $Volt^2$samp scaled
32	CH_x_F	R	For channels configured as current inputs, it returns Amp-squared-samples, channel x, fundamental only For channels configured as voltage inputs, it returns Volt-squared-samples, channel x, fundamental only	uQ24.40	32x8	—	—	—	Amp^2samp scaled
64	P_x	R	Watt-samples, power x, fundamental + harmonics	sQ23.40	31x8	—	—	—	W-samp scaled
95	RESERVED	R	—	—	8	—	—	—	—
96	P_x_F	R	Watt-samples, power x, fundamental only	sQ23.40	31x8	—	—	—	W-samp scaled
127	RESERVED	R	—	—	8	—	—	—	—
128	Q_CH_x	R	VAR-samples, power x, fundamental + harmonics	sQ23.40	31x8	—	—	—	VAR-samp scaled
159	RESERVED	R	—	—	8	—	—	—	—
160	Q_CH_x_F	R	VAR-samples, power x, fundamental only	sQ23.40	31x8	—	—	—	VAR-samp scaled
191	RESERVED	R	—	—	8	—	—	—	—
192	V_AB	R	Volt-squared-samples, VA – VB, fundamental + harmonics	uQ24.40	8	—	—	—	Volt2samp scaled
193	V_BC	R	Volt-squared-samples, VB – VC, fundamental + harmonics	uQ24.40	8	—	—	—	Volt2samp scaled
194	V_CA	R	Volt-squared-samples, VC – VA, fundamental + harmonics	uQ24.40	8	—	—	—	Volt2samp scaled
195	V_AB_F	R	Volt-squared-samples, VA – VB, fundamental only	uQ24.40	8	—	—	—	Volt2samp scaled
196	V_BC_F	R	Volt-squared-samples, VB – VC, fundamental only	uQ24.40	8	—	—	—	Volt2samp scaled
197	V_CA_F	R	Volt-squared-samples, VC – VA, fundamental only	uQ24.40	8	—	—	—	Volt2samp scaled
198	ACC_T0	R	Total accumulated quantities specified by PC0_TYPE	sQ33.30	8	—	—	—	Wh, VArh, Amp2h
199	ACC_T1	R	Total accumulated quantities specified by PC1_TYPE	sQ33.30	8	—	—	—	Wh, VArh, Amp2h
200	ACC_T2	R	Total accumulated quantities specified by PC2_TYPE	sQ33.30	8	—	—	—	Wh, VArh, Amp2h
201~215	RESERVED	R	—	—	8	—	—	—	—

3.3.1 Accumulated Current or Voltage Quantities

Name: CH_x/CH_x_F
Offset: Metrology_Acc_Out[0-63]
Property: Read

There are 32 registers for the fundamental plus harmonics quantities (CH_x) and 32 for the fundamental only ones (CH_x_F).

Current channels:

The metrology module generates the following accumulated current (I^2) quantities: I_x, I_x_F. These accumulators are in units of [Amp^2samp scaled] in format [uQ24.40] and represent the accumulated scaled current quantities in the integration period. They are calculated according to the following formula:

$$I\_x = \sum_{i=1}^{N} (I\_x\_sample_i)^2$$

Where, $I\_x\_sample_i$ is i^{th} sampled current value of channel x in the present integration period; x = [0, …, 31]; and N is the number of samples in the last measurement interval.

They may be used to calculate the RMS value of the current.

Voltage channels:

The metrology module generates the following accumulated phase voltage (V^2) quantities: V_x, V_x_F. These accumulators are in units of [$Volt^2$samp scaled] in format [uQ24.40] and represent the accumulated scaled voltage quantities in the integration period. They are calculated according to the following formula:

$$V\_x = \sum_{i=1}^{N} (V\_x\_sample_i)^2$$

Where, $V\_x\_sample_i$ is i^{th} sampled voltage value of channel x in present integration period; x = [0, …, 31].

They may be used to calculate the RMS value of the voltage.

Bit	63	62	61	60	59	58	57	56
	CH_x/CH_x_F[63:56]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	55	54	53	52	51	50	49	48
	CH_x/CH_x_F[55:48]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	47	46	45	44	43	42	41	40
	CH_x/CH_x_F [47:40]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	39	38	37	36	35	34	33	32
	CH_x/CH_x_F [39:32]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	31	30	29	28	27	26	25	24
	CH_x/CH_x_F [31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	CH_x/CH_x_F [23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	CH_x/CH_x_F [15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	CH_x/CH_x_F[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 63:0 – CH_x/CH_x_F[63:0] Amp-Squared-Samples, uQ24.40 (I_x, I_x_F), or Volt-squared-samples, (uQ24.40)

3.3.2 Accumulated Active Power Quantities

Name: P_x
Offset: Metrology_Acc_Out[64-95]
Property: Read

The metrology module generates the accumulated active power (P) quantities P_x. There are 31 registers, corresponding to the maximum number of supported powers.

They are in units of [W-samp scaled]. They are scaled accumulated active power quantities in the whole integration period. They are calculated according to the following formula:

$$P\_x = \sum_{i=1}^{n} V\_a\_sample_i * I\_b\_sample_i$$

Where, $V\_a\_sample_i$ is i^{th} sampled voltage value in present integration period; $I\_b\_sample_i$ is i^{th} sampled current value in present integration period; N is the number of samples in the last measurement interval.

The pair [a,b] corresponds to the voltage (a) and current (b) channels generating the power x, according to the configuration in the control registers

They are used to calculate the active power.

P_x are stored in sQ23.40 format.

Bit	63	62	61	60	59	58	57	56
	P_x [63:56]							
Access	R	R	R	R	R	R	R	R
Reset								

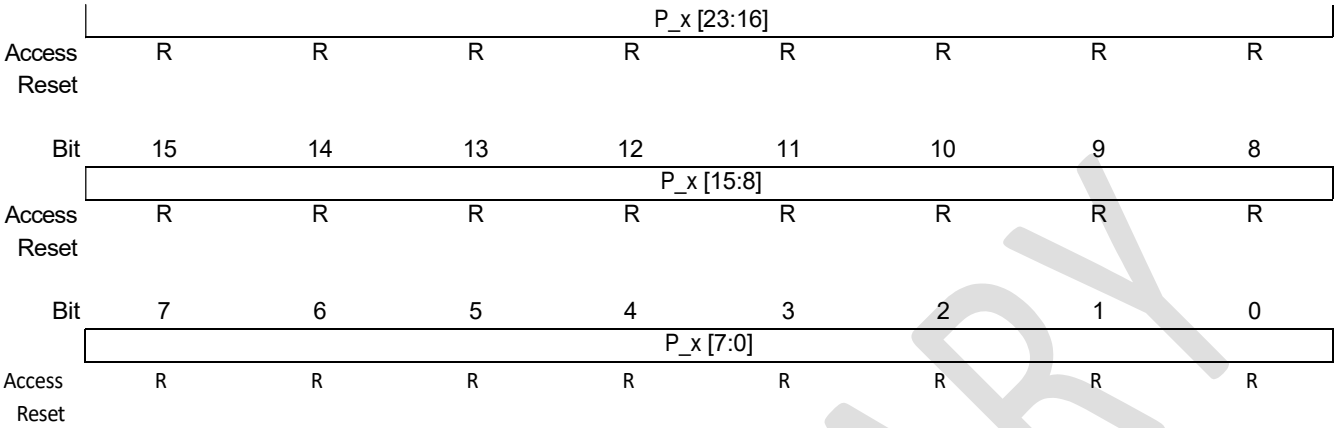
Bit	55	54	53	52	51	50	49	48
	P_x [55:48]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	47	46	45	44	43	42	41	40
	P_x [47:40]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	39	38	37	36	35	34	33	32
	P_x [39:32]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	31	30	29	28	27	26	25	24
	P_x [31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16



Bits 63:0 – P_x[63:0] Watt-samples, power-x (sQ23.40)

3.3.3 Accumulated Active Power Quantities, Fundamental only

Name: P_x_F
Offset: Metrology_Acc_Out[96-126]
Property: Read

The metrology module generates the accumulated active power (P) quantities P_x_F (fundamental only). There are 31 registers, corresponding to the maximum number of supported powers.

They are in units of [W-samp scaled]. They are scaled accumulated active power quantities in the whole integration period. They are calculated according to the following formula:

$$P\_x\_F = \sum_{i=1}^{n} V\_a\_sample_i * I\_b\_sample_i$$

Where, $V\_a\_sample_i$ is i^{th} sampled voltage value in present integration period; $I\_b\_sample_i$ is i^{th} sampled current value in present integration period; N is the number of samples in the last measurement interval.

The pair [a,b] corresponds to the voltage (a) and current (b) channels generating the power x, according to the configuration in the control registers

They are used to calculate the active power.

P_x are stored in sQ23.40 format.

Bit	63	62	61	60	59	58	57	56
	P_x_F [63:56]							
Access	R	R	R	R	R	R	R	R
Reset								

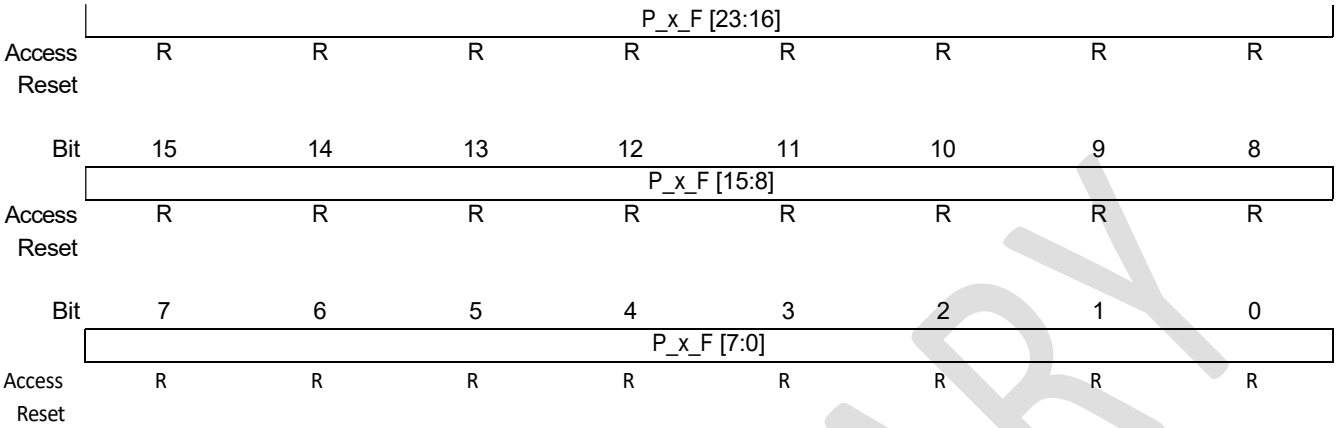
Bit	55	54	53	52	51	50	49	48
	P_x_F [55:48]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	47	46	45	44	43	42	41	40
	P_x_F [47:40]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	39	38	37	36	35	34	33	32
	P_x_F [39:32]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	31	30	29	28	27	26	25	24
	P_x_F [31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16



Bits 63:0 – P_x_F[63:0] Watt-samples, power-x (sQ23.40)

3.3.4 Accumulated Reactive Power Quantities

Name: Q_x
Offset: Metrology_Acc_Out[128-158]
Property: Read

The metrology module generates the accumulated reactive power (Q) quantities Q_x. There are 31 registers, corresponding to the maximum number of supported powers.

They are in units of [VAR samp-scaled]. They are scaled accumulated reactive power quantities in the whole integration period. They are calculated according to the following formula:

$$Q\_x = \sum_{i=1}^{n} V\_a'\_sample_i * I\_b''\_sample_i$$

Where, $V\_a'\_sample_i$ is i[th] sampled voltage value in present integration period; $I\_b''\_sample_i$ is i[th] sampled current value in present integration period; N is the number of samples in the last measurement interval. $V\_a'\_sample_i$, and $I\_b''\_sample_i$ have additional 90 degree phase difference.

The pair [a,b] corresponds to the voltage (a) and current (b) channels generating the power x, according to the configuration in the control registers

They are used to calculate the reactive power.

Q_x are stored in sQ23.40 format.

Bit	63	62	61	60	59	58	57	56
	Q_x [63:56]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	55	54	53	52	51	50	49	48
	Q_x [55:48]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	47	46	45	44	43	42	41	40
	Q_x [47:40]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	39	38	37	36	35	34	33	32
	Q_x [39:32]							

Access	R	R	R	R	R	R	R	R
Reset								
Bit	31	30	29	28	27	26	25	24
	Q_x [31:24]							
Access	R	R	R	R	R	R	R	R
Reset								
Bit	23	22	21	20	19	18	17	16
	Q_x [23:16]							
Access	R	R	R	R	R	R	R	R
Reset								
Bit	15	14	13	12	11	10	9	8
	Q_x [15:8]							
Access	R	R	R	R	R	R	R	R
Reset								
Bit	7	6	5	4	3	2	1	0
	Q_x [7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 63:0 – Q_x[63:0] VAR-Samples, power x (sQ23.40)

3.3.5 Accumulated Reactive Power Quantities, Fundamental only

Name: Q_x_F
Offset: Metrology_Acc_Out[160-190]
Property: Read

The metrology module generates the accumulated reactive power (Q) quantities Q_x_F (fundamental only). There are 31 registers, corresponding to the maximum number of supported powers.

They are in units of [VAR samp-scaled]. They are scaled accumulated reactive power quantities in the whole integration period. They are calculated according to the following formula:

$$Q\_x\_F = \sum_{i=1}^{n} V\_a'\_sample_i * I\_b''\_sample_i$$

Where, $V\_a'\_sample_i$ is i[th] sampled voltage value in present integration period; $I\_b''\_sample_i$ is i[th] sampled current value in present integration period; N is the number of samples in the last measurement interval. $V\_a'\_sample_i$, and $I\_b''\_sample_i$ have additional 90 degree phase difference.

The pair [a,b] corresponds to the voltage (a) and current (b) channels generating the power x, according to the configuration in the control registers

They are used to calculate the reactive power.

Q_x_F are stored in sQ23.40 format.

Bit	63	62	61	60	59	58	57	56
	Q_x_F [63:56]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	55	54	53	52	51	50	49	48
	Q_x_F [55:48]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	47	46	45	44	43	42	41	40
	Q_x_F [47:40]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	39	38	37	36	35	34	33	32
	Q_x_F [39:32]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	31	30	29	28	27	26	25	24
	Q_CH_x_F [31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	Q_x_F [23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	Q_x_F [15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	Q_x_F [7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 63:0 – Q_x_F[63:0] VAR-samples, power x (sQ23.40)

3.3.6 Accumulated Voltage Quantities Between Phases

Name: V_AB/V_BC/V_CA/V_AB_F/V_BC_F/V_CA_F
Offset: Metrology_Acc_Out[192-197]
Property: Read

The metrology module generates the following accumulated voltage to voltage (V) quantities between channels: V_AB, V_BC, V_CA, V_AB_F, V_BC_F and V_CA_F, where:

- V_A is the first (lowest index) voltage channel defined.
- V_B is the second voltage channel defined.
- V_C is the third voltage channel defined.

They are in units of [Volt^{2}samp scaled]. They are scaled accumulated voltage quantities between channels in the whole integration period. They are calculated according to the following formula:

$$V\_xy = \sum_{i=1}^{N} (V\_y\_sample_i - V\_x\_sample_i) * (V\_y\_sample_i - V\_x\_sample_i)$$

Where, $V\_x\_sample_i$ is ith sampled voltage value of channel x in present integration period; $V\_y\_sample_i$ is ith sampled voltage value of channel y in present integration period; x = [A, B, C]; y = [B, C, A]; N is the number of samples in the last measurement interval.

They are used to calculate the RMS value of voltage between channels.

V_xy and V_xy_F are stored in uQ24.40 format.

Bit	63	62	61	60	59	58	57	56
	V_xy/V_xy_F[63:56]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	55	54	53	52	51	50	49	48
	V_xy/V_xy_F[55:48]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	47	46	45	44	43	42	41	40
	V_xy/V_xy_F[47:40]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	39	38	37	36	35	34	33	32
	V_xy/V_xy_F[39:32]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	31	30	29	28	27	26	25	24
	V_xy/V_xy_F[31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	V_xy/V_xy_F[23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	V_xy/V_xy_F[15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	V_xy/V_xy_F[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 63:0 – V_xy/V_xy_F[63:0] Volt-squared-samples, Vx-Vy (uQ24.40)

3.3.7 Total Accumulated Quantities

Name: ACC_T0/ACC_T1/ACC_T2
Offset: Metrology_Acc_Out[198-200]
Property: Read

The metrology module generates the following accumulated total quantities: ACC_T0, ACC_T1 and ACC_T2.

Total accumulated quantities are specified by PCx_TYPE. They are used to save the total accumulated energy. They are updated every full line cycle (20 ms for 50 Hz and 16.667 ms for 60 Hz).

They are stored in sQ33.30 format. Max ±8589934KWh/KVarh/KAmp^{2}h can be stored in these quantities.

Before resetting the metrology firmware, the application must store present ACC_T0, ACC_T1 and ACC_T2. After resetting the metrology firmware, the application must restore ACC_T0, ACC_T1 and ACC_T2.

ACC_Tx is stored in sQ33.30 format.

Bit	63	62	61	60	59	58	57	56
	ACC_Tx[63:56]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	55	54	53	52	51	50	49	48
	ACC_Tx[55:48]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	47	46	45	44	43	42	41	40
	ACC_Tx[47:40]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	39	38	37	36	35	34	33	32
	ACC_Tx[39:32]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	31	30	29	28	27	26	25	24
	ACC_Tx[31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	ACC_Tx[23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	ACC_Tx[15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	ACC_Tx[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 63:0 – ACC_Tx[63:0] Total Accumulated Quantities Specified by PCx_TYPE (sQ33.30)

3.4 Harmonic Analysis Output Quantities

All Metrology 32-bit harmonic analysis output quantities are prefixed “Metrology_Har_Out_”. The start address is 0x20086D10. The Metrology module generates the following primary output measurement quantities for each measurement interval, per-channel quantities with each channel designated by the subscript “_x” (where x = [0, …, 31]).

Internal scaling allows accurate harmonic analysis for integration periods of up to 16 seconds for up to full-scale magnitude input waveforms.

Offset	Variable	Access Mode	Name	Format	# Bytes	Min Value	Max Value	Default	Unit
0	CH_x_m_R	R	The real part of DFT result channel x, m-th harmonics	sQ25.6	32x4	—	—	—	—
32	CH_x_m_I	R	The imaginary part of DFT result channel x, m-th harmonics	sQ25.6	32x4	—	—	—	—

3.4.1 Harmonic Analysis Output Quantities

Name: CH_x_m_R
Offset: Metrology_Har_Out[0-31]
Property: Read

The metrology module generates the following quantities to calculate appointed *m-th* order harmonic current RMS: CH_x_m_R and CH_x_m_I, where:

CH_x_m_R is the real part of DFT of channel x = [0, …, 31].

CH_x_m_I is the imaginary part of DFT of channel x = [0, …, 31].

CH_x_m_R and CH_x_m_I are stored in sQ25.6 format.

The following formula is used to calculate the RMS value of each current channel:

$$I_{RMS\_x\_m} = \frac{\sqrt{2} \times \sqrt{\left(\frac{CH\_x\_m\_R}{2^6}\right)^2 + \left(\frac{CH\_x\_m\_I}{2^6}\right)^2}}{\mathrm{N}} = \frac{\sqrt{2 \times ((CH\_x\_m\_R)^2 + (CH\_x\_m\_I)^2)}}{2^6 \times \mathrm{N}} \; [A_{rms}]$$

The following formula is used to calculate the RMS value of each voltage channel:

$$V_{RMS\_x\_m} = \frac{\sqrt{2} \times \sqrt{\left(\frac{CH\_x\_m\_R}{2^6}\right)^2 + \left(\frac{CH\_x\_m\_I}{2^6}\right)^2}}{\mathrm{N}} = \frac{\sqrt{2 \times ((CH\_x\_m\_R)^2 + (CH\_x\_m\_I)^2)}}{2^6 \times \mathrm{N}} \; [V_{rms}]$$

Note: K_CH_x factors were already applied; therefore, readings are in [Arms] or in [Vrms].

Bit	31	30	29	28	27	26	25	24
	CH_x_m_R/CH_x_m_I[31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	CH_x_m_R/CH_x_m_I[23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	CH_x_m_R/CH_x_m_I[[15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0

	CH_x_m_R[7:0] CH_x_m_I[							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 31:0 – CH_x_m_R/CH_x_m_I[31:0] Channel x, m-th harmonics (sQ25.6)

3.5 Derived Output Quantities

Using Metrology module primary output quantities, the following quantities of interest (per-channel or system) may be derived, using the following formulae.

Note: Care must be exercised when using RMS values with integrated values, depending on the length of the integration period.

3.5.1 RMS Value

Total three kinds of RMS values can be calculated directly from the output of metrology firmware: RMS value of all harmonics, RMS value of fundamental harmonic and the RMS value of *m-th* harmonic.

RMS value of all harmonics and RMS value of fundamental harmonic can be calculated as following:

$$I\_x_{rms} = \frac{K\_Ix}{2^{10}} \times \sqrt{\frac{ACC\_I\_x}{N \times 2^{40}}}$$

$$V\_x_{rms} = \frac{K\_Vx}{2^{10}} \times \sqrt{\frac{ACC\_V\_x}{N \times 2^{40}}}$$

$$I\_x_{1\,rms} = \frac{K\_Ix}{2^{10}} \times \sqrt{\frac{ACC\_I\_x\_F}{N \times 2^{40}}}$$

$$V\_x_{1\,rms} = \frac{K\_Vx}{2^{10}} \times \sqrt{\frac{ACC\_V\_x\_F}{N \times 2^{40}}}$$

Where, x = [A, B, C], and:

- *K_Ix* is the current conversion factor of channel x
- *K_Vx* is the voltage conversion factor
- I_x_{rms} is the fundamental and all harmonics current RMS value
- V_x_{rms} is the fundamental and all harmonics voltage RMS value
- I_x_{1rms} is the fundamental harmonic current RMS value
- V_x_{1rms} is the fundamental harmonic voltage RMS value
- *N* is the number of samples in the integration period
- *ACC_I_x* is the accumulated fundamental and all harmonics current quantity
- *ACC_V_x* is the accumulated fundamental and all harmonics voltage quantity
- *ACC_I_x_F* is the accumulated fundamental harmonic current quantity
- *ACC_V_x_F* is the accumulated fundamental harmonic voltage quantity

Notes:

- *K_Ix* and *K_Vx* are the register values in the metrology control registers.

- *N* is the register value in the metrology status registers.
- *ACC_I_x*, *ACC_V_x*, *ACC_I_x_F* and *ACC_V_x_F* are the register values in the metrology accumulated output quantities.

After the harmonic analysis feature is enabled, RMS value of *m-th* harmonic can be calculated:

$$I_{RMS\_x\_m} = \frac{\sqrt{2} \times \sqrt{\left(\frac{I\_x\_m\_R}{2^6}\right)^2 + \left(\frac{I\_x\_m\_I}{2^6}\right)^2}}{\mathrm{N}} = \frac{\sqrt{2 \times ((I\_x\_m\_R)^2 + (I\_x\_m\_I)^2)}}{2^6 \times \mathrm{N}} [A_{rms}]$$

$$V_{RMS\_x\_m} = \frac{\sqrt{2} \times \sqrt{\left(\frac{V\_x\_m\_R}{2^6}\right)^2 + \left(\frac{V\_x\_m\_I}{2^6}\right)^2}}{\mathrm{N}} = \frac{\sqrt{2 \times ((V\_x\_m\_R)^2 + (V\_x\_m\_I)^2)}}{2^6 \times \mathrm{N}} [V_{rms}]$$

Where, x = [0, …, 31], and:

- *I_x*$_{m\ rms}$ is the *m-th* harmonic current RMS value of channel x
- *V_x*$_{m\ rms}$ is the *m-th* harmonic voltage RMS value
- *I_x_m_R* is the real part of DFT for m-th harmonic current
- *I_x_m_I* is the imaginary part of DFT for m-th harmonic current
- *V_x_m_R* is the real part of DFT for m-th harmonic voltage
- *V_x_m_I* is the imaginary part of DFT for m-th harmonic voltage

Notes:

- I_x_m_R I_x_m_I, V_x_m_R and V_x_m_I are the register values in metrology harmonic analysis output quantities
- *m* is set in the register **FEATURE_CTRL1: HARMONIC_m_REQ[5:0]**
- The voltage/current RMS value is updated every one integration period. **INTEGRATION_IRQ** will be generated at the end of integration period; this interrupt can be used to update derived quantities.

3.5.2 THD

Due to the limit of the code size, THD is not provided directly by the metrology firmware, but you can get them by the following formulas:

$$THD_I = \frac{1}{I_1}\sqrt{\sum_{h=2}^{\infty} I_h^2} = \sqrt{\left(\frac{I_{rms}}{I_{1rms}}\right)^2 - 1}$$

$$THD_V = \frac{1}{V_1}\sqrt{\sum_{h=2}^{\infty} V_h^2} = \sqrt{\left(\frac{V_{rms}}{V_{1rms}}\right)^2 - 1}$$

Where:

- I_1 is the amplitude of fundamental harmonic current

- V_1 is the amplitude of fundamental harmonic voltage
- I_{rms} is the all harmonics current RMS value
- V_{rms} is the all harmonics voltage RMS value
- $I_{1\ rms}$ is the fundamental harmonic current RMS value
- $V_{1\ rms}$ is the fundamental harmonic voltage RMS value

3.5.3 Energy/Quadergy

Energy and quadergy over the integration period can be calculated from the metrology output registers:

$$P\_x = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{1}{3600 \times f_s} \times \frac{ACC\_P\_x}{2^{40}} [Wh]$$

$$Q\_x = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{1}{3600 \times f_s} \times \frac{ACC\_Q\_x}{2^{40}} [VARh]$$

$$P\_x_F = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{1}{3600 \times f_s} \times \frac{ACC\_P\_x\_F}{2^{40}} [Wh]$$

$$Q\_x_F = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{1}{3600 \times f_s} \times \frac{ACC\_Q\_x\_F}{2^{40}} [VARh]$$

Where x corresponds to each one of the powers defined and:

- f_s=4000Hz is the output integration sample rate
- *P_x* is active power of all harmonics of power x
- *Q_x* is reactive power of all harmonics
- *P_x*$_F$ is active power of fundamental harmonic
- *Q_x*$_F$ is reactive power of fundamental harmonic
- *ACC_P_x* is the accumulated active power quantity for all harmonics
- *ACC_Q_x* is the accumulated reactive power quantity for all harmonics
- *ACC_P_x_F* is the accumulated active power quantity for fundamental harmonic
- *ACC_Q_x_F* is the accumulated reactive power quantity for fundamental harmonic

3.5.4 Average Active and Reactive Power

Average active and reactive power over the integration period may be calculated directly from the metrology output registers for power of all harmonics and power of the fundamental harmonic:

$$P\_x\_Watts = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{ACC\_P\_x}{N \times 2^{40}} [W]$$

$$Q\_x\_VARs = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{ACC\_Q\_x}{N \times 2^{40}} [VAR]$$

$$P\_x_F\_Watts = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{ACC\_P\_x\_F}{N \times 2^{40}} [W]$$

$$Q\_x_F\_VARs = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{ACC\_Q\_x\_F}{N \times 2^{40}} [VAR]$$

Where x corresponds to each one of the powers defined and:

- *N* is the number of samples in the integration period
- *P_x_Watts* is the average active power of all harmonics of power x
- *Q_x_VARs* is the average reactive power of all harmonics
- *P_x$_F$_Watts* is the average active power of fundamental harmonic
- *Q_x$_F$_VARs* is the average reactive power of fundamental harmonic
- *ACC_P_x* is the accumulated active power quantity for all harmonics
- *ACC_Q_x* is the accumulated reactive power quantity for all harmonics
- *ACC_P_x_F* is the accumulated active power quantity for fundamental harmonic
- *ACC_Q_x_F* is the accumulated reactive power quantity for fundamental harmonic

3.5.5 Vector Power Quantities

Here are examples of some of the possible vector power quantities that may be computed:

$$U\_x = \sqrt{(P\_x)^2 + (Q\_x)^2 + (D\_x)^2}$$

$$S\_x = \sqrt{(P\_x)^2 + (Q\_x)^2}$$
$$D\_x = \sqrt{(U\_x)^2 - (S\_x)^2}$$
$$F\_x = \sqrt{(Q\_x)^2 + (D\_x)^2}$$

$$N\_x = \sqrt{(U\_x)^2 - (Q\_x)^2}$$
$$U_{aa} = \sum_{x=\{A,B,C\}} U_x$$

$$\mathrm{U_{va}} = \sqrt{\left(\sum_{\mathrm{x=\{A,B,C\}}} \mathrm{P\_x}\right)^2 + \left(\sum_{\mathrm{x=\{A,B,C\}}} \mathrm{Q\_x}\right)^2 + \left(\sum_{\mathrm{x=\{A,B,C\}}} \mathrm{D\_x}\right)^2}$$

Where x corresponds to each one of the powers defined and:

- *U_x* is apparent power of all harmonics of power x
- *S_x* is phasor power, all harmonics
- *D_x* is distortion power, all harmonics
- *F_x* is fictitious power, all harmonics
- *N_x* is nonreactive power, all harmonics
- U_{aa} is system arithmetic apparent power, all harmonics
- U_{va} is system vector apparent power, all harmonics

4 Interface between Metrology and Application

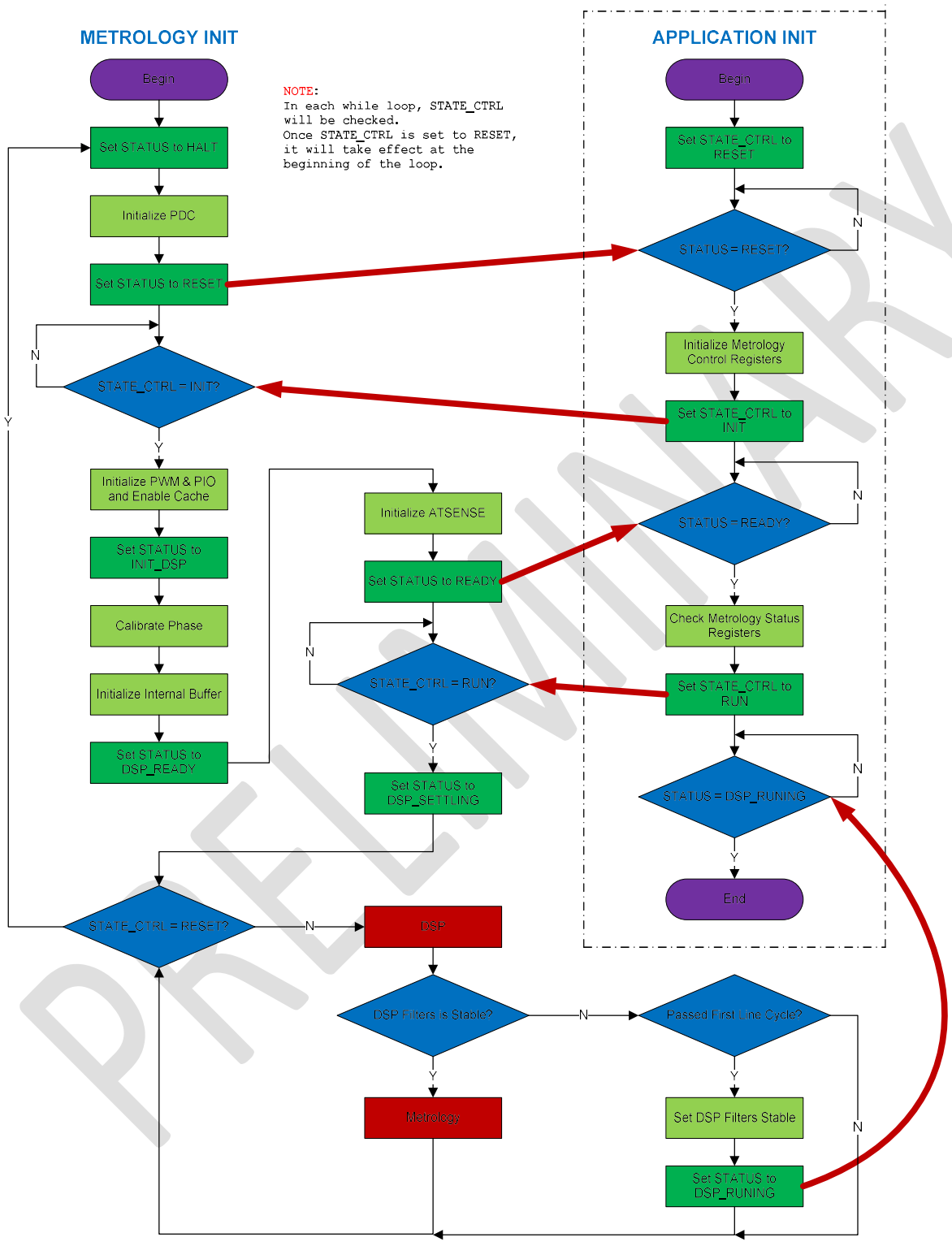
4.1 Interface in Initialization Stage

Application Initialization Sequence:

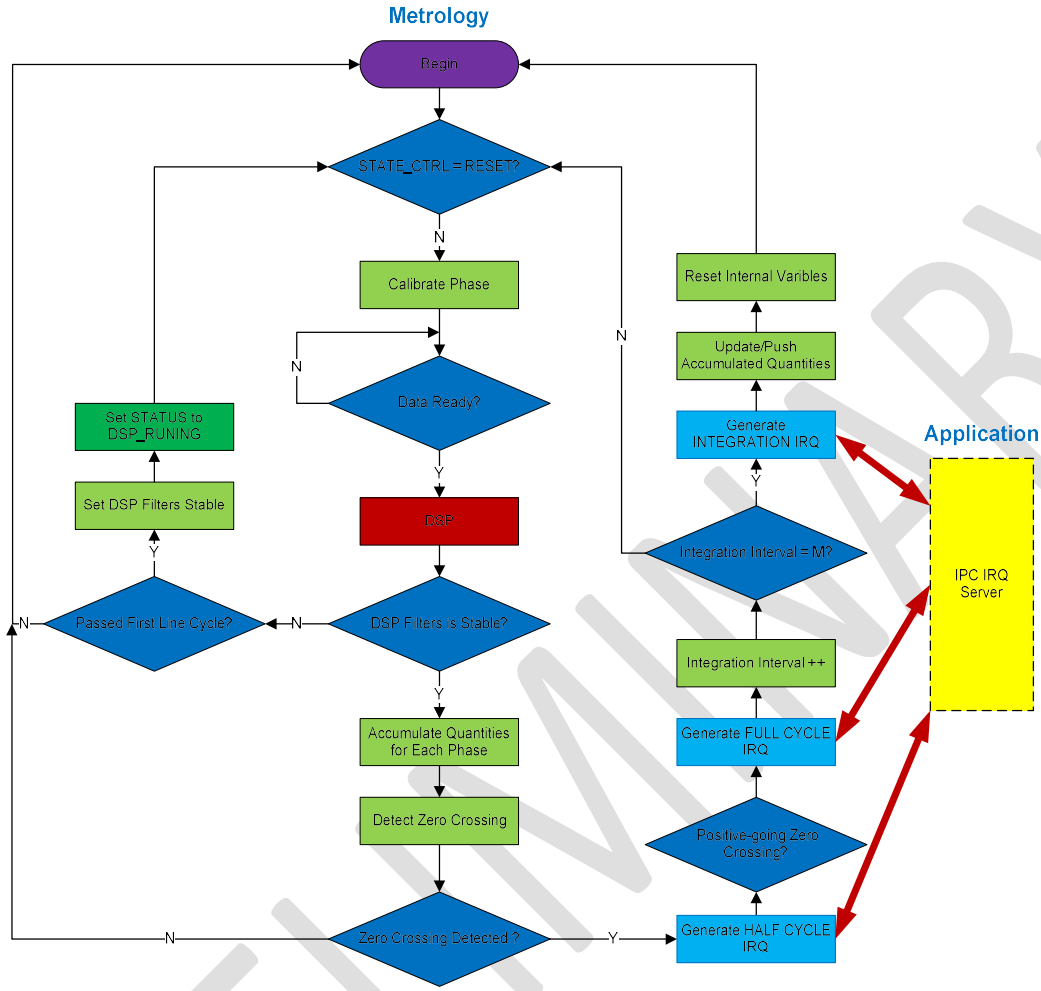
1. Change STATE_CTRL register to **RESET**.
2. Wait until Metrology STATUS changed to **RESET** or wait until the interrupt is generated: IPC_INIT_IRQ.
3. Initialize all other Metrology Control Registers.

Note: STATE_CTRL must be initialized to zero.

4. Change STATE_CTRL register to **RUN**.
5. Wait until Metrology STATUS changed to **DSP_RUNNING**.



4.2 Interrupts in Metrology Stage



The application code can disable any IPC interrupts it does not need.

When an IPC IRQ interrupt arrives, the application code first determines which kind of interrupt occurred. Then, it checks related Metrology Status Registers and executes its specific handler.

IPC interrupt is defined as the following:

31	30	29	28	27	26	25	24
—	—	—	—	—	PULSE2_IRQ	PULSE1_IRQ	PULSE0_IRQ
23	22	21	20	19	18	17	16
—	—	—	INIT_IRQ	—	—	—	STATUS_IRQ
15	14	13	12	11	10	9	8
—	—	—	RZC_IRQ	—	—	—	—
7	6	5	4	3	2	1	0
CREEP_IRQ	—	HALF_CYCLE_IRQ	FULL_CYCLE_IRQ	—	—	—	INTEGRATION_IRQ

The lib provided by Microchip can be used to set this register:

- **PULSE0_IRQ, PULSE1_IRQ, PULSE2_IRQ: Pulse Interrupts**

These interrupts are generated immediately after their respective pulse has computationally committed to be generated, but not necessarily occurred.

- **INIT_IRQ: Initialization Requirement Interrupt**

This interrupt is used to inform the application code to initialize the metrology control registers and the ACC_T0, ACC_T1 and ACC_T2 if necessary. It can work with handshake enable.

- **STATUS_IRQ: STATUS Update Interrupt**

This interrupt is used to inform the application code of change(s) in priority status bit(s). This feature is not implemented.

- **RZC_IRQ: Raw Zero Crossing Interrupt**

This interrupt is generated on zero-crossings using the unfiltered “raw” 16 KHz data stream of the selected direction and selected voltage channel.

- **CREEP_IRQ: CREEP Detection Interrupt**

This interrupt is used to inform the application code of detection of a creep condition. This feature is not implemented.

- **HALF_CYCLE_IRQ: Half Line Cycle Interrupt**

This interrupt is generated every half line cycle. It means that swell and sag flags were updated. Unlike the RZC_IRQ, the HALF_CYCLE_IRQ uses the 4 KHz narrowband filtered voltage channels and exhibit a deterministic but frequency-dependent phase delay.

- **FULL_CYCLE_IRQ: Line Cycle Interrupt**

This interrupt is generated every full line cycle. It means that the frequency and accumulated
energy associated with pulse were updated. Unlike the RZC_IRQ, the FULL_CYCLE_IRQ uses the 4 KHz narrowband filtered voltage channels and exhibits a deterministic but frequency-dependent phase delay.

- **INTEGRATION_IRQ: Integration Period Interrupt**

This interrupt is used to inform the application code that the whole integration period finishes. It means that all accumulated quantities and status N were updated.