PIC32CXMTx Metrology Reference Guide

PIC32CXMTx

Introduction

This document defines the interface of Microchip Smart Meter PIC32CXMTx Metrology firmware. It provides descriptions of the metrology control registers, metrology status registers, and the quantities that are directly computed and accessible through the metrology interface registers, as well as the relevant definitions necessary for proper coding.

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1. Definitions, Acronyms and Abbreviations

Table 1-1. Abbreviations and Acronyms

Abbreviation	Description
ADC	Analog-to-Digital Converter of the ATSENSE or MCP391x AFE, consisting of a PGA, a second order Delta-Sigma modulator, and followed by an integrated third order $sinc^3$ decimation filter. A digitized conversion of an analog voltage, V_{ADCin}, is created using the following equation: $$v_{digitized} = \frac{G_{PGA} \times V_{ADCin}}{V_{REF}}$$ For best linearity, the product of ADC input voltage and the PGA gain must not exceed 0.5V (G_{PGA} * V_{ADCin} ≤ 0.5V) for the ATSENSE AFE, or 0.6V (G_{PGA} * V_{ADCin} ≤ 0.5V) for the MCP391x AFE. G_{PGA} for all voltage channels is fixed at 1 in the case of the ATSENSE AFE.
AFE	Analog Front End
BAMS	Binary Angular Measurement System. Angles are normalized to the binary range [-1.0000, +0.9999] k, where, k may represent any convenient scale, such as 180°, or π-radians. All angles are drawn as if vectors starting to 0° (3 o'clock position) and rotating counter-clockwise for positive phase increases. Using BAMS allows for smooth rollover from ±180º to ∓180º without edge-effects.
CT	Current Transformer
Δ/Σ ADC	Delta-Sigma Analog-to-Digital Converter, an over-sampled converter with noise shaping
DSP	Digital Signal Processing
G_{PGA}	Gain selected for use in the ADC front end, G_{PGA}. In the case of the ATSENSE AFE the gain on the single-ended channels (used for measuring voltage) is fixed to 1, and in the case of the differential channels can be programmed to 1, 2, 4, or 8. In the case of the MCP391x AFE, the gain options are 1, 2, 4, 8, 16, and 32. G_{PGA} = [1, 2, 4, 8, 16, or 32]
Kh	Watt-hour meter constant for electro-mechanical meters, defines an amount of energy indicated by one (1) pulse generated by the meter and does not usually apply to solid-state meters.
Kt	Watt-hour meter test constant for solid-state meters, defines an amount of energy indicated by one (1) optical pulse generated by the meter and does not usually apply to electro-mechanical meters.
MSB	Most Significant Bit, the left-most bit of a binary number.
N	The number of samples in any one measurement interval. This number may vary for each measurement interval.
OSR	Over Sample Rate

Table 1-1. Abbreviations and Acronyms (continued)

Abbreviation	Description
Qformat	To prevent ambiguity, this document uses the following definition of Qformat numbers, being a fixed-point number format representing both integer and fractional numbers, and may be unsigned (uQm.n) or signed (sQm.n). Unsigned Qformat numbers: An (m+n)-bit unsigned number is designated uQm.n. It occupies (m+n) bits and is stored as an unsigned fixed-point binary number. An unsigned uQm.n number may represent numbers in the range: [0, $+(2^{m} - 2^{-n})$]. Signed Qformat numbers: An (m+n+1)-bit signed number is designated sQm.n. It occupies (m+n+1) bits and is stored as a signed fixed-point binary number, where the MSB is used as a sign bit. A signed sQm.n number may represent numbers in the range: [$-(2^{m})$, $+(2^{m} - 2^{-n})$]]. For example, an 8-bit sQ4.3 format number has one (1) sign bit, four (4) bits to the left of the binary point and three (3) bits to the right of the binary point and may be used to represent numbers in the range: [$-(2^{4})$, $+(2^{4} - 2^{-3})$]] = [-16, +15.875]. To convert a sQm.n format number to a decimal equivalent, divide the equivalent twos-complement binary number by 2^{n}. For example: an 8-bit signed sQ2.5 number: [0b0100 0001] = 65/(2^{5}) = 2.03125, an 8-bit [0b1100 0001] = -63/(2^{5}) = -1.96875. To convert a decimal number into a sQm.n format number, multiply by 2^{n} and convert to a signed two's-complement (m+n+1)-bit number. For example: -7.33 => sQ3.4: (-7.33)*(2^{4}) = -117 => -[0b0111 0101] => [0b1000 1011]. Example-1: sQ1.14 A signed 16-bit number, having 1 sign bit, 1 integer bit to the left of the binary point, and 14 mantissa bits to the right of the binary point that can represent numbers in the range: [-2.0, +1.999938965]. Example-2: uQ2.14 An unsigned 16-bit number, having no sign bit, 2 integer bits to the left of the binary point and 14 mantissa bits to the right of the binary point that can represent numbers in the range: [0, +3.999938965].
PGA	Programmable Gain Amplifier: Some of the channels have an internal, selectable, programmable gain amplifier that can provide an additional analog gain equal to GPGA. G_{PGA} = [1, 2, 4, 8, 16 or 32]
V_P, V_{P-M}	Voltage potential: VP is the voltage measured from node P to an implied neutral reference voltage. VP-M is the voltage measured from node P to node M, where a positive voltage is indicative of a voltage rise from node M to node P. All phase diagrams are drawn as if mathematical vectors starting at 0° (3 o'clock) and rotating counter-clockwise for positive phase increases, with 90° being at 12 o'clock, 180° at 9 o'clock and 270° at 6 o'clock.

2. Overall Description

2.1. Power Quantities Definition Perspective

The quantities available in the Metrology module make observable all basic components required to completely define or derive all power system measurement quantities for most currently used definitions of power. All per-phase voltages, currents and power for fundamental and fundamental plus harmonics are available, allowing computation of all modern system or poly-phase power quantities.

Quantities labeled as “ACC_Tx” are totals accumulated energy since power-up, they are the same with those energy calculated with pulse x.

2.2. User Characteristics

Measurement data from one measurement interval is short-lived and does not persist longer than one measurement interval. At the end of a measurement interval, the user is notified by a software interrupt. At this point, all relevant quantities must be read before the next measurement period ends.

There are two primary types of measurement intervals: the integration period, which can be configured through the N_MAX control register, and the line cycle.

Measurement data associated with the integration period includes all registers related to Accumulated Output Quantities and Harmonic Analysis Output Quantities.

Measurement data associated with the line cycle includes all registers related to Per-Cycle Accumulated Output Quantities.

2.3. Constraints

The computed quantities associated with the integration period are integrated over a time interval equivalent to an integral number of periods of the fundamental frequency. All integration periods are approximated by the final output sample rate of the DSP filters, 4000 Hz; therefore, the measurement accuracy will increase using longer integration periods. One second is the recommended minimum integration period (50 cycles of 50 Hz or 60 cycles of 60 Hz). However, fewer numbers of samples may still yield acceptable results.

DSP filters require a settling time before accurate measurements may be used for revenue-quality metering. It is recommended to wait at least 250 ms after start-up before testing to revenue-grade accuracy.

2.4. Assumptions and Dependencies

The Smart Meter DSP module is specifically designed to accept samples from an ATSENSE or MCP391x Δ/Σ ADC, at an input sample rate of 16000 kHz. This input data stream is further filtered to an internal sample rate of 4000 kHz for generation of metrology quantities. The metrology quantities associated with the integration period are available at a rate of approximately 1 Hz when using the default settings.

2.5. Supported AFEs

The metrology library supports the following AFEs, depending on the MCU in use:

- The PIC32CXMTSH supports only its internal AFE, the ATSENSE203, which provides 2 voltage and 2 current channels.
- The PIC32CXMTC supports the ATSENSE301 (offering 3 voltage and 4 current channels) as well as select devices from the MCP391x family. The specific MCP391x devices supported are listed in the description of the AFE_SELECTION register.

2.6. Signals and Phases Defined

The metrology library receives digitized samples from the connected AFE, supporting up to eight primary channels. These channels are assigned to the DSP processing channels through a configurable channel matrix. The DSP processing channels are: I_A, V_A, I_B, V_B, I_C, V_C, V_D, and measured neutral current, I_Nm.

2.7. DSP Channel and Computed Quantity Description

DSP channel nomenclature defines 4 basic voltage channels: V_A, V_B, V_C, and V_D, and 4 basic current channels: I_A, I_B, I_C, and measured neutral current, I_Nm. The channel currents are combined to create an accumulated imputed neutral current, I_Ni, and an accumulated sample-by-sample difference between the measured and imputed neutral currents, I_Nmi.

Values further labeled as '_F' indicate values associated with the fundamental frequency component only, while values without the '_F' indicate values associated with fundamental plus harmonics.

3. Metrology Interface Definition

The metrology module offers various control and status registers, as well as different types of accumulated quantities. Control registers are described in Metrology Control Registers. Status registers are described in Metrology Status Registers. Accumulated quantities are described in Accumulated Output Quantities. Accumulated per-cycle quantities are described in Per-Cycle Accumulated Output Quantities. Harmonic analysis quantities are described in Harmonic Analysis Output Quantities.

The following table provides the register block sizes and addresses implemented in this version.

Table 3-1. Register Block Sizes and Addresses

Register Block	No. of Registers	Width [bytes]	Start Address	End Address
Control Registers	84	4	0x20088000	0x2008814F
Status Registers	36	4	0x20088150	0x200881DF
Accumulator Registers	55	8	0x200881E0	0x20088397
Per-Cycle Accumulator Registers	36	8	0x20088398	0x200884B7
Harmonic Registers	434	4	0x200884B8	0x20088B7F

3.1. Metrology Control Registers

The starting address is 0x20088000.

Table 3-2. Metrology Control Registers

Index	Address	Variable	Access Mode	Name	Format	No. Bytes	Min Value	Max Value	Default	Units
0	0x20088000	STATE_CTRL	R/W	Metrology State Control register	uQ32.0	4	—	—	—	integer
1	0x20088004	FEATURE_CTRL	R/W	Metrology Feature Setting register	uQ32.0	4	—	—	—	integer
2	0x20088008	AFE_SELECTION	R/W	AFE Selection register	uQ32.0	4	—	—	—	integer
3	0x2008800C	CHANNEL_MATRIX	R/W	Physical to logical channel assignment matrix	uQ32.0	4	—	—	—	integer
4	0x20088010	HARMONIC_CTRL	R/W	Harmonic Control register	uQ32.0	4	—	—	—	integer
5	0x20088014	METER_TYPE	R/W	Sensor Type and Service Type Settings register	uQ32.0	4	—	—	—	integer
6	0x20088018	M	R/W	Number of line cycles for integration period	uQ32.0	4	0	1980	0	integer
7	0x2008801C	N_MAX	R/W	Maximum number of samples in an integration period	uQ32.0	4	—	132000	4400	integer
8	0x20088020	PULSE0_CTRL	R/W	Pulse 0 control: enable/disable, polarity, quantity type selection	uQ32.0	4	—	—	—	integer
9	0x20088024	PULSE0_K_t	R/W	Pulse 0 Meter Constant register	uQ8.24	4	—	—	0.3125	Wh/imp, VArh/imp, Amp^2h/imp, VAh/imp
10	0x20088028	PULSE1_CTRL	R/W	Pulse 1 control: enable/disable, polarity, quantity type selection	uQ32.0	4	—	—	—	integer
11	0x2008802C	PULSE1_K_t	R/W	Pulse 1 Meter Constant register	uQ8.24	4	—	—	0.3125	Wh/imp, VArh/imp, Amp^2h/imp, VAh/imp
12	0x20088030	PULSE2_CTRL	R/W	Pulse 2 control: enable/disable, polarity, quantity type selection	uQ32.0	4	—	—	—	integer
13	0x20088034	PULSE2_K_t	R/W	Pulse 2 Meter Constant register	uQ8.24	4	—	—	0.3125	Wh/imp, VArh/imp, Amp^2h/imp, VAh/imp
14	0x20088038	SYNTHESIZER_ADDR	R/W	Synthesizer Address	—	4	—	—	—	integer
15	0x2008803C	CREEP_THRESHOLD_P	R/W	Starting per-cycle total Active Energy for pulse and pulse accumulation	uQ2.30	4	—	—	—	Wh
16	0x20088040	CREEP_THRESHOLD_P_A	R/W	Starting per-cycle phase-A Active Energy. Affects accumulators (P_A, P_A_F, CYCLE_P_A, CYCLE_P_A_F) and pulse measurement	uQ12.20	4	—	—	—	mW scaled
17	0x20088044	CREEP_THRESHOLD_P_B	R/W	Starting per-cycle phase-B Active Energy. Affects accumulators (P_B, P_B_F, CYCLE_P_B, CYCLE_P_B_F) and pulse measurement.	uQ12.20	4	—	—	—	mW scaled
18	0x20088048	CREEP_THRESHOLD_P_C	R/W	Starting per-cycle phase-C Active Energy. Affects accumulators (P_C, P_C_F, CYCLE_P_C, CYCLE_P_C_F) and pulse measurement.	uQ12.20	4	—	—	—	mW scaled
19	0x2008804C	CREEP_THRESHOLD_Q	R/W	Starting per-cycle total Reactive Quadergy for pulse and pulse accumulation.	uQ2.30	4	—	—	—	VARh

Table 3-2. Metrology Control Registers (continued)

Index	Address	Variable	Access Mode	Name	Format	No. Bytes	Min Value	Max Value	Default	Units
20	0x20088050	CREEP_THRESHOLD_Q_A	R/W	Starting per-cycle phase-A Reactive Energy. Affects accumulators (Q_A, Q_A_F, CYCLE_Q_A, CYCLE_Q_A_F) and pulse measurement.	uQ12.20	4	—	—	—	mVAr scaled
21	0x20088054	CREEP_THRESHOLD_Q_B	R/W	Starting per-cycle phase-B Reactive Energy. Affects accumulators (Q_B, Q_B_F, CYCLE_Q_B, CYCLE_Q_B_F) and pulse measurement.	uQ12.20	4	—	—	—	mVAr scaled
22	0x20088058	CREEP_THRESHOLD_Q_C	R/W	Starting per-cycle phase-C Reactive Energy. Affects accumulators (Q_C, Q_C_F, CYCLE_Q_C, CYCLE_Q_C_F) and pulse measurement.	uQ12.20	4	—	—	—	mVAr scaled
23	0x2008805C	CREEP_THRESHOLD_I	R/W	Starting per-phase current for both Energy and Quadergy pulse and pulse accumulation.	uQ12.20	4	—	—	—	mArms scaled
24	0x20088060	CREEP_THRESHOLD_I_A	R/W	Starting phase-A current for both Energy and Quadergy. Affects accumulators (I_A, I_A_F, CYCLE_I_A, CYCLE_I_A_F) and pulse measurement.	uQ12.20	4	—	—	—	mArms scaled
25	0x20088064	CREEP_THRESHOLD_I_B	R/W	Starting phase-B current for both Energy and Quadergy. Affects accumulators (I_B, I_B_F, CYCLE_I_B, CYCLE_I_B_F) and pulse measurement.	uQ12.20	4	—	—	—	mArms scaled
26	0x20088068	CREEP_THRESHOLD_I_C	R/W	Starting phase-C current for both Energy and Quadergy. Affects accumulators (I_C, I_C_F, CYCLE_I_C, CYCLE_I_C_F) and pulse measurement.	uQ12.20	4	—	—	—	mArms scaled
27	0x2008806C	CREEP_THRESHOLD_S	R/W	Starting per-cycle total Apparent energy for pulse and pulse accumulation.	uQ2.30	4	—	—	—	VAh
28	0x20088070	POWER_OFFSET_CTRL	R/W	Power offset control	uQ32.0	4	—	—	—	integer
29	0x20088074	POWER_OFFSET_P	R/W	Pulse computation active power offset compensation used to eliminate voltage effects to small current (cross talk). Affects only pulse measurements.	sQ1.30	4	-2.000	1.9999...	0	Wh/cycle
30	0x20088078	POWER_OFFSET_Q	R/W	Pulse computation reactive power offset compensation used to eliminate voltage effects to small current (cross talk). Affects only pulse measurements.	sQ1.30	4	-2.000	1.9999...	0	VARh/cycle

Table 3-2. Metrology Control Registers (continued)

Index	Address	Variable	Access Mode	Name	Format	No. Bytes	Min Value	Max Value	Default	Units
31	0x2008807C	POWER_OFFSET_S	R/W	Pulse computation apparent power offset compensation used to eliminate voltage effects to small current (cross talk). Affects only pulse measurements.	sQ1.30	4	—	—	—	I^2h/cycle
32	0x20088080	SWELL_THRESHOLD_VA	R/W	Voltage swell threshold for each half cycle of phase-A voltage.	uQ0.32	4	0	0.9999...	—	—
33	0x20088084	SWELL_THRESHOLD_VB	R/W	Voltage swell threshold for each half cycle of phase-B voltage.	uQ0.32	4	0	0.9999...	—	—
34	0x20088088	SWELL_THRESHOLD_VC	R/W	Voltage swell threshold for each half cycle of phase-C voltage.	uQ0.32	4	0	0.9999...	—	—
35	0x2008808C	SAG_THRESHOLD_VA	R/W	Voltage sag threshold for each half cycle of phase-A voltage.	uQ0.32	4	0	0.9999...	—	—
36	0x20088090	SAG_THRESHOLD_VB	R/W	Voltage sag threshold for each half cycle of phase-B voltage.	uQ0.32	4	0	0.9999...	—	—
37	0x20088094	SAG_THRESHOLD_VC	R/W	Voltage sag threshold for each half cycle of phase-C voltage.	uQ0.32	4	0	0.9999...	—	—
38	0x20088098	INTERRUPT_THRESHOLD_VA	R/W	Interrupt threshold for each half cycle of phase-A voltage.	uQ0.32	4	0	0.9999...	—	—
39	0x2008809C	INTERRUPT_THRESHOLD_VB	R/W	Interrupt threshold for each half cycle of phase-B voltage.	uQ0.32	4	0	0.9999...	—	—
40	0x200880A0	INTERRUPT_THRESHOLD_VC	R/W	Interrupt threshold for each half cycle of phase-C voltage.	uQ0.32	4	0	0.9999...	—	—
41	0x200880A4	RESERVED	R/W	—	—	4	—	—	—	—
42	0x200880A8	RESERVED	R/W	—	—	4	—	—	—	—
43	0x200880AC	RESERVED	R/W	—	—	4	—	—	—	—
44	0x200880B0	K_IA	R/W	ADC input current conversion factor = I_A(rms)/Vadc(rms)	uQ22.10	4	—	2,000.00	—	$A_{RMS}/VADC_{RMS}$
45	0x200880B4	K_VA	R/W	ADC input voltage conversion factor = V_A(rms)/Vadc(rms)	uQ22.10	4	—	4,000.00	—	$V_{RMS}/VADC_{RMS}$
46	0x200880B8	K_IB	R/W	ADC input current conversion factor = I_B(rms)/Vadc(rms)	uQ22.10	4	—	2,000.00	—	$A_{RMS}/VADC_{RMS}$
47	0x200880BC	K_VB	R/W	ADC input voltage conversion factor = V_B(rms)/Vadc(rms)	uQ22.10	4	—	4,000.00	—	$V_{RMS}/VADC_{RMS}$
48	0x200880C0	K_IC	R/W	ADC input current conversion factor = I_C(rms)/Vadc(rms)	uQ22.10	4	—	2,000.00	—	$A_{RMS}/VADC_{RMS}$
49	0x200880C4	K_VC	R/W	ADC input voltage conversion factor = V_C(rms)/Vadc(rms)	uQ22.10	4	—	4,000.00	—	$V_{RMS}/VADC_{RMS}$
50	0x200880C8	K_IN	R/W	ADC input current conversion factor = I_N(rms)/Vadc(rms)	uQ22.10	4	—	2,000.00	—	$A_{RMS}/VADC_{RMS}$
51	0x200880CC	K_VD	R/W	ADC input voltage conversion factor = V_D(rms)/Vadc(rms)	uQ22.10	4	—	4,000.00	—	$V_{RMS}/VADC_{RMS}$

Table 3-2. Metrology Control Registers (continued)

Index	Address	Variable	Access Mode	Name	Format	No. Bytes	Min Value	Max Value	Default	Units
52	0x200880D0	CAL_M_IA	R/W	Current magnitude calibration constant, I_A	sQ2.29	4	-4.0000	+3.9999	+1.0000	—
53	0x200880D4	CAL_M_VA	R/W	Voltage magnitude calibration constant, V_A	sQ2.29	4	-4.0000	+3.9999	+1.0000	—
54	0x200880D8	CAL_M_IB	R/W	Current magnitude calibration constant, I_B	sQ2.29	4	-4.0000	+3.9999	+1.0000	—
55	0x200880DC	CAL_M_VB	R/W	Voltage magnitude calibration constant, V_B	sQ2.29	4	-4.0000	+3.9999	+1.0000	—
56	0x200880E0	CAL_M_IC	R/W	Current magnitude calibration constant, I_C	sQ2.29	4	-4.0000	+3.9999	+1.0000	—
57	0x200880E4	CAL_M_VC	R/W	Voltage magnitude calibration constant, V_C	sQ2.29	4	-4.0000	+3.9999	+1.0000	—
58	0x200880E8	CAL_M_IN	R/W	Current magnitude calibration constant, I_N	sQ2.29	4	-4.0000	+3.9999	+1.0000	—
59	0x200880EC	CAL_M_VD	R/W	Voltage magnitude calibration constant, V_D	sQ2.29	4	-4.0000	+3.9999	+1.0000	—
60	0x200880F0	CAL_PH_IA	R/W	Current phase calibration constant, I_A	sQ0.31	4	-1.000	+0.999	0	BAMS
61	0x200880F4	CAL_PH_VA	R/W	Voltage phase calibration constant, V_A	sQ0.31	4	-1.000	+0.999	0	BAMS
62	0x200880F8	CAL_PH_IB	R/W	Current phase calibration constant, I_B	sQ0.31	4	-1.000	+0.999	0	BAMS
63	0x200880FC	CAL_PH_VB	R/W	Voltage phase calibration constant, V_B	sQ0.31	4	-1.000	+0.999	0	BAMS
64	0x20088100	CAL_PH_IC	R/W	Current phase calibration constant, I_C	sQ0.31	4	-1.000	+0.999	0	BAMS
65	0x20088104	CAL_PH_VC	R/W	Voltage phase calibration constant, V_C	sQ0.31	4	-1.000	+0.999	0	BAMS
66	0x20088108	CAL_PH_IN	R/W	Current phase calibration constant, I_N	sQ0.31	4	-1.000	+0.999	0	BAMS
67	0x2008810C	RESERVED	—	—	—	4	—	—	—	—
68	0x20088110	CAPTURE_CTRL	R/W	Waveform capture control register	uQ32.0	4	—	—	—	integer
69	0x20088114	CAPTURE_BUFF_SIZE	R/W	Waveform capture buffer size	uQ32.0	4	1	8000000	—	integer
70	0x20088118	CAPTURE_ADDR	R/W	Waveform capture buffer address pointer	uQ32.0	4	—	—	—	pointer
71	0x2008811C	RESERVED	—	—	—	4	—	—	—	—
72	0x20088120	RESERVED	—	—	—	4	—	—	—	—
73	0x20088124	RESERVED	—	—	—	4	—	—	—	—
74	0x20088128	AFE_CTRL_0	R/W	AFE Control register 0	uQ32.0	4	—	—	—	integer
75	0x2008812C	RESERVED	—	—	—	4	—	—	—	—
76	0x20088130	RESERVED	—	—	—	4	—	—	—	—

Table 3-2. Metrology Control Registers (continued)

Index	Address	Variable	Access Mode	Name	Format	No. Bytes	Min Value	Max Value	Default	Units
77	0x20088134	RESERVED	—	—	—	4	—	—	—	—
78	0x20088138	POWER_OFFSET_P_A	R/W	Phase-A accumulation active power offset compensation used to eliminate voltage effects at small current (cross talk). Affects accumulator and pulse measurement.	sQ-9.40	4	-2.000	1.9999...	0.0	W-samp scaled
79	0x2008813C	POWER_OFFSET_P_B	R/W	Phase-B accumulation active power offset compensation used to eliminate voltage effects at small current (cross talk). Affects accumulator and pulse measurement.	sQ-9.40	4	-2.000	1.9999...	0.0	W-samp scaled
80	0x20088140	POWER_OFFSET_P_C	R/W	Phase-C accumulation active power offset compensation used to eliminate voltage effects at small current (cross talk). Affects accumulator and pulse measurement.	sQ-9.40	4	-2.000	1.9999...	0.0	W-samp scaled
81	0x20088144	POWER_OFFSET_Q_A	R/W	Phase-A accumulation reactive power offset compensation used to eliminate voltage effects at small current (cross talk). Affects accumulator and pulse measurement.	sQ-9.40	4	-2.000	1.9999...	0.0	VAR-samp scaled
82	0x20088148	POWER_OFFSET_Q_B	R/W	Phase-B accumulation reactive power offset compensation used to eliminate voltage effects at small current (cross talk). Affects accumulator and pulse measurement.	sQ-9.40	4	-2.000	1.9999...	0.0	VAR-samp scaled
83	0x2008814C	POWER_OFFSET_Q_C	R/W	Phase-C accumulation reactive power offset compensation used to eliminate voltage effects at small current (cross talk). Affects accumulator and pulse measurement.	sQ-9.40	4	-2.000	1.9999...	0.0	VAR-samp scaled

3.1.1. Metrology State Control

Name: STATE_CTRL
Property: Read-Write

State control bits input to Metrology module from application code.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					STATE_CTRL[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – STATE_CTRL[3:0] State control bits input to Metrology module from application code. Refer to the Interface in Initialization Stage for a detailed description.
Notes: Before entering in a Low-Power mode the Core 0 application should reset the metrology to disable the internal regulator of the ATSENSE. This action reduces the consumption in Low-Power mode. The Core 0 appplication should follow these steps:

1. Write a '0' in the "STATE_CTRL" control register.
2. Wait until the "STATUS" status register changes to "RESET".
3. Continue with the procedure to switch to a Low-Power mode.

Value	Name	Description
0x0	RESET	Reset metrology module, reset ATSENSE and halt metrology filters.
0x1	INIT	Input control registers are initialized and metrology can initialize itself.
0x2	RUN	Metrology filters are free to run, and outputs are updated at commanded rate.
OTHERS	RESERVED	Reserved values.

3.1.2. Metrology Feature Control Register

Name: FEATURE_CTRL
Property: Read-Write

The metrology feature control register contains the main control bits for overall metrology feature.

Note: Bits 24:30: Channel selection for harmonics computation. These bits are used for disabling the harmonics computation on specific channels.

Bit	31	30	29	28	27	26	25	24
		IN_HARM_DIS	VC_HARM_DIS	IC_HARM_DIS	VB_HARM_DIS	IB_HARM_DIS	VA_HARM_DIS	IA_HARM_DIS
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CREEP_S_EN	CREEP_P_EN	CREEP_Q_EN	CREEP_I_EN		V_MAX_RESET	I_MAX_RESET	SWAP_B_and_C
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8
	VD_DC_EN		SYNTH_EN	MAX_INT_SELECT	NEUTRAL_DIS	PHASE_C_EN	PHASE_B_EN	PHASE_A_EN
Access	R/W		R/W	R/W	R/W	RW	RW	RW
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RZC_THRESH_DIS		SYNCH[1:0]		RZC_DIR	RZC_CHAN_SELECT[2:0]		
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 30 – IN_HARM_DIS

Value	Description
0	Harmonic computation for channel IN (neutral current) is enabled.
1	Harmonic computation for channel IN (neutral current) is disabled.

Bit 29 – VC_HARM_DIS

Value	Description
0	Harmonic computation for channel VC (phase C voltage) is enabled.
1	Harmonic computation for channel VC (phase C voltage) is disabled.

Bit 28 – IC_HARM_DIS

Value	Description
0	Harmonic computation for channel IC (phase C current) is enabled.
1	Harmonic computation for channel IC (phase C current) is disabled.

Bit 27 – VB_HARM_DIS

Value	Description
0	Harmonic computation for channel VB (phase B voltage) is enabled.
1	Harmonic computation for channel VB (phase B voltage) is disabled.

Bit 26 – IB_HARM_DIS

Value	Description
0	Harmonic computation for channel IB (phase B current) is enabled.
1	Harmonic computation for channel IB (phase B current) is disabled.

Bit 25 – VA_HARM_DIS

Value	Description
0	Harmonic computation for channel VA (phase A voltage) is enabled.
1	Harmonic computation for channel VA (phase A voltage) is disabled.

Bit 24 – IA_HARM_DIS

Value	Description
0	Harmonic computation for channel IA (phase A current) is enabled.
1	Harmonic computation for channel IA (phase A current) is disabled.

Bit 23 – CREEP_S_EN Apparent Power Creep Threshold Feature Enable

Used to enable/disable metrology creep function of apparent power pulse generation and any associated ACC_Tx total energy pulse value accumulators. Refer to the CREEP_THRESHOLD_S for additional information.

Value	Name	Description
0	DISABLED	Disable apparent power creep threshold feature.
1	ENABLED	Enable apparent power creep threshold feature.

Bit 22 – CREEP_P_EN Active Power Creep Threshold Feature Enable

Used to enable/disable metrology creep function of active power. It affects to both the total creep and the per-phase creeps. Refer to the CREEP_THRESHOLD_P, CREEP_THRESHOLD_P_A, CREEP_THRESHOLD_P_B, and CREEP_THRESHOLD_P_C for additional information.

Value	Name	Description
0	DISABLED	Disable active power creep threshold feature.
1	ENABLED	Enable active power creep threshold feature.

Bit 21 – CREEP_Q_EN Reactive Power Creep Threshold Feature Enable

Used to enable/disable metrology creep function of reactive power. It affects to both the total creep and the per-phase creeps. Refer to the CREEP_THRESHOLD_Q, CREEP_THRESHOLD_Q_A, CREEP_THRESHOLD_Q_B, and CREEP_THRESHOLD_Q_C for additional information.

Value	Name	Description
0	DISABLED	Disable reactive power creep threshold feature.
1	ENABLED	Enable reactive power creep threshold feature.

Bit 20 – CREEP_I_EN Current Creep Threshold Feature Enable

Used to enable/disable metrology creep function of metrology. It affects to both the total creep and the per-phase creeps. Current creep thresholding is used to kill pulse contribution from any or all phases below the current threshold and affects all enabled [P, Q, and I^2] pulsing in the case of the global creep and also to the accumulators in the case of the individual creeps. Refer to the CREEP_THRESHOLD_I, CREEP_THRESHOLD_I_A, CREEP_THRESHOLD_I_B, and CREEP_THRESHOLD_I_C for additional information.

Value	Name	Description
0	DISABLED	Disable current creep threshold feature.
1	ENABLED	Enable current creep threshold feature.

Bit 18 – V_MAX_RESET Reset All V_x_MAX values in Metrology Status Registers
This bit will be cleared by the metrology firmware automatically.

Value	Description
1	Reset all V_x_MAX values in Metrology Status Registers.

Bit 17 – I_MAX_RESET Reset All I_x_MAX values in Metrology Status Registers
This bit will be cleared by the metrology firmware automatically.

Value	Description
1	Reset all I_x_MAX values in Metrology Status Registers.

Bit 16 – SWAP_B_and_C Swap I2/V2 to DSP processing channels I_V/V_C and vice versa
Applies for polyphase processing. Allows Δ-Y transformation when using 2-element ATSENSE203 metering.
If enabled, channel swap is performed before DSP channel calibration factors are applied.

Value	Description
0	DSP input mapping: I2/V2 mapped I_B/V_B; I3/V3 mapped I_C/V_C (default).
1	DSP input mapping: I2/V2 mapped I_C/V_C; I3/V3 mapped I_B/V_B.

Bit 15 – VD_DC_EN Enabled DC measurements in VD

Value	Description
0	DC measurements disabled (default).
1	DC measurements enabled. The DC block filter is not executed.

Bit 13 – SYNTH_EN Synthesizer enabled

Value	Description
0	Synthesizer disabled (default).
1	Synthesizer enabled. The samples coming from the AFE are replaced with synthesized ones.

Bit 12 – MAX_INT_SELECT Max Integration Period Select
Only applies if control word M = 0 (M = Number of cycles for integration period) and affects rounding when determining number of cycles closest to 1 sec.

Value	Description
0	Metrology DSP will integrate for an integral number of cycles closest to 1 second. Due to line frequency drift, the integration period may be slightly longer or shorter than 1 sec, bounded approximately by [0.99, 1.01] sec.
1	Metrology DSP will integrate for an integral number of cycles no greater than 1 second. Due to line frequency drift, the integration period will always be ≤ 1 sec, bounded by approximately by [0.98, 1.00] sec.

Bit 11 – NEUTRAL_DIS Disable neutral measurement
Only applies when the neutral current and the temperature measurements are shared in the same channel, such as in the PIC32CXMTC with external ATSENSE301.

Value	Description
0	Neutral measurement is disabled, and the shared channel is continuously acquiring temperature readings.
1	Neutral and temperature measurements are acquired using the shared channel.

Bits 8, 9, 10 – PHASE_x_EN Enable Phase x (x = A, B or C)
Selects phases used for pulse computation. At least one phase must be enabled for pulsing to function. For typical usage, enable all phases used for pulsing. This feature may be used to temporarily disable or exclude phases from pulse computation.

Value	Name	Description
0	DISABLED	Disable phase
1	ENABLED	Enable phase

Bit 7 – RZC_THRESH_DIS Raw Zero-Crossing Threshold Disable

Selects the raw Zero-Crossing detection algorithm threshold.

Value	Description
0	Threshold set to the average value computed in the last integration period.
1	Threshold set to 0.

Bits 5:4 – SYNCH[1:0] Dominant Voltage Channel Selection

The energy integration period is determined by counting zero-crossings of a narrow-band filtered version of the dominant voltage phase. SYNCH is used to allow the metrology module to dynamically determine which voltage phase is the dominant voltage phase or to statically choose one particular phase for zero-crossing counting. In all cases of active phase cycle counting, measurement quantities are integrated over M-number of (negative-to-positive) zero-crossings. It is recommend that the sync phase is appointed, especially for a single phase application.

Value	Description
0x0	Measurement interval based on dominant phase, determined dynamically.
0x1	Measurement interval based on phase-A.
0x2	Measurement interval based on phase-B.
0x3	Measurement interval based on phase-C.

Bit 3 – RZC_DIR Raw Zero-Crossing Direction Selection

Raw Zero-Crossing Direction selects either positive-going or negative-going raw zero-crossings trigger the IPC interrupt: IPC_RAW_ZERO_CROSSING.

Value	Name	Description
0	POSITIVE	Positive-going raw zero-crossings selected.
1	NEGATIVE	Negative-going raw zero-crossings selected.

Bits 2:0 – RZC_CHAN_SELECT[2:0] Raw Zero-Crossing Channel Select and Enable

Raw Zero-Crossing allows detection of zero-crossings using the raw 16 kHz input voltage channel samples. Unlike the zero-crossing detection used for timing decisions that use a 4 kHz fundamental only filtered data stream, the Raw Zero-Crossing detection feature has no frequency-dependent group delay nor any appreciable bulk filter delay.

Value	Description
0x0	Raw Zero-Crossing detection is disabled.
0x1	Raw Zero-Crossing detection based on input voltage channel V1.
0x3	Raw Zero-Crossing detection based on input voltage channel V2.
0x5	Raw Zero-Crossing detection based on input voltage channel V3.

3.1.3. AFE Selection

Name: AFE_SELECTION
Property: Read-Write

The AFE_SELECTION register enables users to configure the AFE connected to the PIC32CXMTC host microcontroller. For the PIC32CXMTSH device, however, the value of this register is overridden, as it exclusively supports connection to its internal AFE.

When this register is modified, the metrology library must be reset for the changes to take effect.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					AFE_SELECTION[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – AFE_SELECTION[3:0]

Value	Description
0	1xATSENSE301. 7 channels (3 voltages and 4 currents). Poly-phase meter with neutral current measurement.
1	3xMCP3910. Typically used for 3 phase shunt meters.
2	4xMCP3910. Typically used for 3 phase shunt meters with neutral current measurement. The channel 8th provides an extra ADC conversion.
3	1xMCP3912. 4 channels (2 voltages and 2 currents). Single and bi-phase meters.
4	1xMCP3913. 6 channels (3 voltages and 3 currents). Poly-phase meter.
5	1xMCP3914. 8 channels (4 voltages and 4 currents). Poly-phase meter with neutral current measurement. The channel 8th provides an extra ADC conversion.
6-15	Reserved for future uses.

3.1.4. Channel Matrix Register

Name: CHANNEL_MATRIX
Property: Read-Write

The CHANNEL_MATRIX register allows the users to map physical channels to logical channels. The number of available physical channels is defined by the AFE, which is determined in the AFE_SELECTION register except for the PIC32CXMTSH. Some AFEs offer a combination of single-ended and differential channels. For optimal performance when measuring low-level signals, it is recommended to use differential channels for current measurements.

The table below outlines how the physical channels (CHANNEL_x) are mapped to the supported configurations of the AFEs.

Configuration	Physical Channels							
	CHANNEL_0	**CHANNEL_1**	**CHANNEL_2**	**CHANNEL_3**	**CHANNEL_4**	**CHANNEL_5**	**CHANNEL_6**	**CHANNEL_7**
1xATSENSE301	IP0/IN0[1]	IP1/IN1	VP1/VN	IP2/IN2	VP2/VN	IP3/IN3	VP3/VN	N/A
3xMCP3910	CH0+/CH0- (in MCP3910 connected to CS0 of PIC32CXMTC)	CH1+/CH1- (in MCP3910 connected to CS0 of PIC32CXMTC)	CH0+/CH0- (in MCP3910 connected to CS1 of PIC32CXMTC)	CH1+/CH1- (in MCP3910 connected to CS1 of PIC32CXMTC)	CH0+/CH0- (in MCP3910 connected to CS2 of PIC32CXMTC)	CH1+/CH1- (in MCP3910 connected to CS2 of PIC32CXMTC)	N/A	N/A
4xMCP3910	CH0+/CH0- (in MCP3910 connected to CS0 of PIC32CXMTC)	CH1+/CH1- (in MCP3910 connected to CS0 of PIC32CXMTC)	CH0+/CH0- (in MCP3910 connected to CS1 of PIC32CXMTC)	CH1+/CH1- (in MCP3910 connected to CS1 of PIC32CXMTC)	CH0+/CH0- (in MCP3910 connected to CS2 of PIC32CXMTC)	CH1+/CH1- (in MCP3910 connected to CS2 of PIC32CXMTC)	CH0+/CH0- (in MCP3910 connected to CS3 of PIC32CXMTC)	CH1+/CH1- (in MCP3910 connected to CS3 of PIC32CXMTC)
1xMCP3912	CH0+/CH0-	CH1+/CH1-	CH2+/CH2-	CH3+/CH3-	N/A	N/A	N/A	N/A
1xMCP3913	CH0+/CH0-	CH1+/CH1-	CH2+/CH2-	CH3+/CH3-	CH4+/CH4-	CH5+/CH5-	N/A	N/A
1xMCP3914	CH0+/CH0-	CH1+/CH1-	CH2+/CH2-	CH3+/CH3-	CH4+/CH4-	CH5+/CH5-	CH6+/CH6-	CH7+/CH7-
PIC32CXMTSH	IP1/IN1	VP1/VN	IP2/IN2	VP2/VN	N/A	N/A	N/A	N/A

Note:

1. This channel is multiplexed with the internal temperature sensor of the ATSENSE301.

The logical channels defined by the metrology library are as follows:

- I_A, I_B, I_C: Currents for phases A, B, and C
- I_N: Neutral current
- V_A, V_B, V_C: Voltages for phases A, B, and C
- V_D (available only when using an MCP3914 AFE): It provides an additional ADC conversion for the application. The metrology library processes this channel with all metrology filters except for phase correction. This includes the calibration gain and the DC block filter, in case VC_DC_EN is cleared.

Bit	31	30	29	28	27	26	25	24
	CHANNEL_7[3:0]				CHANNEL_6[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CHANNEL_5[3:0]				CHANNEL_4[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CHANNEL_3[3:0]				CHANNEL_2[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CHANNEL_1[3:0]				CHANNEL_0[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:28 – CHANNEL_7[3:0] Physical channel 7 mapping

Value	Description
0	Physical channel mapped to logical channel I_A
1	Physical channel mapped to logical channel V_A
2	Physical channel mapped to logical channel I_B
3	Physical channel mapped to logical channel V_B
4	Physical channel mapped to logical channel I_C
5	Physical channel mapped to logical channel V_C
6	Physical channel mapped to logical channel I_N
7	Physical channel mapped to logical channel V_D
8-14	Reserved for future uses
15	Not used

Bits 27:24 – CHANNEL_6[3:0] Physical channel 6 mapping
For the mapping information, see the previous table in CHANNEL_7.

Bits 23:20 – CHANNEL_5[3:0] Physical channel 5 mapping
For the mapping information, see the previous table in CHANNEL_7.

Bits 19:16 – CHANNEL_4[3:0] Physical channel 4 mapping
For the mapping information, see the previous table in CHANNEL_7.

Bits 15:12 – CHANNEL_3[3:0] Physical channel 3 mapping
For the mapping information, see the previous table in CHANNEL_7.

Bits 11:8 – CHANNEL_2[3:0] Physical channel 2 mapping
For the mapping information, see the previous table in CHANNEL_7.

Bits 7:4 – CHANNEL_1[3:0] Physical channel 1 mapping
For the mapping information, see the previous table in CHANNEL_7.

Bits 3:0 – CHANNEL_0[3:0] Physical channel 0 mapping
For the mapping information, see the previous table in CHANNEL_7.

3.1.5. Harmonic Control Register

Name: HARMONIC_CONTROL
Property: Read-Write

The metrology feature control register contains the main control bits for the overall metrology feature.

Bit	31	30	29	28	27	26	25	24
	HARMONIC_EN	HARMONIC_m_REQ[30:24]						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	HARMONIC_m_REQ[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	HARMONIC_m_REQ[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	HARMONIC_m_REQ[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – HARMONIC_EN Enable Harmonic Analysis

Value	Name	Description
0	DISABLED	Disable harmonic analysis
1	ENABLED	Enable harmonic analysis

Bits 30:0 – HARMONIC_m_REQ[30:0] Request number of harmonic for analysis
Harmonic analysis will be computed for the selected harmonic orders specified in this field. The analysis will produce accurate results when a whole integration period is elapsed. Consequently, the application must discard the results generated in the integration period when the analysis was enabled or the harmonic selection changed.

⚠ WARNING Although the control register can enable up to 31 harmonic orders, the frequency response may be limited by the metrology filters or the input network anti-aliasing filters. With respect to the metrology filters, the accuracy is better than 0.007% up to 1386 Hz, ensuring an extremely accurate response up to the 21st harmonic order (considering a fundamental frequency of 60 Hz, with a 10% deviation). However, the response remains relatively flat up to 1650 Hz, with an error margin of up to 0.05%.

3.1.6. Meter Type Settings Register

Name: METER_TYPE
Property: Read-Write

This register defines the service type settings and type of meter voltage and current sensors.

Bit	31	30	29	28	27	26	25	24
	Dto4WY_TRANSFORM		MISSING_PHASE[1:0]		SERVICE_TYPE[3:0]			
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
			SENSOR_TYPE_I_N[1:0]		SENSOR_TYPE_V_C[1:0]		SENSOR_TYPE_I_C[1:0]	
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SENSOR_TYPE_V_B[1:0]		SENSOR_TYPE_I_B[1:0]		SENSOR_TYPE_V_A[1:0]		SENSOR_TYPE_I_A[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – Dto4WY_TRANSFORM
For use with: 4-Wire and 3-Wire DELTA meters only. Phase voltages (and currents, where applicable) are transformed into an equivalent 4-wire Wye service for metering using alternate equations.

Value	Name	Description
0x0	DISABLED	Phase voltages remain in native service (no transformation).
0x1	ENABLED	Phase voltages transformed into an equivalent 4-wire Wye service. Transformation may lose accuracy in non-Blondel/unbalanced situations. Meter vector transformation is useful in some applications and possible, transforming 3-Phase Delta meters into an equivalent 3-Phase 4WY. However, it is useful only for balanced voltage situations.

Bits 29:28 – MISSING_PHASE[1:0] Missing phase voltage select
For use with Poly-phase 4-wire Wye 2-1/2 element meters only.

Value	Description
0x0	Generate missing phase voltage for Phase_A: V_A = -(V_B + V_C).
0x1	Generate missing phase voltage for Phase_B: V_B = -(V_A + V_C).
0x2	Generate missing phase voltage for Phase_C: V_C = -(V_A + V_B).

Bits 27:24 – SERVICE_TYPE[3:0] Electrical Service Type
The service type determines what meter form is being implemented and how the Metrology DSP core interprets and processes the ADC values. Refer to the Annex – Meter Forms for additional information.

Value	Name	Description
0x0	3P4WY_3E_3V3I	Three-phase 4-wire Wye (3-element)
0x1	3P4WD_3E_3V3I	Three-phase 4-wire Delta (3-element).
0x2	3P3P4WY_2p5E_2V3I	Three-phase 4-wire Wye (2-½ element)

Value	Name	Description
0x3	3P4WD_2E_3V2I	Three-phase 4-wire Delta (2-element)
0x4	3P3WD_2E_2V2I	Three-phase 3-wire) Delta (2-element)
0x5	2P3W_2E_2V2I	Two-phase 3-wire Network (2 element)
0x6	1P3W_1p5E_1V2I	Single-phase 3-wire (1-½ element)
0x7	1P2W_1E_1V1I	Single-phase 2-wire (1 element)
0x8	1P3W_1E_2V1I	Single-phase 3-wire (1 element)

Bits 13:12 – SENSOR_TYPE_I_N[1:0] Current Sensor Type on N Phase
Selects the types of current and voltage sensor used. Read the following table for additional information.

Bits 11:10 – SENSOR_TYPE_V_C[1:0] Voltage Sensor Type on C Phase
Selects the types of current and voltage sensor used. For each channel selected as using a Rogowski sensor, the Metrology DSP implements a digital integrator filter to normalize the effects of the sensor's di/dt behavior.

Value	Name	Description
0x0	CURRENT TRANSFORMER	—
0x1	RESISTIVE SHUNT	May only be used with phase-to-neutral voltage measurement applications.
0x2	ROGOWSKI COIL (CRC) CURRENT SENSOR	A digital integrator function is added to the DSP of all current channels selected as using Rogowski Coils. When SENSOR_TYPE_I_x = 2, an additional phase correction is internally added to each channel with a Rogowski sensor in the amount of -0.3704° (@ 60 Hz) to correct for a linear phase response introduced by the digital integrator filter. This is taken into account during the internal calculation of actual phase-correction filter coefficients, when a new set of phase calibration settings are loaded, and must not be added by the user in the phase-correction entries. When SENSOR_TYPE_I_x is set to other values, it takes no effect.
0x3	RESISTIVE DIVIDER (VRD) VOLTAGE SENSOR	Normally, this is the typical option selected for voltage sensors.

Bits 9:8 – SENSOR_TYPE_I_C[1:0] Current Sensor Type on C Phase
Selects the types of current and voltage sensor used. Read the previous table for additional information.

Bits 7:6 – SENSOR_TYPE_V_B[1:0] Voltage Sensor Type on B Phase
Selects the types of current and voltage sensor used. Read the previous table for additional information.

Bits 5:4 – SENSOR_TYPE_I_B[1:0] Current Sensor Type on B Phase
Selects the types of current and voltage sensor used. Read the previous table for additional information.

Bits 3:2 – SENSOR_TYPE_V_A[1:0] Voltage Sensor Type on A Phase
Selects the types of current and voltage sensor used. Read the previous table for additional information.

Bits 1:0 – SENSOR_TYPE_I_A[1:0] Current Sensor Type on A Phase
Selects the types of current and voltage sensor used. Read the previous table for additional information.

3.1.7. Number of Line Cycles for Integration Period

Name: M
Property: Read-Write

The measurement time unit, t_M, or integration period, is delineated by M-number of negative-to-positive zero-crossings of the fundamental frequency using a selected voltage signal. All primary output quantities are computed for this many number of cycles of the fundamental frequency.

M is the number of cycles of the integration period are provided as input into the metrology module.

Note: After changing this register, verify the value of the N_MAX register.

Note: If the phase voltage for frequency determination is not present, defined as ≥ 1/32 of max range, then the metrology module transitions to a default integration period of "N_MAX" samples. If phase voltage loss occurs before the expected number, then that specific integration period may end with some intermediate number of samples. In all cases, the number of samples used in an integration period is available in the output Register N, at the end of an integration period.

Presently, fixed-precision accumulation is scaled for a maximum integration period of 30 seconds (given max V and I inputs). This has to be changed if a one-minute integration period is desired.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					M[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	M[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – M[11:0] (uQ12.0)

Value	Description
0	Number of cycles for the measurement period will be determined automatically as the number of cycles closest to 1.0 second of integration time. The number of cycles is variable and the measurement period, t_M, will closely track 1.0 sec of measurement time, regardless of line frequency.
Other	Number of cycles is fixed and the measurement period, t_M, will vary with line frequency.

3.1.8. Max Number of Samples in an Integration Period

Name: N_MAX
Property: Read-Write

The maximum number of samples in a measurement time period must be defined, in case of loss of dominant voltage phase detection and zero-crossing cycle synchronization. "N_MAX" and "M" must be chosen in such a way that "N_MAX" is large enough to consider the expected number samples in the number of line cycles for the integration period.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	N_MAX[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	N_MAX[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	N_MAX[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – N_MAX[23:0] (uQ24.0)

3.1.9. Pulse Control Register x (x = 0, 1, 2)

Name: PULSEx_CTRL
Property: Read-Write

Three pulses can be generated simultaneously: PULSE0_CTRL is used to control the pulse output from PD17, PULSE1_CTRL is used to control the pulse output from PD18, and PULSE2_CTRL is used to control the pulse output from PD19. IPC interrupts are triggered at each pulse: IPC_PULSEx.

Bit	31	30	29	28	27	26	25	24
	PCx_ENABLE		PCx_DETENT[1:0]			PCx_ACC_HOLD	PCx_OVERRIDE	PCx_POLARITY
Access	R/W		R/W	R/W		R/W	R/W	R/W
Reset	0		0	0		0	0	0

Bit	23	22	21	20	19	18	17	16
					PCx_TYPE[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PCx_WIDTH[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PCx_WIDTH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – PCx_ENABLE Output Pulse Enable
Used to enable or disable pulse functionality. For short-term disable of pulses, use the PC_OVERRIDE control bit.

Value	Description
0x0	Pulse output disabled, inactive level determined by PULSE_POLARITY
0x1	Pulse output enabled

Bits 29:28 – PCx_DETENT[1:0] Total Absolute Values for P and Q values
When creating P and Q accumulator totals of multiple phases, this option allows taking the absolute values of each phase before adding to make the total. This is used to primarily ignore direction of energy delivered or generated for pulse generation.

Value	Name	Description
0x0	NET	Pulses generated based on (energy delivered – energy generated): Individual sign of each channel's P and Q is taken into account when creating total P and Q accumulator sums.
0x1	ABSOLUTE	Pulses generated based on (energy delivered + energy generated): The absolute value of each phase's P and Q is used when creating the total P and Q accumulator sums.
0x2	DELIVERED	Pulses generated based on (delivered only): Only positive values (energy delivered) of each phase's P and Q are used when creating the total P and Q accumulator sums, with negative values (energy generated) being ignored.
0x3	GENERATED	Pulses generated based on (generated only): Only negative values (energy generated) of each phase's P and Q are used when creating the total P and Q accumulator sums, with positive values (energy delivered) being ignored.

Bit 26 – PCx_ACC_HOLD Pulse Accumulation Hold Control

Value	Description
0x0	Pulse accumulation registers continue to increment even if pulse generation is temporarily disabled.
0x1	Pulse accumulation is held static. All incremental quantities normally used for pulse determination are discarded.

Bit 25 – PCx_OVERRIDE Pulse Override Control

Use to temporarily disable pulse generation. While disabled, pulse accumulation functions as selected with the PC_ACC_HOLD control bit.

Value	Description
0x0	Pulse generation functions as normal
0x1	Pulse generation is temporarily disabled

Bit 24 – PCx_POLARITY Pulse Polarity

Value	Description
0x0	Output pulse is low with width set by K_WIDTH, followed by an inactive level of high
0x1	Output pulse is high with width set by K_WIDTH, followed by an inactive level of low

Bits 19:16 – PCx_TYPE[3:0] Pulse Type Selection

Value	Name	Description
0x0	P_T	Watt-hours, total all phases, fundamental + harmonics.
0x1	P_T_F	Watt-hours, total all phases, fundamental only.
0x2	Q_T	Var-hours, total all phases, fundamental + harmonics.
0x3	Q_T_F	Var-hours, total all phases, fundamental only.
0x4	I_T	Amp-squared-hours, total all phases, fundamental + harmonics.
0x5	I_T_F	Amp-squared-hours, total all phases, fundamental only.
0x6	S_T	VA-hours, total all phases, fundamental + harmonics. It is computed by multiplying Irms by Vrms.
0x7	S_T_F	VA-hours, total all phases, fundamental only. It is computed by multiplying Irms (fundamental) by Vrms (fundamental).
0x8	S2_T	VA-hours, total all phases. It is computed as the square root of (P^2+Q^2).
0x9-0xF	Reserved	—

Bits 15:0 – PCx_WIDTH[15:0] Pulse Width

The granularity for pulse width is in units of 2.1552 µs, corresponding to a clock rate of 464 kHz. The peripheral clock was incremented to 7.424 MHz in version 3.1.00. However, the granularity of the pulse width does not change to assure compatibility with previous versions.

PCx_WIDTH = PULSE_WIDTH[sec] x 464000

For example, for a desired pulse width of 750 µs, the computation for the value PCx_WIDTH will be:

$$PCx\_WIDTH = 750 \times 10^{-6} \times 464000 = 348 = 0x015C$$

There is a limitation on the maximum frequency of pulse occurrence. The pulse width plus 500 microseconds cannot exceed the pulse period duration.

For example, if the pulse width is set at 500 microseconds, the maximum pulse frequency that can be attained is 1 kHz. On the other hand, if the pulse width is reduced to 50 microseconds, the pulse frequency can increase to a maximum of 1.818 kHz.

3.1.10. Pulse Meter Constant Register x (x = 0, 1, 2)

Name: PULSEx_K_t
Property: Read-Write

The PULSE0_K_t, PULSE1_K_t, and PULSE2_K_t registers define the meter test constants for pulses: 0, 1, and 2. The meter constant represents the amount of energy signified by a single output pulse. The type of energy is specified in the PCx_TYPE field of the corresponding PULSEx_CTRL register.

The PULSEx_K_t register is expressed in the following units, depending on the energy type:

- [Wh/pulse] for active energy
- [VARh/pulse] for reactive energy
- [VAh/pulse] for apparent energy
- [Amp^2-h/pulse] for Amp^2

All values are represented in uQ8.24 format.

In Europe and Asia, the pulse constant (MC) is commonly used with units, such as [pulses/kWh], [pulses/kVARh], [pulses/kVAh], or [pulses/kAmp^2-h]. To compute the value to be written in the pulse meter constant register for an specific MC, divide 1000 by the MC and then convert the result into uQ8.24 format by multiplying by 2^{24}. For example:

- Active power: MC = 800 pulses/kWh
  1000/800 = 1.25 Wh/pulse
  Value to program in PULSEx_K_t: round (1.25 * 2^{24}) = 20,971,520 (0x01400000)
- Reactive power: MC = 1000 pulses/kVARh
  1000/1000 = 1 VARh/pulse
  Value to program in PULSEx_K_t: round (1 * 2^{24}) = 16,777,216 (0x01000000)
- Amp squared: MC = 3200 pulses/kAmp^2-h
  1000 / 3200 = 0.3125 Amp^2-h/pulse
  Value to program in PULSEx_K_t: round (0.3125 * 2^{24}) = 5,242,880 (0x00500000)
- Apparent power: MC = 800 pulses/kVAh
  1000 / 800 = 1.25 VAh/pulse
  Value to program in PULSEx_K_t: round (1.25 * 2^{24}) = 20,971,520 (0x01400000)

The frequency of pulse output generated depends on the quantity of energy measured and the defined pulse constants.

Important: There is a limitation on the maximum frequency of pulse occurrence. The pulse width plus 500 microseconds cannot exceed the pulse period duration.

For example, if the pulse width is set at 500 microseconds, the maximum pulse frequency that can be attained is 1 kHz. On the other hand, if the pulse width is reduced to 50 microseconds, the pulse frequency can increase to a maximum of 1.818 kHz.

Updates to PULSEx_K_t take effect at the next negative zero-crossing (narrow-band filtered version) of the present control phase voltage channel.

Bit	31	30	29	28	27	26	25	24
	Pulsex_K_t[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	Pulsex_K_t[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	Pulsex_K_t[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	Pulsex_K_t[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – Pulsex_K_t[31:0] (uQ8.24)

3.1.11. Synthesizer Address

Name: SYNTHESIZER_ADDR
Property: Read-Write

This register allows the user to provide samples to the metrology library, replacing the samples typically received from the ADCs. The register holds a 32-bit address that must point to a descriptor with the following structure.

```
typedef struct {
    DRV_METROLOGY_SYN_CONTROL control;
    uint32_t *pData;
    void *next;
} DRV_METROLOGY_SYN_DESCRIPTOR;
```

Where,

- The `pData` field is a pointer to a table containing the samples.
- The `next` field is a pointer to the next descriptor. If `next` is set to 0 (NULL), there are no additional descriptors.
- The `control` field is a 32-bit value with the following structure.

  ```
  typedef struct
  {
      unsigned int numSamples : 19;
      unsigned int channel : 5;
      unsigned int key : 8;
  } DRV_METROLOGY_SYN_CONTROL;
  ```

  Where,
  - `numSamples` is the number of samples in the table
  - `channel` indicates the physical channel associated with the samples
  - `key` is a security field that must be set to 0x5A

Bits	Name	Description
0-18	`numSamples`	Number of samples in the table
19-23	`channel`	Physical channel number
24-31	`key`	Must be set to 0x5A

Descriptors are processed once the synthesizer is enabled (bit 13 of FEATURE_CTRL). To modify the descriptors, first disable the synthesizer, make the necessary changes, and then re-enable the synthesizer.

Bit	31	30	29	28	27	26	25	24
	SYNTHESIZER_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SYNTHESIZER_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SYNTHESIZER_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SYNTHESIZER_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SYNTHESIZER_ADDR[31:0]

3.1.12. Creep Threshold for Active Energy

Name: CREEP_THRESHOLD_P
Property: Read-Write

Total active energy pulse quantities in any one line cycle interval less than the creep threshold are reset to zero and are not accumulated.

CREEP_THRESHOLD_P is the creep active energy (Watt-hour) in a full cycle (20 ms for 50 Hz, 16.667 ms for 60 Hz).

CREEP_THRESHOLD_P is stored in uQ2.30 format.

If the creep active power is set to 11 Watt, and the system frequency is 60 Hz, then CREEP_THRESHOLD_P = round [11 / (60 * 3600) * 2^{30}] = 54681 = 0x0000D599

Bit	31	30	29	28	27	26	25	24
	CREEP_THRESHOLD_P[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CREEP_THRESHOLD_P[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CREEP_THRESHOLD_P[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CREEP_THRESHOLD_P[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CREEP_THRESHOLD_P[31:0] (uQ2.30)

3.1.13. Per-Phase Creep Threshold for Active Energy

Name: CREEP_THRESHOLD_P_x (x = A, B, C)
Property: Read-Write

If the per-phase active power (fundamental plus harmonics) is less than the creep threshold, then the corresponding accumulators (P_x, P_x_F) are reset to zero. This rule is applied to every single cycle.

This creep affects the power accumulators, the pulse accumulators and measurements. However, the generic creep power threshold (POWER_OFFSET_P) affects only the pulse accumulators and measurements.

The CREEP_THRESHOLD_P_x is stored in the uQ12.20 format and the unit is mWatts-scaled (normalized by K_I_x and K_V_x).

$$CREEP\_THRESHOLD\_P\_x = \frac{P_{CREEP}}{K\_I\_x \times K\_V\_x} \times 2\text{^}20$$

If the creep active power for phase A is set to 5 Watt, K_I_A = 547 and K_V_A = 1651, then CREEP_THRESHOLD_P_A = round [5000 / (K_IA * K_VA) * 2^{20}] = 5805 = 0x000016AD.

Bit	31	30	29	28	27	26	25	24
	CREEP_THRESHOLD_P_x[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CREEP_THRESHOLD_P_x[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CREEP_THRESHOLD_P_x[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CREEP_THRESHOLD_P_x[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CREEP_THRESHOLD_P_x[31:0] (uQ12.20)

3.1.14. Creep Threshold for Quadergy

Name: CREEP_THRESHOLD_Q
Property: Read-Write

Total reactive energy pulse quantities in any one line cycle interval less than the creep threshold are reset to zero and are not accumulated.

The CREEP_THRESHOLD_Q is the creep reactive energy (Var-hour) in a full cycle (20 ms for 50 Hz, 16.667 ms for 60 Hz).

The CREEP_THRESHOLD_Q is stored in the uQ2.30 format.

If the creep active power is set to 11 VAR, and the system frequency is 60 Hz, then CREEP_THRESHOLD_Q = round[11 / (60 * 3600) * 2^{30}] = 54681 = 0x0000D599

Bit	31	30	29	28	27	26	25	24
	CREEP_THRESHOLD_Q[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CREEP_THRESHOLD_Q[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CREEP_THRESHOLD_Q[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CREEP_THRESHOLD_Q[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CREEP_THRESHOLD_Q[31:0] (uQ2.30)

3.1.15. Per-Phase Creep Threshold for Reactive Energy

Name: CREEP_THRESHOLD_Q_x (x = A, B, C)
Property: Read-Write

If the per-phase reactive power (fundamental plus harmonics) is less than the creep threshold, then the corresponding accumulators (Q_x, Q_x_F) are reset to zero. This rule is applied to every single cycle.

This creep affects the power accumulators, the pulse accumulators and measurements. However, the generic creep power threshold (POWER_OFFSET_Q) affects only the pulse accumulators and measurements.

The CREEP_THRESHOLD_Q_x is stored in the uQ12.20 format and the unit is mVArs-scaled (normalized by K_I_x and K_V_x).

$$CREEP\_THRESHOLD\_Q\_x = \frac{Q_{CREEP}}{K\_I\_x \times K\_V\_x} \times 2\text{^}20$$

If the creep reactive power for phase A is set to 5 VAr, K_I_A = 547, and K_V_A = 1651, then CREEP_THRESHOLD_Q_A = round [5000 / (K_IA * K_VA) * 2^{20}] = 5805 = 0x000016AD.

Bit	31	30	29	28	27	26	25	24
	CREEP_THRESHOLD_Q_x[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CREEP_THRESHOLD_Q_x[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CREEP_THRESHOLD_Q_x[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CREEP_THRESHOLD_Q_x[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CREEP_THRESHOLD_Q_x[31:0] (uQ12.20)

3.1.16. Creep Threshold of Phase Current

Name: CREEP_THRESHOLD_I
Property: Read-Write

For each phase with a current less than threshold CREEP_THRESHOLD_I in any one line cycle interval, any contributions to a selected pulse are zeroed out, and quantities from that phase make no contribution toward any selected pulse and its associated pulse accumulator.

The CREEP_THRESHOLD_I is stored in the uQ12.20 format and the unit is mArms-scaled (normalized by a common K_I). A single common K_I is used for all phases for CREEP_THRESHOLD_I determination.

$$CREEP\_THRESHOLD\_I = \frac{I_{CREEP-RMS}}{K\_I} \times 2\text{^}20$$

For example, for a desired creep threshold of 10 mA, K_I = 617.28396, then CREEP_THRESHOLD_I = round[(10 / 617.28396) * 2^{20}] = 16987 = 0x0000425B.

WARNING The CREEP_THRESHOLD_I functionality will be deactivated if any of the registers CREEP_THRESHOLD_I_A, CREEP_THRESHOLD_I_B, or CREEP_THRESHOLD_I_C contain a value other than zero.

Bit	31	30	29	28	27	26	25	24
	CREEP_THRESHOLD_I[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CREEP_THRESHOLD_I[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CREEP_THRESHOLD_I[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CREEP_THRESHOLD_I[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CREEP_THRESHOLD_I[31:0] (uQ12.20)

3.1.17. Per-Phase Creep Threshold of Phase Current

Name: CREEP_THRESHOLD_I_x (x = A, B, C)
Property: Read-Write

These registers allow to establish different current thresholds for each one of the phases.

If the per-phase x (x = A, B or C) current is less than the threshold, then the corresponding accumulators (I_x, I_x_F) are reset to zero. This rule is applied to every single cycle.

This creep affects the power accumulators, the pulse accumulators and measurements. However, the generic creep (CREEP_THRESHOLD_I) affects only the pulse accumulators and measurements.

The CREEP_THRESHOLD_I_x is stored in the uQ12.20 format and the unit is mArms-scaled (normalized by K_I_x).

$$CREEP\_THRESHOLD\_I\_x = \frac{I_{CREEP-RMS}}{K\_I\_x} \times 2\text{^}20$$

For example, for desired creep thresholds of 5 mA for phase A, 10 mA for phase B, and 15 mA for phase C (K_I_A = K_I_B = K_I_C = 617.28396), then:

- CREEP_THRESHOLD_I_A = round [(5 / 617.28396) * 2^{20}] = 8493 = 0x0000212D
- CREEP_THRESHOLD_I_B = round [(10 / 617.28396) * 2^{20}] = 16987 = 0x0000425B
- CREEP_THRESHOLD_I_C = round [(15 / 617.28396) * 2^{20}] = 25840 = 0x000064F0

Bit	31	30	29	28	27	26	25	24
	CREEP_THRESHOLD_I_x[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CREEP_THRESHOLD_I_x[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CREEP_THRESHOLD_I_x[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CREEP_THRESHOLD_I_x[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CREEP_THRESHOLD_I_x[31:0] (uQ12.20)

3.1.18. Creep Threshold for Apparent Energy

Name: CREEP_THRESHOLD_S
Property: Read-Write

Total apparent energy pulse quantities in any one line cycle interval less than the creep threshold are reset to zero and are not accumulated.

The CREEP_THRESHOLD_S is the creep apparent energy (VA-hour) in a full cycle (20 ms for 50 Hz, 16.667 ms for 60 Hz).

The CREEP_THRESHOLD_S is stored in the uQ2.30 format.

If the creep apparent power is set to 11 VA, and the system frequency is 60 Hz, then CREEP_THRESHOLD_S = round [11 / (60 * 3600) * 2^{30}] = 54681 = 0x0000D599.

Bit	31	30	29	28	27	26	25	24
	CREEP_THRESHOLD_S[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CREEP_THRESHOLD_S[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CREEP_THRESHOLD_S[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CREEP_THRESHOLD_S[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CREEP_THRESHOLD_S[31:0] (uQ2.30)

3.1.19. Power Offset Control Register

Name: POWER_OFFSET_CTRL
Property: Read-Write

Bit	31	30	29	28	27	26	25	24
	P_OFFSET_PUL				Q_OFFSET_PUL			S_OFFSET_PUL
Access	R/W				R/W			R/W
Reset	0				0			0

Bit	23	22	21	20	19	18	17	16
		P_OFFSET_ACC_C	P_OFFSET_ACC_B	P_OFFSET_ACC_A		Q_OFFSET_ACC_C	Q_OFFSET_ACC_B	Q_OFFSET_ACC_A
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 31 – P_OFFSET_PUL Active Power Offset for Pulse Quantities Enable
P_OFFSET_PUL is used to enable active power offset functionality for pulse quantities only. P_OFFSET_PUL uses register POWER_OFFSET_P affecting: active energy pulse generation and TX pulse accumulation registers.

Value	Name	Description
0x0	DISABLE	Disables offset
0x1	ENABLE	Enables offset

Bit 27 – Q_OFFSET_PUL Reactive Power Offset for Pulse Quantities Enable
Q_OFFSET_PUL is used to enable reactive power offset functionality for pulse quantities only. Q_OFFSET_PUL uses register POWER_OFFSET_Q affecting: reactive quadergy pulse generation and TX pulse accumulation registers.

Value	Name	Description
0x0	DISABLE	Disable offset
0x1	ENABLE	Enable offset

Bit 24 – S_OFFSET_PUL Apparent Power Offset for Pulse Quantities Enable
S_OFFSET_PUL is used to enable apparent power offset functionality for pulse quantities only. S_OFFSET_PUL uses register POWER_OFFSET_S affecting: apparent energy pulse generation and TX pulse accumulation registers.

Value	Name	Description
0x0	DISABLE	Disable offset
0x1	ENABLE	Enable offset

Bits 20, 21, 22 – P_OFFSET_ACC_x Active Power Offset for Accumulator Quantities Enable
P_OFFSET_ACC_x is used to enable per-channel active power offset added to the 64-bit processing stream. P_OFFSET_ACC_x uses registers POWER_OFFSET_P_x affecting: ACC_P_x 64-bit accumulators, active energy pulse generation and TX pulse accumulation registers.

Value	Name	Description
0x0	DISABLE	Disable offset
0x1	ENABLE	Enable offset

Bits 16, 17, 18 – Q_OFFSET_ACC_x Reactive Power Offset for Accumulator Quantities Enable
Q_OFFSET_ACC_x is used to enable per-channel reactive power offset added to the 64-bit processing stream. Q_OFFSET_ACC_x uses registers POWER_OFFSET_Q_x affecting: ACC_Q_x 64-bit accumulators, reactive quadergy pulse generation and TX pulse accumulation registers.

Value	Name	Description
0x0	DISABLE	Disable offset
0x1	ENABLE	Enable offset

3.1.20. Active Power Offset Register

Name: POWER_OFFSET_P
Property: Read-Write

This value indicates the active power offset of appointed pulse.

The physical significance of POWER_OFFSET_P is total active energy (W-hour) offset per full cycle (20 ms for 50 Hz, 16.667 ms for 60 Hz).

POWER_OFFSET_P is stored in sQ1.30 format and is subtracted each full cycle.

POWER_OFFSET_P affects only P and P_F pulse generation and ACC_Tx pulse accumulators.

If the power offset to be compensated is 0.25 mWh/cycle, the value to be written in the register is:

POWER_OFFSET_P = round [0.25 / 1000 * 2^{30}] = 268435 = 0x00041893.

0.25 mWh/cycle corresponds to an active power of 0.25 / 1000 * 50 * 3600 = 45W (at 50 Hz).

Refer to the “PIC32CXMTx Metrology User Guide” (*DS50003460*) for a more detailed description.

Bit	31	30	29	28	27	26	25	24
	POWER_OFFSET_P[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	POWER_OFFSET_P[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	POWER_OFFSET_P[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	POWER_OFFSET_P[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – POWER_OFFSET_P[31:0] (sQ1.30)

3.1.21. Reactive Power Offset Register

Name: POWER_OFFSET_Q
Property: Read-Write

This value indicates the reactive power offset of appointed pulse.

The physical significance of POWER_OFFSET_Q is total reactive energy (VAR-hour) offset per full cycle (20 ms for 50 Hz, 16.667 ms for 60 Hz).

POWER_OFFSET_Q is stored in sQ1.30 format and is subtracted each full cycle.

POWER_OFFSET_Q affects only Q and Q_F pulse generation and ACC_Tx pulse accumulators.

If the power offset to be compensated is 0.1 mVArh/cycle, the value to be written in the register is:

POWER_OFFSET_Q = round [0.1 / 1000 * 2^{30}] = 107374 = 0x0001A36E.

0.1 mVArh/cycle corresponds to a reactive power of 0.1 / 1000 * 60 * 3600 = 21.6 VAr (at 60 Hz).

Refer to the “PIC32CXMTx Metrology User Guide” (*DS50003460*) for a more detailed description.

Bit	31	30	29	28	27	26	25	24
	POWER_OFFSET_Q[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	POWER_OFFSET_Q[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	POWER_OFFSET_Q[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	POWER_OFFSET_Q[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – POWER_OFFSET_Q[31:0] (sQ1.30)

3.1.22. Apparent Power Offset Register

Name: POWER_OFFSET_S
Property: Read-Write

This value affects the apparent power offset of appointed pulse.

The parameter POWER_OFFSET_S represents the total squared current (Amp²-hour/cycle) offset per full cycle (20 ms for 50 Hz, 16.667 ms for 60 Hz). This offset is subtracted from the current value used to calculate the apparent power:

S = Vrms * (Irms – POWER_OFFSET_S).

Two alternative usage examples are given below.

1. To achieve the accurate result, measure an apparent power load curve with the apparent power offset disabled, follow these steps:
   a. Mathematically calculate the current offset causing the measured errors, in mA.
   b. Convert this value to the units of POWER_OFFSET_S, for example:
      i. The current RMS causing the errors is 21 mA.
      ii. K_I = 617.284.
      iii. Frequency is 50 Hz, resulting in 80 samples per cycle.
      iv. POWER_OFFSET_S = $80 * 2^{40} * (0.021 / 617.284)^2 = 101802$.
2. For a faster computation, use the accumulators I_A, I_B, and I_C, follow these steps:
   a. Apply the nominal voltage to the meter and set the current to zero.
   b. Read the I_A, I_B, and I_C accumulators and compute the average. For improved accuracy, take multiple measurements or increase the integration period.
   c. Calculate the corresponding value for a single cycle, for example:
      i. I_A = 52687391, I_B = 39070069, I_C = 47225301.
      ii. I_Average = 46327587.
      iii. Samples accumulated = 40000 (approximately 10 seconds).
      iv. Samples in 1 cycle = 80 (50 Hz).
      v. POWER_OFFSET_S = 46327587 * 80 / 40000 = 92655.

This register can be used with pulse types 6 (S) and 7 (S_F). However, it must not be used with pulse type 8. For pulse type 8 the per-phase active and reactive power offsets must be used.

POWER_OFFSET_S is stored in the sQ1.30 format and it is applied to each full cycle.
POWER_OFFSET_S affects only S and S_F pulse generation and ACC_Tx pulse accumulators.

Refer to the “PIC32CXMTx Metrology User Guide” (*DS50003460*) for additional information.

Bit	31	30	29	28	27	26	25	24
	POWER_OFFSET_S[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	POWER_OFFSET_S[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	POWER_OFFSET_S[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	POWER_OFFSET_S[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – POWER_OFFSET_S[31:0] (sQ1.30)

3.1.23. Voltage Swell Threshold

Name: SWELL_THRESHOLD_Vx
Property: Read-Write

For each half-cycle of the dominant phase, the RMS values of all voltages are calculated, taking into account both the fundamental and harmonic components. Each calculated value is then compared to the corresponding SWELL_THRESHOLD_Vx, (where x = [A, B, C]), to assess whether a voltage swell condition is present. For each half cycle that a voltage swell exists, the associated flag, SWELL_DET_Vx is set to 1.

A threshold is allowed for each phase and is computed using the native phase voltages before transformation to implied 4WY service. This allows setting different thresholds for non-balanced service types.

The SWELL_THRESHOLD_Vx is stored in the uQ0.32 format, therefore, set the threshold value as follows:

$$V_{x\ SWELL\ THRESHOLD} = \left(\frac{V_{SWELL-RMS}}{K\_Vx}\right)^2 \times 2\text{^}32$$

Bit	31	30	29	28	27	26	25	24
	SWELL_THRESHOLD_Vx[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SWELL_THRESHOLD_Vx[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SWELL_THRESHOLD_Vx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SWELL_THRESHOLD_Vx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SWELL_THRESHOLD_Vx[31:0] (uQ0.32)

3.1.24. Voltage Sag Threshold

Name: SAG_THRESHOLD_Vx
Property: Read-Write

For each half-cycle of the dominant phase, the RMS values of all voltages are calculated, taking into account both the fundamental and harmonic components. Each calculated value is then compared to the corresponding SAG_THRESHOLD_Vx, (where x = [A, B, C]), to assess whether a voltage sag condition is present. For each half cycle that a voltage sag exists, the associated flag, SAG_DET_Vx is set to 1.

A threshold is allowed for each phase and is computed using the native phase voltages, before transformation to implied 4WY service. This allows setting different thresholds for non-balanced service types.

The SAG_THRESHOLD_Vx is stored in the uQ0.32 format, therefore, set the threshold value as follows:

$$V_{x\ SAG\ THRESHOLD} = \left(\frac{V_{SAG-RMS}}{K\_Vx}\right)^2 \times 2\text{^}32$$

Bit	31	30	29	28	27	26	25	24
	SAG_THRESHOLD_Vx[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SAG_THRESHOLD_Vx[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SAG_THRESHOLD_Vx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SAG_THRESHOLD_Vx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SAG_THRESHOLD_Vx[31:0] (uQ0.32)

3.1.25. Voltage Interrupt Thresholds

Name: INTERRUPT_THRESHOLD_Vx (x = A, B, C)
Property: Read-Write

For each cycle of the dominant phase, the RMS values of all voltages are calculated, taking into account just the fundamental component. Each calculated value is then compared to the corresponding INTERRUPT_THRESHOLD_Vx, (where x = [A, B, C]), to assess whether a phase-loss condition is present.

The associated flag, PH_x_ACTIVE, is cleared every cycle in which a phase loss exists. In the same way, PH_x_ACTIVE is set every cycle in which a phase loss is not detected.

A threshold is allowed for each phase after meter form transformation.

The INTERRUPT_THRESHOLD_Vx is stored in the uQ0.32 format, thus, set the threshold value as follows:

$$V_{x\ INTERRUPT} = \left(\frac{V_{\text{INTERRUPT}-RMS}}{K\_Vx}\right)^2 \times 2\text{^}32$$

Bit	31	30	29	28	27	26	25	24
	INTERRUPT_THRESHOLD_Vx[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	INTERRUPT_THRESHOLD_Vx[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	INTERRUPT_THRESHOLD_Vx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INTERRUPT_THRESHOLD_Vx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – INTERRUPT_THRESHOLD_Vx[31:0] (uQ0.32)

3.1.26. Current Conversion Factor

Name: K_Ix
Property: Read-Write

The current conversion factor is used when converting an internal current quantity to an external equivalent RMS current quantity. K_Ix: where x = [A, B, C or N].

For proper ADC function, the differential input voltage proportional to current must be provided by the current sensor (typically a CT in conjunction with a burden resistor). This differential input voltage ($V_{diff} = V_+ - V_-$) must be scaled so that its peak input value is limited to the maximum acceptable ADC input voltage:

$$V_{diff\_max} = \frac{V_{ADCmax}}{G_{PGA}}$$

The maximum acceptable ADC input voltage is specified in the Data Sheet of the device. For example, in the case of ATSENSEs, the limit input value is 0.5V for an ADC PGA gain of G_{PGA} = 1 or 62.5 mV for an ADC PGA gain of G_{PGA} = 8.

The maximum differential input voltage must typically not exceed 0.5V (V_+ = 0.25V, V_- = -0.25V). However, acceptable performance may be achieved with signals as high as 0.55V or slightly higher. The ADC saturates at $V_{diff} \geq 0.6V$. When using single-ended inputs, a single-ended input of 0.5V may be used. However, the highest accuracy will be achieved by limiting single-ended input voltages to 0.25V to avoid introducing non-linearity due to approaching forward conduction of input protection diodes. Reduced input voltage range signal on current input channels may use the programmable gain amplifier to recover input range. In typical applications, external scaling allows for an appropriate over-current factor to maintain linearity during over-current events.

The ADC input voltage is, then, converted by comparing it to the reference voltage V_{REF}, specified in the Data Sheet of the AFE selected. This comparison creates an additional ADC internal input conversion gain, $1.0V/V_{REF}$, due to ratio-metric effect of the reference voltage, approximately 1.0 / 1.2 in the case of the ATSENSE, which is part of the ADC conversion factor and is taken care of internal to the DSP processing and is separate from the current channel calibration factor, CAL_M_Ix.

CT Sensors (Current Transformers)

For example, it is desired to have a max measurement current of 240 A_{RMS} (200 A_{RMS} + 20% over-current). The following three steps must be taken (this example assumes use of a CT turns ratio, T_e= 2500:1 (200 A_{RMS} : 80 mA_{RMS}) and a G_{PGA} = 4):

1. Determine total current burden resistor value, as if it were one single-ended input, then divide by 2 for differential burden resistors:

$$R_{burden\_total} = \frac{V_{diff\_max}}{I_{CTmax}} = \frac{\frac{V_{ADCmax}}{G_{PGA}}}{\sqrt{2} \times \frac{240A_{RMS}}{T_e}} = \frac{\frac{0.5V}{4}}{\sqrt{2} \times 96mA_{RMS}} = \frac{0.125V}{\sqrt{2} \times 96mA_{RMS}} = 0.920712\,\Omega_{se} = 2 \times (0.46\,\Omega_{diff})$$

   Each one of the two burden resistors (for differential inputs) would be selected as 0.46Ω.

2. Next, determine the current conversion factor (the equation shown, first, is the long-form definition):

$$K\_I_x = \frac{I_{CTmax}}{V_{diff\_max} \times G_{PGA}} = \frac{\sqrt{2} \times 240A_{RMS}}{0.125V \times G_{PGA}} = \frac{339.411A}{0.125V \times 4} = 678.823$$

   When using CTs with a burden resistor, the equation for K_I_x simplifies to (the preferred equivalent short-form):

$$K\_I_x = \frac{T_e}{R_{burden\_total} \times G_{PGA}} = \frac{2500}{0.920712\Omega \times 4} = 678.823$$

   Where, T_e= CT equivalent turns ratio.

3. Finally, to compute an equivalent external current, multiply an internal Qformat number, $I_{INTERNAL}$, in the following fashion:

$$I_{LINE\ RMS} = K\_I_x \times I_{INTERNAL}$$

Rogowski Coil Current Sensors

Rogowski coils produce an output voltage proportional to the time derivative of the current being measured and exhibit a gain proportional to the frequency being measured, f, as well as a 90° phase shift relative to the input signal. A 50 Hz signal would have 5/6 the gain as an equivalent 60 Hz signal in addition to the phase shift. The metrology DSP includes a selectable DI (Digital Integrator) to process all current channels using Rogowski coil sensors and introduces a 1/f gain response and an ideal -90° phase shift to compensate for derivative nature of Rogowski coil sensors. The DI (Digital Integrator) filter is adjusted for unity gain at 60 Hz.

For example, it is preferable to have a max measurement current of 240 A_{RMS} (200 A_{RMS} + 20% over-current). The following steps must be taken (this example assumes use of a Rogowski coil with an output of 500 µV/A at 60 Hz (or 416.6 µV/A at 50 Hz) and a G_{PGA} = 4, operating at a frequency of 50 Hz):

When using Rogowski coils, the equation for K_I_x simplifies to (the preferred equivalent short-form):

$$K\_I_x = \frac{k_{sf}(60Hz)}{G_{PGA}} = \frac{2000}{4} = 500$$

where, k_{sf} = Rogowski coil scale factor.

For this discussion, the scale factor, k_{sf}, is defined at the reference frequency, f_r = 60 Hz due to the DI (Digital Integrator) filter was designed for unity gain at 60 Hz. If it is preferred to use k_{sf} defined at another frequency, the gain of the DI filter must be accounted for in the computation as follows:

$$k_{di}(f) = \frac{60Hz}{f}$$

$$K\_I_x = \frac{k_{sf}(f)}{G_{PGA} \times\ k_{di}(f)} = \frac{\left(\frac{I_{pr}(f)}{V_{sr}(f)}\right)}{G_{PGA}\left(\frac{60Hz}{50Hz}\right)} = \frac{\left(\frac{1A}{0.000416V}\right)}{4\left(\frac{6}{5}\right)} = 500$$

where,

- I_{pr} = primary rated current
- V_{sr} = secondary rated voltage
- f = frequency of operation [Hz]

Refer to the “PIC32CXMTx Metrology User Guide” (*DS50003460*) for additional information.

Resistive Shunt Current Sensors

A resistive shunt current sensor produces an output voltage proportional to the current passing through it. Generally, if a shunt is used for measuring the active phase current, then the voltages of the shunt are at the high voltage of line phase being measured and the relative metering ground reference is usually connected directly to that line phase voltage to keep all voltages going into the PIC32CXMx or ATSENSE device at the same relative voltage level. This means the voltage of the neutral line is divided down to a fraction of a volt, relative to the line phase voltage.

$$K_{Ix} = \frac{1}{G_{PGA} \times R_{shunt}}$$

Example:

If R_{shunt} = 100 µΩ = 0.0001Ω and G_{PGA} = 8, then:

K_{Ix} = 1000000 / (8 * 100) = 1250

The metrology firmware uses uQ22.10 to represent both integer and fractional numbers, so set:

K_Ix = ROUND(1250 * 2^{10}) = 0x00138800

Bit	31	30	29	28	27	26	25	24
	K_Ix[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	K_Ix[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	K_Ix[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	K_Ix[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – K_Ix[31:0] (uQ22.10)

3.1.27. Voltage Conversion Factor

Name: K_Vx
Property: Read-Write

The voltage conversion factor is used when converting an internal voltage quantity to an external equivalent RMS voltage quantity. K_Vx: where x = [A, B, C, D].

For proper ADC function, voltage divider circuitry must be provided to reduce each high-voltage input channel from its peak input value to the max peak acceptable ADC differential input voltage.

In the case of the ATSENSE AFEs, all voltage channel inputs are constrained to use single-ended input voltages. While the maximum differential input voltage must not exceed 0.5V (V+ = 0. 25V, V- = -0.25V), it is recommended that the single-ended inputs be limited to ±0.25V to avoid approaching forward conduction of input protection diodes.

In case of using a MCP391x AFE, all the inputs are differential, so the channels used for measuring voltage can be used in differential or in single-ended mode. In this case, the differential input voltage supported is 0.6V and the single-ended voltage must be limited to ±0.3V. In typical applications, external scaling allows for any over-voltage factor (typically 20%). In some applications the over-voltage is increased to be able to measure the phase to phase voltage value (plus the typical 20%), to detect improper connection of the wires to the meter.

For example, it is preferable to have a max measurement voltage of 288 V_{RMS} (240 V_{RMS} + 20% over-voltage). Users need to consider the following three steps:

1. Determine external voltage divider ratio (single-ended input):

$$K_{divider} = \frac{V_{ADCmax\,pk}}{V_{LINEmax\,RMS}} = \frac{0.25V_{pk}}{\sqrt{2} \times 288V_{RMS}} = 0.0006138$$

2. Internal scaling within the DSP takes care of the multiplication factor, V_{REF}, to renormalize the ADC gain, when the channel calibration constant, CAL_M_Vx, is used.
3. Determine the voltage conversion factor:

$$K\_V_x = \frac{V_{LINEmax}}{V_{diff\_max}} = \frac{\sqrt{2} \times 288V_{RMS}}{0.25V_{pk}} = 1629.17$$

   When using a simple resistive voltage divider, the equation for K_V_x simplifies to the equivalent short-form:

$$K\_V_x = \frac{1}{G_{resistor\_divider\_ratio}} = 1629.17$$

   K_Vx is stored in the uQ22.10 format.
4. To compute an equivalent external voltage, multiply an internal Qformat number, $V_{INTERNAL}$, as given below:

$$V_{LINE\,RMS} = K\_V_x \times V_{INTERNAL}$$

Refer to the “PIC32CXMTx Metrology User Guide” (*DS50003460*) for additional information.

Bit	31	30	29	28	27	26	25	24
	K_Vx[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	K_Vx[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	K_Vx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	K_Vx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – K_Vx[31:0] (uQ22.10)

3.1.28. Current Channel Magnitude Calibration Constants

Name: CAL_M_Ix
Property: Read-Write

Multiplicative magnitude calibration constants are provided for each current channel to equalize gain across all channels after an appropriate calibration procedure was exercised. All active input channels, both voltage and current, require final calibration to ensure full accuracy.

CAL_M_Ix: where x = [A, B, C or N] is used to calibrate the current channels.

$$CAL\_M\_Ix = \frac{Ix\_RMS}{K\_Ix \times \sqrt{\frac{ACC\_I\_x}{N \times 2^{40}}}} \times 2^{29}$$

Where,

- *Ix_RMS* is the ideal RMS value of input calibration current
- ACC_I_x is the 64-bit accumulated I^2-scaled quantities provided by metrology firmware
- N = The number of samples in the integration period provided in Metrology Status Registers

Refer to the "PIC32CXMTx Metrology User Guide" (*DS50003460*) for additional information.

WARNING Be aware that this conversion factor is a signed quantity. Assigning a negative value results in an effective phase shift rotation of 180°, which can be particularly useful in specific scenarios, such as certain meter configurations or when dealing with inverted wiring polarity.

Bit	31	30	29	28	27	26	25	24
	CAL_M_Ix[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CAL_M_Ix[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CAL_M_Ix[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CAL_M_Ix[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CAL_M_Ix[31:0] (sQ2.29)

3.1.29. Voltage Channel Magnitude Calibration Constants

Name: CAL_M_Vx
Property: Read-Write

Multiplicative magnitude calibration constants are provided for each voltage channel to equalize gain across all channels after an appropriate calibration procedure was exercised. All active input channels, both voltage and current, require final calibration to ensure full accuracy.

CAL_M_Vx: where x = [A, B, C, D] is used to calibrate the voltage channels.

$$CAL\_M\_Vx = \frac{Vx\_RMS}{K\_Vx \times \sqrt{\frac{ACC\_V\_x}{N \times 2^{40}}}} \times 2^{29}$$

Where,

- *Vx_RMS* is the ideal RMS value of the input test voltage
- ACC_V_x is the 64-bit accumulated V^2-scaled quantities provided by metrology firmware
- N = The number of samples in the integration period provided in Metrology Status registers

Refer to the "PIC32CXMTx Metrology User Guide" (*DS50003460*) for additional information.

WARNING Be aware that this conversion factor is a signed quantity. Assigning a negative value results in an effective phase shift rotation of 180°.

Bit	31	30	29	28	27	26	25	24
	CAL_M_Vx[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CAL_M_Vx[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CAL_M_Vx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CAL_M_Vx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CAL_M_Vx[31:0] (sQ2.29)

3.1.30. Per-Channel Phase Calibration Constants

Name: CAL_PH_Ix, CAL_PH_Vx
Property: Read-Write

Phase calibration constants are provided for each channel to equalize relative phase differences across all channels after an appropriate calibration procedure was exercised. All active input channels, both voltage and current, require final calibration to ensure full accuracy. All phase-correction amounts are in BAMS units.

In cases where neither phase-phase vector transformation nor optimal phase-phase voltage measurement are not required, phase correction values may be set for only current channel, and voltage phase correction values are set to zero. However, if phase-phase equalization is desired, voltage channel phase correction values may be used.

Input requested phase correction values are relative values that may be internally adjusted with an internally computed offset to achieve proper phase shifts for use within the phase correction DSP filters. Any internal offset adjustment made by the DSP is available in the PH_OFFSET status register (see PH_OFFSET). This internal offset phase adjustment is made to shift all requested phase correction values to ≤ -1.35° (at 60 Hz). The maximum phase correction capability among the different channels is 32.39º (at 60 Hz) or 26.99º (at 50 Hz).

The requested input phase correction values may change dynamically and will be used to compute new phase correction filter coefficients at the start of each integration period. If phase correction values do change dynamically and, if it is preferable to keep coefficients as stationary as possible (change as little as possible), then set the phase correction value of an unused channel to a value slightly larger (more positive) than the expected maximum value of the range of allowable phase correction values. Otherwise, all unused channel's phase correction values must be set to zero.

For example, the top row of hex values represents the phase corrections as input into the phase correction registers:

	CAL_PH_IA	CAL_PH_VA
Input phase corr. values (hex)	0xFFEDCBAA	0x00000000
Input phase corr. values (dec)	-0.10º	-0.00º
Internally computed offset	-1.35º	—
Actual internal phase delays	-1.45º	-1.35º

If it is preferable to correlate the phase delays of internal signals with the phase delays of outside world signals, simply compute the actual phase delay values by adding the value of PH_OFFSET to the raw input phase correction values.

All phase correction angles entered must be normalized to 60 Hz. For example, if a phase correction factor of -0.31° is measured at 50 Hz, the value at 60 Hz is easily calculated as:

$$\angle angle_{60Hz} = \frac{60}{50}\angle angle_{50Hz} = \frac{60}{50}(-0.31°)_{50Hz} = -0.372°_{60Hz}$$

and to convert to the proper BAMS input format:

$$-0.372°_{60Hz} = \frac{-0.372°}{180°} \times 2^{31} = 0xFFBC478B$$

At the start of every integration period, the input phase calibration constants are used to compute the proper phase correction filter coefficients. If a requested set of phase-corrections is not possible, an error will be returned in the status register, STATE_FLAG: PC_OUT_OF_RANGE.

Note: Both sensor type and phase-correction inputs are used to properly compute a new set of phase-correction coefficients due to an additional built-in phase shift is used for compensation when the digital integrator is automatically selected when selecting Rogowski coils.

Refer to the “PIC32CXMTx Metrology User Guide” for additional information.

Bit	31	30	29	28	27	26	25	24
	CAL_PH_Ix, CAL_PH_Vx[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CAL_PH_Ix, CAL_PH_Vx[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CAL_PH_Ix, CAL_PH_Vx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CAL_PH_Ix, CAL_PH_Vx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CAL_PH_Ix, CAL_PH_Vx[31:0] (sQ0.31)

3.1.31. Waveform Capture Control Register

Name: CAPTURE_CTRL
Property: Read-Write

Waveform capture of 32-bit samples may be accomplished through exercise of these control bits, to select the Capture mode, which type of samples are to be captured and how many samples are captured. Capture data are written to the buffer starting at the address pointer stored in the CAPTURE_ADDR register. After each set of samples are captured, the number of the last sample set captured is stored in the CAPTURE_STATUS output register.

Upon completion of a one-shot capture sequence, the CAPTURE_STATE bits in the CAPTURE_STATUS register will be updated to COMPLETE, then, after the application code resets the CAPTURE_ENABLE bit to DISABLED, the CAPTURE_STATE bits will, then, be reset to DISABLED.

Bit	31	30	29	28	27	26	25	24
	CAPTURE_EN							
Access	R/W							
Reset	0							

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	CH_SEL_VD	CH_SEL_IN	CH_SEL_VC	CH_SEL_IC	CH_SEL_VB	CH_SEL_IB	CH_SEL_VA	CH_SEL_IA
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		CAPTURE_SOURCE[2:0]					CAPTURE_TYPE[1:0]	
Access		R/W	R/W	R/W			R/W	R/W
Reset		0	0	0			0	0

Bit 31 – CAPTURE_EN Enable Waveform Capture

Value	Description
0x0	Waveform capture is disabled
0x1	Waveform capture is enabled

Bits 8, 9, 10, 11, 12, 13, 14, 15 – CH_SEL_x Capture Channel Select
Up to 8 channels of data may be captured at the same time. Only selected channels are captured.

Value	Description
0x0	Waveform capture is disabled for channel x
0x1	Waveform capture is enabled for channel x

Bits 6:4 – CAPTURE_SOURCE[2:0] Capture Source Select
All captured data is after Vref compensation was applied and are scaled values (normalized by the appropriate K_Ix and K_Vx). In the case of 16 kHz sampling data, the calibration constants were not applied.

Value	Description
0x0	Capture 16 kHz data [sQ1.30] before DSP filtering
0x1	Capture 4 kHz FBW data [sQ2.29] (Full Bandwidth = fundamental + harmonics)

Value	Description
0x2	Capture 4 kHz NBW data [sQ2.29] (Narrow Bandwidth = fundamental only)
0x3	Capture 8 kHz FBW data [sQ2.29] (Full Bandwidth = fundamental + harmonics)
Other	RESERVED

Bits 1:0 – CAPTURE_TYPE[1:0] Selects whether capture is one-shot in nature (no samples captured prior to being enabled) or continuous capturing

Capture must be enabled to initiate a capture process. Once enabled, capture occurs based on the requested Capture mode. If enabled and a continuous Capture mode is selected, capture continues until it is disabled. If enabled and a one-shot Capture mode is selected, capture continues until appointed number of samples is captured.

Value	Name	Description
0x0	One-Shot Capture mode	Capture total CAPTURE_BUFF_SIZE of future data; capture will stop after capture finishes or is disabled.
0x1	Continuous Capture mode	Continuous capture of waveform data in circular-buffer fashion; capture will stop immediately after capture is disabled. CAPTURE_OFFSET indicates the offset of latest sample in capture buffer.

3.1.32. Capture Buffer Size

Name: CAPTURE_BUFF_SIZE
Property: Read-Write

CAPTURE_BUFF_SIZE specifies buffer size used for the capture function in units of 32-bit values. It must be divisible by the number of channels selected.

For example, to capture exactly 8,000 sets of samples of only the three voltage channels, set buffer size to:

CAPTURE_BUFF_SIZE = 8000[sample sets] * 3[samples/set] = 24000[samples] = 0x5DC0

Note: A buffer of 24,000 samples is equal in size to 96,000 bytes.

Table 3-3. Capture Buffer Distribution Samples

Channel IA is selected	All channel are selected	Channel IA and IB are selected
...	...	...
CH_IA_0	CH_IA_0	CH_IA_0
CH_IA_1	CH_VA_0	CH_IB_0
CH_IA_2	CH_IB_0	CH_IA_1
CH_IA_3	CH_VB_0	CH_IB_1
CH_IA_4	CH_IC_0	CH_IA_2
CH_IA_5	CH_VC_0	CH_IB_2
CH_IA_6	CH_IN_0	CH_IA_3
CH_IA_7	CH_VD_0	CH_IB_3
CH_IA_8	CH_IA_1	CH_IA_4
...	CH_VA_1	CH_IB_4
—	CH_IB_1	...
—	CH_VB_1	—
—	CH_IC_1	—
—	CH_VC_1	—
—	CH_IN_1	—
—	CH_VD_1	—
—	CH_IA_2	—
—	CH_VA_2	—
—	CH_IB_2	—
—	CH_VB_2	—
—	CH_IC_2	—
—	CH_VC_2	—
—	CH_IN_2	—
—	CH_VD_2	—
—	CH_IA_3	—
—	CH_VA_3	—
—	...	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CAPTURE_BUFF_SIZE[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CAPTURE_BUFF_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CAPTURE_BUFF_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – CAPTURE_BUFF_SIZE[23:0] (uQ24.0)

3.1.33. Waveform Capture Destination Buffer Address

Name: CAPTURE_ADDR
Property: Read-Write

This entry is used as the starting address of the waveform capture buffer and is interpreted as a pointer to a 32-bit unsigned integer.

The capture address must be set at least one sample period (250 µs) prior to enabling capture to ensure proper registration of the address.

Bit	31	30	29	28	27	26	25	24
	CAPTURE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CAPTURE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CAPTURE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CAPTURE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CAPTURE_ADDR[31:0] (uQ32.0)

3.1.34. AFE Control 0 Register (For ATSENSE203/301)

Name: AFE_CTRL_0 (For ATSENSE203/301)
Property: Read-Write

Different meaning depending on the selected AFE. This is the meaning for ATSENSE203/301.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	I3_GAIN[1:0]		I2_GAIN[1:0]		I1_GAIN[1:0]		I0_GAIN[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0:1, 2:3, 4:5, 6:7 – Ix_GAIN Gain Configuration of the Ix ADC channel
Note: I0_GAIN and I3_GAIN are not used for ATSENSE203.

Value	Name	Description
0	ADC_GAINX1	Input stage of the ADC has a gain of 1
1	ADC_GAINX2	Input stage of the ADC has a gain of 2
2	ADC_GAINX4	Input stage of the ADC has a gain of 4
3	ADC_GAINX8	Input stage of the ADC has a gain of 8

3.1.35. AFE Control 0 Register (For MCP3912/13/14)

Name: AFE_CTRL_0 (For MCP3912/13/14)
Property: Read-Write

Different meaning depending on the selected AFE. This is the meaning for MCP3912/13/14 (for the MCP3910, configuration settings are determined by hardware and cannot be changed through software). For additional information, refer to the MCP391x Data Sheet.

Bit	31	30	29	28	27	26	25	24
					DITHER[1:0]		BOOST[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PGA_CH7[2:0]			PGA_CH6[2:0]			PGA_CH5[2:1]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PGA_CH5[0]	PGA_CH4[2:0]			PGA_CH3[2:0]			PGA_CH2[2]
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PGA_CH2[1:0]		PGA_CH1[2:0]			PGA_CH0[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:26 – DITHER[1:0] Dithering Circuit for Idle Tone´s Cancellation and Improved THD on All Channels

Value	Description
11	Dithering on, Strength = Maximum
10	Dithering on, Strength = Medium
01	Dithering on, Strength = Minimum
00	Dithering turned off

Bits 25:24 – BOOST[1:0] Bias Current Selection for all ADCs (impacts achievable maximum sampling speed)

Value	Description
11	All channels have current x 2
10	All channels have current x 1
01	All channels have current x 0.66
00	All channels have current x 0.5

Bits 0:2, 3:5, 6:8, 9:11, 12:14, 15:17, 18:20, 21:23 – PGA_CHx PGA Setting for Channel x
Note: PGA_CH4 and PGA_CH5 are only for MCP3913/14. PGA_CH6 and PGA_CH7 are only for MCP3914.

Value	Description
111	Reserved (Gain = 1)
110	Reserved (Gain = 1)
101	Gain is 32
100	Gain is 16
011	Gain is 8
010	Gain is 4

Value	Description
001	Gain is 2
000	Gain is 1

3.1.36. Per-Phase Active Power Offset Register

Name: POWER_OFFSET_P_x
Property: RW, Format sQ-9.40 (same format as the lsb 32-bits of 64-bit P_x accumulators)

This value indicates the per-phase active power offset, POWER_OFFSET_P_x: where x = [A, B, C]. The units of POWER_OFFSET_P_x is [W samp-scaled].

For a fixed voltage, this offset may be computed by applying voltage phase(s), setting zero current(s) and reading the phase's active power accumulator, P_x. Averaging over many readings or a longer integration period may provide a more statistically accurate estimate.

$$POWER\_OFFSET\_P\_x = \frac{ACC\_P\_x}{N}$$

Where, N = Number of samples in integration period.

Alternatively, if the offset to be compensated is in units of Watt, the value to be written in the register can be computed as:

POWER_OFFSET_P_x = Offset (Watt) * 2^{40} / (K_Ix * K_Vx)

Example to compensate a 5W offset given K_IA = 617,284179 and K_VA = 1651:

POWER_OFFSET_P_A = round(5 * 2^{40} / (617,284179 * 1651)) = 5394331 = 0x00524F9B

Bit	31	30	29	28	27	26	25	24
	POWER_OFFSET_P_x[31:24]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	POWER_OFFSET_P_x[23:16]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	POWER_OFFSET_P_x[15:8]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	POWER_OFFSET_P_x[7:0]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – POWER_OFFSET_P_x[31:0] Per-Phase Active Power Offset Register
POWER_OFFSET_P is stored in sQ1.30 format, and its value is subtracted each sample at a 4 kHz rate.

3.1.37. Per-Phase Reactive Power Offset Register

Name: POWER_OFFSET_Q_x
Property: RW, Format sQ-9.40 (same format as the lsb 32-bits of 64-bit Q_x accumulators)

This value indicates the per-phase reactive power offset, POWER_OFFSET_Q_x: where x = [A, B, C]. The units of POWER_OFFSET_Q_x is [VAR samp-scaled].

For a fixed voltage, this offset may be computed by applying voltage phase(s), setting zero current(s) and reading the phase's reactive power accumulator, Q_x. Averaging over many readings or a longer integration period may provide a more statistically accurate estimate.

$$POWER\_OFFSET\_Q\_x = \frac{ACC\_Q\_x}{N}$$

Where N = number of samples in integration period.

Alternatively, if the offset to be compensated is in units of VAr, the value to be written in the register can be computed as:

POWER_OFFSET_Q_x = Offset (VAr) * 2^{40} / (K_Ix * K_Vx)

Example to compensate a 5 VAr offset given K_IA = 617,284179 and K_VA = 1651:

POWER_OFFSET_Q_A = round(5 * 2^{40} / (617,284179 * 1651)) = 5394331 = 0x00524F9B

Bit	31	30	29	28	27	26	25	24
	POWER_OFFSET_Q_x[31:24]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	POWER_OFFSET_Q_x[23:16]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	POWER_OFFSET_Q_x[15:8]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	POWER_OFFSET_Q_x[7:0]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – POWER_OFFSET_Q_x[31:0] Per-Phase Reactive Power Offset Register
POWER_OFFSET_Q is stored in sQ1.30 format and its value is subtracted each sample at a 4 kHz rate.

3.2. Metrology Status Registers

The Metrology module generates primary 32-bit output measurement quantities for each measurement interval, per-phase quantities with each phase designated by the subscript "_x". The starting address is 0x20088150.

Table 3-4. Metrology Status Registers

Index	Address	Variable	Access Mode	Name	Format	No. Bytes	Min Value	Max Value	Default	Units
0	0x20088150	VERSION	R	Metrology Firmware version	—	4	—	—	—	integer
1	0x20088154	STATUS	R	Metrology Status register	—	4	—	—	—	integer
2	0x20088158	STATE_FLAG	R	Metrology Version and State Flags register	—	4	—	—	—	integer
3	0x2008815C	CAPTURE_STATUS	R	Waveform capture status	—	4	—	—	—	integer
4	0x20088160	INTERVAL_NUM	R	Interval number	—	4	0	—	—	integer
5	0x20088164	N	R	Number samples in measurement interval	uQ16.0	4	1	3960	0	integer
6	0x20088168	PH_OFFSET	R	Phase calibration offset	sQ0.31	4	-1.000	+0.9999	—	BAMS
7	0x2008816C	FREQ	R	Frequency of fundamental harmonic	uQ20.12	4	42.5	69	—	Hz
8	0x20088170	FREQ_VA	R	Frequency of fundamental harmonic, VA	uQ20.12	4	42.5	69	—	Hz
9	0x20088174	FREQ_VB	R	Frequency of fundamental harmonic, VB	uQ20.12	4	42.5	69	—	Hz
10	0x20088178	FREQ_VC	R	Frequency of fundamental harmonic, VC	uQ20.12	4	42.5	69	—	Hz
11	0x2008817C	RESERVED	—	—	—	—	—	—	—	—
12	0x20088180	TEMPERATURE	R	Temperature, average	sQ23.8	4	—	—	—	°C
13	0x20088184	V_A_MAX	R	Max phase-A voltage during measurement interval	sQ2.29	4	-4.0	3.9999	—	V_{pk} scaled
14	0x20088188	V_B_MAX	R	Max phase-B voltage during measurement interval	sQ2.29	4	-4.0	3.9999	—	V_{pk} scaled
15	0x2008818C	V_C_MAX	R	Max phase-C voltage during measurement interval	sQ2.29	4	-4.0	3.9999	—	V_{pk} scaled
16	0x20088190	RESERVED	-	—	—	4	—	—	—	—
17	0x20088194	I_A_MAX	R	Max phase-A current during measurement interval	sQ2.29	4	-4.0	3.9999	—	A_{pk} scaled
18	0x20088198	I_B_MAX	R	Max phase-B current during measurement interval	sQ2.29	4	-4.0	3.9999	—	A_{pk} scaled
19	0x2008819C	I_C_MAX	R	Max phase-C current during measurement interval	sQ2.29	4	-4.0	3.9999	—	A_{pk} scaled
20	0x200881A0	I_Nm_MAX	R	Max phase-N measured current during measurement interval	sQ2.29	4	—	—	—	A_{pk} scaled
21	0x200881A4	I_Ni_MAX	R	Max phase-N imputed current during measurement interval	sQ16.15	4	—	—	—	Amp_{pk}
22	0x200881A8	FEATURES	R	Compiled feature indicator bits	uQ32.0	4	—	—	—	—
23	0x200881AC	N_CYCLE	R	Number samples in the last cycle	uQ20.12	4	1	3960	0	real number
24	0x200881B0	RESERVED	—	—	—	4	—	—	—	—

Table 3-4. Metrology Status Registers (continued)

Index	Address	Variable	Access Mode	Name	Format	No. Bytes	Min Value	Max Value	Default	Units
25	0x200881B4	RESERVED	—	—	—	4	—	—	—	—
26	0x200881B8	PULSE0_COUNTER	R	Number of pulses issued (Pulse 0)	uQ32.0	4	—	—	0	integer
27	0x200881BC	PULSE1_COUNTER	R	Number of pulses issued (Pulse 1)	uQ32.0	4	—	—	0	integer
28	0x200881C0	PULSE2_COUNTER	R	Number of pulses issued (Pulse 2)	uQ32.0	4	—	—	0	integer
29	0x200881C4	RESERVED	—	—	—	4	—	—	—	—
30	0x200881C8	ZC_N_VA	R	Zero-crossing sample number of phase-A voltage	uQ20.12	4	—	—	—	real number
31	0x200881CC	ZC_N_VB	R	Zero-crossing sample number of phase-B voltage	uQ20.12	4	—	—	—	real number
32	0x200881D0	ZC_N_VC	R	Zero-crossing sample number of phase-C voltage	uQ20.12	4	—	—	—	real number
33	0x200881D4	RESERVED	—	—	—	4	—	—	—	—
34	0x200881D8	ATSENSE_CAL_41_44	R	ATSENSE manufacturing calibration data, registers 41-44	uQ32.0	4	—	—	—	integer
35	0x200881DC	ATSENSE_CAL_45_48	R	ATSENSE manufacturing calibration data, registers 45-48	uQ32.0	4	—	—	—	integer

3.2.1. Metrology Firmware Version

Name: VERSION
Property: Read

This register is defined to indicate the metrology version. It is recommended that the application code check this register to make sure that correct metrology version is used.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	FIRMWARE_MAJOR_VER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	FIRMWARE_MINOR_VER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FIRMWARE_REV[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 23:16 – FIRMWARE_MAJOR_VER[7:0] Major Firmware Version
It indicates the major version number of metrology firmware.

Bits 15:8 – FIRMWARE_MINOR_VER[7:0] Minor Firmware Version
It indicates the minor version number of metrology firmware.

Bits 7:0 – FIRMWARE_REV[7:0] Firmware Revision
It indicates the revision number of metrology firmware.

3.2.2. Metrology Status Register

Name: STATUS
Property: Read

This register provides status information about the metrology.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

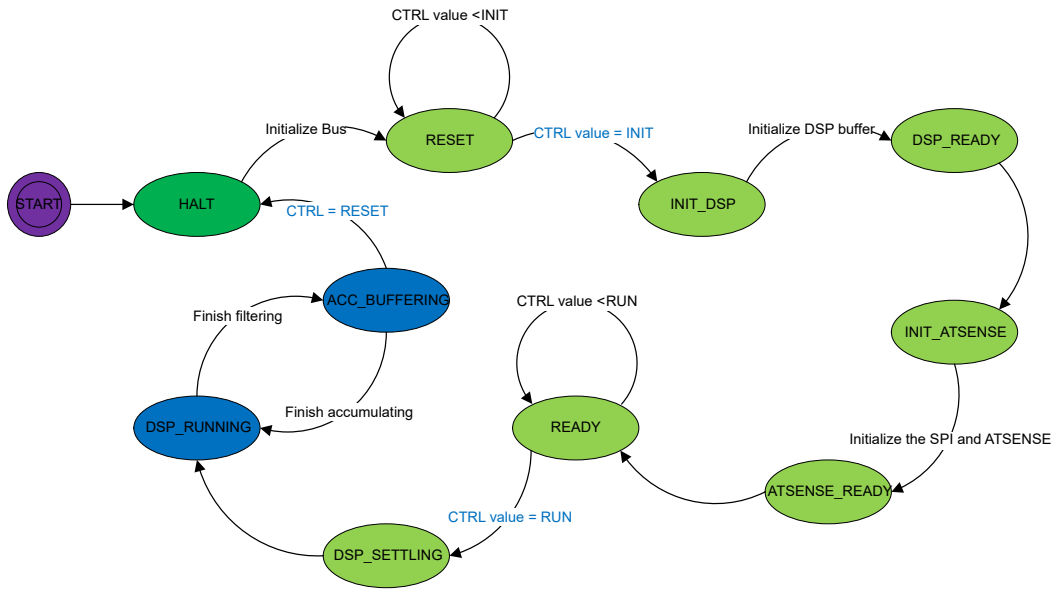
Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					STATUS[3:0]			
Access					R	R	R	R
Reset					0	0	0	0

Bits 3:0 – STATUS[3:0] Metrology Function State
The user can refer to the metrology state diagram for a more detailed description.

Figure 3-1. Metrology State Diagram



Value	Name	Description
0x0	HALT	Metrology module is halted
0x1	RESET	Resetting metrology module

Value	Name	Description
0x2	INIT_DSP	Initializing DSP filters
0x3	DSP_READY	DSP filters were initialized
0x4	INIT_ATSENSE	Initializing ATSENSE
0x5	ATSENSE_READY	ATSENSE was initialized
0x6	READY	ATSENSE temperature configuration and calibration data were copied into output registers
0x7	DSP_SETTLING	Waiting for DSP filters to stabilize to full accuracy
0x8	DSP_RUNNING	DSP filters have stabilized to full accuracy
0x9 and above	RESERVED	—

3.2.3. Metrology State Flags Register

Name: STATE_FLAG
Property: Read

Bit	31	30	29	28	27	26	25	24
		SWELL_DET_VC	SWELL_DET_VB	SWELL_DET_VA		SAG_DET_VC	SAG_DET_VB	SAG_DET_VA
Access		R	R	R		R	R	R
Reset		0	0	0		0	0	0

Bit	23	22	21	20	19	18	17	16
	CREEP_DET_S	PC_OUT_OF_RANGE	ARCH_DETECT_FAIL	CREEP_DET_P	CREEP_DET_Q	CREEP_DET_IC	CREEP_DET_IB	CREEP_DET_IA
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	HOST_ID_FAIL		CREEP_DET_P_C	CREEP_DET_P_B	CREEP_DET_P_A	CREEP_DET_Q_C	CREEP_DET_Q_B	CREEP_DET_Q_A
Access	R		R	R	R	R	R	R
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	AFE_FAIL		FREQ_LOCKED	TIMING_Vx[1:0]		PH_C_ACTIVE	PH_B_ACTIVE	PH_A_ACTIVE
Access	R		R	R	R	R	R	R
Reset	0		0	0	0	0	0	0

Bits 28, 29, 30 – SWELL_DET_Vx Voltage Swell Detected Flag for Channel x

Value	Description
0	Voltage swell is not detected for the current half line cycle
1	Voltage swell is detected for the current half line cycle

Bits 24, 25, 26 – SAG_DET_Vx Voltage Swell Detected Flag for Channel x

Value	Description
0	Voltage sag is not detected in the current half line cycle
1	Voltage sag is detected in the current half line cycle

Bit 23 – CREEP_DET_S Total Apparent Power Creep Detected Flag
CREEP_DET_S status flag only updated when enabled (CREEP_S_EN = 1).

Value	Description
0	Apparent power creep is not detected in the current full line cycle
1	Apparent power creep is detected in the current full line cycle

Bit 22 – PC_OUT_OF_RANGE Phase Corrector Out of Range
Indicates if a set of requested phase correction values are out of range.

Value	Description
0	Requested phase correction values in range
1	Requested phase correction values out of range

Bit 21 – ARCH_DETECT_FAIL Architecture Detect Failure
Indicates that a proper device architecture was not detected (”SH” or “C”).

Value	Description
0	A proper device (”SH” or “C”) was detected
1	An improper device (not ”SH” nor “C”) was detected

Bit 20 – CREEP_DET_P Total Active Power Creep Detected Flag
CREEP_DET_P status flag only updated when enabled (CREEP_P_EN = 1).

Value	Description
0	Active power creep is not detected in the current full line cycle
1	Active power creep is detected in the current full line cycle

Bit 19 – CREEP_DET_Q Total Reactive Power Creep Detected Flag
CREEP_DET_Q status flag only updated when enabled (CREEP_Q_EN = 1).

Value	Description
0	Reactive power creep is not detected in the current full line cycle
1	Reactive power creep is detected in the current full line cycle

Bits 16, 17, 18 – CREEP_DET_Ix Phase x Current Creep Detected Flag
CREEP_DET_I status flag only updated when enabled (CREEP_I_EN = 1).

Value	Description
0	Channel x current creep is not detected in the current full line cycle
1	Channel x current creep is detected in the current full line cycle

Bit 15 – HOST_ID_FAIL Host Identification Failure Indication
The detection process determines if the host has an internal ATSENSE (PIC32CXMTSx) or makes use of an external ATSENSE (PIC32CXMTC). If a proper ID is not made, this bit is used to show this status.

Value	Description
0	Proper PIC32CXMTx part successfully identified
1	Failed to identify proper PIC32CXMTx part

Bits 11, 12, 13 – CREEP_DET_P_x Phase x Power Creep Detected Flag
CREEP_DET_P_x status flag only updated when enabled (CREEP_P_EN = 1).

Value	Description
0	Phase x power creep is not detected in the current full line cycle
1	Phase x power creep is detected in the current full line cycle

Bits 8, 9, 10 – CREEP_DET_Q_x Phase x Reactive Power Creep Detected Flag
CREEP_DET_Q_x status flag only updated when enabled (CREEP_Q_EN = 1).

Value	Description
0	Phase x reactive power creep is not detected in the current full line cycle
1	Phase x reactive power creep is detected in the current full line cycle

Bit 7 – AFE_FAIL State

Value	Description
0	AFE initialization is successful
1	AFE initialization is failed

Bit 5 – FREQ_LOCKED Frequency Locked Flag

Value	Description
0	Line frequency is not determined. Using sample count limit for metrology integration period
1	Line frequency was determined

Bits 4:3 – TIMING_Vx[1:0] Dominant Voltage Channel
Indicates which voltage channel is used for frequency determination and cycle timing. If no voltage phases are active, phase VA is selected by default.

Value	Description
0	Voltage phase VA is used for timing extraction purposes
1	Voltage phase VB is used for timing extraction purposes
2	Voltage phase VC is used for timing extraction purposes

Bits 0, 1, 2 – PH_x_ACTIVE Phase x is active (Voltage Interrupt Detected Flag for Channel x)

Value	Description
0	Voltage phase x is inactive for the current full line cycle
1	Voltage phase x is active for the current full line cycle

3.2.4. Waveform Capture Function Status

Name: CAPTURE_STATUS
Property: Read

Bit	31	30	29	28	27	26	25	24
	CAPTURE_WRAP			INVALID_ADDR	CAPTURE_STATE[3:0]			
Access	R			R	R	R	R	R
Reset	0			0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CAPTURE_OFFSET[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CAPTURE_OFFSET[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CAPTURE_OFFSET[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 31 – CAPTURE_WRAP Capture Buffer Wrapped

Value	Name	Description
0	NOT WRAPPED	Buffer has not wrapped
1	WRAPPED	Buffer has wrapped at least once (in circular buffer fashion, as used in continuous capture modes)

Bit 28 – INVALID_ADDR Invalid Capture Address

Value	Name	Description
0	0	Capture address within valid range [0x20000000, 0x20080000]
1	1	Capture address outside valid range

Bits 27:24 – CAPTURE_STATE[3:0] Waveform Capture Status
Status will be meaningful only when CAPTURE_EN is set to '1'.

Value	Name	Description
0x0	DISABLED	Capture disabled
0x1	ACTIVE	Capture in progress
0x2	COMPLETE	Capture completed
0x3	RESERVED	—

Bits 23:0 – CAPTURE_OFFSET[23:0] Capture Offset
Offset within the buffer indicating the position of the last sample stored.

3.2.5. Measurement Interval Number

Name: INTERVAL_NUM
Property: Read

The measurement interval number associated with the present set of Metrology output data.

Bit	31	30	29	28	27	26	25	24
	INTERVAL_NUM[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	INTERVAL_NUM[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	HALFCYCLE_COUNT[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HALFCYCLE_COUNT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – INTERVAL_NUM[15:0] Interval number (uQ16.0)
The number of the present integration interval. This count rolls over from max count to 0.

Bits 15:0 – HALFCYCLE_COUNT[15:0] Sub-interval number (uQ16.0)
The sub-interval number is the number of half-cycles that have occurred in the present integration interval; depending on how often interrupts are selected. This count resets each new integration interval.

3.2.6. Number of Samples in the Last Measurement Interval

Name: N
Property: Read

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	N[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	N[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – N[15:0] Number of Samples in the Last Measurement Interval (uQ16.0)
The number of samples, N, in the last measurement interval based on zero-crossings of the selected voltage channel.
Note: It is recommended that this value be used to calculate the RMS value or power.

3.2.7. Phase Correction Filter Offset

Name: PH_OFFSET
Property: Read

Bit	31	30	29	28	27	26	25	24
	PH_OFFSET[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PH_OFFSET[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PH_OFFSET[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PH_OFFSET[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PH_OFFSET[31:0] Phase Correction Filter Offset (sQ0.31)
All voltage and current channels may be phase corrected by setting the requested relative phase adjustment values in registers, CAL_PH_Vx and CAL_PH_Iy. The actual phase adjustment angles implemented will be offset by this amount, the minimum required, such that all phase corrections are ≤ -1.35° @ 60 Hz (-1.125° @ 50 Hz). To determine the actual phase correction angle for each channel, add this offset to each requested phase correction amount. See CAL_PH_Ix, CAL_PH_Vx description for detailed example.

3.2.8. Dominant Line Voltage Fundamental Harmonic Frequency

Name: FREQ
Property: Read

Bit	31	30	29	28	27	26	25	24
	FREQ[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	FREQ[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	FREQ[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FREQ[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – FREQ[31:0] Frequency of Fundamental Harmonic (uQ20.12)
Frequency of the line voltage fundamental harmonic component is determined by the Metrology module and provided in the variable FREQ, using the dominant phase. In addition, a separate frequency is determined for each individual voltage phase, for each of three phases, x = [A, B, C].
Note: Maximum accuracy in frequency measurement is achieved at the end of the integration period. Therefore, the register should be read immediately after the integration interrupt is generated. However, since this register is updated each time a positive zero-crossing in the voltage line is detected, it is possible to read the register after the full cycle interrupt, enabling a faster refresh of the value.

3.2.9. Line Voltage Fundamental Harmonic Frequency

Name: FREQ_Vx
Property: Read

Bit	31	30	29	28	27	26	25	24
	FREQ_Vx[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	FREQ_Vx[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	FREQ_Vx[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FREQ_Vx[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – FREQ_Vx[31:0] Frequency of Fundamental Harmonic Vx (uQ20.12)
Frequency of the line voltage fundamental harmonic component is determined by the Metrology module and provided in the variable FREQ. A separate frequency is determined for each individual voltage phase, for each of three phases, x = [A, B, C].
Note: Maximum accuracy in frequency measurement is achieved at the end of the integration period. Therefore, the register should be read immediately after the integration interrupt is generated. However, since this register is updated each time a positive zero-crossing in the voltage line is detected, it is possible to read the register after the full cycle interrupt, enabling a faster refresh of the value.

3.2.10. Sensor Temperature

Name: TEMPERATURE
Property: Read

Bit	31	30	29	28	27	26	25	24
	TEMPERATURE[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TEMPERATURE[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TEMPERATURE[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TEMPERATURE[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TEMPERATURE[31:0] Temperature Average (sQ23.8)
The metrology module generates the average temperature over the measurement interval. The temperature is stored in sQ23.8 format in units of °C.
The temperature measurement reflects the value from the ATSENSE AFE. If an MCP391x device is used, this register is unused.

3.2.11. Voltage Peak Registers

Name: V_A_MAX, V_B_MAX, V_C_MAX
Property: Read

V_x_MAX is the maximum voltage peak absolute value of phase x, x = [A, B, C], in units of [$Volt_{pk}$ scaled].

They can be reset by setting V_MAX_RESET to '1'.

The peak voltage may be calculated by following formula:

$$V\_x\_peak = \frac{V\_x\_MAX}{2^{29}} \times K\_V_x$$

Where,

- K_V_x is the voltage conversion factor in the float format
- V_x_peak is the peak voltage of phase x, in unit of Volt

Phase voltage max values, V_x_MAX for x = [A, B, C], are determined using FBW (Full Band-Width) baseband filtered data.

Bit	31	30	29	28	27	26	25	24
	V_x_MAX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	V_x_MAX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	V_x_MAX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	V_x_MAX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – V_x_MAX[31:0] Max Phase-x Voltage During Measurement Interval (sQ2.29)

3.2.12. Phase Current Peak Registers

Name: I_A_MAX, I_B_MAX, I_C_MAX
Property: Read

I_x_MAX is the maximum current peak absolute value of phase x, x = [A, B, C], in units of [Amp_{pk} scaled].

They can be reset by setting I_MAX_RESET to '1'.

The peak current may be calculated by the following formula:

$$I_{x_{peak}} = \frac{I_{x_{MAX}}}{2^{29}} \times K_{I_x} = \frac{I_{x_{MAX}}}{2^{29}} \times \frac{K\_Ix}{2^{10}}$$

Where,

- K_I_x is the current conversion factor in float format
- K_Ix is the current conversion register value
- *I_x_peak* is the peak current of phase x, in unit of Amp

Phase current max values, I_x_MAX for x = [A,B,C], are determined using FBW (Full Band-Width) baseband DSP-filtered data.

Bit	31	30	29	28	27	26	25	24
	I_x_MAX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	I_x_MAX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	I_x_MAX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	I_x_MAX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – I_x_MAX[31:0] Max Phase-x Current During Measurement Interval (sQ2.29)

3.2.13. Neutral Current Peak Registers

Name: I_Ni_MAX, I_Nm_MAX
Property: Read

I_Nx_MAX is the maximum Neutral current peak absolute value of phase x, x = [Ni, Nm], in units of [Amp_{pk}] (x = [Ni]) or [AmpPK scaled] (x = [Nm]).

They can be reset by setting the I_MAX_RESET to '1'.

The peak currents may be calculated by the following formulas:

$$I\_Ni\_peak = \frac{I\_x\_MAX}{2^{15}}$$

$$I\_Nm\_peak = \frac{I\_x\_MAX}{2^{29}} \times K_{Ix} = \frac{I\_x\_MAX}{2^{29}} \times \frac{K\_Ix}{2^{10}}$$

Neutral current maximum values, I_Nx_MAX for x = [Ni, Nm], are determined using the FBW (Full Band Width) baseband DSP-filtered data.

Bit	31	30	29	28	27	26	25	24
	I_Nx_MAX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	I_Nx_MAX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	I_Nx_MAX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	I_Nx_MAX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – I_Nx_MAX[31:0] Max Neutral-x Current During Measurement Interval (sQ16.15 Format (I_Ni_MAX) and sQ2.29 Format (I_Nm_MAX)).

3.2.14. Compiled Feature Indicator Bits

Name: FEATURES
Property: Read

Bit	31	30	29	28	27	26	25	24
	POLY_PHASE	SINGLE_PHASE				RCZ_OUT		Fs_SAMPLE_RATE
Access	R	R				R		R
Reset	0	0				0		0

Bit	23	22	21	20	19	18	17	16
		ATSENSE_LOC	NUM_PULSES[1:0]		ROGOWSKI_DC_REMOVE	CAPTURE	CREEP	DFT_ENABLED
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CORE_CLK_SPEED[3:0]				RZC_DETECT	PQ_OFFSET_X	I_N_MUXING	HALF_COPROC_CLK
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
								DEBUG_MODES
Access								R
Reset								0

Bit 31 – POLY_PHASE Flag

Value	Description
1	Compiled: Poly-phase metering enabled

Bit 30 – SINGLE_PHASE Flag

Value	Description
1	Compiled: Single-phase metering enabled

Bit 26 – RCZ_OUT Flag

Value	Description
1	Compiled: Detect independent V_A raw zero-crossings and output signal on pin PD19 **Note:** Not compatible with NUM_PULSES = 3

Bit 24 – Fs_SAMPLE_RATE
Metrology baseband sample rate.

Value	Description
0	Baseband sample rate FS = 4000 kHz
1	Baseband sample rate FS = 8000 kHz

Bit 22 – ATSENSE_LOC

Value	Description
0	PIC32CXMTSH, Internal ATSENSE detected (ATSENSE203)

Value	Description
1	PIC32CXMTC, External ATSENSE detected (ATSENSE301)

Bits 21:20 – NUM_PULSES[1:0]

Metrology may be compiled with different number of pulses enabled, [0-3].
NUM_PULSES equals the number of pulses enabled during compile time.

Bit 19 – ROGOWSKI_DC_REMOVE Flag

Value	Description
1	Compiled for DC-removal before integrator filter when using Rogowski coil current sensors

Bit 18 – CAPTURE Flag

Value	Description
1	Compiled for waveform capture

Bit 17 – CREEP Flag

Value	Description
1	Compiled for CREEP thresholding

Bit 16 – DFT_ENABLED Flag

Value	Description
1	Compiled for DFT harmonic analysis

Bits 15:12 – CORE_CLK_SPEED[3:0]

Core-1 (Metrology core) clock fixed at 237.568 MHz in PIC32CXMTxx metrology.

Value	Description
0x0	Compiled to be used with Core-0 clock = undefined
0x1	Compiled to be used with Core-0 clock = 102.400 MHz
0x2	Compiled to be used with Core-0 clock = 106.496 MHz
0x3	Compiled to be used with Core-0 clock = 110.592 MHz
0x4	Compiled to be used with Core-0 clock = 114.688 MHz
0x5	Compiled to be used with Core-0 clock = 118.784 MHz
0x6	Compiled to be used with Core-0 clock = 237.568 MHz
0x7	Reserved

Bit 11 – RZC_DETECT Flag

Value	Description
1	Compiled for raw zero-cross detect

Bit 10 – PQ_OFFSET_X Flag

Value	Description
1	Compiled for use of PQ per-phase offsets

Bit 9 – I_N_MUXING Flag

Value	Description
1	Compiled for near-full bandwidth I_Neutral metrology

Bit 8 – HALF_COPROC_CLK Flag

Value	Description
1	Compiled for Core1 coprocessor to run at half speed of Core0

Bit 0 – DEBUG_MODES

Value	Description
0	Unless specifically compiled for a Debug mode, this bit is always = 0
1	Metrology FW compiled in a Debug mode

3.2.15. Number of Samples in the Last Cycle

Name: N_CYCLE
Property: Read

Bit	31	30	29	28	27	26	25	24
	N_CYCLE[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	N_CYCLE[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	N_CYCLE[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	N_CYCLE[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – N_CYCLE[31:0] Number of Samples in the Last Cycle (uQ20.12)
Fractional number of samples in the last cycle based on the zero-crossings of the dominant voltage channel.
Note: It is recommended to use this value for calculating the RMS value or the power of the Per-Cycle Accumulated Output Quantities.

3.2.16. Pulse Counters

Name: PULSEx_COUNTER
Property: Read

Bit	31	30	29	28	27	26	25	24
	PULSEx_COUNTER[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PULSEx_COUNTER[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PULSEx_COUNTER[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PULSEx_COUNTER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PULSEx_COUNTER[31:0] Pulse counters (uQ32.0)
The registers count the number of pulses generated by the available pulse outputs.

3.2.17. Zero-Crossing Sample Number of Phase-X Voltage

Name: ZC_N_Vx
Property: Read

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	ZC_COUNT_Vx[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ZC_COUNT_Vx[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ZC_COUNT_Vx[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – ZC_COUNT_Vx[23:0] Zero Crossing Count (uQ20.12)
Zero-crossing sample count of last positive-going zero-crossing of the V_x [x = A, B, C] phase voltage channel, in units of the 4 kHz sample rate. Use this to compare with other voltage phases to determine relative phase order.

3.2.18. ATSENSE Calibration Trim Data, Registers: 0x41 – 0x44

Name: ATSENSE_CAL_41_44
Property: Read

Bit	31	30	29	28	27	26	25	24
	TEMP_TL [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
					TEMP_TL [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	REF_TL [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
					REF_TL [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bits 31:24 – TEMP_TL [7:0]

Bits 19:16 – TEMP_TL [11:8] Temperature TL
The following rule applies to recover the real values of ADC_TEMP_OUT from the 12-bit coded values in the product registers.
ADC_TEMP_OUT[23:0] (TL) = TEMP_TL[11:0] << 12
Note: TEMP_TL[11:0] is a signed 12-bit integer.

Bits 15:8 – REF_TL [7:0]

Bits 3:0 – REF_TL [11:8] Reference Voltage
Reference Voltage measured at temperature TL.
VREF(TL) = 1.120V + REF_TL[11:0] * 25 µV

3.2.19. ATSENSE Calibration Trim Data, Registers: 0x45 – 0x48

Name: ATSENSE_CAL_45_48
Property: Read

Bit	31	30	29	28	27	26	25	24
	TEMP_TH [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
					TEMP_TH [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	REF_TH [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
					REF_TH [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bits 31:24 – TEMP_TH [7:0]

Bits 19:16 – TEMP_TH [11:8] Temperature TH
The following rule applies to recover the real values of ADC_TEMP_OUT from the 12-bit coded values in the product registers.
ADC_TEMP_OUT[23:0] (TH) = TEMP_TH[11:0] << 12
Note: TEMP_TH[11:0] is a signed 12-bit integer.

Bits 15:8 – REF_TH [7:0]

Bits 3:0 – REF_TH [11:8] Reference Voltage
Reference Voltage measured at temperature TH.
VREF(TH) = 1.120V + REF_TH[11:0] * 25 µV

3.3. Accumulated Output Quantities

The starting address is 0x200881E0. All values are integrated at an equivalent sampling rate of 4 kHz. The Metrology module generates the following primary output measurement quantities for each measurement interval. Each per-phase quantity is designated by the subscript "_x" (where x = [A, B, C, D] for voltage channels and x = [A, B, C or N] for current channels).

Table 3-5. Accumulated Output Quantities

Index	Address	Variable	Access Mode	Name	Format	No. Bytes	Min Value	Max Value	Default	Units
0	0x200881E0	V_A	R	Volt-squared-samples, phase-A, fundamental + harmonics	uQ24.40	8	—	—	—	Volt^{2}samp scaled
1	0x200881E8	V_B	R	Volt-squared-samples, phase-B, fundamental + harmonics	uQ24.40	8	—	—	—	Volt^{2}samp scaled
2	0x200881F0	V_C	R	Volt-squared-samples, phase-C, fundamental + harmonics	uQ24.40	8	—	—	—	Volt^{2}samp scaled
3	0x200881F8	V_D	R	Volt-squared-samples, phase-D, fundamental + harmonics	uQ24.40	8	—	—	—	Volt^{2}samp scaled
4	0x20088200	V_A_F	R	Volt-squared-samples, phase-A, fundamental only	uQ24.40	8	—	—	—	Volt^{2}samp scaled
5	0x20088208	V_B_F	R	Volt-squared-samples, phase-B, fundamental only	uQ24.40	8	—	—	—	Volt^{2}samp scaled
6	0x20088210	V_C_F	R	Volt-squared-samples, phase-C, fundamental only	uQ24.40	8	—	—	—	Volt^{2}samp scaled
7	0x20088218	V_D_F	R	Volt-squared-samples, phase-D, fundamental only	uQ24.40	8	—	—	—	Volt^{2}samp scaled
8	0x20088220	V_AB	R	Volt-squared-samples, VA – VB, fundamental + harmonics	uQ24.40	8	—	—	—	Volt^{2}samp scaled
9	0x20088228	V_BC	R	Volt-squared-samples, VB – VC, fundamental + harmonics	uQ24.40	8	—	—	—	Volt^{2}samp scaled
10	0x20088230	V_CA	R	Volt-squared-samples, VC – VA, fundamental + harmonics	uQ24.40	8	—	—	—	Volt^{2}samp scaled
11	0x20088238	V_AB_F	R	Volt-squared-samples, VA – VB, fundamental only	uQ24.40	8	—	—	—	Volt^{2}samp scaled
12	0x20088240	V_BC_F	R	Volt-squared-samples, VB – VC, fundamental only	uQ24.40	8	—	—	—	Volt^{2}samp scaled
13	0x20088248	V_CA_F	R	Volt-squared-samples, VC – VA, fundamental only	uQ24.40	8	—	—	—	Volt^{2}samp scaled
14	0x20088250	RESERVED	R	—	—	8	—	—	—	—
15	0x20088258	RESERVED	R	—	—	8	—	—	—	—
16	0x20088260	RESERVED	R	—	—	8	—	—	—	—
17	0x20088268	I_A	R	Amp-squared-samples, phase-A, fundamental + harmonics	uQ24.40	8	—	—	—	Amp^{2}samp scaled
18	0x20088270	I_B	R	Amp-squared-samples, phase-B, fundamental + harmonics	uQ24.40	8	—	—	—	Amp^{2}samp scaled
19	0x20088278	I_C	R	Amp-squared-samples, phase-C, fundamental + harmonics	uQ24.40	8	—	—	—	Amp^{2}samp scaled

Table 3-5. Accumulated Output Quantities (continued)

Index	Address	Variable	Access Mode	Name	Format	No. Bytes	Min Value	Max Value	Default	Units
20	0x20088280	I_Ni	R	Amp-squared-samples, phase-N imputed, fundamental + harmonics	uQ44.20	8	—	—	—	Amp^2samp
21	0x20088288	I_Nm	R	Amp-squared-samples, phase-N measured, fundamental + harmonics	uQ24.40	8	—	—	—	Amp^2samp scaled
22	0x20088290	I_A_F	R	Amp-squared-samples, phase-A, fundamental only	uQ24.40	8	—	—	—	Amp^2samp scaled
23	0x20088298	I_B_F	R	Amp-squared-samples, phase-B, fundamental only	uQ24.40	8	—	—	—	Amp^2samp scaled
24	0x200882A0	I_C_F	R	Amp-squared-samples, phase-C, fundamental only	uQ24.40	8	—	—	—	Amp^2samp scaled
25	0x200882A8	I_Nmi	R	Amp-squared-samples, raw phase-N measured minus imputed, fundamental + harmonics	uQ44.20	8	—	—	—	Amp^2samp
26	0x200882B0	I_Nm_F	R	Amp-squared-samples, phase-N, fundamental only	uQ24.40	8	—	—	—	Amp^2samp scaled
27	0x200882B8	RESERVED	R	—	—	8	—	—	—	—
28	0x200882C0	RESERVED	R	—	—	8	—	—	—	—
29	0x200882C8	RESERVED	R	—	—	8	—	—	—	—
30	0x200882D0	RESERVED	R	—	—	8	—	—	—	—
31	0x200882D8	RESERVED	R	—	—	8	—	—	—	—
32	0x200882E0	P_A	R	Watt-samples, phase-A, fundamental + harmonics	sQ23.40	8	—	—	—	W-samp scaled
33	0x200882E8	P_B	R	Watt-samples, phase-B, fundamental + harmonics	sQ23.40	8	—	—	—	W-samp scaled
34	0x200882F0	P_C	R	Watt-samples, phase-C, fundamental + harmonics	sQ23.40	8	—	—	—	W-samp scaled
35	0x200882F8	P_A_F	R	Watt-samples, phase-A, fundamental only	sQ23.40	8	—	—	—	W-samp scaled
36	0x20088300	P_B_F	R	Watt-samples, phase-B, fundamental only	sQ23.40	8	—	—	—	W-samp scaled
37	0x20088308	P_C_F	R	Watt-samples, phase-C, fundamental only	sQ23.40	8	—	—	—	W-samp scaled
38	0x20088310	P_N	R	Watt-samples, phase-N, fundamental + harmonics	sQ23.40	8	—	—	—	W-samp scaled
39	0x20088318	P_N_F	R	Watt-samples, phase-N, fundamental only	sQ23.40	8	—	—	—	W-samp scaled
40	0x20088320	RESERVED	R	—	—	8	—	—	—	—
41	0x20088328	Q_A	R	VAR-samples, phase-A, fundamental + harmonics	sQ23.40	8	—	—	—	VAR-samp scaled

Table 3-5. Accumulated Output Quantities (continued)

Index	Address	Variable	Access Mode	Name	Format	No. Bytes	Min Value	Max Value	Default	Units
42	0x20088330	Q_B	R	VAR-samples, phase-B, fundamental + harmonics	sQ23.40	8	—	—	—	VAR-samp scaled
43	0x20088338	Q_C	R	VAR-samples, phase-C, fundamental + harmonics	sQ23.40	8	—	—	—	VAR-samp scaled
44	0x20088340	Q_A_F	R	VAR-samples, phase-A, fundamental only	sQ23.40	8	—	—	—	VAR-samp scaled
45	0x20088348	Q_B_F	R	VAR-samples, phase-B, fundamental only	sQ23.40	8	—	—	—	VAR-samp scaled
46	0x20088350	Q_C_F	R	VAR-samples, phase-C, fundamental only	sQ23.40	8	—	—	—	VAR-samp scaled
47	0x20088358	Q_N	R	VAR-samples, phase-N, fundamental + harmonics	sQ23.40	8	—	—	—	VAR-samp scaled
48	0x20088360	Q_N_F	R	VAR-samples, phase-N, fundamental only	sQ23.40	8	—	—	—	VAR-samp scaled
49	0x20088368	RESERVED	R	—	—	8	—	—	—	—
50	0x20088370	ACC_T0	R	Total accumulated quantities specified by PC0_TYPE	sQ33.30	8	—	—	—	Wh, VArh, VAh, Amp^{2}h
51	0x20088378	ACC_T1	R	Total accumulated quantities specified by PC1_TYPE	sQ33.30	8	—	—	—	Wh, VArh, VAh, Amp^{2}h
52	0x20088380	ACC_T2	R	Total accumulated quantities specified by PC2_TYPE	sQ33.30	8	—	—	—	Wh, VArh, VAh, Amp^{2}h
53	0x20088388	RESERVED	R	—	—	8	—	—	—	—
54	0x20088390	RESERVED	R	—	—	8	—	—	—	—

3.3.1. Accumulated Phase Voltage Quantities

Name: V_A, V_B, V_C, V_D, V_A_F, V_B_F, V_C_F, V_D_F
Property: Read

The metrology module generates the following accumulated phase voltage (V^2) quantities: V_A, V_B, V_C, V_D, V_A_F, V_B_F, V_C_F, and V_D_F.

They are in units of [$Volt^2$samp scaled]. They are scaled accumulated phase voltage quantities in the whole integration period. They are calculated according to the following formula:

$$V\_x = \sum_{i=1}^{N} (V\_x\_sample_i)^2$$

Where,

- $V\_x\_sample_i$ is i^{th} sampled phase voltage value of phase x in present integration period
- x = [A, B, C, D]
- N = The number of samples in the last measurement interval

They may be used to calculate the RMS value of phase voltage.

The V_x and V_x_F are stored in the uQ24.40 format.

Note: V_D, available only when using an MCP3914 AFE or 4 MC3910s, provides an additional ADC conversion for the application. The metrology library processes this channel with all metrology filters except for phase correction. This includes the calibration gain and the DC block filter, in case VC_DC_EN is cleared.

Bit	63	62	61	60	59	58	57	56
	V_x/V_x_F[63:56]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	55	54	53	52	51	50	49	48
	V_x/V_x_F[55:48]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	47	46	45	44	43	42	41	40
	V_x/V_x_F[47:40]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	39	38	37	36	35	34	33	32
	V_x/V_x_F[39:32]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	31	30	29	28	27	26	25	24
	V_x/V_x_F[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	V_x/V_x_F[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	V_x/V_x_F[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	V_x/V_x_F[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 63:0 – V_x/V_x_F[63:0] Volt-squared-samples, phase-x (uQ24.40)

3.3.2. Accumulated Voltage Quantities Between Phases

Name: V_AB, V_BC, V_CA, V_AB_F, V_BC_F, V_CA_F
Property: Read

The metrology module generates the following accumulated phase voltage (V^2) quantities between phases: V_AB, V_BC, V_CA, V_AB_F, V_BC_F, and V_CA_F.

They are in units of [$Volt^2$samp scaled]. They are scaled accumulated voltage quantities between phases in the whole integration period. They are calculated according to the following formula:

$$V\_xy = \sum_{i=1}^{N} (V\_y\_sample_i - V\_x\_sample_i) * (V\_y\_sample_i - V\_x\_sample_i)$$

Where,

- $V\_x\_sample_i$ is i^{th} sampled phase voltage value of phase x in present integration period
- $V\_y\_sample_i$ is i^{th} sampled phase voltage value of phase y in present integration period
- x = [A, B, C]
- y = [B, C, A]
- N = The number of samples in the last measurement interval

They are used to calculate the RMS value of voltage between phases.

The V_xy and V_xy_F are stored in the uQ24.40 format.

These accumulators are useful for calculating the phase shift between voltages by applying the Law of Cosines. Depending on the application requirements, it can be utilized either the fundamental plus harmonics or the fundamental only, ended in "_F", registers.

The following numerical example demonstrates the angle computation:

- Data from Metrology Accumulator Registers:
  - V_A: 0x15219DA3DFFC
  - V_B: 0x1521A8F07EDF
  - V_C: 0x1522518EAC3A
  - V_AB: 0x3F63899CA42A
  - V_BC: 0x3F67221A3C5C
  - V_CA: 0x3F661B94C8D4
- The units of these registers are in $Volt^2$ samp scaled, with the uQ24.40 format. To convert these to decimal values, divide by 2^{40}:
  - V_A: 21.13131165
  - V_B: 21.13148406
  - V_C: 21.13405697
  - V_AB: 63.38881854
  - V_BC: 63.40286411
  - V_CA: 63.39885836
- Application of the Law of Cosines:
  - Angle between phase A and phase B (AB_phase):
    AB_phase = arccos ((V_AB - V_A - V_B) / (-2 * sqrt(V_A * V_B)) = 119.992º
  - Angle between phase B and phase C (BC_phase):
    BC_phase = arccos ((V_BC - V_B - V_C) / (-2 * sqrt(V_B * V_C)) = 120.007º

– Angle between phase C and phase A (CA_phase):
CA_phase = arccos ((V_CA - V_A - V_C) / (-2 * sqrt(V_A * V_C)) = 120.001°

In cases where the arccos function is ambiguous (typically when the phase shift approaches 180°), the ZC_NV_x registers can be used to select between the two possible angles.

Bit	63	62	61	60	59	58	57	56
	V_xy/V_xy_F[63:56]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	55	54	53	52	51	50	49	48
	V_xy/V_xy_F[55:48]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	47	46	45	44	43	42	41	40
	V_xy/V_xy_F[47:40]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	39	38	37	36	35	34	33	32
	V_xy/V_xy_F[39:32]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	31	30	29	28	27	26	25	24
	V_xy/V_xy_F[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	V_xy/V_xy_F[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	V_xy/V_xy_F[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	V_xy/V_xy_F[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 63:0 – V_xy/V_xy_F[63:0] Volt-squared-samples, Vx-Vy (uQ24.40)

3.3.3. Accumulated Current Quantities

Name: I_A, I_B, I_C, I_Ni, I_Nm, I_Nmi, I_A_F, I_B_F, I_C_F, I_Nm_F
Property: Read

The metrology module generates the following accumulated current (I^2) quantities: I_A, I_B, I_C, I_Ni, I_Nm, I_Nmi, I_A_F, I_B_F, I_C_F, and I_Nm_F.

I_x, and I_x_F

These accumulators are in units of [Amp^2 samp scaled] in format [uQ24.40] and represent the accumulated scaled current quantities in the integration period. They are calculated according to the following formula:

$$I\_x = \sum_{i=1}^{N} (I\_x\_sample_i)^2$$

Where,

- $I\_x\_sample_i$ is i^{th} sampled current value of phase x in the present integration period
- x = [A, B, C]
- N = The number of samples in the last measurement interval

I_Nm, and I_Nm_F are the accumulator for measured neutral current. These accumulators are in units of [Amp^2samp scaled] in the uQ24.40 format.

In the case of being multiplexed with temperature measurement acquisition, such as when using the PIC32CXMTC with an external ATSENSE301, slightly less performance may be expected than DSP-filtered full bandwidth data, calculated according to the following formula:

$$I\_Nm = \sum_{i=1}^{N} (I\_Nm\_sample_i)^2$$

Where,

- $I\_Nm\_sample_i$ is i^{th} sampled measured neutral current value from current input I0 in the last integration period
- N = The number of samples in the last measurement interval

I_Ni, and I_Nmi

These neutral currents are unscaled in units of [Amp^2samp] and are computed directly from DSP-filtered baseband current channel data streams. These neutral currents are unscaled (not normalized by the K_Ix current sensor scale factors); therefore, these accumulators are all in units of (Amp^2samples) in the uQ44.20 format.

I_Ni is the accumulator for imputed neutral current using full bandwidth (fundamental + harmonics) DSP-filtered baseband current channel data calculated according to the following formulas:

$$I\_Ni\_sample_i = \sum_{x}^{A,B,C} I\_x\_sample_i$$

$$I\_Ni = \sum_{i=1}^{N} (I\_Ni\_sample_i)^2$$

Where,

- $I\_Ni\_sample_i$ is i^{th} sampled imputed neutral current value computed from the sum of all active current phase currents in the present integration period

- N = The number of samples in the last measurement interval

I_Nmi is the accumulator for the difference between the sample-by-sample measured and imputed neutral currents. This integration is sensitive to both magnitude and/or phase differences between the measured and imputed neutral currents, calculated according to the following formula:

$$I\_Nmi = \sum_{i=1}^{N} (I\_Nm\_sample_i - I\_Ni\_sample_i)^2$$

Where,

- $I\_Nm\_sample_i$ is i^{th} sampled measured neutral current
- $I\_Ni\_sample_i$ is i^{th} sampled imputed neutral current value computed from the sum of all active current phase inputs in the present integration period
- N = The number of samples in the last measurement interval

Bit	63	62	61	60	59	58	57	56
	I_x/I_x_F[63:56]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	55	54	53	52	51	50	49	48
	I_x/I_x_F[55:48]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	47	46	45	44	43	42	41	40
	I_x/I_x_F[47:40]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	39	38	37	36	35	34	33	32
	I_x/I_x_F[39:32]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	31	30	29	28	27	26	25	24
	I_x/I_x_F[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	I_x/I_x_F[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	I_x/I_x_F[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	I_x/I_x_F[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 63:0 – I_x/I_x_F[63:0] Amp-Squared-Samples, uQ24.40 (I_x, I_x_F, I_Nm, I_Nm_F), uQ44.20 (I_Ni, I_Nmi)

3.3.4. Accumulated Active Power Quantities

Name: P_A, P_B, P_C, P_A_F, P_B_F, P_C_F, P_N, P_N_F
Property: Read

The metrology module generates the following accumulated active power (P) quantities: P_A, P_B, P_C, P_A_F, P_B_F, P_C_F, P_N, and P_N_F.

They are in units of [W-samp scaled]. They are scaled accumulated active power quantities in the whole integration period. They are calculated according to the following formulas:

$$P\_x = \sum_{i=1}^{N} V\_x\_sample_i \times I\_x\_sample_i \qquad x = [A, B, C]$$

$$P\_x = \sum_{i=1}^{N} V\_avc\_sample_i \times I\_x\_sample_i \qquad x = [N]$$

Where,

- $V\_x\_sample_i$ is i^{th} sampled phase voltage value of phase x in present integration period
- $V\_avc\_sample_i$ is i^{th} sampled phase voltage value of the active voltage channel (according to STATE_FLAG.TIMING_Vx) in present integration period
- $I\_x\_sample_i$ is i^{th} sampled phase current value of phase x in present integration period
- x = [A, B, C, N]
- N = The number of samples in the last measurement interval

They are used to calculate the active power. In the case of the neutral channel, it is useful for calculating the angle of the neutral current.

The P_x and P_x_F are stored in the sQ23.40 format.

Bit	63	62	61	60	59	58	57	56
	P_x/P_x_F[63:56]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	55	54	53	52	51	50	49	48
	P_x/P_x_F[55:48]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	47	46	45	44	43	42	41	40
	P_x/P_x_F[47:40]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	39	38	37	36	35	34	33	32
	P_x/P_x_F[39:32]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	31	30	29	28	27	26	25	24
	P_x/P_x_F[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	P_x/P_x_F[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	P_x/P_x_F[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	P_x/P_x_F[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 63:0 – P_x/P_x_F[63:0] Watt-samples, phase-x (sQ23.40)

3.3.5. Accumulated Reactive Power Quantities

Name: Q_A, Q_B, Q_C, Q_A_F, Q_B_F, Q_C_F, Q_N, Q_N_F
Property: Read

The metrology module generates the following accumulated reactive power (Q) quantities: Q_A, Q_B, Q_C, Q_A_F, Q_B_F, Q_C_F, Q_N, and Q_N_F.

They are in units of [VAR samp-scaled]. They are scaled accumulated reactive power quantities in the whole integration period. They are calculated according to the following formula:

$$Q\_x = \sum_{i=1}^{N} V'\_x\_sample_i \times I''\_x\_sample_i \qquad x = [A, B, C]$$

$$Q\_x = \sum_{i=1}^{N} V'\_avc\_sample_i \times I''\_x\_sample_i \qquad x = [N]$$

Where,

- $V'\_x\_sample_i$ is i^{th} filtered phase voltage value of phase x in present integration period
- $V'\_avc\_sample_i$ is i^{th} filtered phase voltage value of the active voltage channel (according to STATE_FLAG.TIMING_Vx) in present integration period
- $I''\_x\_sample_i$ is i^{th} filtered phase current value of phase x in present integration period
- $V'\_x\_sample_i$, $V'\_avc\_sample_i$ and $I''\_x\_sample_i$ have additional 90 degree phase difference
- x = [A, B, C]
- N = The number of samples in the last measurement interval

They are used to calculate the reactive power. In the case of the neutral channel, it is useful for calculating the angle of the neutral current.

The Q_x and Q_x_F are stored in the sQ23.40 format.

Bit	63	62	61	60	59	58	57	56
	Q_x/Q_x_F[63:56]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	55	54	53	52	51	50	49	48
	Q_x/Q_x_F[55:48]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	47	46	45	44	43	42	41	40
	Q_x/Q_x_F[47:40]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	39	38	37	36	35	34	33	32
	Q_x/Q_x_F[39:32]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	31	30	29	28	27	26	25	24
	Q_x/Q_x_F[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	Q_x/Q_x_F[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	Q_x/Q_x_F[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	Q_x/Q_x_F[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 63:0 – Q_x/Q_x_F[63:0] VAR-Samples, Phase-X (sQ23.40)

3.3.6. Total Accumulated Quantities

Name: ACC_T0, ACC_T1, ACC_T2
Property: Read

The metrology module generates the following accumulated total quantities: ACC_T0, ACC_T1, and ACC_T2.

Total accumulated quantities are specified by PCx_TYPE. They are used to save the total accumulated energy. They are updated every full line cycle (20 ms for 50 Hz and 16.667 ms for 60 Hz).

They are stored in the sQ33.30 format. Maximum ±8589934 KWh/KVarh/KAmp^{2}h/KVAh can be stored in these quantities.

Before resetting the metrology firmware, the application must store present ACC_T0, ACC_T1 and ACC_T2. After resetting the metrology firmware, the application must restore ACC_T0, ACC_T1, and ACC_T2.

The ACC_Tx is stored in the sQ33.30 format.

⚠ WARNING Version 030400 improves the limits for pulse accumulation. In previous versions, if the energy accumulated in a cycle for any phase exceeded 0.5825 (Wh, VARh, Amp^2-h, or VAh), the ACC_TX accumulators and the pulse issue rate were incorrect. This limit corresponds to 125.8 kW at 60 Hz, which occurs with 1143.9A at 110V and a power factor of 1. Version 030400 increases this limit by a factor of 1024.

Bit	63	62	61	60	59	58	57	56
	ACC_Tx[63:56]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	55	54	53	52	51	50	49	48
	ACC_Tx[55:48]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	47	46	45	44	43	42	41	40
	ACC_Tx[47:40]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	39	38	37	36	35	34	33	32
	ACC_Tx[39:32]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	31	30	29	28	27	26	25	24
	ACC_Tx[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ACC_Tx[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ACC_Tx[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ACC_Tx[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 63:0 – ACC_Tx[63:0] Total Accumulated Quantities Specified by PCx_TYPE (sQ33.30)

3.4. Per-Cycle Accumulated Output Quantities

The starting address is 0x20088398. All values are integrated at an equivalent sampling rate of 4 kHz. The registers are updated upon detection of a positive zero-crossing in the dominant phase.

The Metrology module generates the following per-cycle output measurements.

Table 3-6. Per-Cycle Accumulated Output Quantities

Index	Address	Variable	Access Mode	Name	Format	No. Bytes	Min Value	Max Value	Default	Units
0	0x20088398	CYCLE_V_A	R	Per-cycle Volt-squared-samples, phase-A, fundamental + harmonics	uQ24.40	8	—	—	—	Volt²samp scaled
1	0x200883A0	CYCLE_V_B	R	Per-cycle Volt-squared-samples, phase-B, fundamental + harmonics	uQ24.40	8	—	—	—	Volt²samp scaled
2	0x200883A8	CYCLE_V_C	R	Per-cycle Volt-squared-samples, phase-C, fundamental + harmonics	uQ24.40	8	—	—	—	Volt²samp scaled
3	0x200883B0	CYCLE_V_A_F	R	Per-cycle Volt-squared-samples, phase-A, fundamental only	uQ24.40	8	—	—	—	Volt²samp scaled
4	0x200883B8	CYCLE_V_B_F	R	Per-cycle Volt-squared-samples, phase-B, fundamental only	uQ24.40	8	—	—	—	Volt²samp scaled
5	0x200883C0	CYCLE_V_C_F	R	Per-cycle Volt-squared-samples, phase-C, fundamental only	uQ24.40	8	—	—	—	Volt²samp scaled
6	0x200883C8	CYCLE_V_AB	R	Per-cycle Volt-squared-samples, VA – VB, fundamental + harmonics	uQ24.40	8	—	—	—	Volt²samp scaled
7	0x200883D0	CYCLE_V_BC	R	Per-cycle Volt-squared-samples, VB – VC, fundamental + harmonics	uQ24.40	8	—	—	—	Volt²samp scaled
8	0x200883D8	CYCLE_V_CA	R	Per-cycle Volt-squared-samples, VC – VA, fundamental + harmonics	uQ24.40	8	—	—	—	Volt²samp scaled
9	0x200883E0	CYCLE_V_AB_F	R	Per-cycle Volt-squared-samples, VA – VB, fundamental only	uQ24.40	8	—	—	—	Volt²samp scaled
10	0x200883E8	CYCLE_V_BC_F	R	Per-cycle Volt-squared-samples, VB – VC, fundamental only	uQ24.40	8	—	—	—	Volt²samp scaled
11	0x200883F0	CYCLE_V_CA_F	R	Per-cycle Volt-squared-samples, VC – VA, fundamental only	uQ24.40	8	—	—	—	Volt²samp scaled
12	0x200883F8	CYCLE_I_A	R	Per-cycle Amp-squared-samples, phase-A, fundamental + harmonics	uQ24.40	8	—	—	—	Amp²samp scaled
13	0x20088400	CYCLE_I_B	R	Per-cycle Amp-squared-samples, phase-B, fundamental + harmonics	uQ24.40	8	—	—	—	Amp²samp scaled
14	0x20088408	CYCLE_I_C	R	Per-cycle Amp-squared-samples, phase-C, fundamental + harmonics	uQ24.40	8	—	—	—	Amp²samp scaled
15	0x20088410	CYCLE_I_Nm	R	Per-cycle Amp-squared-samples, phase-N measured, fundamental + harmonics	uQ24.40	8	—	—	—	Amp²samp scaled
16	0x20088418	CYCLE_I_A_F	R	Per-cycle Amp-squared-samples, phase-A, fundamental only	uQ24.40	8	—	—	—	Amp²samp scaled
17	0x20088420	CYCLE_I_B_F	R	Per-cycle Amp-squared-samples, phase-B, fundamental only	uQ24.40	8	—	—	—	Amp²samp scaled

Table 3-6. Per-Cycle Accumulated Output Quantities (continued)

Index	Address	Variable	Access Mode	Name	Format	No. Bytes	Min Value	Max Value	Default	Units
18	0x20088428	CYCLE_I_C_F	R	Per-cycle Amp-squared-samples, phase-C, fundamental only	uQ24.40	8	—	—	—	Amp^2samp scaled
19	0x20088430	CYCLE_I_Nm_F	R	Per-cycle Amp-squared-samples, phase-N, fundamental only	uQ24.40	8	—	—	—	Amp^2samp scaled
20	0x20088438	CYCLE_P_A	R	Per-cycle Watt-samples, phase-A, fundamental + harmonics	sQ23.40	8	—	—	—	W-samp scaled
21	0x20088440	CYCLE_P_B	R	Per-cycle Watt-samples, phase-B, fundamental + harmonics	sQ23.40	8	—	—	—	W-samp scaled
22	0x20088448	CYCLE_P_C	R	Per-cycle Watt-samples, phase-C, fundamental + harmonics	sQ23.40	8	—	—	—	W-samp scaled
23	0x20088450	CYCLE_P_A_F	R	Per-cycle Watt-samples, phase-A, fundamental only	sQ23.40	8	—	—	—	W-samp scaled
24	0x20088458	CYCLE_P_B_F	R	Per-cycle Watt-samples, phase-B, fundamental only	sQ23.40	8	—	—	—	W-samp scaled
25	0x20088460	CYCLE_P_C_F	R	Per-cycle Watt-samples, phase-C, fundamental only	sQ23.40	8	—	—	—	W-samp scaled
26	0x20088468	CYCLE_P_N	R	Per-cycle Watt-samples, phase-N, fundamental + harmonics	sQ23.40	8	—	—	—	W-samp scaled
27	0x20088470	CYCLE_P_N_F	R	Per-cycle Watt-samples, phase-N, fundamental only	sQ23.40	8	—	—	—	W-samp scaled
28	0x20088478	CYCLE_Q_A	R	Per-cycle VAR-samples, phase-A, fundamental + harmonics	sQ23.40	8	—	—	—	VAR-samp scaled
29	0x20088480	CYCLE_Q_B	R	Per-cycle VAR-samples, phase-B, fundamental + harmonics	sQ23.40	8	—	—	—	VAR-samp scaled
30	0x20088488	CYCLE_Q_C	R	Per-cycle VAR-samples, phase-C, fundamental + harmonics	sQ23.40	8	—	—	—	VAR-samp scaled
31	0x20088490	CYCLE_Q_A_F	R	Per-cycle VAR-samples, phase-A, fundamental only	sQ23.40	8	—	—	—	VAR-samp scaled
32	0x20088498	CYCLE_Q_B_F	R	Per-cycle VAR-samples, phase-B, fundamental only	sQ23.40	8	—	—	—	VAR-samp scaled
33	0x200884A0	CYCLE_Q_C_F	R	Per-cycle VAR-samples, phase-C, fundamental only	sQ23.40	8	—	—	—	VAR-samp scaled
34	0x200884A8	CYCLE_Q_N	R	Per-cycle VAR-samples, phase-N, fundamental + harmonics	sQ23.40	8	—	—	—	VAR-samp scaled
35	0x200884B0	CYCLE_Q_N_F	R	Per-cycle VAR-samples, phase-N, fundamental only	sQ23.40	8	—	—	—	VAR-samp scaled

3.4.1. Per-Cycle Accumulated Phase Voltage Quantities

Name: CYCLE_V_A, CYCLE_V_B, CYCLE_V_C, CYCLE_V_A_F, CYCLE_V_B_F, CYCLE_V_C_F
Property: Read

The metrology module generates the following accumulated phase voltage (V^2) quantities: CYCLE_V_A, CYCLE_V_B, CYCLE_V_C, CYCLE_V_A_F, CYCLE_V_B_F, and CYCLE_V_C_F.

They are in units of [Volt^{2}samp scaled]. They are scaled accumulated phase voltage quantities in the last line cycle measurement period. They are calculated according to the following formula:

$$CYCLE\_V\_x = \sum_{i=1}^{N} (V\_x\_sample_i)^2$$

Where,

- $V\_x\_sample_i$ is ith sampled phase voltage value of phase x in present cycle
- x = [A, B, C]
- N = The number of samples in the last line cycle measurement interval

They may be used to calculate the RMS value of phase voltage.

The CYCLE_V_x and CYCLE_V_x_F are stored in the uQ24.40 format.

Bit	63	62	61	60	59	58	57	56
	CYCLE_V_x/CYCLE_V_x_F[63:56]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	55	54	53	52	51	50	49	48
	CYCLE_V_x/CYCLE_V_x_F[55:48]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	47	46	45	44	43	42	41	40
	CYCLE_V_x/CYCLE_V_x_F[47:40]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	39	38	37	36	35	34	33	32
	CYCLE_V_x/CYCLE_V_x_F[39:32]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	31	30	29	28	27	26	25	24
	CYCLE_V_x/CYCLE_V_x_F[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CYCLE_V_x/CYCLE_V_x_F[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CYCLE_V_x/CYCLE_V_x_F[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CYCLE_V_x/CYCLE_V_x_F[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 63:0 – CYCLE_V_x/CYCLE_V_x_F[63:0] Per-cycle Volt-squared-samples, phase-x (uQ24.40)

3.4.2. Per-Cycle Accumulated Voltage Quantities Between Phases

Name: CYCLE_V_AB, CYCLE_V_BC, CYCLE_V_CA, CYCLE_V_AB_F, CYCLE_V_BC_F, CYCLE_V_CA_F
Property: Read

The metrology module generates the following accumulated phase voltage (V^2) quantities between phases: CYCLE_V_AB, CYCLE_V_BC, CYCLE_V_CA, CYCLE_V_AB_F, CYCLE_V_BC_F, and CYCLE_V_CA_F.

They are in units of [$Volt^2$samp scaled]. They are scaled accumulated voltage quantities between phases in the last line cycle measurement period. They are calculated according to the following formula:

$$CYCLE\_V\_xy = \sum_{i=1}^{N} (V\_y\_sample_i - V\_x\_sample_i) \cdot (V\_y\_sample_i - V\_x\_sample_i)$$

Where,

- $V\_x\_sample_i$ is i^{th} sampled phase voltage value of phase x in present cycle
- $V\_y\_sample_i$ is i^{th} sampled phase voltage value of phase y in present cycle
- x = [A, B, C]
- y = [B, C, A]
- N = The number of samples in the last line cycle measurement interval

They are used to calculate the RMS value of voltage between phases.

The V_xy and V_xy_F are stored in the uQ24.40 format.

These accumulators are useful for calculating the phase shift between voltages by applying the Law of Cosines. Depending on the application requirements, it can be utilized either the fundamental plus harmonics or the fundamental only, ended in the "_F", registers.

Bit	63	62	61	60	59	58	57	56
	CYCLE_V_xy/CYCLE_V_xy_F[63:56]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	55	54	53	52	51	50	49	48
	CYCLE_V_xy/CYCLE_V_xy_F[55:48]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	47	46	45	44	43	42	41	40
	CYCLE_V_xy/CYCLE_V_xy_F[47:40]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	39	38	37	36	35	34	33	32
	CYCLE_V_xy/CYCLE_V_xy_F[39:32]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	31	30	29	28	27	26	25	24
	CYCLE_V_xy/CYCLE_V_xy_F[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CYCLE_V_xy/CYCLE_V_xy_F[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CYCLE_V_xy/CYCLE_V_xy_F[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CYCLE_V_xy/CYCLE_V_xy_F[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 63:0 – CYCLE_V_xy/CYCLE_V_xy_F[63:0] Per-cycle Volt-squared-samples, Vx-Vy (uQ24.40)

3.4.3. Per-Cycle Accumulated Current Quantities

Name: CYCLE_I_A, CYCLE_I_B, CYCLE_I_C, CYCLE_I_Nm, CYCLE_I_A_F, CYCLE_I_B_F, CYCLE_I_C_F, CYCLE_I_Nm_F
Property: Read

Depending on the AFE selected, the metrology module generates the following accumulated current (I^2) quantities: CYCLE_I_A, CYCLE_I_B, CYCLE_I_C, CYCLE_I_Nm, CYCLE_I_A_F, CYCLE_I_B_F, CYCLE_I_C_F, and CYCLE_I_Nm_F.

CYCLE_I_x, CYCLE_I_x_F

These accumulators are in units of [Amp^2 samp scaled] in the [uQ24.40] format and represent the accumulated scaled current in the last line cycle measurement period. They are calculated according to the following formula:

$$CYCLE\_I\_x = \sum_{i=1}^{N} (I\_x\_sample_i)^2$$

Where,

- $I\_x\_sample_i$ is i^{th} sampled current value of phase x in the present cycle
- x = [A, B, C, A_F, B_F, C_F]
- N = The number of samples in the last cycle

CYCLE_I_Nm, CYCLE_I_Nm_F

These accumulators are in units of [Amp^2 samp scaled] in the uQ24.40 format and represent the accumulated scaled neutral current in the last line cycle measurement period. They are calculated according to the following formula:

$$CYCLE\_I\_x = \sum_{i=1}^{N} (I\_x\_sample_i)^2$$

Where,

- $I\_x\_sample_i$ is i^{th} sampled neutral current value in the present cycle
- x = [Nm, Nm_F]
- N = The number of samples in the last cycle

In the case of being multiplexed with temperature measurement acquisition, such as when using the PIC32CXMTC with an external ATSENSE301, slightly less performance may be expected than DSP-filtered full bandwidth data.

Bit	63	62	61	60	59	58	57	56
	CYCLE_I_x/CYCLE_I_x_F/CYCLE_I_Nm/CYCLE_I_Nm_F[63:56]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	55	54	53	52	51	50	49	48
	CYCLE_I_x/CYCLE_I_x_F/CYCLE_I_Nm/CYCLE_I_Nm_F[55:48]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	47	46	45	44	43	42	41	40
	CYCLE_I_x/CYCLE_I_x_F/CYCLE_I_Nm/CYCLE_I_Nm_F[47:40]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	39	38	37	36	35	34	33	32
	CYCLE_I_x/CYCLE_I_x_F/CYCLE_I_Nm/CYCLE_I_Nm_F[39:32]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	31	30	29	28	27	26	25	24
	CYCLE_I_x/CYCLE_I_x_F/CYCLE_I_Nm/CYCLE_I_Nm_F[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CYCLE_I_x/CYCLE_I_x_F/CYCLE_I_Nm/CYCLE_I_Nm_F[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CYCLE_I_x/CYCLE_I_x_F/CYCLE_I_Nm/CYCLE_I_Nm_F[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CYCLE_I_x/CYCLE_I_x_F/CYCLE_I_Nm/CYCLE_I_Nm_F[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 63:0 – CYCLE_I_x/CYCLE_I_x_F/CYCLE_I_Nm/CYCLE_I_Nm_F[63:0] Amp-squared-samples, (uQ24.40)

3.4.4. Per-Cycle Accumulated Active Power Quantities

Name: CYCLE_P_A, CYCLE_P_B, CYCLE_P_C, CYCLE_P_A_F, CYCLE_P_B_F, CYCLE_P_C_F, CYCLE_P_N, CYCLE_P_N_F
Property: Read

The metrology module generates the following accumulated active power (P) quantities: CYCLE_P_A, CYCLE_P_B, CYCLE_P_C, CYCLE_P_A_F, CYCLE_P_B_F, CYCLE_P_C_F, CYCLE_P_N, CYCLE_P_N_F.

They are in units of [W-samp scaled]. They are scaled accumulated active power quantities in the last line cycle measurement period. They are calculated according to the following formulas:

$$CYCLE\_P\_x = \sum_{i=1}^{N} V\_x\_sample_i * I\_x\_sample_i \quad \text{x = [A, B, C, A\_F, B\_F, C\_F]}$$

$$CYCLE\_P\_x = \sum_{i=1}^{N} V\_avc\_sample_i * I\_x\_sample_i \quad \text{x = [N, N\_F]}$$

Where,

- $V\_x\_sample_i$ is i^{th} sampled phase voltage value of phase x in present cycle
- $V\_avc\_sample_i$ is i^{th} sampled phase voltage value of the active voltage channel (according to STATE_FLAG.TIMING_Vx) in present cycle
- $I\_x\_sample_i$ is i^{th} sampled phase current value of phase x in present cycle
- N = The number of samples in the last cycle

They are used to calculate the active power. In the case of the neutral channel, it is useful for calculating the angle of the neutral current.

The CYCLE_P_x and CYCLE_P_x_F are stored in the sQ23.40 format.

Bit	63	62	61	60	59	58	57	56
	CYCLE_P_x/CYCLE_P_x_F[63:56]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	55	54	53	52	51	50	49	48
	CYCLE_P_x/CYCLE_P_x_F[55:48]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	47	46	45	44	43	42	41	40
	CYCLE_P_x/CYCLE_P_x_F[47:40]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	39	38	37	36	35	34	33	32
	CYCLE_P_x/CYCLE_P_x_F[39:32]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	31	30	29	28	27	26	25	24
	CYCLE_P_x/CYCLE_P_x_F[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CYCLE_P_x/CYCLE_P_x_F[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CYCLE_P_x/CYCLE_P_x_F[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CYCLE_P_x/CYCLE_P_x_F[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 63:0 – CYCLE_P_x/CYCLE_P_x_F[63:0] Watt-samples, phase-x (sQ23.40)

3.4.5. Per-Cycle Accumulated Reactive Power Quantities

Name: CYCLE_Q_A, CYCLE_Q_B, CYCLE_Q_C, CYCLE_Q_A_F, CYCLE_Q_B_F, CYCLE_Q_C_F, CYCLE_Q_N, CYCLE_Q_N_F
Property: Read

The metrology module generates the following accumulated reactive power (Q) quantities: CYCLE_Q_A, CYCLE_Q_B, CYCLE_Q_C, CYCLE_Q_A_F, CYCLE_Q_B_F, CYCLE_Q_C_F, CYCLE_Q_N, CYCLE_Q_N_F.

They are in units of [VAR samp-scaled]. They are scaled accumulated reactive power quantities in the last line cycle measurement period. They are calculated according to the following formulas:

$$CYCLE\_Q\_x = \sum_{i=1}^{N} V'\_x\_sample_i * I''\_x\_sample_i \quad \text{x = [A, B, C, A\_F, B\_F, C\_F]}$$

$$CYCLE\_Q\_x = \sum_{i=1}^{N} V'\_avc\_sample_i * I''\_x\_sample_i \quad \text{x = [N, N\_F]}$$

Where,

- $V'\_x\_sample_i$ is i^{th} filtered phase voltage value of phase x in present cycle
- $V'\_avc\_sample_i$ is i^{th} filtered phase voltage value of the active voltage channel (according to STATE_FLAG.TIMING_Vx) in present cycle
- $I''\_x\_sample_i$ is i^{th} filtered phase current value of phase x in present cycle
- $V'\_x\_sample_i$, $V'\_avc\_sample_i$ and $I''\_x\_sample_i$ have additional 90 degree phase difference
- N = The number of samples in the last cycle

They are used to calculate the reactive power. In the case of the neutral channel, it is useful for calculating the angle of the neutral current.

The CYCLE_Q_x and CYCLE_Q_x_F are stored in the sQ23.40 format.

Bit	63	62	61	60	59	58	57	56
	CYCLE_Q_x/CYCLE_Q_x_F[63:56]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	55	54	53	52	51	50	49	48
	CYCLE_Q_x/CYCLE_Q_x_F[55:48]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	47	46	45	44	43	42	41	40
	CYCLE_Q_x/CYCLE_Q_x_F[47:40]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	39	38	37	36	35	34	33	32
	CYCLE_Q_x/CYCLE_Q_x_F[39:32]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	31	30	29	28	27	26	25	24
	CYCLE_Q_x/CYCLE_Q_x_F[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CYCLE_Q_x/CYCLE_Q_x_F[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CYCLE_Q_x/CYCLE_Q_x_F[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CYCLE_Q_x/CYCLE_Q_x_F[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 63:0 – CYCLE_Q_x/CYCLE_Q_x_F[63:0] VAR-samples, phase-x (sQ23.40)

3.5. Harmonic Analysis Output Quantities

The starting address is 0x200884B8. The Metrology module generates the following primary output measurement quantities for each measurement interval, per-phase quantities with each phase designated by the subscript "_x" (where x = [A, B, C] for voltage channels and x = [A, B, C, N] for current channels).

Internal scaling allows accurate harmonic analysis for integration periods of up to 16 seconds for up to full-scale magnitude input waveforms.

Table 3-7. Harmonic Analysis Output Registers

Index	Address	Variable	Access Mode	Name	Format	No. Bytes	Min Value	Max Value	Default	Units
0-30	0x200884B8 - 0x20088530	I_A_m_R	R	The real part of DFT result for current, phase A, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Amp samp scaled
31-61	0x20088534 - 0x200885AC	V_A_m_R	R	The real part of DFT result for voltage, phase A, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Volt samp scaled
62-92	0x200885B0 - 0x20088628	I_B_m_R	R	The real part of DFT result for current, phase B, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Amp samp scaled
93-123	0x2008862C - 0x200886A4	V_B_m_R	R	The real part of DFT result for voltage, phase B, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Volt samp scaled
124-154	0x200886A8 - 0x20088720	I_C_m_R	R	The real part of DFT result for current, phase C, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Amp samp scaled
155-185	0x20088724 - 0x2008879C	V_C_m_R	R	The real part of DFT result for voltage, phase C, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Volt samp scaled
186-216	0x200887A0 - 0x20088818	I_N_m_R	R	The real part of DFT result for current, phase N (neutral), m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Amp samp scaled
217-247	0x2008881C - 0x20088894	I_A_m_I	R	The imaginary part of DFT result for current, phase A, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Amp samp scaled
248-278	0x20088898 - 0x20088910	V_A_m_I	R	The imaginary part of DFT result for voltage, phase A, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Volt samp scaled
279-309	0x20088914 - 0x2008898C	I_B_m_I	R	The imaginary part of DFT result for current, phase B, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Amp samp scaled
310-340	0x2008899A - 0x20088A08	V_B_m_I	R	The imaginary part of DFT result for voltage, phase B, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Volt samp scaled
341-371	0x20088A0C - 0x20088A84	I_C_m_I	R	The imaginary part of DFT result for current, phase C, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Amp samp scaled
372-402	0x20088A88 - 0x20088B00	V_C_m_I	R	The imaginary part of DFT result for voltage, phase C, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Volt samp scaled
403-433	0x20088B04 - 0x20088B7C	I_N_m_I	R	The imaginary part of DFT result for current, phase N (neutral), m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Amp samp scaled

3.5.1. Harmonic Analysis Output Quantities

Name: I_x_m_R, I_x_m_I, V_x_m_R, V_x_m_I
Property: Read

The metrology module generates the following quantities to calculate appointed *m-th* order harmonic current RMS: I_A_m_R, I_A_m_I, I_B_m_R, I_B_m_I, I_C_m_R, I_C_m_I, I_N_m_R, and I_N_m_I.

I_x_m_R is the real part of DFT of phase x current, x = [A, B, C, N].

I_x_m_I is imaginary part of DFT of phase x current, x = [A, B, C, N].

I_x_m_R and I_x_m_I are stored in the sQ13.18 format.

Where, m is the harmonic order number from 1 to 31.

The following formula is used to calculate the current RMS value of each phase:

$$I_{RMS\_x\_m} = \frac{\sqrt{2} \times \sqrt{\left(\frac{I\_x\_m\_Rx \times K\_Ix}{2^{18}}\right)^2 + \left(\frac{I\_x\_m\_I \times K\_Ix}{2^{18}}\right)^2}}{\mathrm{N}} = \frac{\sqrt{2 \times \left((I\_x\_m\_Rx \times K\_Ix)^2 + (I\_x\_m\_I \times K\_Ix)^2\right)}}{2^{18} \times \mathrm{N}} [A_{rms}]$$

Where,

- x = [A, B, C, N]
- N = The number of samples in the last measurement interval

The metrology module generates the following quantities to calculate appointed *m-th* order harmonic voltage RMS: V_A_m_R, V_A_m_I, V_B_m_R, V_B_m_I, V_C_m_R, and V_C_m_I.

V_x_m_R is the real part of DFT of phase x voltage, x = [A, B, C].

V_x_m_I is imaginary part of DFT of phase x voltage, x = [A, B, C].

V_x_m_R and V_x_m_I are stored in the sQ13.18 format.

Where, m is the harmonic order number from 1 to 31.

The following formula is used to calculate the voltage RMS value of each phase:

$$V_{RMS\_x\_m} = \frac{\sqrt{2} \times \sqrt{\left(\frac{V\_x\_m\_R \times K\_Vx}{2^{18}}\right)^2 + \left(\frac{V\_x\_m\_I \times K\_Vx}{2^{18}}\right)^2}}{\mathrm{N}} = \frac{\sqrt{2 \times \left((V\_x\_m\_R \times K\_Vx)^2 + (V\_x\_m\_I \times K\_Vx)^2\right)}}{2^{18} \times \mathrm{N}} [V_{rms}]$$

Where,

x = [A, B, C]

N = The number of samples in the last measurement interval

Bit	31	30	29	28	27	26	25	24
	I_x_m_R/I_x_m_I/V_x_m_R/V_x_m_I[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	I_x_m_R/I_x_m_I/V_x_m_R/V_x_m_I[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	I_x_m_R/I_x_m_I/V_x_m_R/V_x_m_I[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	I_x_m_R/I_x_m_I/V_x_m_R/V_x_m_I[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – I_x_m_R/I_x_m_I/V_x_m_R/V_x_m_I[31:0] Current/Voltage, phase-x, m-th harmonics (sQ13.18)

3.6. Derived Output Quantities

Using Metrology module primary output quantities, the following quantities of interest (per-phase or system) may be derived, using the formulae indicated in the following sections.

Note: Care must be exercised when using RMS values with integrated values, depending on the length of the integration period.

3.6.1. RMS Value

Total three kinds of RMS values can be calculated directly from the output of metrology firmware: RMS value of all harmonics, RMS value of fundamental harmonic and the RMS value of *m-th* harmonic.

RMS value of all harmonics and RMS value of fundamental harmonic can be calculated as following:

$$I\_x_{rms} = \frac{K\_Ix}{2^{10}} \times \sqrt{\frac{ACC\_I\_x}{N \times 2^{40}}}$$

$$V\_x_{rms} = \frac{K\_Vx}{2^{10}} \times \sqrt{\frac{ACC\_V\_x}{N \times 2^{40}}}$$

$$I\_x_{1\,rms} = \frac{K\_Ix}{2^{10}} \times \sqrt{\frac{ACC\_I\_x\_F}{N \times 2^{40}}}$$

$$V\_x_{1\,rms} = \frac{K\_Vx}{2^{10}} \times \sqrt{\frac{ACC\_V\_x\_F}{N \times 2^{40}}}$$

Where, x = [A, B, C], and:

- *K_Ix* is the current conversion factor of phase x
- *K_Vx* is the voltage conversion factor
- I_x_{rms} is the fundamental and all harmonics current RMS value

- V_x_{rms} is the fundamental and all harmonics voltage RMS value
- I_x_{1rms} is the fundamental harmonic current RMS value
- V_x_{1rms} is the fundamental harmonic voltage RMS value
- *N* is the number of samples in the integration period
- *ACC_I_x* is the accumulated fundamental and all harmonics current quantity
- *ACC_V_x* is the accumulated fundamental and all harmonics voltage quantity
- *ACC_I_x_F* is the accumulated fundamental harmonic current quantity
- *ACC_V_x_F* is the accumulated fundamental harmonic voltage quantity

Notes:

- *K_Ix* and *K_Vx* are the register values in the metrology control registers.
- *N* is the register value in the metrology status registers.
- *ACC_I_x*, *ACC_V_x*, *ACC_I_x_F* and *ACC_V_x_F* are the register values in the metrology accumulated output quantities.

After the harmonic analysis feature is enabled, RMS value of *m-th* harmonic can be calculated:

$$I_{RMS\_x\_m} = \frac{\sqrt{2} \times \sqrt{\left(\frac{I\_x\_m\_R}{2^6}\right)^2 + \left(\frac{I\_x\_m\_I}{2^6}\right)^2}}{N} = \frac{\sqrt{2 \times ((I\_x\_m\_R)^2 + (I\_x\_m\_I)^2)}}{2^6 \times N} [A_{rms}]$$

$$V_{RMS\_x\_m} = \frac{\sqrt{2} \times \sqrt{\left(\frac{V\_x\_m\_R}{2^6}\right)^2 + \left(\frac{V\_x\_m\_I}{2^6}\right)^2}}{N} = \frac{\sqrt{2 \times ((V\_x\_m\_R)^2 + (V\_x\_m\_I)^2)}}{2^6 \times N} [V_{rms}]$$

Where, x = [A, B, C], and:

- $I\_x_{m\ rms}$ is the *m-th* harmonic current RMS value of phase x
- $V\_x_{m\ rms}$ is the *m-th* harmonic voltage RMS value
- *I_x_m_R* is the real part of DFT for m-th harmonic current
- *I_x_m_I* is the imaginary part of DFT for m-th harmonic current
- *V_x_m_R* is the real part of DFT for m-th harmonic voltage
- *V_x_m_I* is the imaginary part of DFT for m-th harmonic voltage

Notes:

- I_x_m_R I_x_m_I, V_x_m_R and V_x_m_I are the register values in metrology harmonic analysis output quantities
- The voltage/current RMS value is updated every one integration period. INTEGRATION_IRQ will be generated at the end of integration period and this interrupt can be used to update derived quantities.

3.6.2. THD

Due to the limit of the code size, THD is not provided directly by the metrology firmware. However, it can be computed by the following formulas:

$$THD_I = \frac{1}{I_1}\sqrt{\sum_{h=2}^{\infty} I_h^2} = \sqrt{\left(\frac{I_{rms}}{I_{1rms}}\right)^2 - 1}$$

$$THD_V = \frac{1}{V_1}\sqrt{\sum_{h=2}^{\infty} V_h^2} = \sqrt{\left(\frac{V_{rms}}{V_{1rms}}\right)^2 - 1}$$

Where,

- I_1 is the amplitude of fundamental harmonic current
- V_1 is the amplitude of fundamental harmonic voltage
- I_{rms} is the all harmonics current RMS value
- V_{rms} is the all harmonics voltage RMS value
- $I_{1\ rms}$ is the fundamental harmonic current RMS value
- $V_{1\ rms}$ is the fundamental harmonic voltage RMS value

3.6.3. Energy/Quadergy

Energy and quadergy over the integration period can be calculated from the metrology output registers:

$$P\_x = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{1}{3600 \times f_s} \times \frac{ACC\_P\_x}{2^{40}}\ [Wh]$$

$$Q\_x = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{1}{3600 \times f_s} \times \frac{ACC\_Q\_x}{2^{40}}\ [VARh]$$

$$S\_x = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{1}{3600 \times f_s} \times \sqrt{\frac{ACC\_I\_x}{2^{40}}} \times \sqrt{\frac{ACC\_V\_x}{2^{40}}}\ [VAh]$$

$$P\_x_F = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{1}{3600 \times f_s} \times \frac{ACC\_P\_x\_F}{2^{40}}\ [Wh]$$

$$Q\_x_F = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{1}{3600 \times f_s} \times \frac{ACC\_Q\_x\_F}{2^{40}}\ [VARh]$$

$$S\_x_F = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{1}{3600 \times f_s} \times \sqrt{\frac{ACC\_I\_x\_F}{2^{40}}} \times \sqrt{\frac{ACC\_V\_x\_F}{2^{40}}}\ [VAh]$$

Where,

- x = [A, B, C]
- f_s = 4000 Hz is the output integration sample rate
- *P_x* is active power of all harmonics of phase x
- *Q_x* is reactive power of all harmonics
- *S_x* is apparent power of phase x

- *P_x_F* is active power of fundamental harmonic
- *Q_x_F* is reactive power of fundamental harmonic
- *S_x_F* is fundamental apparent power of phase x
- *ACC_P_x* is the accumulated active power quantity for all harmonics
- *ACC_Q_x* is the accumulated reactive power quantity for all harmonics
- *ACC_P_x_F* is the accumulated active power quantity for fundamental harmonic
- *ACC_Q_x_F* is the accumulated reactive power quantity for fundamental harmonic
- *ACC_I_x* is the accumulated fundamental and all harmonics current quantity
- *ACC_V_x* is the accumulated fundamental and all harmonics voltage quantity
- *ACC_I_x_F* is the accumulated fundamental harmonic current quantity
- *ACC_V_x_F* is the accumulated fundamental harmonic voltage quantity

3.6.4. Average Active and Reactive Power

Average active and reactive power over the integration period may be calculated directly from the metrology output registers for power of all harmonics and power of the fundamental harmonic:

$$P\_x\_Watts = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{ACC\_P\_x}{N \times 2^{40}} [W]$$

$$Q\_x\_VARs = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{ACC\_Q\_x}{N \times 2^{40}} [VAR]$$

$$P\_x_F\_Watts = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{ACC\_P\_x\_F}{N \times 2^{40}} [W]$$

$$Q\_x_F\_VARs = \frac{K\_Ix}{2^{10}} \times \frac{K\_Vx}{2^{10}} \times \frac{ACC\_Q\_x\_F}{N \times 2^{40}} [VAR]$$

Where,

- x = [A, B, C]
- *N* is the number of samples in the integration period
- *P_x_Watts* is the average active power of all harmonics of phase x
- *Q_x_VARs* is the average reactive power of all harmonics
- *P_x_F_Watts* is the average active power of fundamental harmonic
- *Q_x_F_VARs* is the average reactive power of fundamental harmonic
- *ACC_P_x* is the accumulated active power quantity for all harmonics
- *ACC_Q_x* is the accumulated reactive power quantity for all harmonics
- *ACC_P_x_F* is the accumulated active power quantity for fundamental harmonic
- *ACC_Q_x_F* is the accumulated reactive power quantity for fundamental harmonic

3.6.5. Average Apparent Power

Average apparent power over the integration period may be calculated directly from the current and voltage RMS values, as defined in IEEE® 1459:

$$S\_x\_VAs = I\_x_{rms} \times V\_x_{rms} [VA]$$

$$S\_x_F\_VAs = I\_x_{1\,rms} \times V\_x_{1\,rms} [VA]$$

Where,

- x = [A, B, C]
- *S_x_VAs* is the average apparent power of phase x
- *S_x$_f$_VAs* is the average fundamental apparent power of phase x
- *I_x$_{rms}$* is the fundamental and all harmonics current RMS value
- *V_x$_{rms}$* is the fundamental and all harmonics voltage RMS value
- *I_x$_{1\ rms}$* is the fundamental harmonic current RMS value
- *V_x$_{1\ rms}$* is the fundamental harmonic voltage RMS value

3.6.6. Vector Power Quantities

Here are examples of some of the possible vector power quantities that may be computed (There are multiple definitions for vector power quantities, and the symbols used can vary, such as "U" and "S"):

$$U\_x = \sqrt{(P\_x)^2 + (Q\_x)^2 + (D\_x)^2}$$

$$S\_x = \sqrt{(P\_x)^2 + (Q\_x)^2}$$

$$D\_x = \sqrt{(U\_x)^2 - (S\_x)^2}$$

$$F\_x = \sqrt{(Q\_x)^2 + (D\_x)^2}$$

$$N\_x = \sqrt{(U\_x)^2 - (Q\_x)^2}$$

$$U_{aa} = \sum_{x=\{A,B,C\}} U_x$$

$$\mathrm{U_{va}} = \sqrt{\left(\sum_{\mathrm{x=\{A,B,C\}}} \mathrm{P\_x}\right)^2 + \left(\sum_{\mathrm{x=\{A,B,C\}}} \mathrm{Q\_x}\right)^2 + \left(\sum_{\mathrm{x=\{A,B,C\}}} \mathrm{D\_x}\right)^2}$$

Where,

- x = [A, B, C]
- *U_x* is apparent power of all harmonics of phase x
- *S_x* is phasor power, all harmonics
- *D_x* is distortion power, all harmonics
- *F_x* is fictitious power, all harmonics
- *N_x* is nonreactive power, all harmonics
- *U$_{aa}$* is system arithmetic apparent power, all harmonics
- *U$_{va}$* is system vector apparent power, all harmonics

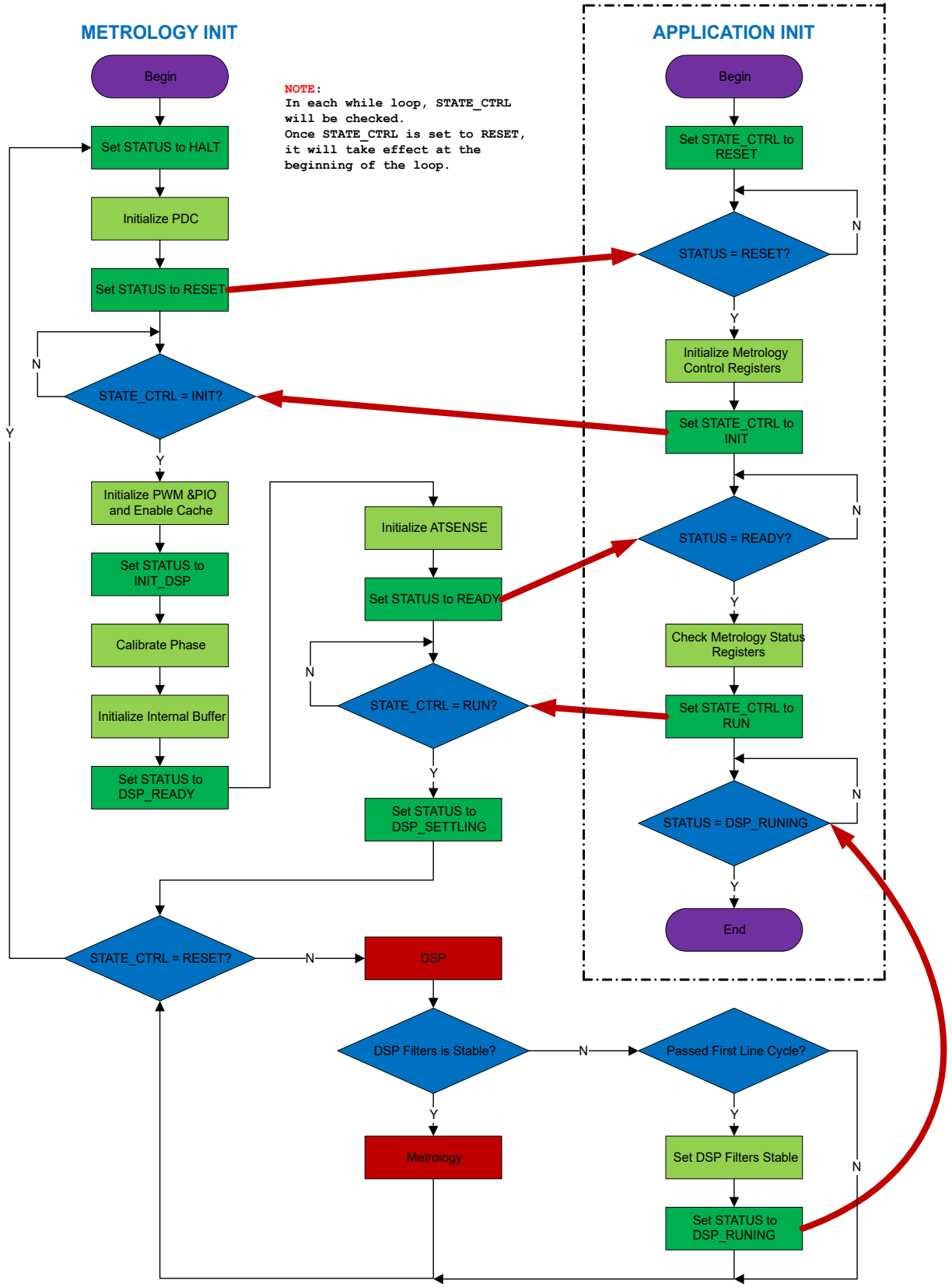
4. Interface between Metrology and Application

4.1. Interface in Initialization Stage

Application Initialization Sequence:

1. Change the STATE_CTRL register to RESET.
2. Wait until Metrology STATUS changed to RESET or wait until the interrupt is generated: IPC_INIT_IRQ.
3. Initialize all other Metrology Control Registers.
   Note: The STATE_CTRL register must be initialized to zero.
4. Change the STATE_CTRL register to RUN.
5. Wait until Metrology STATUS changed to DSP_RUNNING.

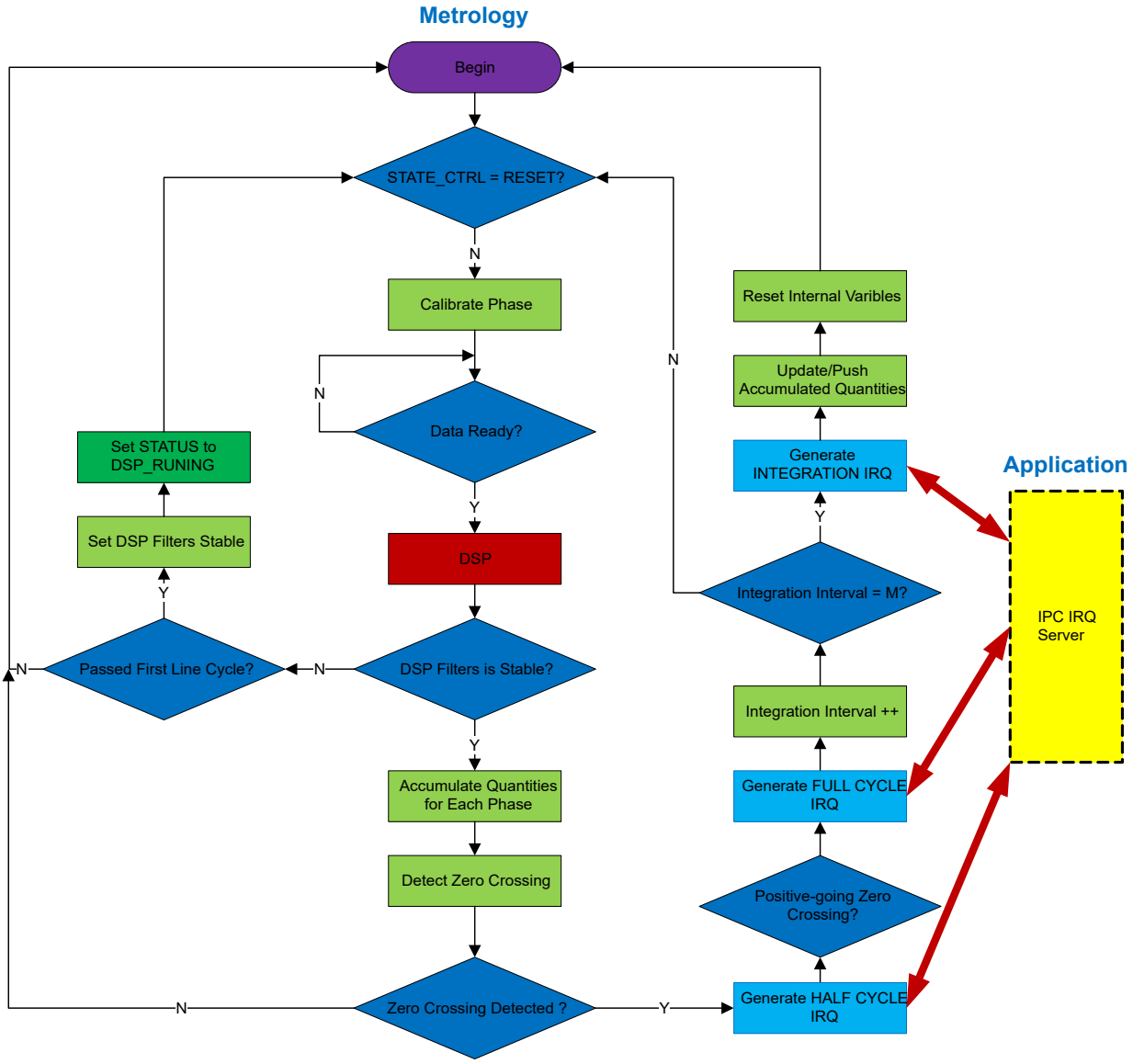
Figure 4-1. Metrology Initialization Flowchart



4.2. Interrupts in Metrology Stage

The following figure illustrates the metrology interrupts flowchart.

Figure 4-2. Metrology Interrupts Flowchart



The application code can disable any IPC interrupts it does not need.

When an IPC IRQ interrupt arrives, the application code first determines which kind of interrupt occurred and then it checks related Metrology Status Registers and executes its specific handler.

The IPC interrupt is defined as the following:

31	30	29	28	27	26	25	24
—	—	—	—	—	PULSE2_IRQ	PULSE1_IRQ	PULSE0_IRQ
23	22	21	20	19	18	17	16
—	—	—	INIT_IRQ	—	—	—	STATUS_IRQ
15	14	13	12	11	10	9	8
—	—	—	RZC_IRQ	—	—	—	—

7	6	5	4	3	2	1	0
CREEP_IRQ	—	HALF_CYCLE_IRQ	FULL_CYCLE_IRQ	—	—	—	INTEGRATION_IRQ

The sef lib provided by Microchip can be used to set this register:

- **PULSE0_IRQ, PULSE1_IRQ, PULSE2_IRQ: Pulse Interrupts**

These interrupts are generated immediately after the pulse has occurred. The typical delay is less than 1 µs. However, if the metrology code is attending a high-priority interrupt, such as the one triggered when the AFE has a new sample ready to be read, the delay could be higher.

- **INIT_IRQ: Initialization Requirement Interrupt**

This interrupt is used to inform the application code to initialize the metrology control registers and the ACC_T0, ACC_T1 and ACC_T2 if necessary.

- **STATUS_IRQ: STATUS Update Interrupt**

This interrupt is used to inform the application code of change(s) in priority status bit(s). This feature is not implemented.

- **RZC_IRQ: Raw Zero Crossing Interrupt**

This interrupt is generated on zero-crossings using the unfiltered *raw* 16 kHz data stream of the selected direction and selected voltage channel.

- **CREEP_IRQ: CREEP Detection Interrupt**

This interrupt is used to inform the application code of detection of a creep condition. This feature is not implemented.

- **HALF_CYCLE_IRQ: Half Line Cycle Interrupt**

This interrupt is generated every half line cycle. It means that swell and sag flags were updated. Unlike the RZC_IRQ, the HALF_CYCLE_IRQ uses the 4 kHz narrowband filtered voltage channels and exhibit a deterministic but frequency-dependent phase delay.

- **FULL_CYCLE_IRQ: Line Cycle Interrupt**

This interrupt is generated every full line cycle. It means that the Per-Cycle Accumulated Output Quantities, frequency and accumulated energy associated with pulse (including the ACC_T0, ACC_T1, ACC_T2 accumulators) were updated. Unlike the RZC_IRQ, the FULL_CYCLE_IRQ uses the 4 kHz narrowband filtered voltage channels and exhibits a deterministic but frequency-dependent phase delay.

- **INTEGRATION_IRQ: Integration Period Interrupt**

This interrupt is used to inform the application code that the whole integration period finishes. It means that all accumulated quantities and status N were updated.

5. Annex – Meter Forms

The service type determines what meter form is being implemented and how the Metrology DSP core interprets and processes the ADC values.

The table below provides the configuration for each Service Type.

Table 5-1. Service Types

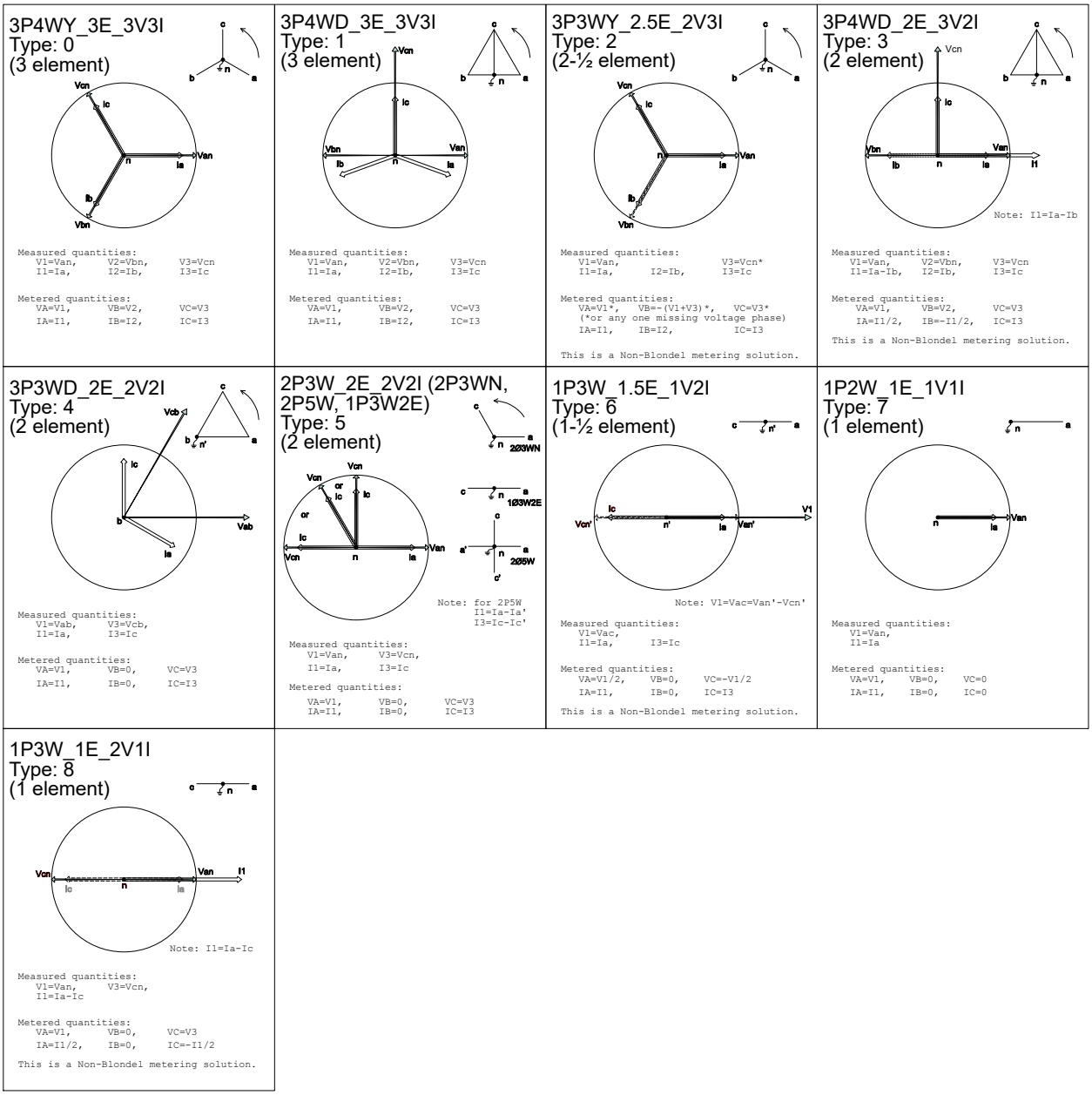
TYPE	Service Type		Elements	V inputs [Voltage Channels]	#I inputs [Current Channels]	P/S
0	Three-phase 4-wire Wye (3-element)	3P4WY_3E_3V3I	3	3 [v1, v2, v3]	3 [i1,i2,i3]	P
1	Three-phase 4-wire Delta (3-element)	3P4WD_3E_3V3I	3	3 [v1, v2, v3]	3 [i1,i2,i3]	P
2	Three-phase 4-wire Wye (2-½ element) (Note 1)	3P4WY_2p5E_2V3I	2 1/2	2 [v1, v2, v3]	3 [i1,i2,i3]	P
3	Three-phase 4-wire Delta (2-element) (Note 2)	3P4WD_2E_3V2I	2	3 [v1, v2, v3]	2 [i1,i3]	P
4	Three-phase 3-wire Delta (2-element)	3P3WD_2E_2V2I	2	2 [v1, v3]	2 [i1,i3]	P
5	Two-phase 3-wire Network (2 element) (Note 3)	2P3W_2E_2V2I	2	2 [v1, v3]	2 [i1,i3]	P
6	Single-phase 3-wire (1-½ element) (Note 4)	1P3W_1p5E_1V2I	1 1/2	1 [v1]	2 [i1,i3]	P
7	Single-phase 2-wire (1 element)	1P2W_1E_1V1I	1	1 [v1]	1 [i1]	P/S
8	Single-phase 3-wire (1 element) (Note 5)	1P3W_1E_2V1I	1	2 [v1, v3]	1 [i1]	P

Note:

1. For the Three-phase 4-wire Wye 2-½ element meter, any one phase voltage may be selected to be the missing phase, and the missing voltage will be internally imputed from the other 2 phase voltages.
2. For the Three-phase 4-wire Delta 2 element meter, one current sensor is used to measure the collective current of two phases, (IA-IB). All phase voltages VA, VB, and VC are measured.
3. For the Two-phase 3-wire 2 element meter, three common service types with two separate voltage phases and two separate currents may be metered by this mathematically identical service type. These are commonly known as:
   - Two-phase 3-wire Network (2p3WN)
   - Single-phase 3-wire 2 element (1p3W_2E)
   - Two-phase 5-wire (2p5W) with 2 current sensors each used to measure the collective currents of (IA-IA') and (IC-IC')
4. For the Single-phase 3-wire 1-½ element meter where only one phase-phase voltage, VAC, is measured. However, 2 current elements are measured.
5. For the Single-phase 3-wire 1 element meter where two individual phase voltages, VA and VC, are measured. However, only one current element is measured.

The METER_TYPE contains all the possibilities for the Service Type available and their configurations.

Figure 5-1. Meter Forms Summary

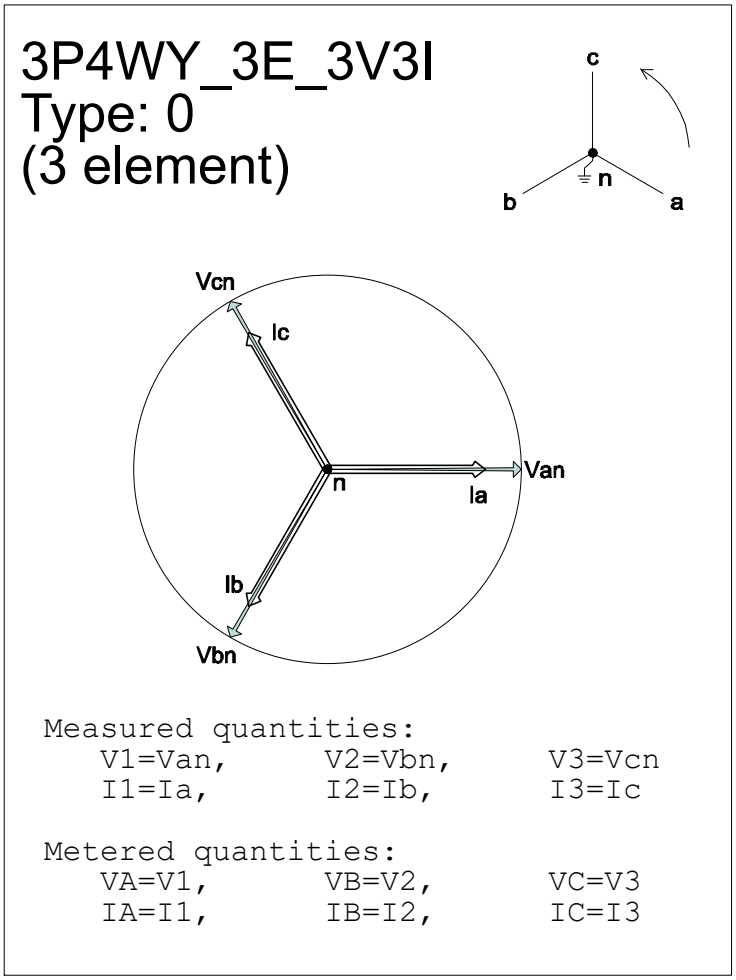


5.1. Service Type 0 – 3P4WY_3E_3V3I

Metering form 3-Phase 4-Wire WYE, 3-Elements, 3-Voltages, 3-Currents

This is the default metrology metering form.

Figure 5-2. Service Type 0 – 3P4WY_3E_3V3I

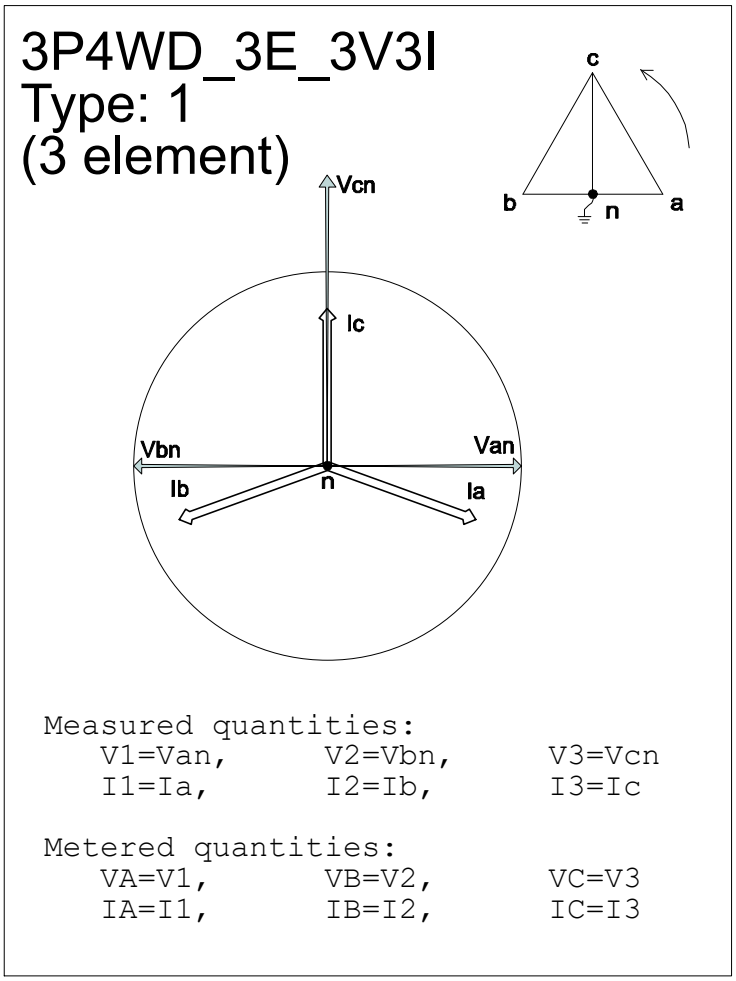


In the most straight-forward, default non-transformational processing, metering with form type:0 is mathematically the equivalent to metering with form type:1. However, as expected, differences would be evident in different reported results for phase-phase voltage values as well as phasing between the voltage and current channels.

5.2. Service Type 1 – 3P4WD_3E_3V3I

Metering form 3-Phase 4-Wire DELTA, 3-Elements, 3-Voltages, 3-Currents

Figure 5-3. Service Type 1 – 3P4WD_3E_3V3I



In the most straight-forward, default non-transformational processing, metering with form type:1 is mathematically the equivalent to metering with form type:0. However, as expected, differences would be evident in different reported results for phase-phase voltage values as well as phasing between the voltage and current channels.

Dto4WY_TRANSFORM EQUATIONS:

The DtoY_TRANSFORM option enables the following alternate transform equations:

- VA = V1 – V3/3
- VB = V2 – V3/3
- VC = (2/3)V3

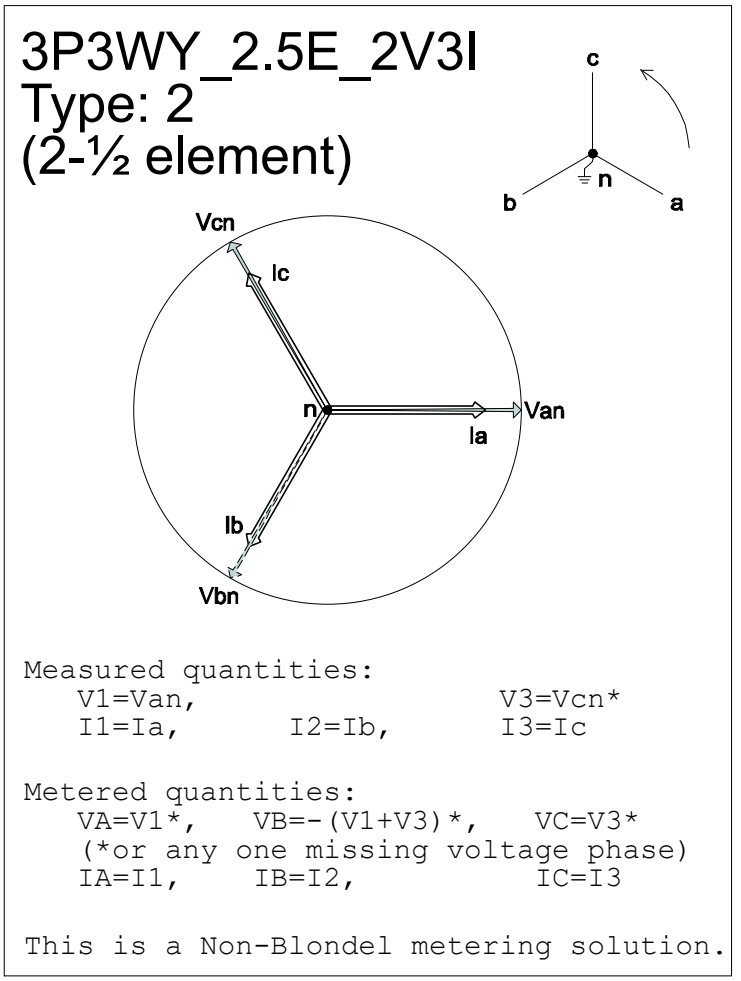
Note: Transforms may introduce metering artifacts in the case of non-Blondel and unbalanced situations.

5.3. Service Type 2 – 3P4WY_2.5E_2V3I

Meter form 3-Phase 3-Wire WYE, 2½-Elements, 2-Voltages, 3-Currents

Use this meter form type to mathematically generate any one missing voltage phase for a 3-wire WYE 2-½ element service.

Figure 5-4. Service Type 2 – 3P4WY_2p5E_2V3I



To minimize lost revenue, this meter form type may be dynamically selected to generate any one missing phase potential when detecting a dropped phase voltage of a 4-wire WYE 3-element service.

Notes: Some applications may require monitoring whether the missing voltage has returned in order to revert to Service Type 0. In such cases, be aware that when Service Type 2 is enabled, the STATE_FLAG_PH_x_ACTIVE flags cannot be used to detect the recovery of the missing voltage. This is because the flag references the voltage that is mathematically generated from the two existing phases, making the status flags unsuitable for detecting voltage recovery.
The following alternatives are available for detecting the recovery of the missing voltage:

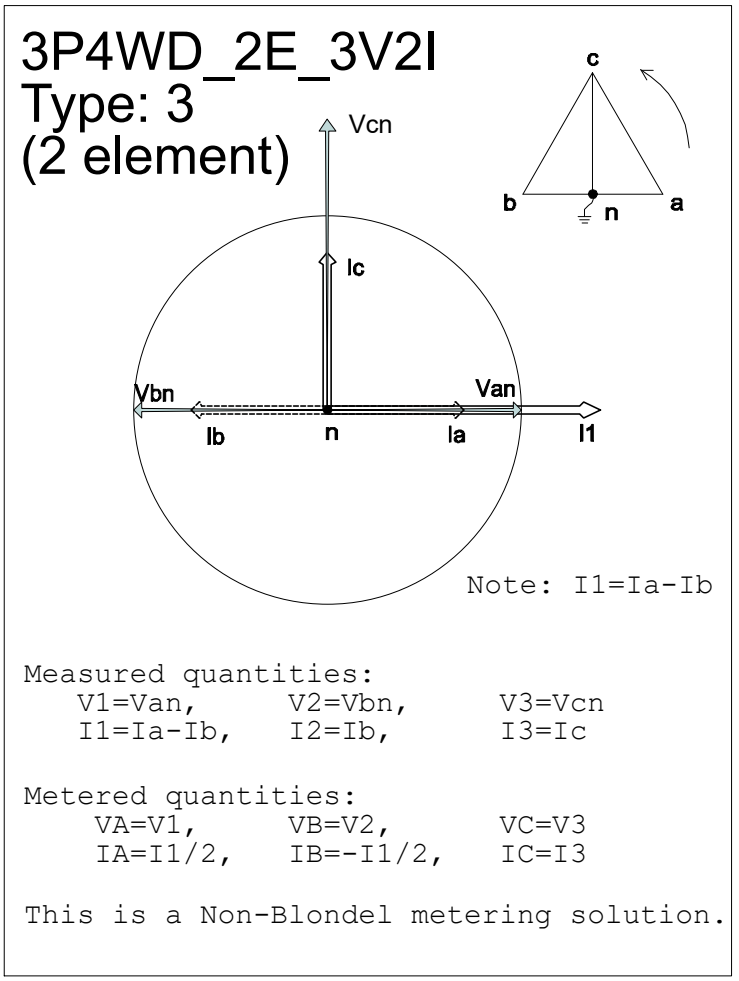
1. Enable waveform capture (at 8K or 16K source) and analyze the captured data for the relevant voltage. This may conflict with applications that utilize waveform capture at 4 kHz.
2. Enable harmonics analysis and monitor the magnitude of the first (fundamental) harmonic of the voltage in question.

5.4. Service Type 3 – 3P4WD_2E_3V2I

3-Phase 4-Wire DELTA, 2-Elements, 3-Voltages, 2-Currents

Use this meter form type to mathematically generate balanced currents for Phase-A and Phase-B from a single shared current sensor for the lighting load phases.

Figure 5-5. Service Type 3 – 3P4WD_2E_3V2I



Dto4WY_TRANSFORM EQUATIONS:

The DtoY_TRANSFORM option enables the following alternate transform equations:

- VA = V1 – V3/3 IA = I1/2 – I3/2
- VB = V2 – V3/3 IB = -I1/2 – I3/2
- VC = (2/3)V3

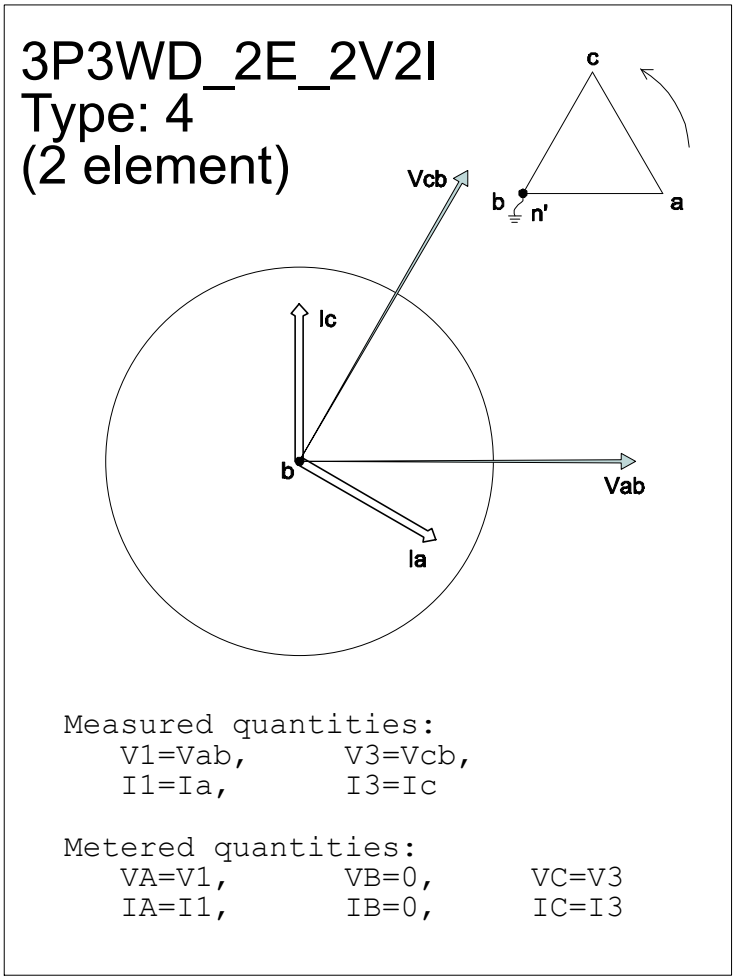
Note: Transforms may introduce metering artifacts in the case of non-Blondel and unbalanced situations.

5.5. Service Type 4 – 3P3WD_2E_2V2I

3-Phase 3-Wire DELTA, 3-Elements, 2-Voltages, 2-Currents

Use this meter form type to meter the typical 3-phase 3-wire delta 2 element service.

Figure 5-6. Service Type 4 – 3P3WD_2E_2V2I



In the most straight-forward, default non-transformational processing, metering with form type:4 is mathematically the equivalent to metering with form type:5. However, as expected, differences would be evident in different reported results for phase-phase voltage values as well as phasing between the voltage and current channels.

Dto4WY_TRANSFORM EQUATIONS:

The DtoY_TRANSFORM option enables the following alternate transform equations:

- VA = (2/3)V1 – V3/3
- VB = -(V1 + V3)/3 IB = -(I1 + I3)
- VC = (2/3)V3 – V1/3

Note: Transforms may introduce metering artifacts in the case of non-Blondel and unbalanced situations.

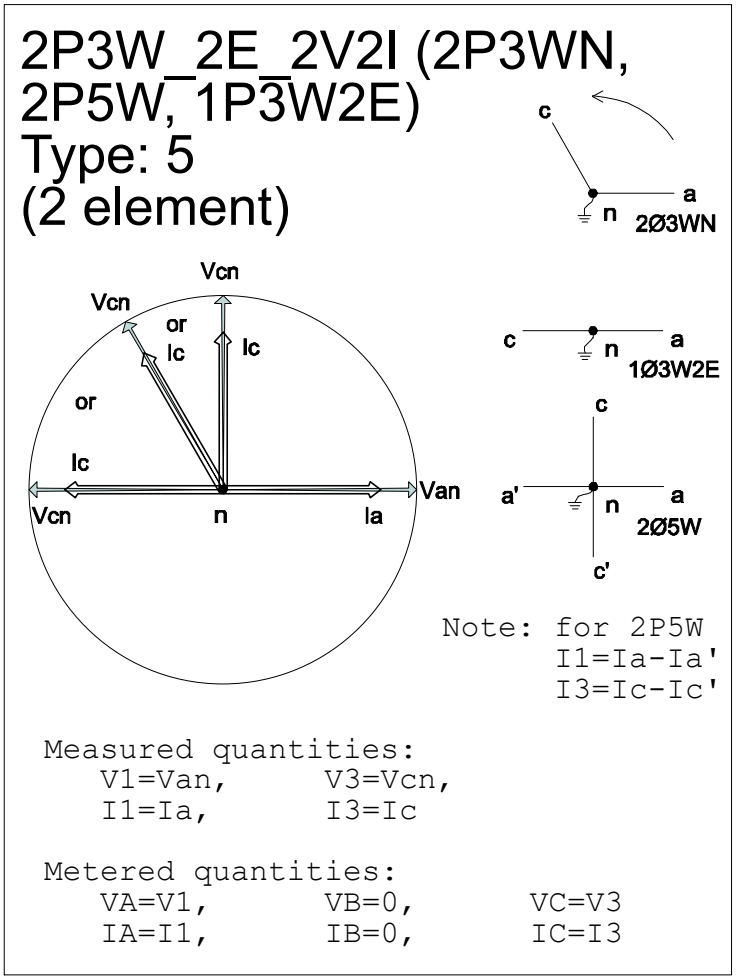
5.6. Service Type 5 – 2P3W_2E_2V2I

2-Phase 3-Wire NETWORK, 2-Elements, 2-Voltages, 2-Currents

Use this meter form type when metering any 2-Phase service with two phases of voltage measurement, each with its own current measurement. Mathematically, this makes three seemingly different services: 2-Phase 3-Wire Network, 2-Phase 5-Wire, and the “1-Phase” 3-Wire 2-Element

meter forms all mathematically equivalent, except for the results reported for phase-phase voltages and voltage-current phasing.

Figure 5-7. Service Type 5 – 2P3W_2E_2V2I



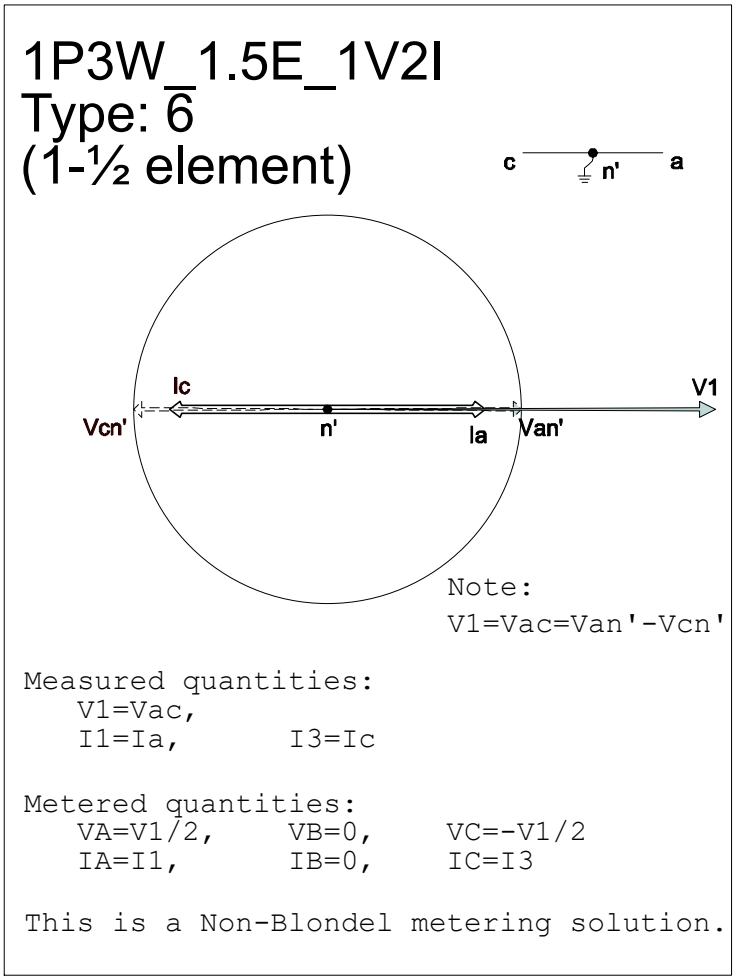
In the most straightforward, default non-transformational processing, metering with form type:5 is mathematically the equivalent to metering with form type:4. However, as expected, differences would be evident in different reported results for phase-phase voltage values as well as phasing between the voltage and current channels.

5.7. Service Type 6 – 1P3W_1.5E_1V2I

1-Phase 3-Wire, 1½-Elements, 1-Voltage, 2-Currents

Use this meter form type when metering a single-phase application using a single phase-phase voltage sensor, but two separate current measuring elements. In this application, it would be expected that the meter is *hot* with the metrology not explicitly connected to an external neutral reference.

Figure 5-8. Service Type 6 – 1P3W_1p5E_1V2I

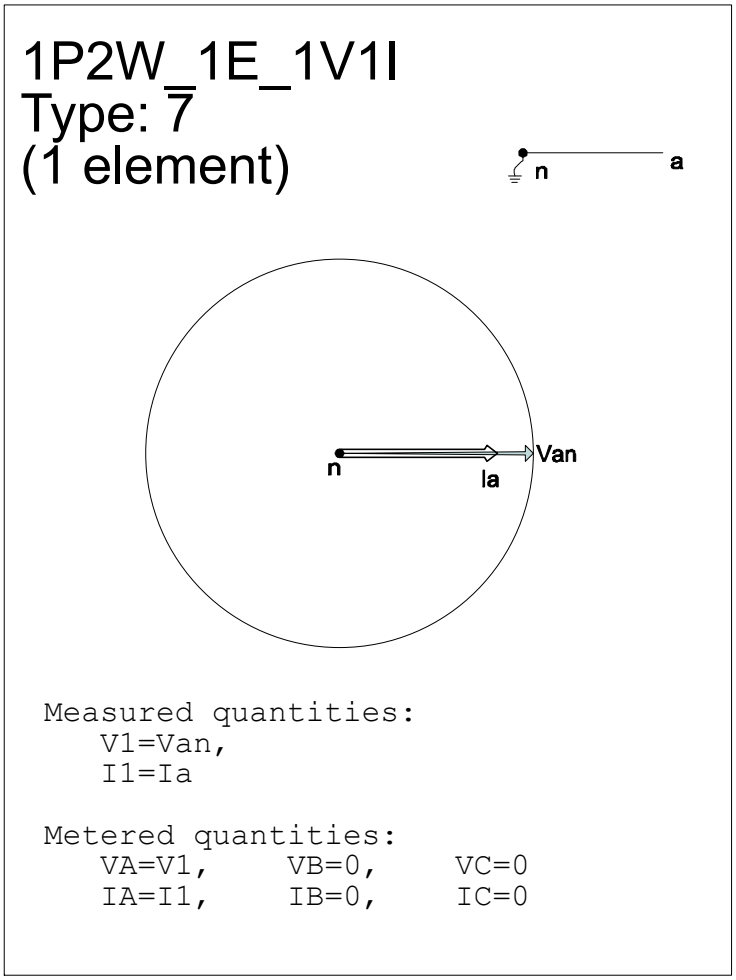


5.8. Service Type 7 – 1P2W_1E_1V1I

1-Phase 2-Wire, 1-Element, 1-Voltage, 1-Current

Use this meter form type when metering a single-phase metering application with one voltage and one current.

Figure 5-9. Service Type 7 – 1P2W_1E_1V1I

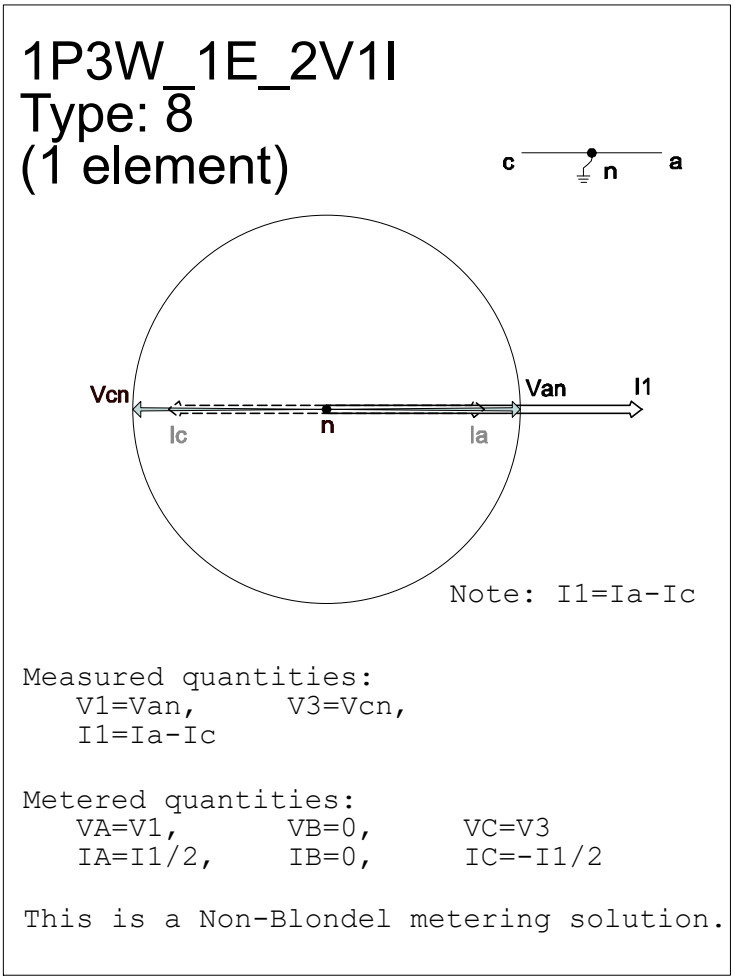


5.9. Service Type 8 – 1P3W_1E_2V1I

1-Phase 3-Wire, 1-Element, 2-Voltages, 1-Current

Use this meter form type when metering a single-phase application using a single shared current sensor but two separate phase voltage measurement inputs 180° out of phase.

Figure 5-10. Service Type 8 – 1P3W_1E_2V1I



6. References

- ATSENSE-101/ATSENSE-301(H) Multi-Channel Sigma-Delta Analog Front End (*DS60001524*)
- Microchip PIC32CXMTx Metrology User Guide (*DS50003460*)
- MCP3910 Data Sheet (*DS20005116*)
- MCP3912 Data Sheet (*DS20005348*)
- MCP3913 Data Sheet (*DS20005227*)
- MCP3914 Data Sheet (*DS20005216*)

7. Revision History

Revision F - 01/2026

Document	• Metrology library version v03.4.00. • Minor changes of format. • Updated ADC, G_{PGA}, and PGA descriptions in Table 1-1. • Added three paragraphs in User Characteristics section. • Added reference to MCP391x in Assumptions and Dependencies section. • Added Supported AFEs section. • Updated Signals and Phases Defined section. • Added voltage channel, V_D, in DSP Channel and Computed Quantity Description section. • Updated Metrology Interface Definition section. • Added *AFE_SELECTION*, *CHANNEL_MATRIX*, *PULSEx_K_t*, *SYNTHESIZER_ADDR*, *CREEP_THRESHOLD_P_x*, *CREEP_THRESHOLD_Q_x*, *CREEP_THRESHOLD_I_x*, *INTERRUPT_THRESHOLD_Vx*, and *AFE_CTRL_0* variables in Metrology Control Registers. • The control register FEATURE_CTRL now includes two new flags, *VD_DC_EN* and *SYNTH_EN*. • Updated descriptions in *CREEP_P_EN*, *CREEP_Q_EN*, *CREEP_I_EN*, and *NEUTRAL_DIS* flags of the control register FEATURE_CTRL. • Added new control registers AFE_SELECTION, CHANNEL_MATRIX, PULSEx_K_t, SYNTHESIZER_ADDR, CREEP_THRESHOLD_P_x (x = A, B, C), CREEP_THRESHOLD_Q_x (x = A, B, C), CREEP_THRESHOLD_I_x (x = A, B, C), INTERRUPT_THRESHOLD_Vx (x = A, B, C), and AFE_CTRL_0. • Removed the following control registers: *P_K_t*, *Q_K_t*, *I_K_t*, *S_K_t*, *ATSENSE_CTRL_20_23*, *ATSENSE_CTRL_24_27*, and *ATSENSE_CTRL_28_2B*. • Added warning in the ACC_Tx, CREEP_THRESHOLD_I registers. • Changed *11 WA* by *11 VA* in CREEP_THRESHOLD_S register. • Added examples of POWER_OFFSET_x in POWER_OFFSET_P, and POWER_OFFSET_Q registers. • Added voltage channel, D, in K_Vx register and updated the description. • Added voltage channel, D, in CAL_M_Vx register. • The control register CAPTURE_CTRL now includes a new flag, *CH_SEL_VD*. • Added *CH_VD_0*, *CH_VD_1*, and *CH_VD_2* in Table 3-3. • Added examples of POWER_OFFSET_X_x in POWER_OFFSET_P_x, and POWER_OFFSET_Q_x registers. • Updated starting address in Metrology Status Registers, Accumulated Output Quantities, and Harmonic Analysis Output Quantities sections. So, the address of all variables changed. • Modified the order of variables in Table 3-4 and added *N_CYCLE* register. • The status register STATE_FLAG now includes six new flags, *CREEP_DET_Q_A*, *CREEP_DET_Q_B*, *CREEP_DET_Q_C*, *CREEP_DET_P_A*, *CREEP_DET_P_B*, and *CREEP_DET_P_C*, and changed *ATSENSE_FAIL* by *AFE_FAIL* in this register. • Added a new paragraph in the description of TEMPERATURE register. • Added new status register N_CYCLE. • Updated Accumulated Output Quantities and modified the order of variables in Table 3-5. • Added voltage channel, D, in V_A, V_B, V_C, V_D, V_A_F, V_B_F, V_C_F, V_D_F register and added note. • Added a new paragraph in V_AB, V_BC, V_CA, V_AB_F, V_BC_F, V_CA_F register. • Added Per-Cycle Accumulated Output Quantities section. • Updated the description of *PULSE0_IRQ, PULSE1_IRQ, PULSE2_IRQ, INIT_IRQ* in Interrupts in Metrology Stage section. • Added note and last paragraphs in Service Type 2 – 3P4WY_2.5E_2V3I section.

Revision E - 06/2025

Document	• Metrology library version v3.3.00. • Apparent energy has been integrated as a source for metrology pulses. • The Metrology Interface Definition section provides detailed information regarding the sizes and addresses of the register blocks. • Updated Index and added Address column in the following tables: Table 3-2, Table 3-4, Table 3-5, and Table 3-7. • Added Reset Value = 0 in all Registers. • Updated start address in Metrology Status Registers, Accumulated Output Quantities, and Harmonic Analysis Output Quantities sections. • Added new control registers *S_K_t*, CREEP_THRESHOLD_S, and POWER_OFFSET_S. • The control register FEATURE_CTRL now includes a new flag, *CREEP_S_EN*, and the flag, *SYNCH*, changed the name from "*Active Voltage Channel Selection*" to "*Dominant Voltage Channel Selection*". • The control register PULSEx_CTRL has been modified to support the new functionalities related to apparent power pulsing capabilities. • The control register POWER_OFFSET_CTRL now includes a new flag, *S_OFFSET_PUL*. • Added warning in the HARMONIC_CONTROL, CAL_M_Ix, and CAL_M_Vx registers. • The status register STATE_FLAG now includes a new flag, *CREEP_DET_S*, and the flag, *TIMING_Vx*, changed the name from "*Active Voltage Channel*" to "*Dominant Voltage Channel*". • The status register FREQ changed the name from "*Active Line Voltage Fundamental Harmonic Frequency*" to "*Dominant Line Voltage Fundamental Harmonic Frequency*". • Added Note in FREQ, and FREQ_Vx registers. • Added an example for calculating the phase shift between voltages by applying the Law of Cosines in V_AB, V_BC, V_CA, V_AB_F, V_BC_F, V_CA_F register. • Added VAh unit in ACC_T0, ACC_T1, and ACC_T2 in Table 3-5 and in ACC_T0, ACC_T1, ACC_T2 register. • Changed *sQ13.8* by *sQ13.18* in Harmonic Analysis Output Quantities section. • Updated the first paragraph in THD section. • Updated Energy/Quadergy, and Vector Power Quantities sections. • Added Average Apparent Power section.

Revision D - 12/2024

Document	• Metrology library version v3.2.00. • The library is able to compute up to 31 harmonic orders simultaneously. • Functionality in FEATURE_CTRL0 and FEATURE_CTRL1 has been unified in FEATURE_CTRL0. • FEATURE_CTRL1 was renamed to HARMONIC_CTRL. This register is used to enable the harmonic computation and for selecting the desired harmonics orders to be calculated. • STATE_FLAG.HARMONIC_m_CONF[7:0] field was removed. • HARMONIC output registers increased to 434 registers. The format changes. The values are not scaled with K_I_x and K_V_x registers. • PU (Pull-Up) and OPD (Open-Drain) features removed from pulse control registers, as these functionalities are not available while under PWM peripheral control. • Added a protection mechanism to avoid the issue that sometimes happened when the library was incorrectly configured to pulse all the energy being applied. The improper configuration occurred when the configured meter constants and pulse widths generated a pulse rate not supported, when applying energies above a threshold. The effect was that sometimes the library was not working properly, affecting the accuracy of the measurements. • In previous version, the metrology library disabled the watchdogs. Now the watchdog control register is not written.

Rev C - 03/2024

Document	• Metrology library version v3.1.02. • Pulse algorithm changed to support testing inter-harmonics in the current circuits (burst fired waveform test, as defined in IEC62052-11:2021) using the pulses. • Added counters for the number of pulses issued in the three pulse outputs. The counters are shown in the status registers 25, 26 and 27. • Corrected a bug that in certain circumstances could generate unexpected pulses when transitioning from a high pulse rate to a very low or zero pulse rate. • Included a clarification regarding the maximum metrology pulse rate.

Rev B - 10/2023

Document	• Changed name of document from "*Microchip PIC32CXMTx Metrology Data Sheet*" to "*PIC32CXMTx Metrology Reference Guide*". • Metrology library version v3.1.00. • Metrology pulses peripheral clock rate increased to 7.424 MHz. • Pulse algorithm improved. • Bug affecting the frequency measurements corrected. In previous versions, the frequency of the non-dominant phases was not accurate. • Maximum metrology pulse rate increased to 1800 pulses/sec.

Rev A - 12/2022

Document	• Initial release. • Metrology library version v3.0.0b.

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