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## Introduction

This document defines the interface of Microchip Smart Meter PIC32CXMTx Metrology firmware. It describes the metrology control registers, metrology status registers, and the quantities that are directly computed and available through the metrology interface registers as well as provides pertinent definitions required for proper coding, given the target ARM4 hardware.

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# 1. Definitions, Acronyms and Abbreviations

**Table 1-1.** Abbreviations and Acronyms

Abbreviation	Description
ADC	<p>Analog-to-Digital Converter of the ATSENSE AFE, consisting of a PGA, a second-order <math>\Delta/\Sigma</math> modulator, and followed by an integrated third-order sinc<sup>3</sup> decimation filter. A digitized conversion of an analog voltage, <math>V_{ADCin}</math>, is created using the following equation:</p> $v_{digitized} = \frac{G_{PGA} \times V_{ADCin}}{V_{REF}} = \frac{[1, 2, 4, \text{or } 8] \times V_{ADCin}}{V_{REF}}$ <p>For best linearity, the product of ADC input voltage and the PGA gain must not exceed 0.5V, <math>G_{PGA} \times V_{ADCin} \leq 0.5V</math>, where <math>G_{PGA}</math> for all voltage channels is fixed at 1.</p>
AFE	Analog Front End
BAMS	Binary Angular Measurement System. Angles are normalized to the binary range [-1.0000, +0.9999] k, where k may represent any convenient scale, such as 180°, or $\pi$ -radians. In this metering discussion, all angles are drawn as if vectors starting to 0° (3 o'clock position) and rotating counter-clockwise for positive phase increases. Using BAMS allows for graceful rollover from $\pm 180^\circ$ to $\mp 180^\circ$ without edge-effects.
CT	Current Transformer
$\Delta/\Sigma$ ADC	Delta-Sigma Analog-to-Digital Converter, an over-sampled converter with noise shaping
DSP	Digital Signal Processing
$G_{PGA}$	<p>Gain selected for use in the ADC front end, <math>G_{PGA}</math>, on current measurement channels only (<math>G_{PGA}</math> gain for voltage channels is fixed to 1).</p> <p><math>G_{PGA} = [1, 2, 4 \text{ or } 8]</math></p>
Kh	Watt-hour meter constant for electro-mechanical meters, defines an amount of energy indicated by one (1) pulse generated by the meter and does not usually apply to solid-state meters.
Kt	Watt-hour meter test constant for solid-state meters, defines an amount of energy indicated by one (1) optical pulse generated by the meter and does not usually apply to electro-mechanical meters.
MSB	Most Significant Bit, the left-most bit of a binary number.
N	The number of samples in any one measurement interval. This number may vary for each measurement interval.
OSR	Over Sample Rate

**Table 1-1. Abbreviations and Acronyms (continued)**

Abbreviation	Description
Qformat	<p>To prevent ambiguity, this document uses the following definition of Qformat numbers, being a fixed-point number format representing both integer and fractional numbers, and may be unsigned (uQm.n) or signed (sQm.n).</p> <p><u>Unsigned Qformat numbers:</u> An (m+n)-bit unsigned number is designated uQm.n. It occupies (m+n) bits and is stored as an unsigned fixed-point binary number. An unsigned uQm.n number may represent numbers in the range: <math>[0, +(2^m - 2^{-n})]</math>.</p> <p><u>Signed Qformat numbers:</u> An (m+n+1)-bit signed number is designated sQm.n. It occupies (m+n+1) bits and is stored as a signed fixed-point binary number, where the MSB is used as a sign bit. A signed sQm.n number may represent numbers in the range: <math>[-(2^m), +(2^m - 2^{-n})]</math>.</p> <p>For example, an 8-bit sQ4.3 format number has one (1) sign bit, four (4) bits to the left of the binary point and three (3) bits to the right of the binary point and may be used to represent numbers in the range: <math>[-(2^4), +(2^4 - 2^{-3})] = [-16, +15.875]</math>.</p> <p>To convert a sQm.n format number to a decimal equivalent, divide the equivalent two's-complement binary number by <math>2^n</math>. For example: an 8-bit signed sQ2.5 number: <math>[0b0100\ 0001] = 65/(2^5) = 2.03125</math>, an 8-bit <math>[0b1100\ 0001] = -63/(2^5) = -1.96875</math>.</p> <p>To convert a decimal number into a sQm.n format number, multiply by <math>2^n</math> and convert to a signed two's-complement (m+n+1)-bit number. For example: <math>-7.33 \Rightarrow \text{sQ3.4}: (-7.33) \times (2^4) = -117 \Rightarrow [0b0111\ 0101] \Rightarrow [0b1000\ 1011]</math>.</p> <p>Example-1: sQ1.14</p> <p>A signed 16-bit number, having 1 sign bit, 1 integer bit to the left of the binary point, and 14 mantissa bits to the right of the binary point that can represent numbers in the range: <math>[-2.0, +1.999938965]</math>.</p> <p>Example-2: uQ2.14</p> <p>An unsigned 16-bit number, having no sign bit, 2 integer bits to the left of the binary point and 14 mantissa bits to the right of the binary point that can represent numbers in the range: <math>[0, +3.999938965]</math>.</p>
PGA	<p>Programmable Gain Amplifier: The four ADC channels associated with the current measurement have an internal, selectable, programmable gain amplifier that can provide an additional analog gain equal to G<sub>PGA</sub>.</p> <p><math>G_{PGA} = [1, 2, 4 \text{ or } 8]</math></p>
V <sub>P</sub> , V <sub>P-M</sub>	<p>Voltage potential: V<sub>P</sub> is the voltage measured from node P to an implied neutral reference voltage.</p> <p>V<sub>P-M</sub> is the voltage measured from node P to node M, where a positive voltage is indicative of a voltage rise from node M to node P.</p> <p>All phase diagrams are drawn as if mathematical vectors starting at 0° (3 o'clock) and rotating counter-clockwise for positive phase increases, with 90° being at 12 o'clock, 180° at 9 o'clock and 270° at 6 o'clock.</p>

## 2. Overall Description

### 2.1. Power Quantities Definition Perspective

The quantities available in the Metrology module make observable all basic components required to completely define or derive all power system measurement quantities for most currently used definitions of power. All per-phase voltages, currents and power for fundamental and fundamental + harmonics are available, allowing computation of all modern system or poly-phase power quantities.

Quantities labeled as “ACC\_Tx” are totals accumulated energy since power-up, they are the same with those energy calculated with pulse x.

### 2.2. User Characteristics

Measurement data from one measurement interval is short-lived and does not persist longer than one measurement interval. At the end of a measurement interval, the user will be informed by a software interrupt, at which point, the user must read all pertinent quantities before the next measurement period ends.

### 2.3. Constraints

All computed quantities available through the Metrology module are integrated over a time interval equivalent to an integral number of periods of the fundamental frequency. All integration periods are approximated by the final output sample rate of the DSP filters, 4000 Hz; so, measurement accuracy will increase using longer integration periods. One second is the recommended minimum integration period (50 cycles of 50 Hz or 60 cycles of 60 Hz), but fewer numbers of samples may still yield acceptable results.

DSP filters require a settling time before accurate measurements may be used for revenue-quality metering. It is recommended to wait at least 250 ms after start-up before testing to revenue-grade accuracy.

### 2.4. Assumptions and Dependencies

The Smart Meter DSP module is specifically designed to accept samples from an ATSENSE  $\Delta/\Sigma$  ADC using an OSR = 64, at an input sample rate of 16000 kHz. This input data stream is further filtered to an internal sample rate of 4000 kHz for generation of metrology quantities. All computed metrology quantities are available at a rate of approximately 1 Hz when using recommended settings.

### 2.5. Signals and Phases Defined

The ATSENSE constantly digitizes its seven primary input signals from inputs [V1, V2, V3] and [I0, I1, I2, I3] and assigns these to the DSP processing channels: I\_A, V\_A, I\_B, V\_B, I\_C, V\_C, and measured neutral current, I\_Nm. Imputed neutral current, I\_Ni, and the sample-by-sample difference between measured and imputed neutral currents, I\_Nmi, are also computed.

### 2.6. DSP Channel and Computed Quantity Description

DSP channel nomenclature defines 3 basic voltage channels: V\_A, V\_B and V\_C, and 4 basic current channels: I\_A, I\_B, I\_C, and measured neutral current, I\_Nm. The channel currents are combined to create an accumulated imputed neutral current, I\_Ni, and an accumulated sample-by-sample difference between the measured and imputed neutral currents, I\_Nmi.

Values further labeled as '\_F' indicate values associated with the fundamental frequency component only, while values without the '\_F' indicate values associated with fundamental + harmonics.

### 3. Metrology Interface Definition

The metrology module provides the following control registers and status registers; it also provides different kinds of accumulated quantities. Control registers are introduced in [Metrology Control Registers](#) and Status registers are introduced in [Metrology Status Registers](#). Accumulated quantities are introduced in [Accumulated Output Quantities](#) and Harmonic analysis quantities are introduced in [Harmonic Analysis Output Quantities](#).

The following table provides the register block sizes and addresses presently implemented.

**Table 3-1.** Register Block Sizes and Addresses

Register Block	No. of registers	Width [bytes]	Start address	End address
Control Registers	64	4	0x20088000	0x200880FF
Status Registers	36	4	0x20088100	0x2008818F
Accumulator Registers	55	8	0x20088190	0x20088347
Harmonic Registers	434	4	0x20088348	0x20088A0F

#### 3.1. Metrology Control Registers

The start address is 0x20088000.

**Table 3-2. Metrology Control Registers**

Index	Address	Variable	Access Mode	Name	Format	No. of Bytes	Min Value	Max Value	Default	Units
0	0x20088000	STATE_CTRL	R/W	Metrology State Control register	uQ32.0	4	—	—	—	integer
1	0x20088004	FEATURE_CTRL	R/W	Metrology Feature Setting register	uQ32.0	4	—	—	—	integer
2	0x20088008	HARMONIC_CTRL	R/W	Harmonic Control register	uQ32.0	4	—	—	—	integer
3	0x2008800C	METER_TYPE	R/W	Sensor Type and Service Type Settings register	uQ32.0	4	—	—	—	integer
4	0x20088010	M	R/W	Number of line cycles for integration period	uQ32.0	4	0	1980	0	integer
5	0x20088014	N_MAX	R/W	Maximum number of samples in an integration period	uQ32.0	4	—	132000	4400	integer
6	0x20088018	PULSE0_CTRL	R/W	Pulse 0 control: enable/disable, polarity, quantity type selection	uQ32.0	4	—	—	—	integer
7	0x2008801C	PULSE1_CTRL	R/W	Pulse 1 control: enable/disable, polarity, quantity type selection	uQ32.0	4	—	—	—	integer
8	0x20088020	PULSE2_CTRL	R/W	Pulse 2 control: enable/disable, polarity, quantity type selection	uQ32.0	4	—	—	—	integer
9	0x20088024	P_K_t	R/W	Watt-hour meter constant for pulse output	uQ8.24	4	—	—	0.3125	Wh/imp
10	0x20088028	Q_K_t	R/W	Var-hour meter constant for pulse output	uQ8.24	4	—	—	0.3125	VARh/imp
11	0x2008802C	I_K_t	R/W	Amp-squared-hour meter constant for pulse output	uQ8.24	4	—	—	0.3125	Amp²h/imp
12	0x20088030	S_K_t	R/W	VA-hour meter constant for pulse output	uQ8.24	4	—	—	0.3125	VAh/imp
13	0x20088034	CREEP_THRESHOLD_P	R/W	Starting per-cycle total Active Energy for pulse and pulse accumulation	uQ2.30	4	—	—	—	Wh
14	0x20088038	CREEP_THRESHOLD_Q	R/W	Starting per-cycle total Reactive Quadergy for pulse and pulse accumulation	uQ2.30	4	—	—	—	VARh
15	0x2008803C	CREEP_THRESHOLD_I	R/W	Starting per-phase current for both Energy and Quadergy pulse and pulse accumulation	uQ12.20	4	—	—	—	mArms scaled
16	0x20088040	CREEP_THRESHOLD_S	R/W	Starting per-cycle total Apparent energy for pulse and pulse accumulation	uQ2.30	4	—	—	—	VAh
17	0x20088044	POWER_OFFSET_CTRL	R/W	Power offset control	uQ32.0	4	—	—	—	integer
18	0x20088048	POWER_OFFSET_P	R/W	Pulse computation active power offset compensation used to eliminate voltage effects to small current (cross talk). Affects only pulse measurements.	sQ1.30	4	-2.000	1.9999...	0	Wh/cycle
19	0x2008804C	POWER_OFFSET_Q	R/W	Pulse computation reactive power offset compensation used to eliminate voltage effects to small current (cross talk). Affects only pulse measurements.	sQ1.30	4	-2.000	1.9999...	0	VARh/cycle
20	0x20088050	POWER_OFFSET_S	R/W	Pulse computation apparent power offset compensation used to eliminate voltage effects to small current (cross talk). Affects only pulse measurements.	sQ1.30	4	—	—	—	I²h/cycle
21	0x20088054	SWELL_THRESHOLD_VA	R/W	Voltage swell threshold for each half cycle of phase-A voltage	uQ0.32	4	0	0.9999...	—	—

**Table 3-2.** Metrology Control Registers (continued)

Index	Address	Variable	Access Mode	Name	Format	No. of Bytes	Min Value	Max Value	Default	Units
22	0x20088058	SWELL_THRESHOLD_VB	R/W	Voltage swell threshold for each half cycle of phase-B voltage	uQ0.32	4	0	0.9999...	—	—
23	0x2008805C	SWELL_THRESHOLD_VC	R/W	Voltage swell threshold for each half cycle of phase-C voltage	uQ0.32	4	0	0.9999...	—	—
24	0x20088060	SAG_THRESHOLD_VA	R/W	Voltage sag threshold for each half cycle of phase-A voltage	uQ0.32	4	0	0.9999...	—	—
25	0x20088064	SAG_THRESHOLD_VB	R/W	Voltage sag threshold for each half cycle of phase-B voltage	uQ0.32	4	0	0.9999...	—	—
26	0x20088068	SAG_THRESHOLD_VC	R/W	Voltage sag threshold for each half cycle of phase-C voltage	uQ0.32	4	0	0.9999...	—	—
27	0x2008806C	K_IA	R/W	ADC input current conversion factor = $I_A(\text{rms})/V_{\text{adc}}(\text{rms})$	uQ22.10	4	—	2,000.00	—	$A_{\text{RMS}}/V_{\text{ADC-RMS}}$
28	0x20088070	K_VA	R/W	ADC input voltage conversion factor = $V_A(\text{rms})/V_{\text{adc}}(\text{rms})$	uQ22.10	4	—	4,000.00	—	$V_{\text{RMS}}/V_{\text{ADC-RMS}}$
29	0x20088074	K_IB	R/W	ADC input current conversion factor = $I_B(\text{rms})/V_{\text{adc}}(\text{rms})$	uQ22.10	4	—	2,000.00	—	$A_{\text{RMS}}/V_{\text{ADC-RMS}}$
30	0x20088078	K_VB	R/W	ADC input voltage conversion factor = $V_B(\text{rms})/V_{\text{adc}}(\text{rms})$	uQ22.10	4	—	4,000.00	—	$V_{\text{RMS}}/V_{\text{ADC-RMS}}$
31	0x2008807C	K_IC	R/W	ADC input current conversion factor = $I_C(\text{rms})/V_{\text{adc}}(\text{rms})$	uQ22.10	4	—	2,000.00	—	$A_{\text{RMS}}/V_{\text{ADC-RMS}}$
32	0x20088080	K_VC	R/W	ADC input voltage conversion factor = $V_C(\text{rms})/V_{\text{adc}}(\text{rms})$	uQ22.10	4	—	4,000.00	—	$V_{\text{RMS}}/V_{\text{ADC-RMS}}$
33	0x20088084	K_IN	R/W	ADC input current conversion factor = $I_N(\text{rms})/V_{\text{adc}}(\text{rms})$	uQ22.10	4	—	2,000.00	—	$A_{\text{RMS}}/V_{\text{ADC-RMS}}$
34	0x20088088	CAL_M_IA	R/W	Current magnitude calibration constant, $I_A$	sQ2.29	4	-4.0000	+3.9999	+1.0000	—
35	0x2008808C	CAL_M_VA	R/W	Voltage magnitude calibration constant, $V_A$	sQ2.29	4	-4.0000	+3.9999	+1.0000	—
36	0x20088090	CAL_M_IB	R/W	Current magnitude calibration constant, $I_B$	sQ2.29	4	-4.0000	+3.9999	+1.0000	—
37	0x20088094	CAL_M_VB	R/W	Voltage magnitude calibration constant, $V_B$	sQ2.29	4	-4.0000	+3.9999	+1.0000	—
38	0x20088098	CAL_M_IC	R/W	Current magnitude calibration constant, $I_C$	sQ2.29	4	-4.0000	+3.9999	+1.0000	—
39	0x2008809C	CAL_M_VC	R/W	Voltage magnitude calibration constant, $V_C$	sQ2.29	4	-4.0000	+3.9999	+1.0000	—
40	0x200880A0	CAL_M_IN	R/W	Current magnitude calibration constant, $I_N$	sQ2.29	4	-4.0000	+3.9999	+1.0000	—
41	0x200880A4	CAL_PH_IA	R/W	Current phase calibration constant, $I_A$	sQ0.31	4	-1.000	+0.999	0	BAMS
42	0x200880A8	CAL_PH_VA	R/W	Voltage phase calibration constant, $V_A$	sQ0.31	4	-1.000	+0.999	0	BAMS
43	0x200880AC	CAL_PH_IB	R/W	Current phase calibration constant, $I_B$	sQ0.31	4	-1.000	+0.999	0	BAMS
44	0x200880B0	CAL_PH_VB	R/W	Voltage phase calibration constant, $V_B$	sQ0.31	4	-1.000	+0.999	0	BAMS
45	0x200880B4	CAL_PH_IC	R/W	Current phase calibration constant, $I_C$	sQ0.31	4	-1.000	+0.999	0	BAMS
46	0x200880B8	CAL_PH_VC	R/W	Voltage phase calibration constant, $V_C$	sQ0.31	4	-1.000	+0.999	0	BAMS
47	0x200880BC	CAL_PH_IN	R/W	Current phase calibration constant, $I_N$	sQ0.31	4	-1.000	+0.999	0	BAMS
48	0x200880C0	CAPTURE_CTRL	R/W	Waveform capture control register	uQ32.0	4	—	—	—	integer



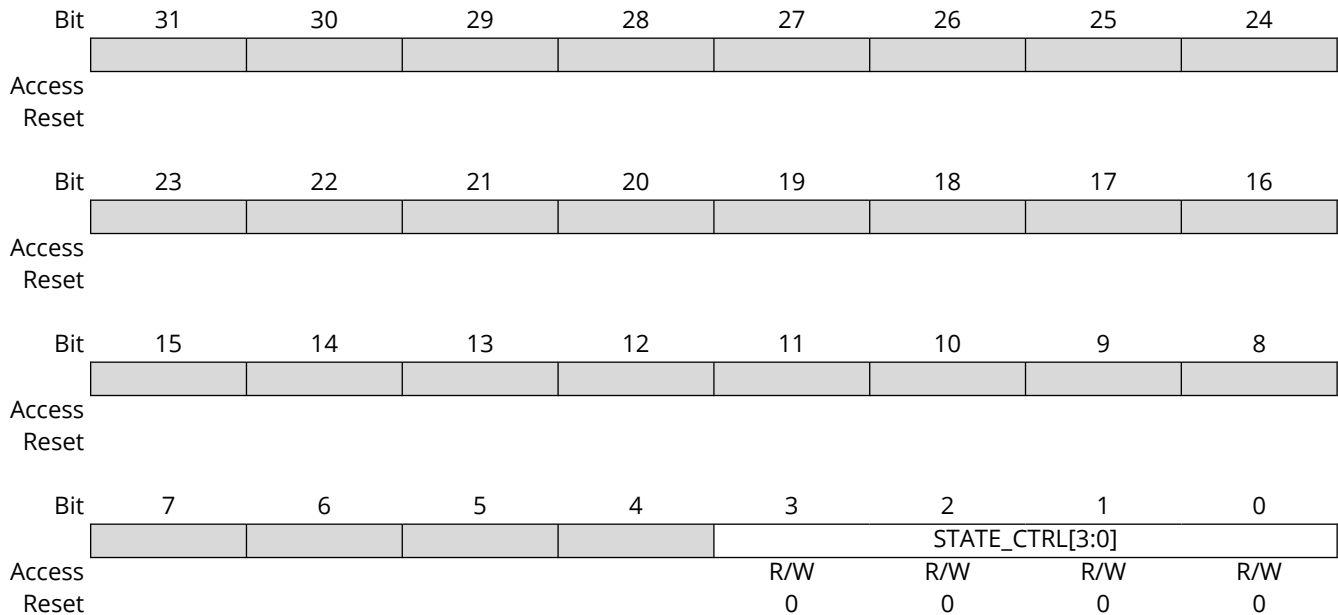
**Table 3-2.** Metrology Control Registers (continued)

Index	Address	Variable	Access Mode	Name	Format	No. of Bytes	Min Value	Max Value	Default	Units
49	0x200880C4	<a href="#">CAPTURE_BUFF_SIZE</a>	R/W	Waveform capture buffer size	uQ32.0	4	1	8000000	—	integer
50	0x200880C8	<a href="#">CAPTURE_ADDR</a>	R/W	Waveform capture buffer address pointer	uQ32.0	4	—	—	—	pointer
51	0x200880CC	RESERVED	—	—	—	4	—	—	—	—
52	0x200880D0	RESERVED	—	—	—	4	—	—	—	—
53	0x200880D4	RESERVED	—	—	—	4	—	—	—	—
54	0x200880D8	<a href="#">ATSENSE_CTRL_20_23</a>	R/W	ATSense control: channels I0,I1,V1,I2 (Registers_20_23)	uQ32.0	4	—	—	—	integer
55	0x200880DC	<a href="#">ATSENSE_CTRL_24_27</a>	R/W	ATSense control: channels V2,I3,V3,ANA (Registers_24_27)	uQ32.0	4	—	—	—	integer
56	0x200880E0	<a href="#">ATSENSE_CTRL_28_2B</a>	R/W	ATSense control: Registers: x28, x2A-2B, x2D	uQ32.0	4	—	—	—	integer
57	0x200880E4	RESERVED	—	—	—	4	—	—	—	—
58	0x200880E8	<a href="#">POWER_OFFSET_P_A</a>	R/W	Phase-A accumulation active power offset compensation used to eliminate voltage effects at small current (cross talk). Affects accumulator and pulse measurement.	sQ-9.40	4	-2.000	1.9999...	0.0	W-samp scaled
59	0x200880EC	<a href="#">POWER_OFFSET_P_B</a>	R/W	Phase-B accumulation active power offset compensation used to eliminate voltage effects at small current (cross talk). Affects accumulator and pulse measurement.	sQ-9.40	4	-2.000	1.9999...	0.0	W-samp scaled
60	0x200880F0	<a href="#">POWER_OFFSET_P_C</a>	R/W	Phase-C accumulation active power offset compensation used to eliminate voltage effects at small current (cross talk). Affects accumulator and pulse measurement.	sQ-9.40	4	-2.000	1.9999...	0.0	W-samp scaled
61	0x200880F4	<a href="#">POWER_OFFSET_Q_A</a>	R/W	Phase-A accumulation reactive power offset compensation used to eliminate voltage effects at small current (cross talk). Affects accumulator and pulse measurement.	sQ-9.40	4	-2.000	1.9999...	0.0	VAR-samp scaled
62	0x200880F8	<a href="#">POWER_OFFSET_Q_B</a>	R/W	Phase-B accumulation reactive power offset compensation used to eliminate voltage effects at small current (cross talk). Affects accumulator and pulse measurement.	sQ-9.40	4	-2.000	1.9999...	0.0	VAR-samp scaled
63	0x200880FC	<a href="#">POWER_OFFSET_Q_C</a>	R/W	Phase-C accumulation reactive power offset compensation used to eliminate voltage effects at small current (cross talk). Affects accumulator and pulse measurement.	sQ-9.40	4	-2.000	1.9999...	0.0	VAR-samp scaled

### 3.1.1. Metrology State Control

**Name:** STATE\_CTRL  
**Property:** Read-Write

State control bits input to Metrology module from application code.



**Bits 3:0 – STATE\_CTRL[3:0]** State control bits input to Metrology module from application code. Refer to [Interface in Initialization Stage](#) for a detailed description.

**Notes:** Before entering in a Low-Power mode the Core 0 application should reset the metrology to disable the internal regulator of the ATSENSE. This action reduces the consumption in Low-Power mode. The Core 0 application should follow these steps:

1. Write a '0' in the "STATE\_CTRL" control register.
2. Wait until the "STATUS" status register changes to "RESET".
3. Continue with the procedure to switch to a Low-Power mode.

Value	Name	Description
0x0	RESET	Reset metrology module, reset ATSENSE and halt metrology filters.
0x1	INIT	Input control registers are initialized and metrology can initialize itself.
0x2	RUN	Metrology filters are free to run, and outputs are updated at commanded rate.
OTHERS	RESERVED	Reserved values

### 3.1.2. Metrology Feature Control Register

**Name:** FEATURE\_CTRL

**Property:** Read-Write

The metrology feature control register contains the main control bits for overall metrology feature

**Note:** Bits 24:30: Channel selection for harmonics computation. These bits are used for disabling the harmonics computation on specific channels.

Bit	31	30	29	28	27	26	25	24
		IN_HARM_DIS	VC_HARM_DIS	IC_HARM_DIS	VB_HARM_DIS	IB_HARM_DIS	VA_HARM_DIS	IA_HARM_DIS
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	CREEP_S_EN	CREEP_P_EN	CREEP_Q_EN	CREEP_I_EN		V_MAX_RESET	I_MAX_RESET	SWAP_B_and_C
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8
				MAX_INT_SELECT	NEUTRAL_DIS	PHASE_C_EN	PHASE_B_EN	PHASE_A_EN
Access				R/W	R/W	RW	RW	RW
Reset				0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	RZC_THRESH_DIS		SYNCH[1:0]		RZC_DIR		RZC_CHAN_SELECT[2:0]	
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

#### Bit 30 – IN\_HARM\_DIS

Value	Description
0	Harmonic computation for channel IN (neutral current) is enabled.
1	Harmonic computation for channel IN (neutral current) is disabled.

#### Bit 29 – VC\_HARM\_DIS

Value	Description
0	Harmonic computation for channel VC (phase C voltage) is enabled.
1	Harmonic computation for channel VC (phase C voltage) is disabled.

#### Bit 28 – IC\_HARM\_DIS

Value	Description
0	Harmonic computation for channel IC (phase C current) is enabled.
1	Harmonic computation for channel IC (phase C current) is disabled.

#### Bit 27 – VB\_HARM\_DIS

Value	Description
0	Harmonic computation for channel VB (phase B voltage) is enabled.
1	Harmonic computation for channel VB (phase B voltage) is disabled.

**Bit 26 – IB\_HARM\_DIS**

Value	Description
0	Harmonic computation for channel IB (phase B current) is enabled.
1	Harmonic computation for channel IB (phase B current) is disabled.

**Bit 25 – VA\_HARM\_DIS**

Value	Description
0	Harmonic computation for channel VA (phase A voltage) is enabled.
1	Harmonic computation for channel VA (phase A voltage) is disabled.

**Bit 24 – IA\_HARM\_DIS**

Value	Description
0	Harmonic computation for channel IA (phase A current) is enabled.
1	Harmonic computation for channel IA (phase A current) is disabled.

**Bit 23 – CREEP\_S\_EN** Apparent Power Creep Threshold Feature Enable

Used to enable/disable metrology creep function of apparent power pulse generation and any associated ACC\_Tx total energy pulse value accumulators. Refer to [CREEP\\_THRESHOLD\\_S](#) for more information.

Value	Name	Description
0	DISABLED	Disable apparent power creep threshold feature.
1	ENABLED	Enable apparent power creep threshold feature.

**Bit 22 – CREEP\_P\_EN** Active Power Creep Threshold Feature Enable

Used to enable/disable metrology creep function of active power pulse generation and any associated ACC\_Tx total energy pulse value accumulators. Refer to [CREEP\\_THRESHOLD\\_P](#) for more information.

Value	Name	Description
0	DISABLED	Disable active power creep threshold feature.
1	ENABLED	Enable active power creep threshold feature.

**Bit 21 – CREEP\_Q\_EN** Reactive Power Creep Threshold Feature Enable

Used to enable/disable metrology creep function of reactive power pulse generation and any associated ACC\_Tx total quadergy pulse value accumulators. Refer to [CREEP\\_THRESHOLD\\_Q](#) for more information.

Value	Name	Description
0	DISABLED	Disable reactive power creep threshold feature.
1	ENABLED	Enable reactive power creep threshold feature.

**Bit 20 – CREEP\_I\_EN** Current Creep Threshold Feature Enable

Used to enable/disable creep function of metrology, both for pulse generation and any associated ACC\_Tx total pulse value accumulators. Current creep thresholding is used to kill pulse contribution from any or all phases below the current threshold and affects all enabled [P, Q, and I<sup>2</sup>] pulsing. Refer to [CREEP\\_THRESHOLD\\_I](#) for more information.

Value	Name	Description
0	DISABLED	Disable current creep threshold feature.
1	ENABLED	Enable current creep threshold feature.

**Bit 18 – V\_MAX\_RESET** Reset All V<sub>x</sub>\_MAX values in Metrology Status Registers

This bit will be cleared by the metrology firmware automatically.

Value	Description
1	Reset all V <sub>x</sub> _MAX values in Metrology Status Registers.

**Bit 17 – I\_MAX\_RESET** Reset All I<sub>x</sub>\_MAX values in Metrology Status Registers  
This bit will be cleared by the metrology firmware automatically.

Value	Description
1	Reset all I <sub>x</sub> _MAX values in Metrology Status Registers.

**Bit 16 – SWAP\_B\_and\_C** Swap I2/V2 to DSP processing channels I<sub>V</sub>/V<sub>C</sub> and vice versa.  
Applies for polyphase processing. Allows  $\Delta$ -Y transformation when using 2-element ATSense203 metering.  
If enabled, channel swap is performed before DSP channel calibration factors are applied.

Value	Description
0	DSP input mapping: I2/V2 mapped I <sub>B</sub> /V <sub>B</sub> ; I3/V3 mapped I <sub>C</sub> /V <sub>C</sub> (default).
1	DSP input mapping: I2/V2 mapped I <sub>C</sub> /V <sub>C</sub> ; I3/V3 mapped I <sub>B</sub> /V <sub>B</sub> .

**Bit 12 – MAX\_INT\_SELECT** Max Integration Period Select.  
Only applies if control word M = 0 (M = Number of cycles for integration period) and affects rounding when determining number of cycles closest to 1 sec.

Value	Description
0	Metrology DSP will integrate for an integral number of cycles closest to 1 second. Due to line frequency drift, the integration period may be slightly longer or shorter than 1 sec, bounded approximately by [0.99, 1.01] sec.
1	Metrology DSP will integrate for an integral number of cycles no greater than 1 second. Due to line frequency drift, the integration period will always be $\leq$ 1 sec, bounded by approximately by [0.98, 1.00] sec.

**Bit 11 – NEUTRAL\_DIS** Disable neutral measurement.  
Only applies when the neutral current and the temperature measurements are shared in the same channel, like in the PIC32CXMTx with external ATSense301. It does not apply to PIC32CXMTSH, including an internal ATSense203.

Value	Description
0	Neutral measurement is disabled, and the shared channel is continuously acquiring temperature readings.
1	Neutral and temperature measurements are acquired using the shared channel.

**Bits 8, 9, 10 – PHASE\_x\_EN** Enable Phase x (x = A, B or C).  
Selects phases used for pulse computation. At least one phase must be enabled for pulsing to function. For typical usage, enable all phases used for pulsing. This feature may be used to temporarily disable or exclude phases from pulse computation.

Value	Name	Description
0	DISABLED	Disable phase
1	ENABLED	Enable phase

**Bit 7 – RZC\_THRESH\_DIS** Raw Zero-Crossing Threshold Disable.  
Selects the raw Zero-Crossing detection algorithm threshold.

Value	Description
0	Threshold set to the average value computed in the last integration period.
1	Threshold set to 0.

**Bits 5:4 – SYNCH[1:0]** Dominant Voltage Channel Selection  
The energy integration period is determined by counting zero-crossings of a narrow-band filtered version of the dominant voltage phase. SYNCH is used to allow the metrology module to dynamically determine which voltage phase is the dominant voltage phase or to statically choose one particular phase for zero-crossing counting. In all cases of active phase cycle counting, measurement

quantities are integrated over M-number of (negative-to-positive) zero-crossings. We recommend the sync phase is appointed, especially for a single phase application.

Value	Description
0x0	Measurement interval based on dominant phase, determined dynamically.
0x1	Measurement interval based on phase-A.
0x2	Measurement interval based on phase-B.
0x3	Measurement interval based on phase-C.

### Bit 3 – RZC\_DIR Raw Zero-Crossing Direction Selection

Raw Zero-Crossing Direction selects either positive-going or negative-going raw zero-crossings trigger the IPC interrupt: IPC\_RAW\_ZERO\_CROSSING.

Value	Name	Description
0	POSITIVE	Positive-going raw zero-crossings selected.
1	NEGATIVE	Negative-going raw zero-crossings selected.

### Bits 2:0 – RZC\_CHAN\_SELECT[2:0] Raw Zero-Crossing Channel Select and Enable

Raw Zero-Crossing allows detection of zero-crossings using the raw 16 kHz input voltage channel samples. Unlike the zero-crossing detection used for timing decisions that use a 4 kHz fundamental-only filtered data stream, the Raw Zero-Crossing detection feature has no frequency-dependent group delay nor any appreciable bulk filter delay.

Value	Description
0x0	Raw Zero-Crossing detection is disabled.
0x1	Raw Zero-Crossing detection based on input voltage channel V1.
0x3	Raw Zero-Crossing detection based on input voltage channel V2.
0x5	Raw Zero-Crossing detection based on input voltage channel V3.

### 3.1.3. Harmonic Control Register

**Name:** HARMONIC\_CONTROL

**Property:** Read-Write

The metrology feature control register contains the main control bits for the overall metrology feature.

Bit	31	30	29	28	27	26	25	24
	HARMONIC_EN	HARMONIC_m_REQ[30:24]						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	HARMONIC_m_REQ[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	HARMONIC_m_REQ[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	HARMONIC_m_REQ[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

#### Bit 31 – HARMONIC\_EN Enable Harmonic Analysis

Value	Name	Description
0	DISABLED	Disable harmonic analysis
1	ENABLED	Enable harmonic analysis

#### Bits 30:0 – HARMONIC\_m\_REQ[30:0] Request number of harmonic for analysis

Harmonic analysis will be computed for the selected harmonic orders specified in this field. The analysis will produce accurate results when a whole integration period is elapsed. Consequently, the application must discard the results generated in the integration period when the analysis was enabled or the harmonic selection changed.



#### WARNING

Although the control register can enable up to 31 harmonic orders, the frequency response may be limited by the metrology filters or the input network anti-aliasing filters. With respect to the metrology filters, the accuracy is better than 0.007% up to 1386 Hz, ensuring an extremely accurate response up to the 21<sup>st</sup> harmonic order (considering a fundamental frequency of 60 Hz, with a 10% deviation). However, the response remains relatively flat up to 1650 Hz, with an error margin of up to 0.05%.

### 3.1.4. Meter Type Settings Register

**Name:** METER\_TYPE

**Property:** Read-Write

This register defines the service type settings and type of meter voltage and current sensors.

Bit	31	30	29	28	27	26	25	24
	Dto4WY_TRANSFORM		MISSING_PHASE[1:0]		SERVICE_TYPE[3:0]			
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
			SENSOR_TYPE_I_N[1:0]		SENSOR_TYPE_V_C[1:0]		SENSOR_TYPE_I_C[1:0]	
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	SENSOR_TYPE_V_B[1:0]		SENSOR_TYPE_I_B[1:0]		SENSOR_TYPE_V_A[1:0]		SENSOR_TYPE_I_A[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

#### Bit 31 – Dto4WY\_TRANSFORM

For use with: 4-Wire and 3-Wire DELTA meters only. Phase voltages (and currents, where applicable) are transformed into an equivalent 4-wire Wye service for metering using alternate equations.

Value	Name	Description
0x0	DISABLED	Phase voltages remain in native service (no transformation).
0x1	ENABLED	Phase voltages transformed into an equivalent 4-wire Wye service. Transformation may lose accuracy in non-Blondel/unbalanced situations. Meter vector transformation is useful in some applications and possible, transforming 3-Phase Delta meters into an equivalent 3-Phase 4WY, but is useful only for balanced voltage situations.

#### Bits 29:28 – MISSING\_PHASE[1:0] Missing phase voltage select

For use with Poly-phase 4-wire Wye 2-1/2 element meters only

Value	Description
0x0	Generate missing phase voltage for Phase_A: $V_A = -(V_B + V_C)$ ;
0x1	Generate missing phase voltage for Phase_B: $V_B = -(V_A + V_C)$ ;
0x2	Generate missing phase voltage for Phase_C: $V_C = -(V_A + V_B)$ .

#### Bits 27:24 – SERVICE\_TYPE[3:0] Electrical Service Type

The service type determines what meter form is being implemented and how the Metrology DSP core interprets and processes the ADC values. For more information, refer to [Annex. Meter Forms](#).

Value	Name	Description
0x0	3P4WY_3E_3V3I	Three-phase 4-wire Wye (3-element)
0x1	3P4WD_3E_3V3I	Three-phase 4-wire Delta (3-element)
0x2	3P3P4WY_2p5E_2V3I	Three-phase 4-wire Wye (2-½ element)
0x3	3P4WD_2E_3V2I	Three-phase 4-wire Delta (2-element)



Value	Name	Description
0x4	3P3WD_2E_2V2I	Three-phase 3-wire) Delta (2-element)
0x5	2P3W_2E_2V2I	Two-phase 3-wire Network (2 element)
0x6	1P3W_1p5E_1V2I	Single-phase 3-wire (1-½ element)
0x7	1P2W_1E_1V1I	Single-phase 2-wire (1 element)
0x8	1P3W_1E_2V1I	Single-phase 3-wire (1 element)

**Bits 13:12 – SENSOR\_TYPE\_I\_N[1:0]** Current Sensor Type on N Phase

Selects the types of current and voltage sensor used. Read the following table for additional information.

**Bits 11:10 – SENSOR\_TYPE\_V\_C[1:0]** Voltage Sensor Type on C Phase

Selects the types of current and voltage sensor used. For each channel selected as using a Rogowski sensor, the Metrology DSP implements a digital integrator filter to normalize the effects of the sensor's di/dt behavior.

Value	Name	Description
0x0	CURRENT TRANSFORMER	—
0x1	RESISTIVE SHUNT	May only be used with phase-to-neutral voltage measurement applications.
0x2	ROGOWSKI COIL (CRC) CURRENT SENSOR	A digital integrator function is added to the DSP of all current channels selected as using Rogowski Coils. When SENSOR_TYPE_I_x = 2, an additional phase correction is internally added to each channel with a Rogowski sensor in the amount of -0.3704° (@ 60 Hz) to correct for a linear phase response introduced by the digital integrator filter. This is taken into account during the internal calculation of actual phase-correction filter coefficients, when a new set of phase calibration settings are loaded, and must not be added by the user in the phase-correction entries. When SENSOR_TYPE_I_x is set to other values, it takes no effect.
0x3	RESISTIVE DIVIDER (VRD) VOLTAGE SENSOR	Normally, this is the typical option selected for voltage sensors.

**Bits 9:8 – SENSOR\_TYPE\_I\_C[1:0]** Current Sensor Type on C Phase

Selects the types of current and voltage sensor used. Read the previous table for additional information.

**Bits 7:6 – SENSOR\_TYPE\_V\_B[1:0]** Voltage Sensor Type on B Phase

Selects the types of current and voltage sensor used. Read the previous table for additional information.

**Bits 5:4 – SENSOR\_TYPE\_I\_B[1:0]** Current Sensor Type on B Phase

Selects the types of current and voltage sensor used. Read the previous table for additional information.

**Bits 3:2 – SENSOR\_TYPE\_V\_A[1:0]** Voltage Sensor Type on A Phase

Selects the types of current and voltage sensor used. Read the previous table for additional information.

**Bits 1:0 – SENSOR\_TYPE\_I\_A[1:0]** Current Sensor Type on A Phase

Selects the types of current and voltage sensor used. Read the previous table for additional information.

### 3.1.5. Number of Line Cycles for Integration Period

**Name:** M

**Property:** Read-Write

The measurement time unit,  $t_M$ , or integration period, is delineated by M-number of negative-to-positive zero-crossings of the fundamental frequency using a selected voltage signal. All primary output quantities are computed for this many number of cycles of the fundamental frequency.

M is the number of cycles of the integration period are provided as input into the metrology module.

**Note:** After changing this register, verify the value of the N\_MAX register.

**Note:** If the phase voltage for frequency determination is not present, defined as  $\geq 1/32$  of max range, then the metrology module transitions to a default integration period of "N\_MAX" samples. If phase voltage loss occurs before the expected number, then that specific integration period may end with some intermediate number of samples. In all cases, the number of samples used in an integration period is available in the output Register N, at the end of an integration period.

Presently, fixed-precision accumulation is scaled for a maximum integration period of 30 seconds (given max V & I inputs). This has to be changed if a one-minute integration period is desired.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
					M[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	7	6	5	4	3	2	1	0
	M[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

#### Bits 11:0 – M[11:0] (uQ12.0)

Value	Description
0	Number of cycles for the measurement period will be determined automatically as the number of cycles closest to 1.0 second of integration time. The number of cycles is variable and the measurement period, $t_M$ , will closely track 1.0 sec of measurement time, regardless of line frequency.
Other	Number of cycles is fixed and the measurement period, $t_M$ , will vary with line frequency.

### 3.1.6. Max Number of Samples in an Integration Period

**Name:** N\_MAX

**Property:** Read-Write

The maximum number of samples in a measurement time period must be defined, in case of loss of dominant voltage phase detection and zero-crossing cycle synchronization. "N\_MAX" and "M" must be chosen in such a way that "N\_MAX" is large enough to consider the expected number samples in the number of line cycles for the integration period.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	N_MAX[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	N_MAX[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	N_MAX[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 23:0 – N\_MAX[23:0]** (uQ24.0)

### 3.1.7. Pulse Control Register x (x = 0, 1, 2)

**Name:** PULSEx\_CTRL

**Property:** Read-Write

Three pulses can be generated simultaneously: PULSE0\_CTRL is used to control the pulse output from PD17, PULSE1\_CTRL is used to control the pulse output from PD18, and PULSE2\_CTRL is used to control the pulse output from PD19. IPC interrupts are triggered at each pulse: IPC\_PULSEx.

Bit	31	30	29	28	27	26	25	24
	PCx_ENABLE		PCx_DETENT[1:0]			PCx_ACC_HOLD	PCx_OVERRIDE	PCx_POLARITY
Access	R/W		R/W	R/W		R/W	R/W	R/W
Reset	0		0	0		0	0	0
Bit	23	22	21	20	19	18	17	16
					PCx_TYPE[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	15	14	13	12	11	10	9	8
	PCx_WIDTH[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	PCx_WIDTH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

#### Bit 31 – PCx\_ENABLE Output Pulse Enable

Used to enable or disable pulse functionality. For short-term disable of pulses, use the PC\_OVERRIDE control bit.

Value	Description
0x0	Pulse output disabled, inactive level determined by PULSE_POLARITY
0x1	Pulse output enabled

#### Bits 29:28 – PCx\_DETENT[1:0] Total Absolute Values for P and Q values

When creating P and Q accumulator totals of multiple phases, this option allows taking the absolute values of each phase before adding to make the total. This is used to primarily ignore direction of energy delivered or generated for pulse generation.

Value	Name	Description
0x0	NET	Pulses generated based on (energy delivered – energy generated): Individual sign of each channel's P and Q is taken into account when creating total P and Q accumulator sums.
0x1	ABSOLUTE	Pulses generated based on (energy delivered + energy generated): The absolute value of each phase's P and Q is used when creating the total P and Q accumulator sums.
0x2	DELIVERED	Pulses generated based on (delivered only): Only positive values (energy delivered) of each phase's P and Q are used when creating the total P and Q accumulator sums, with negative values (energy generated) being ignored.
0x3	GENERATED	Pulses generated based on (generated only): Only negative values (energy generated) of each phase's P and Q are used when creating the total P and Q accumulator sums, with positive values (energy delivered) being ignored.

#### Bit 26 – PCx\_ACC\_HOLD Pulse Accumulation Hold Control

Value	Description
0x0	Pulse accumulation registers continue to increment even if pulse generation is temporarily disabled.
0x1	Pulse accumulation is held static. All incremental quantities normally used for pulse determination are discarded.

**Bit 25 – PCx\_OVERRIDE** Pulse Override Control

Use to temporarily disable pulse generation. While disabled, pulse accumulation functions as selected with the PC\_ACC\_HOLD control bit.

Value	Description
0x0	Pulse generation functions as normal
0x1	Pulse generation is temporarily disabled

**Bit 24 – PCx\_POLARITY** Pulse Polarity

Value	Description
0x0	Output pulse is low with width set by K_WIDTH, followed by an inactive level of high
0x1	Output pulse is high with width set by K_WIDTH, followed by an inactive level of low

**Bits 19:16 – PCx\_TYPE[3:0]** Pulse Type Selection

Types described as “all phases” are based on all active phases: [A,B,C]. Types described as “S” use only the synthesized voltage channel, phase: [S] if available.

Value	Name	Description
0x0	P_T	Watt-hours, total all phases, fundamental + harmonics.
0x1	P_T_F	Watt-hours, total all phases, fundamental only.
0x2	Q_T	Var-hours, total all phases, fundamental + harmonics.
0x3	Q_T_F	Var-hours, total all phases, fundamental only.
0x4	I_T	Amp-squared-hours, total all phases, fundamental + harmonics.
0x5	I_T_F	Amp-squared-hours, total all phases, fundamental only.
0x6	S_T	VA-hours, total all phases, fundamental + harmonics. It is computed by multiplying Irms by Vrms.
0x7	S_T_F	VA-hours, total all phases, fundamental only. It is computed by multiplying Irms (fundamental) by Vrms (fundamental).
0x8	S2_T	VA-hours, total all phases. It is computed as the square root of (P <sup>2</sup> +Q <sup>2</sup> ).
0x9–0xF	Reserved	—

**Bits 15:0 – PCx\_WIDTH[15:0]** Pulse Width

The granularity for pulse width is in units of 2.1552 μs, corresponding to a clock rate of 464 kHz. The peripheral clock was incremented to 7.424 MHz in version 3.1.00, but the granularity of the pulse width does not change to assure compatibility with previous versions.

$PCx\_WIDTH = PULSE\_WIDTH[sec] \times 464000$

For example, for a desired pulse width of 750 μs, the computation for the value PCx\_WIDTH will be:

$$PCx\_WIDTH = 750 \times 10^{-6} \times 464000 = 348 = 0x015C$$

There is a limitation on the maximum frequency of pulse occurrence: the pulse period duration cannot exceed the sum of the pulse width plus an additional 500 microseconds.

For example, if the pulse width is set at 500 microseconds, the maximum pulse frequency that can be attained is 1 kHz. On the other hand, if the pulse width is reduced to 50 microseconds, the pulse frequency can increase to a maximum of 1.818 kHz.

### 3.1.8. Meter Active Power Pulse Constant

**Name:** P\_K\_t

**Property:** Read-Write

P\_K\_t register defines the meter test constant, which is the amount of active energy signified by one output pulse. P\_K\_t is in units of [Wh/pulse]. P\_K\_t is stored in uQ8.24 format.

In Europe and Asia, the pulse constant, MC, is used where MC is in units of [pulses/kWh]. First, convert from units of MC to units of P\_K\_t ( $P_K_t = 1000/MC$ ), then convert into uQ8.24 format by multiplying by  $2^{24}$ .

For example, if  $MC = 800$  pulses/kWh, then  $P_K_t = 1000/800 = 1.25$  Wh/pulse and  $P_K_t = \text{round}[1.25 \times 2^{24}] = 20971520 = 0x01400000$

The frequency of pulse output generated depends on the quantity of energy measured and the defined pulse constants (P\_K\_t, Q\_K\_t, I\_K\_t, and S\_K\_t). It is important to note that there is a limitation on the maximum frequency of pulse occurrence: the pulse period duration cannot exceed the sum of the pulse width plus an additional 500 microseconds.

For example, if the pulse width is set at 500 microseconds, the maximum pulse frequency that can be attained is 1 kHz. On the other hand, if the pulse width is reduced to 50 microseconds, the pulse frequency can increase to a maximum of 1.818 kHz.

Updates to P\_K\_t take effect at the next negative zero-crossing (narrow-band filtered version) of the present control phase voltage channel.

Bit	31	30	29	28	27	26	25	24
	P_K_t[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	P_K_t[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	P_K_t[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	P_K_t[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – P\_K\_t[31:0] (uQ8.24)**

### 3.1.9. Meter Reactive Power Pulse Constant

**Name:** Q\_K\_t  
**Property:** Read-Write

Q\_K\_t defines the meter test constant, which is the amount of reactive energy signified by one output pulse. Q\_K\_t is in units of [VARh/pulse].

Q\_K\_t is stored in uQ8.24 format.

In Europe and Asia, the pulse constant, MC, is used where MC is in units of [pulses/kVARh]. First, convert from units of MC to units of Q\_K\_t ( $Q_K_t = 1000/MC$ ), then convert into uQ8.24 format by multiplying by  $2^{24}$ .

For example, if  $MC = 800$  pulses/kVARh, then  $Q_K_t = 1000/800 = 1.25$  VARh/pulse, and  $Q_K_t = \text{round}[1.25 \times 2^{24}] = 20971520 = 0x01400000$

The frequency of pulse output generated depends on the quantity of energy measured and the defined pulse constants (P\_K\_t, Q\_K\_t, I\_K\_t, and S\_K\_t). It is important to note that there is a limitation on the maximum frequency of pulse occurrence: the pulse period duration cannot exceed the sum of the pulse width plus an additional 500 microseconds.

For example, if the pulse width is set at 500 microseconds, the maximum pulse frequency that can be attained is 1 kHz. On the other hand, if the pulse width is reduced to 50 microseconds, the pulse frequency can increase to a maximum of 1.818 kHz.

Updates to Q\_K\_t take effect at the next negative zero-crossing (narrow-band filtered version) of the present control phase voltage channel.

Bit	31	30	29	28	27	26	25	24
	Q_K_t[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	Q_K_t[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	Q_K_t[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	Q_K_t[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – Q\_K\_t[31:0] (uQ8.24)**

### 3.1.10. Meter Current Pulse Constant

**Name:** I\_K\_t

**Property:** Read-Write

I\_K\_t defines the meter test constant, which is the amount of Amp<sup>2</sup>-h signified by one output pulse. I\_K\_t is in units of [Amp<sup>2</sup>-h/pulse].

I\_K\_t is stored in uQ8.24 format.

In Europe and Asia, the pulse constant, MC, is used where MC is in units of [pulses/kAmp<sup>2</sup>-h]. First, convert from units of MC to units of I\_K\_t

(I\_K\_t = 1000/MC), then convert into uQ8.24 format by multiplying by 2<sup>24</sup>.

For example, if MC=800 pulses/kAmp<sup>2</sup>-h, then I\_K\_t = 1000/800 = 1.25 I<sup>2</sup>-h/pulse, and:

I\_K\_t = round[1.25 × 2<sup>24</sup>] = 20971520 = 0x01400000

The frequency of pulse output generated depends on the quantity of energy measured and the defined pulse constants (P\_K\_t, Q\_K\_t, I\_K\_t, and S\_K\_t). It is important to note that there is a limitation on the maximum frequency of pulse occurrence: the pulse period duration cannot exceed the sum of the pulse width plus an additional 500 microseconds.

For example, if the pulse width is set at 500 microseconds, the maximum pulse frequency that can be attained is 1 kHz. On the other hand, if the pulse width is reduced to 50 microseconds, the pulse frequency can increase to a maximum of 1.818 kHz.

Updates to I\_K\_t take effect at the next negative zero-crossing (narrow-band filtered version) of the present control phase voltage channel.

Bit	31	30	29	28	27	26	25	24
	I_K_t[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	I_K_t[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	I_K_t[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	I_K_t[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – I\_K\_t[31:0] (uQ8.24)**



### 3.1.11. Meter Apparent Power Pulse Constant

**Name:** S\_K\_t

**Property:** Read-Write

S\_K\_t defines the meter test constant, which is the amount of apparent energy signified by one output pulse. S\_K\_t is in units of [VAh/pulse].

S\_K\_t is stored in uQ8.24 format.

In Europe and Asia, the pulse constant, MC, is used where MC is in units of [pulses/kVAh]. First, convert from units of MC to units of S\_K\_t ( $S_K_t = 1000/MC$ ), then convert into uQ8.24 format by multiplying by  $2^{24}$ .

For example, if  $MC = 800$  pulses/kVAh, then  $S_K_t = 1000/800 = 1.25$  VAh/pulse, and  $S_K_t = \text{round}[1.25 \times 2^{24}] = 20971520 = 0x01400000$

The frequency of pulse output generated depends on the quantity of energy measured and the defined pulse constants (P\_K\_t, Q\_K\_t, I\_K\_t and S\_K\_t). It is important to note that there is a limitation on the maximum frequency of pulse occurrence: the pulse period duration cannot exceed the sum of the pulse width plus an additional 500 microseconds.

For example, if the pulse width is set at 500 microseconds, the maximum pulse frequency that can be attained is 1 kHz. On the other hand, if the pulse width is reduced to 50 microseconds, the pulse frequency can increase to a maximum of 1.818 kHz.

Updates to S\_K\_t take effect at the next negative zero-crossing (narrow-band filtered version) of the present control phase voltage channel.

Bit	31	30	29	28	27	26	25	24
	S_K_t[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	S_K_t[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	S_K_t[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	S_K_t[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – S\_K\_t[31:0]** (uQ8.24)

### 3.1.12. Creep Threshold for Active Energy

**Name:** CREEP\_THRESHOLD\_P

**Property:** Read-Write

Total active energy pulse quantities in any one line cycle interval less than the creep threshold are reset to zero and are not accumulated.

CREEP\_THRESHOLD\_P is the creep active energy (Watt-hour) in a full cycle (20 ms for 50 Hz, 16.667 ms for 60 Hz).

CREEP\_THRESHOLD\_P is stored in uQ2.30 format.

If the creep active power is set to 11 Watt, and the system frequency is 60 Hz, then  
 $CREEP\_THRESHOLD\_P = \text{round} [11 / (60 * 3600) * 2^{30}] = 54681 = 0x0000D599$

Bit	31	30	29	28	27	26	25	24
	CREEP_THRESHOLD_P[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	CREEP_THRESHOLD_P[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	CREEP_THRESHOLD_P[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	CREEP_THRESHOLD_P[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – CREEP\_THRESHOLD\_P[31:0] (uQ2.30)**

### 3.1.13. Creep Threshold for Quadergy

**Name:** CREEP\_THRESHOLD\_Q

**Property:** Read-Write

Total reactive energy pulse quantities in any one line cycle interval less than the creep threshold are reset to zero and are not accumulated.

CREEP\_THRESHOLD\_Q is the creep reactive energy (Var-hour) in a full cycle (20 ms for 50 Hz, 16.667 ms for 60 Hz).

CREEP\_THRESHOLD\_Q is stored in uQ2.30 format.

If the creep active power is set to 11 VAR, and the system frequency is 60 Hz, then  
 $CREEP\_THRESHOLD\_Q = \text{round}[11/(60*3600)*2^{30}] = 54681 = 0x0000D599$

Bit	31	30	29	28	27	26	25	24
	CREEP_THRESHOLD_Q[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	CREEP_THRESHOLD_Q[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	CREEP_THRESHOLD_Q[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	CREEP_THRESHOLD_Q[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – CREEP\_THRESHOLD\_Q[31:0] (uQ2.30)**

### 3.1.14. Creep Threshold of Phase Current

**Name:** CREEP\_THRESHOLD\_I  
**Property:** Read-Write

For each phase with a current less than threshold CREEP\_THRESHOLD\_I in any one line cycle interval, any contributions to a selected pulse are zeroed out, and quantities from that phase make no contribution toward any selected pulse and its associated pulse accumulator.

CREEP\_THRESHOLD\_I is stored in uQ12.20 format and the unit is mArms-scaled (normalized by a common K\_I). A single common K\_I is used for all phases for CREEP\_THRESHOLD\_I determination.

$$CREEP\_THRESHOLD\_I = \frac{I_{CREEP-RMS}}{K_I} \times 2^{20}$$

For example, for a desired creep threshold of 10 mA, K\_I = 617.28396, then CREEP\_THRESHOLD\_I = round[(10/617.28396)\*2<sup>20</sup>] = 16987 = 0x0000425B

Bit	31	30	29	28	27	26	25	24
	CREEP_THRESHOLD_I[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	CREEP_THRESHOLD_I[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	CREEP_THRESHOLD_I[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	CREEP_THRESHOLD_I[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – CREEP\_THRESHOLD\_I[31:0] (uQ12.20)**

### 3.1.15. Creep Threshold for Apparent Energy

**Name:** CREEP\_THRESHOLD\_S

**Property:** Read-Write

Total apparent energy pulse quantities in any one line cycle interval less than the creep threshold are reset to zero and are not accumulated.

CREEP\_THRESHOLD\_S is the creep active energy (VA-hour) in a full cycle (20 ms for 50 Hz, 16.667 ms for 60 Hz).

CREEP\_THRESHOLD\_S is stored in uQ2.30 format.

If the creep apparent power is set to 11 WA, and the system frequency is 60 Hz, then  
 $CREEP\_THRESHOLD\_S = \text{round} [11 / (60 * 3600) * 2^{30}] = 54681 = 0x0000D599$ .

Bit	31	30	29	28	27	26	25	24
	CREEP_THRESHOLD_S[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	CREEP_THRESHOLD_S[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	CREEP_THRESHOLD_S[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	CREEP_THRESHOLD_S[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – CREEP\_THRESHOLD\_S[31:0] (uQ2.30)**

### 3.1.16. Power Offset Control Register

**Name:** POWER\_OFFSET\_CTRL

**Property:** Read-Write

Bit	31	30	29	28	27	26	25	24
	P_OFFSET_PUL				Q_OFFSET_PUL			S_OFFSET_PUL
Access	R/W				R/W			R/W
Reset	0				0			0

Bit	23	22	21	20	19	18	17	16
		P_OFFSET_AC_C_C	P_OFFSET_AC_C_B	P_OFFSET_AC_C_A		Q_OFFSET_AC_C_C	Q_OFFSET_AC_C_B	Q_OFFSET_AC_C_A
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

#### Bit 31 – P\_OFFSET\_PUL Active Power Offset for Pulse Quantities Enable

P\_OFFSET\_PUL is used to enable active power offset functionality for pulse quantities only.

P\_OFFSET\_PUL uses register POWER\_OFFSET\_P affecting: active energy pulse generation and TX pulse accumulation registers.

Value	Name	Description
0x0	DISABLE	Disables offset
0x1	ENABLE	Enables offset

#### Bit 27 – Q\_OFFSET\_PUL Reactive Power Offset for Pulse Quantities Enable

Q\_OFFSET\_PUL is used to enable reactive power offset functionality for pulse quantities only.

Q\_OFFSET\_PUL uses register POWER\_OFFSET\_Q affecting: reactive quadergy pulse generation and TX pulse accumulation registers.

Value	Name	Description
0x0	DISABLE	Disable offset
0x1	ENABLE	Enable offset

#### Bit 24 – S\_OFFSET\_PUL Apparent Power Offset for Pulse Quantities Enable

S\_OFFSET\_PUL is used to enable apparent power offset functionality for pulse quantities only.

S\_OFFSET\_PUL uses register POWER\_OFFSET\_S affecting: apparent energy pulse generation and TX pulse accumulation registers.

Value	Name	Description
0x0	DISABLE	Disable offset
0x1	ENABLE	Enable offset

**Bits 20, 21, 22 – P\_OFFSET\_ACC\_x** Active Power Offset for Accumulator Quantities Enable

P\_OFFSET\_ACC\_x is used to enable per-channel active power offset added to the 64-bit processing stream. P\_OFFSET\_ACC\_x uses registers POWER\_OFFSET\_P\_x affecting: ACC\_P\_x 64-bit accumulators, active energy pulse generation and TX pulse accumulation registers.

Value	Name	Description
0x0	DISABLE	Disable offset
0x1	ENABLE	Enable offset

**Bits 16, 17, 18 – Q\_OFFSET\_ACC\_x** Reactive Power Offset for Accumulator Quantities Enable

Q\_OFFSET\_ACC\_x is used to enable per-channel reactive power offset added to the 64-bit processing stream. Q\_OFFSET\_ACC\_x uses registers POWER\_OFFSET\_Q\_x affecting: ACC\_Q\_x 64-bit accumulators, reactive quadergy pulse generation and TX pulse accumulation registers.

Value	Name	Description
0x0	DISABLE	Disable offset
0x1	ENABLE	Enable offset

### 3.1.17. Active Power Offset Register

**Name:** POWER\_OFFSET\_P

**Property:** Read-Write

This value indicates the active power offset of appointed pulse.

The physical significance of POWER\_OFFSET\_P is total active energy (W-hour) offset per full cycle (20 ms for 50 Hz, 16.667 ms for 60 Hz).

POWER\_OFFSET\_P is stored in sQ1.30 format and is subtracted each full cycle.

POWER\_OFFSET\_P affects only P and P\_F pulse generation and ACC\_Tx pulse accumulators.

Refer to “PIC32CXMTx Metrology User Guide” (DS50003460) for a more detailed description.

Bit	31	30	29	28	27	26	25	24
	POWER_OFFSET_P[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	POWER_OFFSET_P[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	POWER_OFFSET_P[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	POWER_OFFSET_P[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – POWER\_OFFSET\_P[31:0]** (sQ1.30)



### 3.1.18. Reactive Power Offset Register

**Name:** POWER\_OFFSET\_Q

**Property:** Read-Write

This value indicates the reactive power offset of appointed pulse.

The physical significance of POWER\_OFFSET\_Q is total reactive energy (VAR-hour) offset per full cycle (20 ms for 50 Hz, 16.667 ms for 60 Hz).

POWER\_OFFSET\_Q is stored in sQ1.30 format and is subtracted each full cycle.

POWER\_OFFSET\_Q affects only Q and Q\_F pulse generation and ACC\_Tx pulse accumulators.

Refer to "PIC32CXMTx Metrology User Guide" (DS50003460) for a more detailed description.

Bit	31	30	29	28	27	26	25	24
	POWER_OFFSET_Q[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	POWER_OFFSET_Q[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	POWER_OFFSET_Q[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	POWER_OFFSET_Q[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – POWER\_OFFSET\_Q[31:0] (sQ1.30)**

### 3.1.19. Apparent Power Offset Register

**Name:** POWER\_OFFSET\_S

**Property:** Read-Write

This value affects the apparent power offset of appointed pulse.

The parameter POWER\_OFFSET\_S represents the total squared current (Amp<sup>2</sup>-hour/cycle) offset per full cycle (20 ms for 50 Hz, 16.667 ms for 60 Hz). This offset is subtracted from the current value used to calculate the apparent power:  $S = V_{rms} \times (I_{rms} - \text{POWER\_OFFSET\_S})$ .

Usage example (two alternatives):

1. To achieve the most accurate result, measure an apparent power load curve with the apparent power offset disabled. Follow this procedure:
  - a. Mathematically calculate the current offset causing the measured errors, in mA.
  - b. Convert this value to the units of POWER\_OFFSET\_S.
  - c. Example:
    - i. The current RMS causing the errors is 21 mA.
    - ii.  $K_I = 617.284$ .
    - iii. Frequency is 50 Hz, resulting in 80 samples per cycle.
    - iv.  $\text{POWER\_OFFSET\_S} = 80 \times 2^{40} \times (0.021 / 617.284)^2 = 101802$ .
2. For a faster computation, use the accumulators I\_A, I\_B, and I\_C, following this procedure:
  - a. Apply the nominal voltage to the meter and set the current to zero.
  - b. Read the I\_A, I\_B, and I\_C accumulators and compute the average. For improved accuracy, take multiple measurements or increase the integration period.
  - c. Calculate the corresponding value for a single cycle.
  - d. Example:
    - i.  $I_A = 52687391$ ,  $I_B = 39070069$ ,  $I_C = 47225301$ .
    - ii.  $I_{\text{Average}} = 46327587$ .
    - iii. Samples accumulated = 40000 (approximately 10 seconds).
    - iv. Samples in 1 cycle = 80 (50 Hz).
    - v.  $\text{POWER\_OFFSET\_S} = 46327587 \times 80 / 40000 = 105375$ .

This register can be used with pulse types 6 (S) and 7 (S\_F), but it must not be used with pulse type 8. For pulse type 8 the per-phase active and reactive power offsets must be used.

POWER\_OFFSET\_S is stored in sQ1.30 format and it is applied each full cycle.

POWER\_OFFSET\_S affects only S and S\_F pulse generation and ACC\_Tx pulse accumulators.

Refer to "PIC32CXMTx Metrology User Guide" (DS50003460) for a more detailed description.

Bit	31	30	29	28	27	26	25	24
	POWER_OFFSET_S[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	POWER_OFFSET_S[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	POWER_OFFSET_S[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	POWER_OFFSET_S[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – POWER\_OFFSET\_S[31:0]** (sQ1.30)

### 3.1.20. Voltage Swell Threshold

**Name:** SWELL\_THRESHOLD\_Vx

**Property:** Read-Write

For each half cycle of the fundamental period,  $V_{x_{RMS}}$  is calculated, per phase, and compared to the value set in SWELL\_THRESHOLD\_Vx: where  $x = [A, B, C]$ , to determine if a voltage swell condition exists. For each half cycle that a voltage swell exists, the associated flag, SWELL\_DET\_Vx is set to 1.

A threshold is allowed for each phase and is computed using the native phase voltages before transformation to implied 4WY service. This allows setting different thresholds for non-balanced service types.

SWELL\_THRESHOLD\_Vx is stored in uQ0.32 format. So, set the threshold value as follows:

$$V_{x \text{ SWELL\_THRESHOLD}} = \left( \frac{V_{\text{SWELL-RMS}}}{K_{Vx}} \right)^2 \times 2^{32}$$

Bit	31	30	29	28	27	26	25	24
	SWELL_THRESHOLD_Vx[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	SWELL_THRESHOLD_Vx[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	SWELL_THRESHOLD_Vx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	SWELL_THRESHOLD_Vx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – SWELL\_THRESHOLD\_Vx[31:0] (uQ0.32)**

### 3.1.21. Voltage Sag Threshold

**Name:** SAG\_THRESHOLD\_Vx

**Property:** Read-Write

For each half cycle of the fundamental period, VxRMS is calculated, per phase, and compared to the value set in SAG\_THRESHOLD\_Vx: where x = [A, B, C], to determine if a voltage sag condition exists. For each half cycle that a voltage sag exists, the associated flag, SWAG\_DET\_Vx is set to 1.

A threshold is allowed for each phase and is computed using the native phase voltages, before transformation to implied 4WY service. This allows setting different thresholds for non-balanced service types.

SAG\_THRESHOLD\_Vx is stored in uQ0.32 format. So, set the threshold value as follows:

$$V_{x \text{ SAG THRESHOLD}} = \left( \frac{V_{SAG-RMS}}{K_{Vx}} \right)^2 \times 2^{32}$$

Bit	31	30	29	28	27	26	25	24
	SAG_THRESHOLD_Vx[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	SAG_THRESHOLD_Vx[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	SAG_THRESHOLD_Vx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	SAG_THRESHOLD_Vx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – SAG\_THRESHOLD\_Vx[31:0]** (uQ0.32)

### 3.1.22. Current Conversion Factor

**Name:** K<sub>Ix</sub>

**Property:** Read-Write

The current conversion factor is used when converting an internal current quantity to an external equivalent RMS current quantity. K<sub>Ix</sub>: where x = [A, B, C or N].

For proper ADC function, the differential input voltage proportional to current must be provided by the current sensor (typically a CT in conjunction with a burden resistor). This differential input voltage ( $V_{diff} = V_+ - V_-$ ) must be scaled so that its peak input value is limited to the max acceptable ADC input voltage:

$$V_{diff\_max} = \frac{V_{ADCmax}}{G_{PGA}}$$

For example, 0.5V for an ADC PGA gain of  $G_{PGA} = 1$  or 62.5 mV for an ADC PGA gain of  $G_{PGA} = 8$ .

The maximum differential input voltage must typically not exceed 0.5V ( $V_+ = 0.25V$ ,  $V_- = -0.25V$ ), but acceptable performance may be achieved with signals as high as 0.55V or slightly higher. The ADC saturates at  $V_{diff} \geq 0.6V$ . When using single-ended inputs, a single-ended input of 0.5V may also be used, but the highest accuracy will be achieved by limiting single-ended input voltages to 0.25V to avoid introducing non-linearity due to approaching forward conduction of input protection diodes. Reduced input voltage range signal on current input channels may use the programmable gain amplifier to recover input range. In typical applications, external scaling allows for an appropriate over-current factor to maintain linearity during over-current events.

The ADC input voltage is, then, converted by comparing it to the reference voltage  $V_{REF}$ . This comparison creates an additional ADC internal input conversion gain,  $1.0V/V_{REF}$ , due to ratio-metric effect of the reference voltage, approximately 1.0 / 1.2, which is also part of the ADC conversion factor and is taken care of internal to the DSP processing and is separate from the current channel calibration factor, CAL<sub>M\_Ix</sub>.

#### CT Sensors (Current Transformers)

For example, it is desired to have a max measurement current of  $240A_{RMS}$  ( $200A_{RMS} + 20\%$  over-current). The following three steps must be taken (this example assumes use of a CT turns ratio,  $T_e = 2500:1$  ( $200A_{RMS}$ :  $80mA_{RMS}$ ) and a  $G_{PGA} = 4$ ):

1. Determine total current burden resistor value, as if it were one single-ended input, then divide by 2 for differential burden resistors:

$$R_{burden\_total} = \frac{V_{diff\_max}}{I_{CTmax}} = \frac{\frac{V_{ADCmax}}{G_{PGA}}}{\sqrt{2} \times \frac{240A_{RMS}}{T_e}} = \frac{\frac{0.5V}{4}}{\sqrt{2} \times 96mA_{RMS}} = \frac{0.125V}{\sqrt{2} \times 96mA_{RMS}} = 0.920712 \Omega_{se} = 2 \times (0.46 \Omega_{diff})$$

Each one of the two burden resistors (for differential inputs) would be selected as  $0.46\Omega$ .

2. Next, determine the current conversion factor (the equation shown, first, is the long-form definition):

$$K_{Ix} = \frac{I_{CTmax}}{V_{diff\_max} \times G_{PGA}} = \frac{\sqrt{2} \times 240A_{RMS}}{0.125V \times G_{PGA}} = \frac{339.411A}{0.125V \times 4} = 678.823$$

When using CTs with a burden resistor, the equation for  $K_{Ix}$  simplifies to (the preferred equivalent short-form):

$$K_{Ix} = \frac{T_e}{R_{burden\_total} \times G_{PGA}} = \frac{2500}{0.920712\Omega \times 4} = 678.823$$

Where,  $T_e$  = CT equivalent turns ratio.

3. Finally, to compute an equivalent external current, multiply an internal Qformat number,  $I_{INTERNAL}$ , in the following fashion:

$$I_{LINE\ RMS} = K_{Ix} \times I_{INTERNAL}$$

### Rogowski Coil Current Sensors

Rogowski coils produce an output voltage proportional to the time derivative of the current being measured and exhibit a gain proportional to the frequency being measured,  $f$ , as well as a 90° phase shift relative to the input signal. A 50 Hz signal would have 5/6 the gain as an equivalent 60 Hz signal in addition to the phase shift. The metrology DSP includes a selectable DI (Digital Integrator) to process all current channels using Rogowski coil sensors and introduces a 1/f gain response and an ideal -90° phase shift to compensate for derivative nature of Rogowski coil sensors. The DI (Digital Integrator) filter is adjusted for unity gain at 60 Hz.

For example, it is preferable to have a max measurement current of 240A<sub>RMS</sub> (200A<sub>RMS</sub> + 20% over-current). The following steps must be taken (this example assumes use of a Rogowski coil with an output of 500 uV/A at 60 Hz (or 416.6uV/A at 50 Hz) and a  $G_{PGA} = 4$  but operating at a frequency of 50 Hz):

When using Rogowski coils, the equation for  $K_{Ix}$  simplifies to (the preferred equivalent short-form):

$$K_{Ix} = \frac{k_{sf}(60Hz)}{G_{PGA}} = \frac{2000}{4} = 500$$

where,  $k_{sf}$  = Rogowski coil scale factor.

For this discussion, the scale factor,  $k_{sf}$ , is defined at the reference frequency,  $f_r = 60$  Hz because the DI (Digital Integrator) filter was designed for unity gain at 60 Hz. If it is preferred to use  $k_{sf}$  defined at another frequency, the gain of the DI filter must be accounted for in the computation as follows:

$$k_{di}(f) = \frac{60Hz}{f}$$

$$K_{Ix} = \frac{k_{sf}(f)}{G_{PGA} \times k_{di}(f)} = \frac{\left(\frac{I_{pr}(f)}{V_{sr}(f)}\right)}{G_{PGA} \left(\frac{60Hz}{50Hz}\right)} = \frac{\left(\frac{1A}{0.000416V}\right)}{4 \left(\frac{6}{5}\right)} = 500$$

where,  $I_{pr}$  = primary rated current,  $V_{sr}$  = secondary rated voltage,  $f$  = frequency of operation [Hz].

Refer to "PIC32CXMTx Metrology User Guide" (DS50003460) for a more detailed description.

### Resistive Shunt Current Sensors

A resistive shunt current sensor produces an output voltage proportional to the current passing through it. Generally, if a shunt is used for measuring the active phase current, then the voltages of the shunt are at the high voltage of line phase being measured and the relative metering ground reference is usually connected directly to that line phase voltage to keep all voltages going into the PIC32CXMTx or ATSENSE device at the same relative voltage level. This means the voltage of the neutral line is divided down to a fraction of a volt, also relative to the line phase voltage.

$$K_{Ix} = \frac{1}{G_{PGA} \times R_{shunt}}$$

#### Example:

If  $R_{shunt} = 100\mu\text{ ohm} = 0.0001\text{ ohm}$  and  $G_{PGA} = 8$ , then we can get:

$$K_{Ix} = 1000000 / (8 * 100) = 1250$$

The metrology firmware uses uQ22.10 to represent both integer and fractional numbers, so set:

$$K_{Ix} = \text{ROUND}(1250 * 2^{10}) = 0x00138800$$

Bit	31	30	29	28	27	26	25	24
	K_Ix[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	K_Ix[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	K_Ix[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	K_Ix[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – K\_Ix[31:0] (uQ22.10)**



### 3.1.23. Voltage Conversion Factor

**Name:** K\_Vx

**Property:** Read-Write

The voltage conversion factor is used when converting an internal voltage quantity to an external equivalent RMS voltage quantity. K\_Vx: where x=[A, B, or C].

For proper ADC function, voltage divider circuitry must be provided to reduce each high-voltage input channel from its peak input value to the max peak acceptable ADC differential input voltage.

All voltage channel inputs are constrained to use single-ended input voltages. While the maximum differential input voltage must not exceed 0.5V ( $V_+ = 0.25V$ ,  $V_- = -0.25V$ ), it is recommended that the single-ended inputs be limited to  $\pm 0.25V$  to avoid approaching forward conduction of input protection diodes. In typical applications, external scaling allows for any over-voltage factor (typically 20%). In some applications the over-voltage is increased to be able to measure the phase to phase voltage value (plus the typical 20%), to detect improper connection of the wires to the meter.

The ADC input voltage is, then, converted by comparing it to the reference voltage,  $V_{REF}$ . This comparison creates an additional ADC internal input conversion gain,  $1.0V/V_{REF}$ , due to ratio-metric effect of the reference voltage, typically 1.0/1.2, which is also part of the ADC conversion factor, and is taken care of internal to the DSP and is separate from the voltage channel calibration factor, CAL\_M\_Vx.

For example, it is preferable to have a max measurement voltage of  $288V_{RMS}$  ( $240V_{RMS} + 20\%$  over-voltage). The following three steps must be taken:

1. Determine external voltage divider ratio (single-ended input):

$$K_{divider} = \frac{V_{ADCmax\ pk}}{V_{LINEmax\ RMS}} = \frac{0.25V_{pk}}{\sqrt{2} \times 288V_{RMS}} = 0.0006138$$

2. Internal scaling within the DSP takes care of the multiplication factor,  $V_{REF}$ , to renormalize the ADC gain, when the channel calibration constant, CAL\_M\_Vx, is used.
3. Next, determine voltage conversion factor:

$$K_{V_x} = \frac{V_{LINEmax}}{V_{diff\_max}} = \frac{\sqrt{2} \times 288V_{RMS}}{0.25V_{pk}} = 1629.17$$

When using a simple resistive voltage divider, the equation for K\_Vx simplifies to the equivalent short-form:

$$K_{V_x} = \frac{1}{G_{resistor\_divider\_ratio}} = 1629.17$$

K\_Vx is stored in uQ22.10 format.

4. Finally, to compute an equivalent external voltage, multiply an internal Qformat number,  $V_{INTERNAL}$ , in the following fashion:

$$V_{LINE\ RMS} = K_{V_x} \times V_{INTERNAL}$$

Refer to "PIC32CXMTx Metrology User Guide" (DS50003460) for a more detailed description.

Bit	31	30	29	28	27	26	25	24
	K_Vx[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	K_Vx[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	K_Vx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	K_Vx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – K\_Vx[31:0]** (uQ22.10)

### 3.1.24. Current Channel Magnitude Calibration Constants

**Name:** CAL\_M\_Ix

**Property:** Read-Write

Multiplicative magnitude calibration constants are provided for each current channel to equalize gain across all channels after an appropriate calibration procedure was exercised. All active input channels, both voltage and current, require final calibration to ensure full accuracy.

CAL\_M\_Ix: where x=[A, B, C or N] is used to calibrate the current channels.

$$CAL\_M\_Ix = \frac{I_{x\_RMS}}{K\_Ix \times \sqrt{\frac{ACC\_I\_x}{N \times 2^{40}}}} \times 2^{29}$$

$I_{x\_RMS}$  is the ideal RMS value of input calibration current.  $ACC\_I\_x$  is the 64-bit accumulated  $I^2$ -scaled quantities provided by metrology firmware. The value of N is the number of samples in the integration period provided in Metrology Status Registers.

Refer to "PIC32CXMTx Metrology User Guide" (DS50003460) for a more detailed description.



**WARNING**

Be aware that this conversion factor is a signed quantity. Assigning a negative value results in an effective phase shift rotation of 180°, which can be particularly useful in specific scenarios, such as certain meter configurations or when dealing with inverted wiring polarity.

Bit	31	30	29	28	27	26	25	24
	CAL_M_Ix[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	CAL_M_Ix[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	CAL_M_Ix[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	CAL_M_Ix[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – CAL\_M\_Ix[31:0]** (sQ2.29)

### 3.1.25. Voltage Channel Magnitude Calibration Constants

**Name:** CAL\_M\_Vx

**Property:** Read-Write

Multiplicative magnitude calibration constants are provided for each voltage channel to equalize gain across all channels after an appropriate calibration procedure was exercised. All active input channels, both voltage and current, require final calibration to ensure full accuracy.

CAL\_M\_Vx: where x=[A, B, or C] is used to calibrate the voltage channels.

$$CAL\_M\_Vx = \frac{Vx\_RMS}{K\_Vx \times \sqrt{\frac{ACC\_V\_x}{N \times 2^{40}}}} \times 2^{29}$$

$Vx\_RMS$  is the ideal RMS value of the input test voltage.  $ACC\_V\_x$  is the 64-bit accumulated  $V^2$ -scaled quantities provided by metrology firmware. The value of N is the number of samples in the integration period provided in Metrology Status Registers.

Refer to "PIC32CXMTx Metrology User Guide" (DS50003460) for a more detailed description.



**WARNING** Be aware that this conversion factor is a signed quantity. Assigning a negative value results in an effective phase shift rotation of 180°.

Bit	31	30	29	28	27	26	25	24
	CAL_M_Vx[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	CAL_M_Vx[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	CAL_M_Vx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	CAL_M_Vx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – CAL\_M\_Vx[31:0] (sQ2.29)**

### 3.1.26. Per-Channel Phase Calibration Constants

**Name:** CAL\_PH\_Ix, CAL\_PH\_Vx

**Property:** Read-Write

Phase calibration constants are provided for each channel to equalize relative phase differences across all channels after an appropriate calibration procedure was exercised. All active input channels, both voltage and current, require final calibration to ensure full accuracy. All phase-correction amounts are in BAMS units.

In cases where neither phase-phase vector transformation nor optimal phase-phase voltage measurement are not required, phase correction values may be set for only current channel, and voltage phase correction values are set to zero. However, if phase-phase equalization is also desired, voltage channel phase correction values may be used.

Input requested phase correction values are relative values that may be internally adjusted with an internally computed offset to achieve proper phase shifts for use within the phase correction DSP filters. Any internal offset adjustment made by the DSP is available in the PH\_OFFSET status register (see PH\_OFFSET). This internal offset phase adjustment is made to shift all requested phase correction values to  $\leq -1.35^\circ$  (at 60 Hz). The maximum phase correction capability among the different channels is  $32.39^\circ$  (at 60Hz) or  $26.99^\circ$  (at 50Hz).

The requested input phase correction values may change dynamically and will be used to compute new phase correction filter coefficients at the start of each integration period. If phase correction values do change dynamically and, if it is preferable to keep coefficients as stationary as possible (change as little as possible), then set the phase correction value of an unused channel to a value slightly larger (more positive) than the expected maximum value of the range of allowable phase correction values. Otherwise, all unused channel's phase correction values must be set to zero.

For example, the top row of hex values represents the phase corrections as input into the phase correction registers:

	CAL_PH_IA	CAL_PH_VA
Input phase corr. values (hex)	0xFFEDCBAA	0x00000000
Input phase corr. values (dec)	-0.10°	-0.00°
Internally computed offset	-1.35°	—
Actual internal phase delays	-1.45°	-1.35°

If it is preferable to correlate the phase delays of internal signals with the phase delays of outside world signals, simply compute the actual phase delay values by adding the value of PH\_OFFSET to the raw input phase correction values.

All phase correction angles entered must be normalized to 60 Hz. For example, if a phase correction factor of  $-0.31^\circ$  is measured at 50 Hz, the value at 60 Hz is easily calculated as:

$$\angle_{60\text{Hz}} = \frac{60}{50} \angle_{50\text{Hz}} = \frac{60}{50} (-0.31^\circ)_{50\text{Hz}} = -0.372^\circ_{60\text{Hz}}$$

and to convert to the proper BAMS input format:

$$-0.372^\circ_{60\text{Hz}} = \frac{-0.372^\circ}{180^\circ} \times 2^{31} = 0xFFBC478B$$

At the start of every integration period, the input phase calibration constants are used to compute the proper phase correction filter coefficients. If a requested set of phase-corrections is not possible, an error will be returned in the status register STATE\_FLAG: PC\_OUT\_OF\_RANGE.

**Note:** Both sensor type and phase-correction inputs are used to properly compute a new set of phase-correction coefficients because an additional built-in phase shift is used for compensation when the digital integrator is automatically selected when selecting Rogowski coils.

Refer to “PIC32CXMTx Metrology User Guide” for a more detailed description.

Bit	31	30	29	28	27	26	25	24
	CAL_PH_Ix, CAL_PH_Vx[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	CAL_PH_Ix, CAL_PH_Vx[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	CAL_PH_Ix, CAL_PH_Vx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	CAL_PH_Ix, CAL_PH_Vx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – CAL\_PH\_Ix, CAL\_PH\_Vx[31:0] sQ0.31**

### 3.1.27. Waveform Capture Control Register

**Name:** CAPTURE\_CTRL

**Property:** Read-Write

Waveform capture of 32-bit samples may be accomplished through exercise of these control bits, to select the capture mode, which type of samples are to be captured and how many samples are captured. Capture data are written to the buffer starting at the address pointer stored in the CAPTURE\_ADDR register. After each set of samples are captured, the number of the last sample set captured is stored in the CAPTURE\_STATUS output register.

Upon completion of a one-shot capture sequence, the CAPTURE\_STATE bits in the CAPTURE\_STATUS register will be updated to COMPLETE, then, after the application code resets the CAPTURE\_ENABLE bit to DISABLED, the CAPTURE\_STATE bits will, then, be reset to DISABLED.

Bit	31	30	29	28	27	26	25	24
	CAPTURE_EN							
Access	R/W							
Reset	0							
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
		CH_SEL_IN	CH_SEL_VC	CH_SEL_IC	CH_SEL_VB	CH_SEL_IB	CH_SEL_VA	CH_SEL_IA
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
		CAPTURE_SOURCE[2:0]					CAPTURE_TYPE[1:0]	
Access		R/W	R/W	R/W			R/W	R/W
Reset		0	0	0			0	0

#### Bit 31 – CAPTURE\_EN Enable Waveform Capture

Value	Description
0x0	Waveform capture is disabled
0x1	Waveform capture is enabled

#### Bits 8, 9, 10, 11, 12, 13, 14 – CH\_SEL\_x Capture Channel Select

Up to 7 channels of data may be captured at the same time. Only selected channels are captured.

Value	Description
0x0	Waveform capture is disabled for channel x
0x1	Waveform capture is enabled for channel x

#### Bits 6:4 – CAPTURE\_SOURCE[2:0] Capture Source Select

All captured data is after Vref compensation was applied and are scaled values (normalized by the appropriate K<sub>Ix</sub> and K<sub>Vx</sub>). In the case of 16 kHz sampling data, the calibration constants were not applied.

Value	Description
0x0	Capture 16 kHz data [sQ1.30] before DSP filtering
0x1	Capture 4 kHz FBW data [sQ2.29] (Full Bandwidth = fundamental + harmonics)

Value	Description
0x2	Capture 4 kHz NBW data [sQ2.29] (Narrow Bandwidth = fundamental only)
0x3	Capture 8 kHz FBW data [sQ2.29] (Full Bandwidth = fundamental + harmonics)
Other	RESERVED

**Bits 1:0 – CAPTURE\_TYPE[1:0]** Selects whether capture is one-shot in nature (no samples captured prior to being enabled) or continuous capturing.

Capture must be enabled to initiate a capture process. Once enabled, capture occurs based on the requested capture mode. If enabled and a continuous capture mode is selected, capture continues until it is disabled. If enabled and a one-shot capture mode is selected, capture continues until appointed number of samples is captured.

Value	Name	Description
0x0	One-Shot Capture Mode	Capture total CAPTURE_BUFF_SIZE of future data; capture will stop after capture finishes or is disabled.
0x1	Continuous Capture Mode	Continuous capture of waveform data in circular-buffer fashion; capture will stop immediately after capture is disabled. CAPTURE_OFFSET indicates the offset of latest sample in capture buffer.



### 3.1.28. Capture Buffer Size

**Name:** CAPTURE\_BUFF\_SIZE  
**Property:** Read-Write

CAPTURE\_BUFF\_SIZE specifies buffer size used for the capture function in units of 32-bit values. It must be divisible by the number of channels selected.

For example, to capture exactly 8,000 sets of samples of only the three voltage channels, set buffer size to:

$$CAPTURE\_BUFF\_SIZE = 8000[\text{sample sets}] \times 3[\text{samples/set}] = 24000[\text{samples}] = 0x5DC0$$

**Note:** A buffer of 24,000 samples is equal in size to 96,000 bytes.

**Table 3-3.** Capture Buffer Distribution Samples:

Channel IA is selected	All channel are selected	Channel IA & IB are selected
...	...	...
CH_IA_0	CH_IA_0	CH_IA_0
CH_IA_1	CH_VA_0	CH_IB_0
CH_IA_2	CH_IB_0	CH_IA_1
CH_IA_3	CH_VB_0	CH_IB_1
CH_IA_4	CH_IC_0	CH_IA_2
CH_IA_5	CH_VC_0	CH_IB_2
CH_IA_6	CH_IN_0	CH_IA_3
CH_IA_7	CH_IA_1	CH_IB_3
CH_IA_8	CH_VA_1	CH_IA_4
...	CH_IB_1	CH_IB_4
—	CH_VB_1	...
—	CH_IC_1	—
—	CH_VC_1	—
—	CH_IN_1	—
—	CH_IA_2	—
—	CH_VA_2	—
—	CH_IB_2	—
—	CH_VB_2	—
—	CH_IC_2	—
—	CH_VC_2	—
—	CH_IN_2	—
—	CH_IA_3	—
—	CH_VA_3	—
—	...	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	CAPTURE_BUFF_SIZE[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	CAPTURE_BUFF_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	CAPTURE_BUFF_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 23:0 – CAPTURE\_BUFF\_SIZE[23:0]** (uQ24.0)

### 3.1.29. Waveform Capture Destination Buffer Address

**Name:** CAPTURE\_ADDR

**Property:** Read-Write

This entry is used as the starting address of the waveform capture buffer and is interpreted as a pointer to a 32-bit unsigned integer.

The capture address must be set at least one sample period (250  $\mu$ s) prior to enabling capture to ensure proper registration of the address.

Bit	31	30	29	28	27	26	25	24
	CAPTURE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	CAPTURE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	CAPTURE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	CAPTURE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – CAPTURE\_ADDR[31:0]** (uQ32.0)

### 3.1.30. ATSENSE ADC Control Register 0

**Name:** ATSENSE\_CTRL\_20\_23

**Property:** Read-Write

This register is a consolidation of ADC control bits for the ATSense AFE, channels: I0, I1, V1 and I2.

Bit	31	30	29	28	27	26	25	24
			I2_GAIN[1:0]					I2_ON
Access			R/W	R/W				R/W
Reset			0	0				0

Bit	23	22	21	20	19	18	17	16
								V1_ON
Access								R/W
Reset								0

Bit	15	14	13	12	11	10	9	8
			I1_GAIN[1:0]					I1_ON
Access			R/W	R/W				R/W
Reset			0	0				0

Bit	7	6	5	4	3	2	1	0
			I0_GAIN[1:0]				TEMPMEAS	I0_ON
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

**Bits 29:28 – I2\_GAIN[1:0]** Channel I2 Gain  
See ATSense register SDI2, offset 0x23

Value	Description
0x0	Channel has a gain of 1
0x1	Channel has a gain of 2
0x2	Channel has a gain of 4
0x3	Channel has a gain of 8

**Bit 24 – I2\_ON** Enable Channel I2  
See ATSense register SDI2, offset 0x23

Value	Description
0x0	Channel is disabled
0x1	Channel is enabled

**Bit 16 – V1\_ON** Enable Channel V1  
See ATSense register SDV1, offset 0x22

Value	Description
0x0	Channel is disabled
0x1	Channel is enabled

**Bits 13:12 – I1\_GAIN[1:0]** Channel I1 Gain  
See ATSense register SDI1, offset 0x21

Value	Description
0x0	Channel has gain of 1
0x1	Channel has gain of 2

Value	Description
0x2	Channel has gain of 4
0x3	Channel has gain of 8

**Bit 8 – I1\_ON** Enable Channel I1  
See ATSense register SDI1, offset 0x21

Value	Description
0x0	Channel is disabled
0x1	Channel is enabled

**Bits 5:4 – I0\_GAIN[1:0]** Channel I0 Gain  
See ATSense register SDI0, offset 0x20

Value	Description
0x0	Channel has a gain of 1
0x1	Channel has a gain of 2
0x2	Channel has a gain of 4
0x3	Channel has a gain of 8

**Bit 1 – TEMPMEAS** Channel I0/Temperature Multiplex Select Bit  
See ATSense register SDI0, offset 0x20.  
**Note:** This bit is automatically controlled by the metrology DSP for proper multiplexing between I0 and internal temperature measurement.

Value	Name	Description
0x0	CURRENT_I0	Measurement of external current I0
0x1	TEMP	Measurement of internal temperature sensor

**Bit 0 – I0\_ON** Enable Channel I0  
See ATSense register SDI0, offset 0x20

Value	Description
0x0	Channel is disabled
0x1	Channel is enabled

### 3.1.31. ATSENSE ADC Control Register 1

**Name:** ATSENSE\_CTRL\_24\_27

**Property:** Read-Write

This register is a consolidation of ADC control bits for the ATSense AFE, channels: V2, BIAS.

Bit	31	30	29	28	27	26	25	24
						ONLDO	ONREF	ONBIAS
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	23	22	21	20	19	18	17	16
								V3_ON
Access								R/W
Reset								0

Bit	15	14	13	12	11	10	9	8
			I3_GAIN[1:0]					I3_ON
Access			R/W	R/W				R/W
Reset			0	0				0

Bit	7	6	5	4	3	2	1	0
								V2_ON
Access								R/W
Reset								0

**Bit 26 – ONLDO** Enable internal LDO (see ATSense register ANA\_CTRL, offset 0x27).

Value	Description
0x0	Internal LDO is disabled.
0x1	Internal LDO is enabled.

**Bit 25 – ONREF** Enable internal reference (see ATSense register ANA\_CTRL, offset 0x27).

Value	Description
0x0	Internal reference is disabled.
0x1	Internal reference is enabled.

**Bit 24 – ONBIAS** Enable bias (see ATSense register ANA\_CTRL, offset 0x27).

Value	Description
0x0	Bias is disabled.
0x1	Bias is enabled.

**Bit 16 – V3\_ON** Enable channel V3 (see ATSense register SDV3, offset 0x26)

Value	Description
0x0	Channel is disabled.
0x1	Channel is enabled.

**Bits 13:12 – I3\_GAIN[1:0]** Channel I3 gain (see ATSense register SDI3, offset 0x25)

Value	Description
0x0	Channel has gain of 1.
0x1	Channel has gain of 2.

Value	Description
0x2	Channel has gain of 4.
0x3	Channel has gain of 8.

**Bit 8 – I3\_ON** Enable channel I3 (see ATSense register SDI3, offset 0x25)

Value	Description
0x0	Channel is disabled.
0x1	Channel is enabled.

**Bit 0 – V2\_ON** Enable channel V2 (see ATSense register SDV2, offset 0x24)

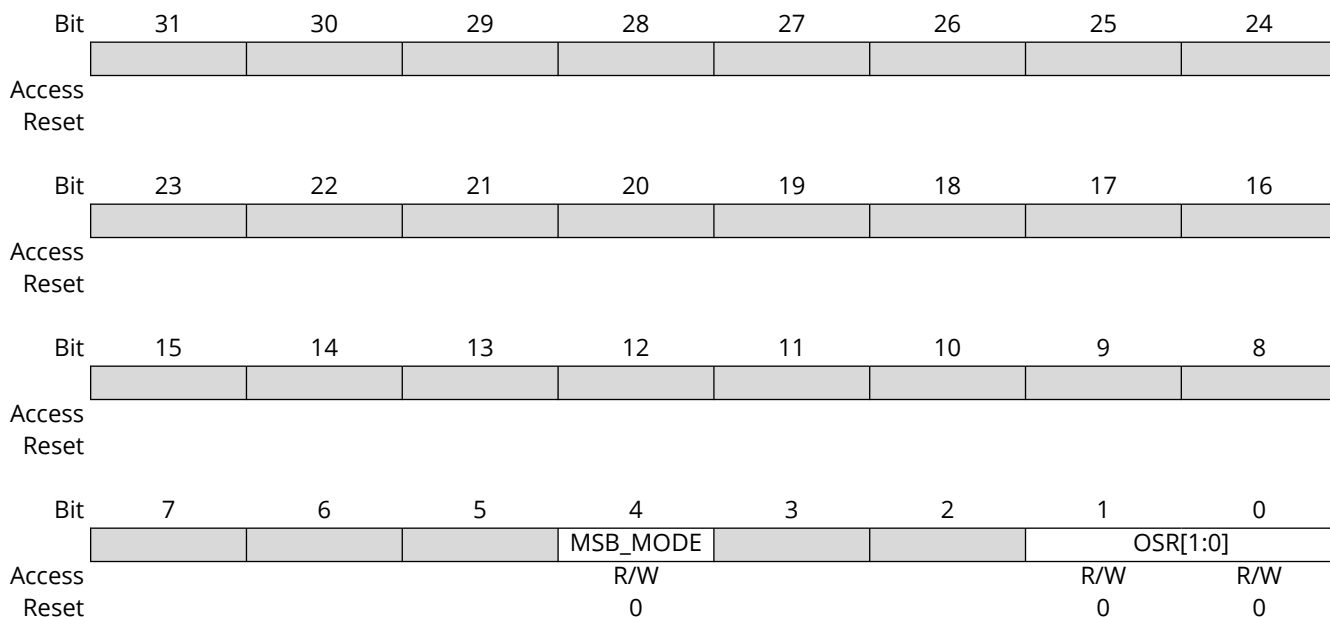
Value	Description
0x0	Channel is disabled.
0x1	Channel is enabled.

### 3.1.32. ATSENSE ADC Control Register 2

**Name:** ATSENSE\_CTRL\_28\_2B

**Property:** Read-Write

This register is a consolidation of the ADC control bits for the ATSense AFE: configure registers.



**Bit 4 – MSB\_MODE** Mode Selection (see ATSense register ATCFG, offset 0x28)

Value	Description
0x0	32-bits mode
0x1	16-bits mode

**Bits 1:0 – OSR[1:0]** Over Sampling Ratio (see ATSense register ATCFG, offset 0x28)

Value	Description
0x0	System OSR = 8
0x1	System OSR = 16
0x2	System OSR = 32
0x3	System OSR = 64



### 3.1.33. Per-Phase Active Power Offset Register

**Name:** POWER\_OFFSET\_P\_x

**Property:** RW, Format sQ-9.40 (same format as the lsb 32-bits of 64-bit P\_x accumulators)

This value indicates the per-phase active power offset, POWER\_OFFSET\_P\_x: where x = [A, B, C]. The units of POWER\_OFFSET\_P\_x is [W samp-scaled].

For a fixed voltage, this offset may be computed by applying voltage phase(s), setting zero current(s) and reading the phase's active power accumulator, P\_x. Averaging over many readings or a longer integration period may provide a more statistically accurate estimate.

$$POWER\_OFFSET\_P\_x = \frac{ACC\_P\_x}{N}$$

Where, N = Number of samples in integration period.

Bit	31	30	29	28	27	26	25	24
	POWER_OFFSET_P_x[31:24]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	POWER_OFFSET_P_x[23:16]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	POWER_OFFSET_P_x[15:8]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	POWER_OFFSET_P_x[7:0]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

#### Bits 31:0 – POWER\_OFFSET\_P\_x[31:0] Per-Phase Active Power Offset Register

POWER\_OFFSET\_P is stored in sQ1.30 format, and its value is subtracted each sample at a 4 kHz rate.

### 3.1.34. Per-Phase Reactive Power Offset Register

**Name:** POWER\_OFFSET\_Q\_x

**Property:** RW, Format sQ-9.40 (same format as the lsb 32-bits of 64-bit Q\_x accumulators)

This value indicates the per-phase reactive power offset, POWER\_OFFSET\_Q\_x: where x = [A, B, C]. The units of POWER\_OFFSET\_Q\_x is [VAR samp-scaled].

For a fixed voltage, this offset may be computed by applying voltage phase(s), setting zero current(s) and reading the phase's reactive power accumulator, Q\_x. Averaging over many readings or a longer integration period may provide a more statistically accurate estimate.

$$POWER\_OFFSET\_Q\_x = \frac{ACC\_Q\_x}{N}$$

where N = number of samples in integration period.

Bit	31	30	29	28	27	26	25	24
	POWER_OFFSET_Q_x[31:24]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	POWER_OFFSET_Q_x[23:16]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	POWER_OFFSET_Q_x[15:8]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	POWER_OFFSET_Q_x[7:0]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – POWER\_OFFSET\_Q\_x[31:0]** Per-Phase Reactive Power Offset Register

POWER\_OFFSET\_Q is stored in sQ1.30 format and its value is subtracted each sample at a 4 kHz rate.

## 3.2. Metrology Status Registers

The Metrology module generates primary 32-bit output measurement quantities for each measurement interval, per-phase quantities with each phase designated by the subscript “\_x”. The start address is 0x20088100.

**Table 3-4. Metrology Status Registers**

Index	Address	Variable	Access Mode	Name	Format	Num Bytes	Min Value	Max Value	Default	Units
0	0x20088100	VERSION	R	Metrology Firmware version	—	4	—	—	—	integer
1	0x20088104	STATUS	R	Metrology Status register	—	4	—	—	—	integer
2	0x20088108	STATE_FLAG	R	Metrology Version and State Flags register	—	4	—	—	—	integer
3	0x2008810C	CAPTURE_STATUS	R	Waveform capture status	—	4	—	—	—	integer
4	0x20088110	INTERVAL_NUM	R	Interval number	—	4	0	—	—	integer
5	0x20088114	N	R	Number samples in measurement interval	uQ16.0	4	1	3960	0	integer
6	0x20088118	PH_OFFSET	R	Phase calibration offset	sQ0.31	4	-1.000	+0.9999	—	BAMS
7	0x2008811C	FREQ	R	Frequency of fundamental harmonic	uQ20.12	4	45.000	135.000	—	Hz
8	0x20088120	FREQ_VA	R	Frequency of fundamental harmonic, VA	uQ20.12	4	45.000	124.000	—	Hz
9	0x20088124	FREQ_VB	R	Frequency of fundamental harmonic, VB	uQ20.12	4	45.000	124.000	—	Hz
10	0x20088128	FREQ_VC	R	Frequency of fundamental harmonic, VC	uQ20.12	4	45.000	124.000	—	Hz
11	0x2008812C	Reserved	—	—	—	—	—	—	—	—
12	0x20088130	TEMPERATURE	R	Temperature, average	sQ23.8	4	—	—	—	°C
13	0x20088134	I_A_MAX	R	Max phase-A current during measurement interval	sQ2.29	4	-4.0	3.9999	—	A <sub>pk</sub> scaled
14	0x20088138	I_B_MAX	R	Max phase-B current during measurement interval	sQ2.29	4	-4.0	3.9999	—	A <sub>pk</sub> scaled
15	0x2008813C	I_C_MAX	R	Max phase-C current during measurement interval	sQ2.29	4	-4.0	3.9999	—	A <sub>pk</sub> scaled
16	0x20088140	I_Nm_MAX	R	Max phase-N measured current during measurement interval	sQ2.29	4	—	—	—	A <sub>pk</sub> scaled
17	0x20088144	I_Ni_MAX	R	Max phase-N imputed current during measurement interval	sQ16.15	4	—	—	—	Amp <sub>pk</sub>
18	0x20088148	V_A_MAX	R	Max phase-A voltage during measurement interval	sQ2.29	4	-4.0	3.9999	—	V <sub>pk</sub> scaled
19	0x2008814C	V_B_MAX	R	Max phase-B voltage during measurement interval	sQ2.29	4	-4.0	3.9999	—	V <sub>pk</sub> scaled
20	0x20088150	V_C_MAX	R	Max phase-C voltage during measurement interval	sQ2.29	4	-4.0	3.9999	—	V <sub>pk</sub> scaled
21	0x20088154	FEATURES	R	Compiled feature indicator bits	uQ32.0	4	—	—	—	—
22	0x20088158	Reserved	—	—	—	—	—	—	—	—
23	0x2008815C	Reserved	—	—	—	—	—	—	—	—
24	0x20088160	Reserved	—	—	—	—	—	—	—	—

**Table 3-4.** Metrology Status Registers (continued)

Index	Address	Variable	Access Mode	Name	Format	Num Bytes	Min Value	Max Value	Default	Units
25	0x20088164	PULSE0_COUNTER	R	Number of pulses issued (Pulse 0)	uQ32.0	4	—	—	0	integer
26	0x20088168	PULSE1_COUNTER	R	Number of pulses issued (Pulse 1)	uQ32.0	4	—	—	0	integer
27	0x2008816C	PULSE2_COUNTER	R	Number of pulses issued (Pulse 2)	uQ32.0	4	—	—	0	integer
28	0x20088170	Reserved	—	—	—	—	—	—	—	—
29	0x20088174	Reserved	—	—	—	—	—	—	—	—
30	0x20088178	ZC_N_VA	R	Zero-crossing sample number of phase-A voltage	uQ20.12	4	—	—	—	real number
31	0x2008817C	ZC_N_VB	R	Zero-crossing sample number of phase-B voltage	uQ20.12	4	—	—	—	real number
32	0x20088180	ZC_N_VC	R	Zero-crossing sample number of phase-C voltage	uQ20.12	4	—	—	—	real number
33	0x20088184	ATSENSE_CAL_41_44	R	ATSense manufacturing calibration data, registers 41-44	uQ32.0	4	—	—	—	integer
34	0x20088188	ATSENSE_CAL_45_48	R	ATSense manufacturing calibration data, registers 45-48	uQ32.0	4	—	—	—	integer
35	0x2008818C	Reserved	—	—	—	4	—	—	—	—

### 3.2.1. Metrology Firmware Version

**Name:** VERSION

**Property:** Read

This register is defined to indicate the metrology version. It is recommended that the application code check this register to make sure that correct metrology version is used.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	FIRMWARE_MAJOR_VER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	FIRMWARE_MINOR_VER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	FIRMWARE_REV[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

**Bits 23:16 – FIRMWARE\_MAJOR\_VER[7:0]** Major Firmware Version  
It indicates the major version number of metrology firmware.

**Bits 15:8 – FIRMWARE\_MINOR\_VER[7:0]** Minor Firmware Version  
It indicates the minor version number of metrology firmware.

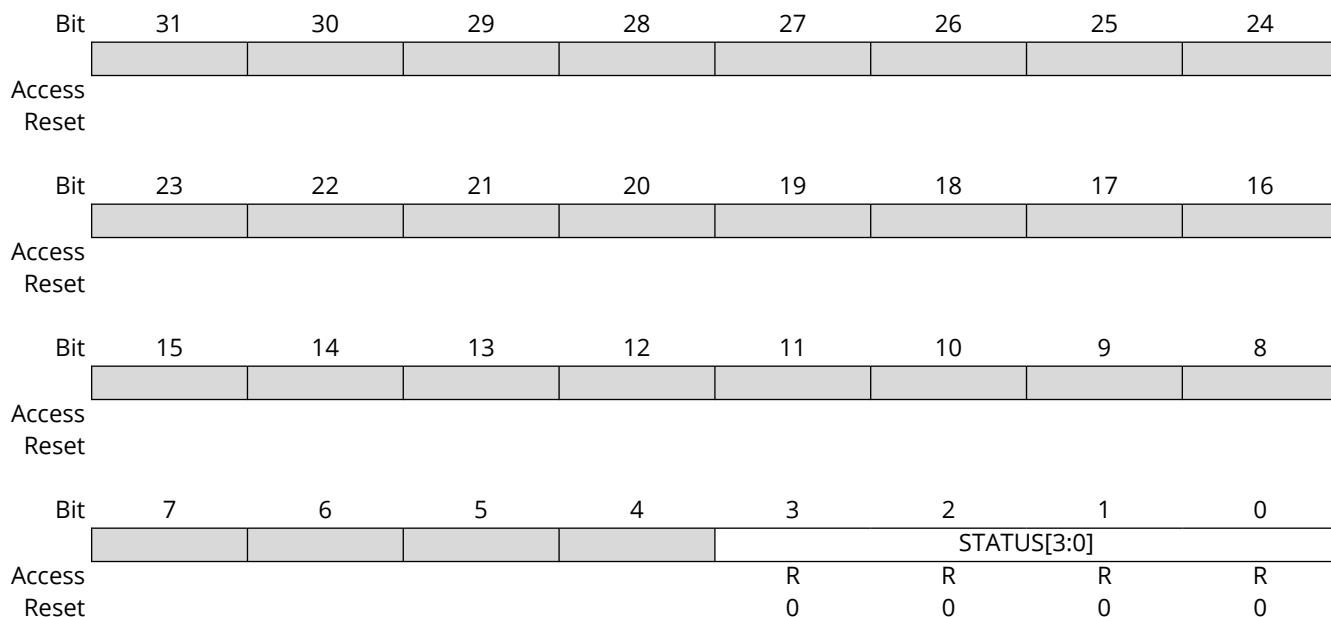
**Bits 7:0 – FIRMWARE\_REV[7:0]** Firmware Revision  
It indicates the revision number of metrology firmware.

### 3.2.2. Metrology Status Register

**Name:** STATUS

**Property:** Read

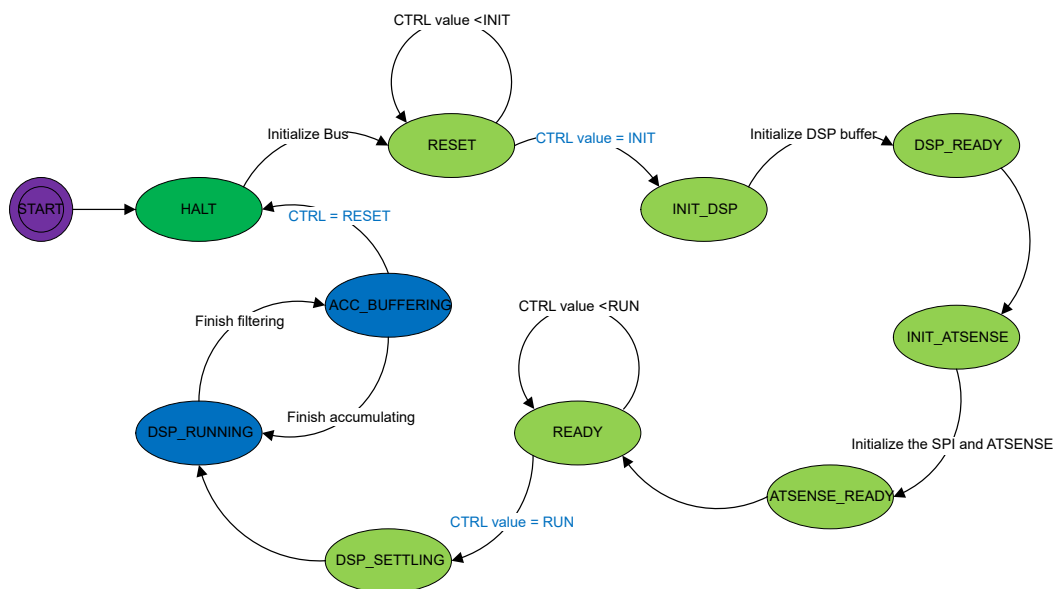
This register provides status information about the metrology.



#### Bits 3:0 – STATUS[3:0] Metrology Function State

The user can refer to the metrology state diagram for a more detailed description.

**Figure 3-1.** Metrology State Diagram



Value	Name	Description
0x0	HALT	Metrology module is halted
0x1	RESET	Resetting metrology module

Value	Name	Description
0x2	INIT_DSP	Initializing DSP filters
0x3	DSP_READY	DSP filters were initialized
0x4	INIT_ATSENSE	Initializing ATSENSE
0x5	ATSENSE_READY	ATSENSE was initialized
0x6	READY	ATSENSE temperature configuration & calibration data were copied into output registers
0x7	DSP_SETTLING	Waiting for DSP filters to stabilize to full accuracy
0x8	DSP_RUNNING	DSP filters have stabilized to full accuracy
0x9 and above	RESERVED	—

### 3.2.3. Metrology State Flags Register

**Name:** STATE\_FLAG

**Property:** Read

Bit	31	30	29	28	27	26	25	24
		SWELL_DET_V	SWELL_DET_V	SWELL_DET_V		SAG_DET_VC	SAG_DET_VB	SAG_DET_VA
		C	B	A				
Access		R	R	R		R	R	R
Reset		0	0	0		0	0	0

Bit	23	22	21	20	19	18	17	16
	CREEP_DET_S	PC_OUT_OF_RANGE	ARCH_DETECT_FAIL	CREEP_DET_P	CREEP_DET_Q	CREEP_DET_C	CREEP_DET_B	CREEP_DET_A
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	HOST_ID_FAIL							
Access	R							
Reset	0							

Bit	7	6	5	4	3	2	1	0
	ATSENSE_FAIL		FREQ_LOCKED	TIMING_Vx[1:0]		PH_C_ACTIVE	PH_B_ACTIVE	PH_A_ACTIVE
Access	R		R	R	R	R	R	R
Reset	0		0	0	0	0	0	0

#### Bits 28, 29, 30 – SWELL\_DET\_Vx Voltage Swell Detected Flag for Channel x

Value	Description
0	Voltage swell is not detected for the current half line cycle
1	Voltage swell is detected for the current half line cycle

#### Bits 24, 25, 26 – SAG\_DET\_Vx Voltage Sag Detected Flag for Channel x

Value	Description
0	Voltage sag is not detected in the current half line cycle
1	Voltage sag is detected in the current half line cycle

#### Bit 23 – CREEP\_DET\_S Total Apparent Power Creep Detected Flag CREEP\_DET\_S status flag only updated when enabled (CREEP\_S\_EN = 1).

Value	Description
0	Apparent power creep is not detected in the current full line cycle
1	Apparent power creep is detected in the current full line cycle

#### Bit 22 – PC\_OUT\_OF\_RANGE Phase Corrector Out of Range Indicates if a set of requested phase correction values are out of range.

Value	Description
0	Requested phase correction values in range
1	Requested phase correction values out of range



**Bit 21 – ARCH\_DETECT\_FAIL** Architecture Detect Failure

Indicates that a proper device architecture was not detected ("SH" or "C").

Value	Description
0	A proper device ("SH" or "C") was detected
1	An improper device (not "SH" nor "C") was detected

**Bit 20 – CREEP\_DET\_P** Total Active Power Creep Detected Flag

CREEP\_DET\_P status flag only updated when enabled (CREEP\_P\_EN = 1).

Value	Description
0	Active power creep is not detected in the current full line cycle
1	Active power creep is detected in the current full line cycle

**Bit 19 – CREEP\_DET\_Q** Total Reactive Power Creep Detected Flag

CREEP\_DET\_Q status flag only updated when enabled (CREEP\_Q\_EN = 1).

Value	Description
0	Reactive power creep is not detected in the current full line cycle
1	Reactive power creep is detected in the current full line cycle

**Bits 16, 17, 18 – CREEP\_DET\_Ix** Phase x Current Creep Detected Flag

CREEP\_DET\_I status flag only updated when enabled (CREEP\_I\_EN = 1).

Value	Description
0	Channel x current creep is not detected in the current full line cycle
1	Channel x current creep is detected in the current full line cycle

**Bit 15 – HOST\_ID\_FAIL** Host Identification Failure Indication

The detection process determines if the host has an internal ATSense (PIC32CXMTSx) or makes use of an external ATSense (PIC32CXMTC). If a proper ID is not made, this bit is used to show this status.

Value	Description
0	Proper PIC32CXMTx part successfully identified
1	Failed to identify proper PIC32CXMTx part

**Bit 7 – ATSENSE\_FAIL** ATSENSE State

Value	Description
0	ATSENSE initialization is successful
1	ATSENSE initialization is failed

**Bit 5 – FREQ\_LOCKED** Frequency Locked Flag

Value	Description
0	Line frequency is not determined. Using sample count limit for metrology integration period.
1	Line frequency was determined

**Bits 4:3 – TIMING\_Vx[1:0]** Dominant Voltage Channel

Indicates which voltage channel is used for frequency determination and cycle timing. If no voltage phases are active, phase VA is selected by default.

Value	Description
0	Voltage phase VA is used for timing extraction purposes
1	Voltage phase VB is used for timing extraction purposes
2	Voltage phase VC is used for timing extraction purposes

**Bits 0, 1, 2 – PH\_x\_ACTIVE** Phase x is active

Value	Description
0	Voltage phase x is inactive
1	Voltage phase x is active

### 3.2.4. Waveform Capture Function Status

**Name:** CAPTURE\_STATUS

**Property:** Read

Bit	31	30	29	28	27	26	25	24
	CAPTURE_WRA P			INVALID_ADD R	CAPTURE_STATE[3:0]			
Access	R			R	R	R	R	R
Reset	0			0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CAPTURE_OFFSET[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CAPTURE_OFFSET[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CAPTURE_OFFSET[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

#### Bit 31 – CAPTURE\_WRAP Capture Buffer Wrapped

Value	Name	Description
0	NOT WRAPPED	Buffer has not wrapped
1	WRAPPED	Buffer has wrapped at least once (in circular buffer fashion, as used in continuous capture modes)

#### Bit 28 – INVALID\_ADDR Invalid Capture Address

Value	Name	Description
0	0	Capture address within valid range [0x20000000, 0x20080000)
1	1	Capture address outside valid range

#### Bits 27:24 – CAPTURE\_STATE[3:0] Waveform Capture Status

Status will be meaningful only when CAPTURE\_EN is set to '1'.

Value	Name	Description
0x0	DISABLED	Capture disabled
0x1	ACTIVE	Capture in progress
0x2	COMPLETE	Capture completed
0x3	RESERVED	—

#### Bits 23:0 – CAPTURE\_OFFSET[23:0] Capture Offset

Offset within the buffer indicating the position of the last sample stored.

### 3.2.5. Measurement Interval Number

**Name:** INTERVAL\_NUM

**Property:** Read

The measurement interval number associated with the present set of Metrology output data.

Bit	31	30	29	28	27	26	25	24
	INTERVAL_NUM[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	INTERVAL_NUM[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	HALFCYCLE_COUNT[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	HALFCYCLE_COUNT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

**Bits 31:16 – INTERVAL\_NUM[15:0]** Interval number (uQ16.0)

The number of the present integration interval. This count rolls over from max count to 0.

**Bits 15:0 – HALFCYCLE\_COUNT[15:0]** Sub-interval number (uQ16.0)

The sub-interval number is the number of half-cycles that have occurred in the present integration interval; depending on how often interrupts are selected. This count resets each new integration interval.

### 3.2.6. Number of Samples in the Last Measurement Interval

**Name:** N  
**Property:** Read

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
	N[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	N[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

#### Bits 15:0 – N[15:0] Number of Samples in the Last Measurement Interval (uQ16.0)

The number of samples, N, in the last measurement interval based on zero-crossings of the selected voltage channel.

**Note:** It is recommended that this value be used to calculate the RMS value or power.

### 3.2.7. Phase Correction Filter Offset

**Name:** PH\_OFFSET

**Property:** Read

Bit	31	30	29	28	27	26	25	24
	PH_OFFSET[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	PH_OFFSET[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	PH_OFFSET[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	PH_OFFSET[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

#### Bits 31:0 – PH\_OFFSET[31:0] Phase Correction Filter Offset (sQ0.31)

All voltage and current channels may be phase corrected by setting the requested relative phase adjustment values in registers: CAL\_PH\_Vx & CAL\_PH\_Iy. The actual phase adjustment angles implemented will be offset by this amount, the minimum required, such that all phase corrections are  $\leq -1.35^\circ$  @ 60 Hz ( $-1.125^\circ$  @ 50 Hz). To determine the actual phase correction angle for each channel, add this offset to each requested phase correction amount. See “CAL\_PH\_Ix, CAL\_PH\_Vx” description for detailed example.

### 3.2.8. Dominant Line Voltage Fundamental Harmonic Frequency

**Name:**     FREQ

**Property:** Read

Bit	31	30	29	28	27	26	25	24
	FREQ[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	FREQ[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	FREQ[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	FREQ[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

#### Bits 31:0 – FREQ[31:0] Frequency of Fundamental Harmonic (uQ20.12)

Frequency of the line voltage fundamental harmonic component is determined by the Metrology module and provided in the variable FREQ, using the dominant phase. In addition, a separate frequency is determined for each individual voltage phase, for each of three phases,  $x = [A, B, C]$ .

**Note:** Maximum accuracy in frequency measurement is achieved at the end of the integration period. Therefore, the register should be read immediately after the integration interrupt is generated. However, since this register is updated each time a positive zero-crossing in the voltage line is detected, it is possible to read the register after the full cycle interrupt, enabling a faster refresh of the value.

### 3.2.9. Line Voltage Fundamental Harmonic Frequency

**Name:**     FREQ\_Vx

**Property:** Read

Bit	31	30	29	28	27	26	25	24
	FREQ_Vx[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	FREQ_Vx[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	FREQ_Vx[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	FREQ_Vx[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

#### Bits 31:0 – FREQ\_Vx[31:0] Frequency of Fundamental Harmonic Vx (uQ20.12)

Frequency of the line voltage fundamental harmonic component is determined by the Metrology module and provided in the variable FREQ. A separate frequency is determined for each individual voltage phase, for each of three phases, x = [A, B, C].

**Note:** Maximum accuracy in frequency measurement is achieved at the end of the integration period. Therefore, the register should be read immediately after the integration interrupt is generated. However, since this register is updated each time a positive zero-crossing in the voltage line is detected, it is possible to read the register after the full cycle interrupt, enabling a faster refresh of the value.



### 3.2.10. Sensor Temperature

**Name:** TEMPERATURE

**Property:** Read

Bit	31	30	29	28	27	26	25	24
	TEMPERATURE[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	TEMPERATURE[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	TEMPERATURE[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	TEMPERATURE[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

#### Bits 31:0 – TEMPERATURE[31:0] Temperature Average (sQ23.8)

The metrology module generates the average temperature over the measurement interval. The temperature is stored in sQ23.8 format in units of °C.

### 3.2.11. Phase Current Peak Registers

**Name:** I\_A\_MAX/I\_B\_MAX/I\_C\_MAX

**Property:** Read

I\_x\_MAX is the maximum current peak absolute value of phase x, x = [A, B, C], in units of [Amp<sub>pk</sub> scaled].

They can be reset by setting I\_MAX\_RESET to '1'.

The peak current may be calculated by the following formula:

$$I_{x_{peak}} = \frac{I_{x_{MAX}}}{2^{29}} \times K_{I_x} = \frac{I_{x_{MAX}}}{2^{29}} \times \frac{K_{I_x}}{2^{10}}$$

Where  $K_{I_x}$  is the current conversion factor in float format, or  $K_{I_x}$  is the current conversion register value, and  $I_{x_{peak}}$  is the peak current of phase x, in unit of Amp.

Phase current max values, I\_x\_MAX for x=[A,B,C], are determined using FBW (Full Band-Width) baseband DSP-filtered data.

Bit	31	30	29	28	27	26	25	24
	I_x_MAX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	I_x_MAX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	I_x_MAX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	I_x_MAX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – I\_x\_MAX[31:0]** Max Phase-x Current During Measurement Interval (sQ2.29)

### 3.2.12. Neutral Current Peak Registers

**Name:** I\_Ni\_MAX/I\_Nm\_MAX

**Property:** Read

I\_Nx\_MAX is the maximum Neutral current peak absolute value of phase x, x = [Ni, Nm], in units of [Amp<sub>pk</sub>] (x = [Ni]) or [AmpPK scaled] (x = [Nm]).

They can be reset by setting I\_MAX\_RESET to '1'.

The peak currents may be calculated by the following formulas:

$$I_{Ni\_peak} = \frac{I_{x\_MAX}}{2^{15}}$$

$$I_{Nm\_peak} = \frac{I_{x\_MAX}}{2^{29}} \times K_{Ix} = \frac{I_{x\_MAX}}{2^{29}} \times \frac{K_{Ix}}{2^{10}}$$

Neutral current max values, I\_Nx\_MAX for x=[Ni, Nm], are determined using FBW (Full Band Width) baseband DSP-filtered data.

Bit	31	30	29	28	27	26	25	24
	I_Nx_MAX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	I_Nx_MAX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	I_Nx_MAX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	I_Nx_MAX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – I\_Nx\_MAX[31:0]** Max Neutral-x Current During Measurement Interval (sQ16.15 Format (I\_Ni\_MAX) and sQ2.29 Format (I\_Nm\_MAX)).

### 3.2.13. Voltage Peak Registers

**Name:** V\_A\_MAX/V\_B\_MAX/V\_C\_MAX

**Property:** Read

V\_x\_MAX is the maximum voltage peak absolute value of phase x (x = [A, B, C]) in units of [Volt<sub>pk</sub> scaled].

They can be reset by setting V\_MAX\_RESET to '1'.

The peak voltage may be calculated by following formula:

$$V_{x\_peak} = \frac{V_{x\_MAX}}{2^{29}} \times K_{V_x}$$

Where K\_V<sub>x</sub> is the voltage conversion factor in float format; V\_x\_peak is the peak voltage of phase x, in unit of Volt.

Phase voltage max values, V\_x\_MAX for x=[A, B, C], are determined using FBW (Full Band-Width) baseband filtered data.

Bit	31	30	29	28	27	26	25	24
	V_x_MAX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	V_x_MAX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	V_x_MAX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	V_x_MAX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – V\_x\_MAX[31:0]** Max Phase-x Voltage During Measurement Interval (sQ2.29)

### 3.2.14. Compiled Feature Indicator Bits

**Name:** FEATURES

**Property:** Read

Bit	31	30	29	28	27	26	25	24
	POLY_PHASE	SINGLE_PHASE				RCZ_OUT		Fs_SAMPLE_RATE
Access	R	R				R		R
Reset	0	0				0		0

Bit	23	22	21	20	19	18	17	16
		ATSense_LOC	NUM_PULSES[1:0]		ROGOWSKI_DC_REMOVE	CAPTURE	CREEP	DFT_ENABLE
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CORE_CLK_SPEED[3:0]				RZC_DETECT	PQ_OFFSET_X	I_N_MUXING	HALF_COPROC_CLK
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
								DEBUG_MODES
Access								R
Reset								0

#### Bit 31 – POLY\_PHASE Flag

Value	Description
1	Compiled: Poly-phase metering enabled.

#### Bit 30 – SINGLE\_PHASE Flag

Value	Description
1	Compiled: Single-phase metering enabled.

#### Bit 26 – RCZ\_OUT Flag

Value	Description
1	Compiled: Detect independent V <sub>A</sub> raw zero-crossings and output signal on pin PD19 <b>Note:</b> Not compatible with NUM_PULSES = 3

#### Bit 24 – Fs\_SAMPLE\_RATE

Metrology baseband sample rate

Value	Description
0	Baseband sample rate FS = 4000 KHz
1	Baseband sample rate FS = 8000 KHz

#### Bit 22 – ATSense\_LOC

Value	Description
0	PIC32CXMTSH, Internal ATSense detected (ATSense203)

Value	Description
1	PIC32CXMTx, External ATSense detected (ATSense301)

#### Bits 21:20 – NUM\_PULSES[1:0]

Metrology may be compiled with different number of pulses enabled, [0-3].  
NUM\_PULSES equals the number of pulses enabled during compile time.

#### Bit 19 – ROGOWSKI\_DC\_REMOVE Flag

Value	Description
1	Compiled for DC-removal before integrator filter when using Rogowski coil current sensors

#### Bit 18 – CAPTURE Flag

Value	Description
1	Compiled for waveform capture

#### Bit 17 – CREEP Flag

Value	Description
1	Compiled for CREEP thresholding

#### Bit 16 – DFT\_ENABLED Flag

Value	Description
1	Compiled for DFT harmonic analysis

#### Bits 15:12 – CORE\_CLK\_SPEED[3:0]

Core-1 (Metrology core) clock fixed at 237.568 MHz in PIC32CXMTxx metrology

Value	Description
0x0	Compiled to be used with Core-0 clock = undefined
0x1	Compiled to be used with Core-0 clock = 102.400 MHz
0x2	Compiled to be used with Core-0 clock = 106.496 MHz
0x3	Compiled to be used with Core-0 clock = 110.592 MHz
0x4	Compiled to be used with Core-0 clock = 114.688 MHz
0x5	Compiled to be used with Core-0 clock = 118.784 MHz
0x6	Compiled to be used with Core-0 clock = 237.568 MHz
0x7	Reserved

#### Bit 11 – RZC\_DETECT Flag

Value	Description
1	Compiled for raw zero-cross detect

#### Bit 10 – PQ\_OFFSET\_X Flag

Value	Description
1	Compiled for use of PQ per-phase offsets

#### Bit 9 – I\_N\_MUXING Flag

Value	Description
1	Compiled for near-full bandwidth I_Neutral metrology

#### Bit 8 – HALF\_COPROC\_CLK Flag

Value	Description
1	Compiled for Core1 coprocessor to run at half speed of Core0

**Bit 0 – DEBUG\_MODES**

Value	Description
0	Unless specifically compiled for a debug mode, this bit is always = 0
1	Metrology FW compiled in a DEBUG mode

### 3.2.15. Pulse counters

**Name:** PULSEx\_COUNTER

**Property:** Read

Bit	31	30	29	28	27	26	25	24
	PULSEx_COUNTER[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	PULSEx_COUNTER[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	PULSEx_COUNTER[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	PULSEx_COUNTER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

#### Bits 31:0 – PULSEx\_COUNTER[31:0] Pulse counters (uQ32.0)

The registers count the number of pulses generated by the available pulse outputs.



### 3.2.16. Zero-Crossing Sample Number of Phase-X Voltage

**Name:** ZC\_N\_Vx

**Property:** Read

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	ZC_COUNT_Vx[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	ZC_COUNT_Vx[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	ZC_COUNT_Vx[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

#### Bits 23:0 – ZC\_COUNT\_Vx[23:0] Zero Crossing Count (uQ20.12)

Zero-crossing sample count of last positive-going zero-crossing of the V<sub>x</sub> [x = A, B and C] phase voltage channel, in units of the 4K Hz sample rate. Use this to compare with other voltage phases to determine relative phase order.

### 3.2.17. ATSENSE Calibration Trim Data, Registers: 0x41 – 0x44

**Name:** ATSENSE\_CAL\_41\_44

**Property:** Read

Bit	31	30	29	28	27	26	25	24
	TEMP_TL [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
					TEMP_TL [11:8]			
Access					R	R	R	R
Reset					0	0	0	0
Bit	15	14	13	12	11	10	9	8
	REF_TL [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
					REF_TL [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

#### Bits 31:24 – TEMP\_TL [7:0]

#### Bits 19:16 – TEMP\_TL [11:8] Temperature TL

The following rule applies to recover the real values of ADC\_TEMP\_OUT from the 12-bit coded values in the product registers:

ADC\_TEMP\_OUT[23:0] (TL) = TEMP\_TL[11:0] << 12

**Note:** TEMP\_TL[11:0] is a signed 12-bit integer.

#### Bits 15:8 – REF\_TL [7:0]

#### Bits 3:0 – REF\_TL [11:8] Reference Voltage

Reference Voltage measured at temperature TL

$V_{REF}(TL) = 1.120V + REF\_TL[11:0] * 25 \mu V$

### 3.2.18. ATSENSE Calibration Trim Data, Registers: 0x45 – 0x48

**Name:** ATSENSE\_CAL\_45\_48

**Property:** Read

Bit	31	30	29	28	27	26	25	24
	TEMP_TH [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
					TEMP_TH [11:8]			
Access					R	R	R	R
Reset					0	0	0	0
Bit	15	14	13	12	11	10	9	8
	REF_TH [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
					REF_TH [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

#### Bits 31:24 – TEMP\_TH [7:0]

#### Bits 19:16 – TEMP\_TH [11:8] Temperature TH

The following rule applies to recover the real values of ADC\_TEMP\_OUT from the 12-bit coded values in the product registers:

ADC\_TEMP\_OUT[23:0] (TH) = TEMP\_TH[11:0] << 12

**Note:** TEMP\_TH[11:0] is a signed 12-bit integer.

#### Bits 15:8 – REF\_TH [7:0]

#### Bits 3:0 – REF\_TH [11:8] Reference Voltage

Reference Voltage measured at temperature TH

$V_{REF}(TH) = 1.120V + REF\_TH[11:0] * 25 \mu V$

### 3.3. Accumulated Output Quantities

The start address is 0x20088190. All values are integrated at an equivalent sampling rate of 4000 KHz. The Metrology module generates the following primary output measurement quantities for each measurement interval, per-phase quantities with each phase designated by the subscript “\_x” (where x = [A, B, or C] for voltage channels and x = [A, B, C or N] for current channels).

**Table 3-5. Accumulated Output Quantities**

Index	Address	Variable	Access Mode	Name	Format	Num Bytes	Min Value	Max Value	Default	Units
0	0x20088190	I_A	R	Amp-squared-samples, phase-A, fundamental + harmonics	uQ24.40	8	—	—	—	Amp <sup>2</sup> samp scaled
1	0x20088198	I_B	R	Amp-squared-samples, phase-B, fundamental + harmonics	uQ24.40	8	—	—	—	Amp <sup>2</sup> samp scaled
2	0x200881A0	I_C	R	Amp-squared-samples, phase-B, fundamental + harmonics	uQ24.40	8	—	—	—	Amp <sup>2</sup> samp scaled
3	0x200881A8	I_Ni	R	Amp-squared-samples, phase-N imputed, fundamental + harmonics	uQ44.20	8	—	—	—	Amp <sup>2</sup> samp
4	0x200881B0	I_Nm	R	Amp-squared-samples, phase-N measured, fundamental + harmonics	uQ24.40	8	—	—	—	Amp <sup>2</sup> samp scaled
5	0x200881B8	I_A_F	R	Amp-squared-samples, phase-A, fundamental only	uQ24.40	8	—	—	—	Amp <sup>2</sup> samp scaled
6	0x200881C0	I_B_F	R	Amp-squared-samples, phase-B, fundamental only	uQ24.40	8	—	—	—	Amp <sup>2</sup> samp scaled
7	0x200881C8	I_C_F	R	Amp-squared-samples, phase-C, fundamental only	uQ24.40	8	—	—	—	Amp <sup>2</sup> samp scaled
8	0x200881D0	I_Nmi	R	Amp-squared-samples, raw phase-N measured minus imputed, fundamental + harmonics	uQ44.20	8	—	—	—	Amp <sup>2</sup> samp
9	0x200881D8	I_Nm_F	R	Amp-squared-samples, phase-N measured, fundamental only	uQ24.40	8	—	—	—	Amp <sup>2</sup> samp scaled
10	0x200881E0	RESERVED	R	—	—	8	—	—	—	—
11	0x200881E8	RESERVED	R	—	—	8	—	—	—	—
12	0x200881F0	RESERVED	R	—	—	8	—	—	—	—
13	0x200881F8	RESERVED	R	—	—	8	—	—	—	—
14	0x20088200	RESERVED	R	—	—	8	—	—	—	—
15	0x20088208	P_A	R	Watt-samples, phase-A, fundamental + harmonics	sQ23.40	8	—	—	—	W-samp scaled
16	0x20088210	P_B	R	Watt-samples, phase-B, fundamental + harmonics	sQ23.40	8	—	—	—	W-samp scaled
17	0x20088218	P_C	R	Watt-samples, phase-C, fundamental + harmonics	sQ23.40	8	—	—	—	W-samp scaled
18	0x20088220	P_A_F	R	Watt-samples, phase-A, fundamental only	sQ23.40	8	—	—	—	W-samp scaled
19	0x20088228	P_B_F	R	Watt-samples, phase-B, fundamental only	sQ23.40	8	—	—	—	W-samp scaled
20	0x20088230	P_C_F	R	Watt-samples, phase-C, fundamental only	sQ23.40	8	—	—	—	W-samp scaled
21	0x20088238	P_N	R	Watt-samples, phase-N, fundamental + harmonics	sQ23.40	8	—	—	—	W-samp scaled

**Table 3-5.** Accumulated Output Quantities (continued)

Index	Address	Variable	Access Mode	Name	Format	Num Bytes	Min Value	Max Value	Default	Units
22	0x20088240	P_N_F	R	Watt-samples, phase-N, fundamental only	sQ23.40	8	—	—	—	W-samp scaled
23	0x20088248	RESERVED	—	—	—	8	—	—	—	—
24	0x20088250	Q_A	R	VAR-samples, phase-A, fundamental + harmonics	sQ23.40	8	—	—	—	VAR-samp scaled
25	0x20088258	Q_B	R	VAR-samples, phase-B, fundamental + harmonics	sQ23.40	8	—	—	—	VAR-samp scaled
26	0x20088260	Q_C	R	VAR-samples, phase-C, fundamental + harmonics	sQ23.40	8	—	—	—	VAR-samp scaled
27	0x20088268	Q_A_F	R	VAR-samples, phase-A, fundamental only	sQ23.40	8	—	—	—	VAR-samp scaled
28	0x20088270	Q_B_F	R	VAR-samples, phase-B, fundamental only	sQ23.40	8	—	—	—	VAR-samp scaled
29	0x20088278	Q_C_F	R	VAR-samples, phase-C, fundamental only	sQ23.40	8	—	—	—	VAR-samp scaled
30	0x20088280	Q_N	R	VAR-samples, phase-N, fundamental + harmonics	sQ23.40	8	—	—	—	VAR-samp scaled
31	0x20088288	Q_N_F	R	VAR-samples, phase-N, fundamental only	sQ23.40	8	—	—	—	VAR-samp scaled
32	0x20088290	RESERVED	R	—	—	8	—	—	—	—
33	0x20088298	V_A	R	Volt-squared-samples, phase-A, fundamental + harmonics	sQ24.40	8	—	—	—	Volt <sup>2</sup> samp scaled
34	0x200882A0	V_B	R	Volt-squared-samples, phase-B, fundamental + harmonics	sQ24.40	8	—	—	—	Volt <sup>2</sup> samp scaled
35	0x200882A8	V_C	R	Volt-squared-samples, phase-C, fundamental + harmonics	sQ24.40	8	—	—	—	Volt <sup>2</sup> samp scaled
36	0x200882B0	RESERVED	R	—	—	8	—	—	—	—
37	0x200882B8	V_A_F	R	Volt-squared-samples, phase-A, fundamental only	uQ24.40	8	—	—	—	Volt <sup>2</sup> samp scaled
38	0x200882C0	V_B_F	R	Volt-squared-samples, phase-B, fundamental only	uQ24.40	8	—	—	—	Volt <sup>2</sup> samp scaled
39	0x200882C8	V_C_F	R	Volt-squared-samples, phase-C, fundamental only	uQ24.40	8	—	—	—	Volt <sup>2</sup> samp scaled
40	0x200882D0	RESERVED	R	—	—	8	—	—	—	—
41	0x200882D8	V_AB	R	Volt-squared-samples, VA – VB, fundamental + harmonics	uQ24.40	8	—	—	—	Volt <sup>2</sup> samp scaled
42	0x200882E0	V_BC	R	Volt-squared-samples, VB – VC, fundamental + harmonics	uQ24.40	8	—	—	—	Volt <sup>2</sup> samp scaled
43	0x200882E8	V_CA	R	Volt-squared-samples, VC – VA, fundamental + harmonics	uQ24.40	8	—	—	—	Volt <sup>2</sup> samp scaled

**Table 3-5.** Accumulated Output Quantities (continued)

Index	Address	Variable	Access Mode	Name	Format	Num Bytes	Min Value	Max Value	Default	Units
44	0x200882F0	V_AB_F	R	Volt-squared-samples, VA – VB, fundamental only	uQ24.40	8	—	—	—	Volt <sup>2</sup> samp scaled
45	0x200882F8	V_BC_F	R	Volt-squared-samples, VB – VC, fundamental only	uQ24.40	8	—	—	—	Volt <sup>2</sup> samp scaled
46	0x20088300	V_CA_F	R	Volt-squared-samples, VC – VA, fundamental only	uQ24.40	8	—	—	—	Volt <sup>2</sup> samp scaled
47	0x20088308	RESERVED	R	—	—	8	—	—	—	—
48	0x20088310	RESERVED	R	—	—	8	—	—	—	—
49	0x20088318	RESERVED	R	—	—	8	—	—	—	—
50	0x20088320	ACC_T0	R	Total accumulated quantities specified by PC0_TYPE	sQ33.30	8	—	—	—	Wh, VARh, Amp <sub>2</sub> h, VAh
51	0x20088328	ACC_T1	R	Total accumulated quantities specified by PC1_TYPE	sQ33.30	8	—	—	—	Wh, VARh, Amp <sub>2</sub> h, VAh
52	0x20088330	ACC_T2	R	Total accumulated quantities specified by PC2_TYPE	sQ33.30	8	—	—	—	Wh, VARh, Amp <sub>2</sub> h, VAh
53	0x20088338	RESERVED	R	—	—	8	—	—	—	—
54	0x20088340	RESERVED	R	—	—	8	—	—	—	—

### 3.3.1. Accumulated Current Quantities

**Name:** I\_A/I\_B/I\_C/I\_Ni/I\_Nm/I\_Nmi/I\_A\_F/I\_B\_F/I\_C\_F/I\_Nm\_F

**Property:** Read

The metrology module generates the following accumulated current ( $I^2$ ) quantities: I\_A, I\_B, I\_C, I\_Ni, I\_Nm, I\_Nmi, I\_A\_F, I\_B\_F, I\_C\_F and I\_Nm\_F.

#### I\_x, I\_x\_F, and I\_Nm\_F

These accumulators are in units of [Amp<sup>2</sup>sample scaled] in format [uQ24.40] and represent the accumulated scaled current quantities in the integration period. They are calculated according to the following formula:

$$I_x = \sum_{i=1}^N (I_{x\_sample_i})^2$$

Where,  $I_{x\_sample_i}$  is  $i^{\text{th}}$  sampled current value of phase x in the present integration period; x = [A, B, C]; and N is the number of samples in the last measurement interval.

**I\_Nm** is the accumulator for measured neutral current. This accumulators is in units of [Amp<sup>2</sup>sample scaled] in format [uQ24.40].

In the case of being multiplexed with temperature measurement acquisition, such as when using the PIC32CXMTx with an external ATSense-301, slightly less performance may be expected than DSP-filtered full bandwidth data, calculated according to the following formula:

$$I_{Nm} = \sum_{i=1}^N (I_{Nm\_sample_i})^2$$

Where,  $I_{Nm\_sample_i}$  is  $i^{\text{th}}$  sampled measured neutral current value from current input I0 in the last integration period; and N is the number of samples in the last measurement interval.

#### I\_Ni, and I\_Nmi

These neutral currents are unscaled in units of [Amp<sup>2</sup>sample] and are computed directly from DSP-filtered baseband current channel data streams. These neutral currents are unscaled (not normalized by the K\_Ix current sensor scale factors); therefore, these accumulators are all in units of (Amp<sup>2</sup>samples) in format [uQ44.20].

**I\_Ni** is the accumulator for imputed neutral current using full bandwidth (fundamental + harmonics) DSP-filtered baseband current channel data calculated according to the following formulas:

$$I_{Ni\_sample_i} = \sum_x^{A,B,C} I_{x\_sample_i}$$

$$I_{Ni} = \sum_{i=1}^N (I_{Ni\_sample_i})^2$$

Where,  $I_{Ni\_sample_i}$  is  $i^{\text{th}}$  sampled imputed neutral current value computed from the sum of all active current phase currents in the present integration period, and N is the number of samples in the last measurement interval.

**I\_Nmi** is the accumulator for the difference between the sample-by-sample measured and imputed neutral currents. This integration is sensitive to both magnitude and/or phase differences between the measured and imputed neutral currents, calculated according to the following formula:

$$I_{Nmi} = \sum_{i=1}^N (I_{Nm\_sample_i} - I_{Ni\_sample_i})^2$$

Where,  $I_{Nm\_sample_i}$  is  $i^{th}$  sampled measured neutral current,  $I_{Ni\_sample_i}$  is  $i^{th}$  sampled imputed neutral current value computed from the sum of all active current phase inputs in the present integration period, and N is the number of samples in the last measurement interval.

Bit	63	62	61	60	59	58	57	56
	I <sub>x</sub> /I <sub>x_F</sub> [63:56]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	55	54	53	52	51	50	49	48
	I <sub>x</sub> /I <sub>x_F</sub> [55:48]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	47	46	45	44	43	42	41	40
	I <sub>x</sub> /I <sub>x_F</sub> [47:40]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	39	38	37	36	35	34	33	32
	I <sub>x</sub> /I <sub>x_F</sub> [39:32]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	31	30	29	28	27	26	25	24
	I <sub>x</sub> /I <sub>x_F</sub> [31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	I <sub>x</sub> /I <sub>x_F</sub> [23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	I <sub>x</sub> /I <sub>x_F</sub> [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	I <sub>x</sub> /I <sub>x_F</sub> [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

**Bits 63:0 – I<sub>x</sub>/I<sub>x\_F</sub>[63:0]** Amp-Squared-Samples, uQ24.40 (I<sub>x</sub>, I<sub>x\_F</sub>, I<sub>Nm</sub>, I<sub>Nm\_F</sub>), uQ44.20 (I<sub>Ni</sub>, I<sub>Nmi</sub>)



### 3.3.2. Accumulated Phase Voltage Quantities

**Name:** V\_A/V\_B/V\_C/V\_A\_F/V\_B\_F/V\_C\_F

**Property:** Read

The metrology module generates the following accumulated phase voltage ( $V^2$ ) quantities: V\_A, V\_B, V\_C, V\_A\_F, V\_B\_F and V\_C\_F.

They are in units of [Volt<sup>2</sup>samp scaled]. They are scaled accumulated phase voltage quantities in the whole integration period. They are calculated according to the following formula:

$$V_x = \sum_{i=1}^N (V_{x\_sample_i})^2$$

Where,  $V_{x\_sample_i}$  is  $i^{\text{th}}$  sampled phase voltage value of phase x in present integration period; x = [A, B, C]; N is the number of samples in the last measurement interval.

They may be used to calculate the RMS value of phase voltage.

V\_x and V\_x\_F are stored in uQ24.40 format.

Bit	63	62	61	60	59	58	57	56
	V <sub>x</sub> /V <sub>x_F</sub> [63:56]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	55	54	53	52	51	50	49	48
	V <sub>x</sub> /V <sub>x_F</sub> [55:48]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	47	46	45	44	43	42	41	40
	V <sub>x</sub> /V <sub>x_F</sub> [47:40]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	39	38	37	36	35	34	33	32
	V <sub>x</sub> /V <sub>x_F</sub> [39:32]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	31	30	29	28	27	26	25	24
	V <sub>x</sub> /V <sub>x_F</sub> [31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	V <sub>x</sub> /V <sub>x_F</sub> [23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	V <sub>x</sub> /V <sub>x_F</sub> [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	V <sub>x</sub> /V <sub>x_F</sub> [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

**Bits 63:0 – V<sub>x</sub>/V<sub>x\_F</sub>[63:0]** Volt-squared-samples, phase-x (uQ24.40)

### 3.3.3. Accumulated Voltage Quantities Between Phases

**Name:** V\_AB/V\_BC/V\_CA/V\_AB\_F/V\_BC\_F/V\_CA\_F

**Property:** Read

The metrology module generates the following accumulated phase voltage (V) quantities between phases: V\_AB, V\_BC, V\_CA, V\_AB\_F, V\_BC\_F, and V\_CA\_F.

They are in units of [Volt<sup>2</sup>samp scaled]. They are scaled accumulated voltage quantities between phases in the whole integration period. They are calculated according to the following formula:

$$V_{xy} = \sum_{i=1}^N (V_{y\_sample_i} - V_{x\_sample_i}) * (V_{y\_sample_i} - V_{x\_sample_i})$$

Where,

- $V_{x\_sample_i}$  is  $i^{\text{th}}$  sampled phase voltage value of phase x in present integration period
- $V_{y\_sample_i}$  is  $i^{\text{th}}$  sampled phase voltage value of phase y in present integration period
- $x = [A, B, C]$
- $y = [B, C, A]$
- N is the number of samples in the last measurement interval.

They are used to calculate the RMS value of voltage between phases.

V\_xy and V\_xy\_F are stored in uQ24.40 format.

These accumulators are useful for calculating the phase shift between voltages by applying the Law of Cosines. Depending on the application requirements, it can be utilized either the fundamental plus harmonics or the fundamental only, ended in "\_F", registers.

The following numerical example demonstrates the angle computation:

- Data from Metrology Accumulator Registers:
  - V\_A: 0x15219DA3DFFC
  - V\_B: 0x1521A8F07EDF
  - V\_C: 0x1522518EAC3A
  - V\_AB: 0x3F63899CA42A
  - V\_BC: 0x3F67221A3C5C
  - V\_CA: 0x3F661B94C8D4
- The units of these registers are in Volt<sup>2</sup> samp scaled, with a uQ24.40 format. To convert these to decimal values, divide by 2<sup>40</sup>:
  - V\_A: 21.13131165
  - V\_B: 21.13148406
  - V\_C: 21.13405697
  - V\_AB: 63.38881854
  - V\_BC: 63.40286411
  - V\_CA: 63.39885836
- Application of the Law of Cosines:
  - Angle between phases A and B (AB\_phase):  
 $AB\_phase = \arccos((V_{AB} - V_A - V_B) / (-2 * \sqrt{V_A * V_B})) = 119.992^\circ$
  - Angle between phases B and C (BC\_phase):  
 $BC\_phase = \arccos((V_{BC} - V_B - V_C) / (-2 * \sqrt{V_B * V_C})) = 120.007^\circ$

- Angle between phases C and A (CA\_phase):  

$$CA\_phase = \arccos((V\_CA - V\_A - V\_C) / (-2 * \sqrt{V\_A * V\_C})) = 120.001^\circ$$

Bit	63	62	61	60	59	58	57	56
	V_xy/V_xy_F[63:56]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	55	54	53	52	51	50	49	48
	V_xy/V_xy_F[55:48]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	47	46	45	44	43	42	41	40
	V_xy/V_xy_F[47:40]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	39	38	37	36	35	34	33	32
	V_xy/V_xy_F[39:32]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	31	30	29	28	27	26	25	24
	V_xy/V_xy_F[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	V_xy/V_xy_F[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	V_xy/V_xy_F[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	V_xy/V_xy_F[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

**Bits 63:0 – V\_xy/V\_xy\_F[63:0]** Volt-squared-samples, Vx-Vy (uQ24.40)

### 3.3.4. Accumulated Active Power Quantities

**Name:** P\_A/P\_B/P\_C/P\_A\_F/P\_B\_F/P\_C\_F/P\_N/P\_N\_F

**Property:** Read

The metrology module generates the following accumulated active power (P) quantities: P\_A, P\_B, P\_C, P\_A\_F, P\_B\_F, P\_C\_F, P\_N and P\_N\_F.

They are in units of [W-samp scaled]. They are scaled accumulated active power quantities in the whole integration period. They are calculated according to the following formulas:

$$P_x = \sum_{i=1}^N V_{x\_sample_i} \times I_{x\_sample_i} \quad x = [A, B, C]$$

$$P_x = \sum_{i=1}^N V_{avc\_sample_i} \times I_{x\_sample_i} \quad x = [N]$$

Where,  $V_{x\_sample_i}$  is  $i^{\text{th}}$  sampled phase voltage value of phase x in present integration period;  $V_{avc\_sample_i}$  is  $i^{\text{th}}$  sampled phase voltage value of the active voltage channel (according to STATE\_FLAG.TIMING\_Vx) in present integration period;  $I_{x\_sample_i}$  is  $i^{\text{th}}$  sampled phase current value of phase x in present integration period;  $x = [A, B, C, N]$ ; N is the number of samples in the last measurement interval.

They are used to calculate the active power. In the case of the neutral channel, it is useful for calculating the angle of the neutral current.

P\_x and P\_x\_F are stored in sQ23.40 format.

Bit	63	62	61	60	59	58	57	56
	P_x/P_x_F[63:56]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	55	54	53	52	51	50	49	48
	P_x/P_x_F[55:48]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	47	46	45	44	43	42	41	40
	P_x/P_x_F[47:40]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	39	38	37	36	35	34	33	32
	P_x/P_x_F[39:32]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	31	30	29	28	27	26	25	24
	P_x/P_x_F[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	P_x/P_x_F[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	P_x/P_x_F[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	P_x/P_x_F[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

**Bits 63:0 – P\_x/P\_x\_F[63:0]** Watt-samples, phase-x (sQ23.40)

### 3.3.5. Accumulated Reactive Power Quantities

**Name:** Q\_A/Q\_B/Q\_C/Q\_A\_F/Q\_B\_F/Q\_C\_F/Q\_N/Q\_N\_F

**Property:** Read

The metrology module generates the following accumulated reactive power (Q) quantities: Q\_A, Q\_B, Q\_C, Q\_A\_F, Q\_B\_F, Q\_C\_F, Q\_N and Q\_N\_F.

They are in units of [VAR samp-scaled]. They are scaled accumulated reactive power quantities in the whole integration period. They are calculated according to the following formula:

$$Q_x = \sum_{i=1}^N V'_x_{sample_i} \times I''_x_{sample_i} \quad x = [A, B, C]$$

$$Q_x = \sum_{i=1}^N V'_{avc\_sample_i} \times I''_x_{sample_i} \quad x = [N]$$

Where,  $V'_x_{sample_i}$  is  $i^{\text{th}}$  filtered phase voltage value of phase x in present integration period;  $V'_{avc\_sample_i}$  is  $i^{\text{th}}$  filtered phase voltage value of the active voltage channel (according to STATE\_FLAG.TIMING\_Vx) in present integration period;  $I''_x_{sample_i}$  is  $i^{\text{th}}$  filtered phase current value of phase x in present integration period;  $V'_x_{sample_i}$ ,  $V'_{avc\_sample_i}$  and  $I''_x_{sample_i}$  have additional 90 degree phase difference;  $x = [A, B, C]$ ; N is the number of samples in the last measurement interval.

They are used to calculate the reactive power. In the case of the neutral channel, it is useful for calculating the angle of the neutral current.

Q\_x and Q\_x\_F are stored in sQ23.40 format.

Bit	63	62	61	60	59	58	57	56
	Q_x/Q_x_F[63:56]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	55	54	53	52	51	50	49	48
	Q_x/Q_x_F[55:48]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	47	46	45	44	43	42	41	40
	Q_x/Q_x_F[47:40]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	39	38	37	36	35	34	33	32
	Q_x/Q_x_F[39:32]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	31	30	29	28	27	26	25	24
	Q_x/Q_x_F[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	Q_x/Q_x_F[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	Q_x/Q_x_F[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	Q_x/Q_x_F[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

**Bits 63:0 – Q\_x/Q\_x\_F[63:0]** VAR-Samples, Phase-X (sQ23.40)



### 3.3.6. Total Accumulated Quantities

**Name:** ACC\_T0/ACC\_T1/ACC\_T2

**Property:** Read

The metrology module generates the following accumulated total quantities: ACC\_T0, ACC\_T1 and ACC\_T2.

Total accumulated quantities are specified by PCx\_TYPE. They are used to save the total accumulated energy. They are updated every full line cycle (20 ms for 50 Hz and 16.667 ms for 60 Hz).

They are stored in sQ33.30 format. Max  $\pm 8589934$  KWh/KVarh/KAmph/KVAh can be stored in these quantities.

Before resetting the metrology firmware, the application must store present ACC\_T0, ACC\_T1 and ACC\_T2. After resetting the metrology firmware, the application must restore ACC\_T0, ACC\_T1 and ACC\_T2.

ACC\_Tx is stored in sQ33.30 format.

Bit	63	62	61	60	59	58	57	56
	ACC_Tx[63:56]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	55	54	53	52	51	50	49	48
	ACC_Tx[55:48]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	47	46	45	44	43	42	41	40
	ACC_Tx[47:40]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	39	38	37	36	35	34	33	32
	ACC_Tx[39:32]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	31	30	29	28	27	26	25	24
	ACC_Tx[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	ACC_Tx[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	ACC_Tx[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	ACC_Tx[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

**Bits 63:0 – ACC\_Tx[63:0]** Total Accumulated Quantities Specified by PCx\_TYPE (sQ33.30)

### 3.4. Harmonic Analysis Output Quantities

The start address is 0x20088348. The Metrology module generates the following primary output measurement quantities for each measurement interval, per-phase quantities with each phase designated by the subscript “\_x” (where x = [A, B, C] for voltage channels and x = [A, B, C, N] for current channels).

Internal scaling allows accurate harmonic analysis for integration periods of up to 16 seconds for up to full-scale magnitude input waveforms.

**Table 3-6. Harmonic Analysis Output Registers**

Index	Address	Variable	Access Mode	Name	Format	Num Bytes	Min Value	Max Value	Default	Units
0-30	0x20088348 - 0x200883C0	I_A_m_R	R	The real part of DFT result for current, phase A, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Amp samp scaled
31-61	0x200883C4 - 0x2008843C	V_A_m_R	R	The real part of DFT result for voltage, phase A, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Volt samp scaled
62-92	0x20088440 - 0x200884B8	I_B_m_R	R	The real part of DFT result for current, phase B, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Amp samp scaled
93-123	0x200884BC - 0x20088534	V_B_m_R	R	The real part of DFT result for voltage, phase B, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Volt samp scaled
124-154	0x20088538 - 0x200885B0	I_C_m_R	R	The real part of DFT result for current, phase C, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Amp samp scaled
155-185	0x200885B4 - 0x2008862C	V_C_m_R	R	The real part of DFT result for voltage, phase C, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Volt samp scaled
186-216	0x20088630 - 0x200886A8	I_N_m_R	R	The real part of DFT result for current, phase N (neutral), m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Amp samp scaled
217-247	0x200886AC - 0x20088724	I_A_m_I	R	The imaginary part of DFT result for current, phase A, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Amp samp scaled
248-278	0x20088728 - 0x200887A0	V_A_m_I	R	The imaginary part of DFT result for voltage, phase A, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Volt samp scaled
279-309	0x200887A4 - 0x2008881C	I_B_m_I	R	The imaginary part of DFT result for current, phase B, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Amp samp scaled
310-340	0x20088820 - 0x20088898	V_B_m_I	R	The imaginary part of DFT result for voltage, phase B, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Volt samp scaled
341-371	0x2008889C - 0x20088914	I_C_m_I	R	The imaginary part of DFT result for current, phase C, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Amp samp scaled
372-402	0x20088918 - 0x20088990	V_C_m_I	R	The imaginary part of DFT result for voltage, phase C, m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Volt samp scaled
403-433	0x20088994 - 0x20088A0C	I_N_m_I	R	The imaginary part of DFT result for current, phase N (neutral), m-th harmonics (from m=1 to m=31)	sQ13.18	31*4	-	-	-	Amp samp scaled

### 3.4.1. Harmonic Analysis Output Quantities

**Name:** I\_x\_m\_R, I\_x\_m\_I, V\_x\_m\_R, V\_x\_m\_I

**Property:** Read

The metrology module generates the following quantities to calculate appointed *m-th* order harmonic current RMS: I\_A\_m\_R, I\_A\_m\_I, I\_B\_m\_R, I\_B\_m\_I, I\_C\_m\_R, I\_C\_m\_I, I\_N\_m\_R and I\_N\_m\_I.

I\_x\_m\_R is the real part of DFT of phase x current, x = [A, B, C, N].

I\_x\_m\_I is imaginary part of DFT of phase x current, x = [A, B, C, N].

I\_x\_m\_R and I\_x\_m\_I are stored in sQ13.18 format.

Where m is the harmonic order number, from 1 to 31.

The following formula is used to calculate the current RMS value of each phase:

$$I_{RMS\_x\_m} = \frac{\sqrt{2} \times \sqrt{\left(\frac{I_{x\_m\_R} \times K_{Ix}}{2^{18}}\right)^2 + \left(\frac{I_{x\_m\_I} \times K_{Ix}}{2^{18}}\right)^2}}{N} = \frac{\sqrt{2 \times ((I_{x\_m\_R} \times K_{Ix})^2 + (I_{x\_m\_I} \times K_{Ix})^2)}}{2^{18} \times N} [A_{rms}]$$

Where, x = [A, B, C, N]; N is the number of samples in the last measurement interval.

The metrology module generates the following quantities to calculate appointed *m-th* order harmonic voltage RMS: V\_A\_m\_R, V\_A\_m\_I, V\_B\_m\_R, V\_B\_m\_I, V\_C\_m\_R and V\_C\_m\_I.

V\_x\_m\_R is the real part of DFT of phase x voltage, x = [A, B, C].

V\_x\_m\_I is imaginary part of DFT of phase x voltage, x = [A, B, C].

V\_x\_m\_R and V\_x\_m\_I are stored in sQ13.18 format.

Where m is the harmonic order number, from 1 to 31.

The following formula is used to calculate the voltage RMS value of each phase:

$$V_{RMS\_x\_m} = \frac{\sqrt{2} \times \sqrt{\left(\frac{V_{x\_m\_R} \times K_{Vx}}{2^{18}}\right)^2 + \left(\frac{V_{x\_m\_I} \times K_{Vx}}{2^{18}}\right)^2}}{N} = \frac{\sqrt{2 \times ((V_{x\_m\_R} \times K_{Vx})^2 + (V_{x\_m\_I} \times K_{Vx})^2)}}{2^{18} \times N} [V_{rms}]$$

Where, x = [A, B, C]; N is the number of samples in the last measurement interval.

Bit	31	30	29	28	27	26	25	24
	I <sub>x_m_R</sub> /I <sub>x_m_I</sub> /V <sub>x_m_R</sub> /V <sub>x_m_I</sub> [31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	I <sub>x_m_R</sub> /I <sub>x_m_I</sub> /V <sub>x_m_R</sub> /V <sub>x_m_I</sub> [23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	I <sub>x_m_R</sub> /I <sub>x_m_I</sub> /V <sub>x_m_R</sub> /V <sub>x_m_I</sub> [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	I <sub>x_m_R</sub> /I <sub>x_m_I</sub> /V <sub>x_m_R</sub> /V <sub>x_m_I</sub> [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

**Bits 31:0 – I<sub>x\_m\_R</sub>/I<sub>x\_m\_I</sub>/V<sub>x\_m\_R</sub>/V<sub>x\_m\_I</sub>[31:0]** Current/Voltage, phase-x, m-th harmonics (sQ13.18)

### 3.5. Derived Output Quantities

Using Metrology module primary output quantities, the following quantities of interest (per-phase or system) may be derived, using the following formulae.

**Note:** Care must be exercised when using RMS values with integrated values, depending on the length of the integration period.

#### 3.5.1. RMS Value

Total three kinds of RMS values can be calculated directly from the output of metrology firmware: RMS value of all harmonics, RMS value of fundamental harmonic and the RMS value of *m*-th harmonic.

RMS value of all harmonics and RMS value of fundamental harmonic can be calculated as following:

$$I_{x_{rms}} = \frac{K_{Ix}}{2^{10}} \times \sqrt{\frac{ACC\_I_x}{N \times 2^{40}}}$$

$$V_{x_{rms}} = \frac{K_{Vx}}{2^{10}} \times \sqrt{\frac{ACC\_V_x}{N \times 2^{40}}}$$

$$I_{x1_{rms}} = \frac{K_{Ix}}{2^{10}} \times \sqrt{\frac{ACC\_I_{x\_F}}{N \times 2^{40}}}$$

$$V_{x1_{rms}} = \frac{K_{Vx}}{2^{10}} \times \sqrt{\frac{ACC\_V_{x\_F}}{N \times 2^{40}}}$$

Where, x = [A, B, C], and:

- $K_{Ix}$  is the current conversion factor of phase x
- $K_{Vx}$  is the voltage conversion factor
- $I_{x_{rms}}$  is the fundamental and all harmonics current RMS value

- $V_{x_{rms}}$  is the fundamental and all harmonics voltage RMS value
- $I_{x1_{rms}}$  is the fundamental harmonic current RMS value
- $V_{x1_{rms}}$  is the fundamental harmonic voltage RMS value
- $N$  is the number of samples in the integration period
- $ACC\_I\_x$  is the accumulated fundamental and all harmonics current quantity
- $ACC\_V\_x$  is the accumulated fundamental and all harmonics voltage quantity
- $ACC\_I\_x\_F$  is the accumulated fundamental harmonic current quantity
- $ACC\_V\_x\_F$  is the accumulated fundamental harmonic voltage quantity

**Notes:**

- $K\_Ix$  and  $K\_Vx$  are the register values in the metrology control registers.
- $N$  is the register value in the metrology status registers.
- $ACC\_I\_x$ ,  $ACC\_V\_x$ ,  $ACC\_I\_x\_F$  and  $ACC\_V\_x\_F$  are the register values in the metrology accumulated output quantities.

After the harmonic analysis feature is enabled, RMS value of  $m$ -th harmonic can be calculated:

$$I_{RMS\_x\_m} = \frac{\sqrt{2} \times \sqrt{\left(\frac{I_{x\_m\_R}}{2^6}\right)^2 + \left(\frac{I_{x\_m\_I}}{2^6}\right)^2}}{N} = \frac{\sqrt{2 \times ((I_{x\_m\_R})^2 + (I_{x\_m\_I})^2)}}{2^6 \times N} [A_{rms}]$$

$$V_{RMS\_x\_m} = \frac{\sqrt{2} \times \sqrt{\left(\frac{V_{x\_m\_R}}{2^6}\right)^2 + \left(\frac{V_{x\_m\_I}}{2^6}\right)^2}}{N} = \frac{\sqrt{2 \times ((V_{x\_m\_R})^2 + (V_{x\_m\_I})^2)}}{2^6 \times N} [V_{rms}]$$

Where,  $x = [A, B, C]$ , and:

- $I_{x\_m\_rms}$  is the  $m$ -th harmonic current RMS value of phase  $x$
- $V_{x\_m\_rms}$  is the  $m$ -th harmonic voltage RMS value
- $I_{x\_m\_R}$  is the real part of DFT for  $m$ -th harmonic current
- $I_{x\_m\_I}$  is the imaginary part of DFT for  $m$ -th harmonic current
- $V_{x\_m\_R}$  is the real part of DFT for  $m$ -th harmonic voltage
- $V_{x\_m\_I}$  is the imaginary part of DFT for  $m$ -th harmonic voltage

**Notes:**

- $I_{x\_m\_R}$ ,  $I_{x\_m\_I}$ ,  $V_{x\_m\_R}$  and  $V_{x\_m\_I}$  are the register values in metrology harmonic analysis output quantities
- The voltage/current RMS value is updated every one integration period. `INTEGRATION_IRQ` will be generated at the end of integration period and this interrupt can be used to update derived quantities.

**3.5.2. THD**

Due to the limit of the code size, THD is not provided directly by the metrology firmware, but it can be computed by the following formulas:

$$THD_I = \frac{1}{I_1} \sqrt{\sum_{h=2}^{\infty} I_h^2} = \sqrt{\left(\frac{I_{rms}}{I_{1rms}}\right)^2 - 1}$$

$$THD_V = \frac{1}{V_1} \sqrt{\sum_{h=2}^{\infty} V_h^2} = \sqrt{\left(\frac{V_{rms}}{V_{1rms}}\right)^2 - 1}$$

Where:

- $I_1$  is the amplitude of fundamental harmonic current
- $V_1$  is the amplitude of fundamental harmonic voltage
- $I_{rms}$  is the all harmonics current RMS value
- $V_{rms}$  is the all harmonics voltage RMS value
- $I_{1rms}$  is the fundamental harmonic current RMS value
- $V_{1rms}$  is the fundamental harmonic voltage RMS value

### 3.5.3. Energy/Quadergy

Energy and quadergy over the integration period can be calculated from the metrology output registers:

$$P_x = \frac{K_{Ix}}{2^{10}} \times \frac{K_{Vx}}{2^{10}} \times \frac{1}{3600 \times f_s} \times \frac{ACC\_P\_x}{2^{40}} [Wh]$$

$$Q_x = \frac{K_{Ix}}{2^{10}} \times \frac{K_{Vx}}{2^{10}} \times \frac{1}{3600 \times f_s} \times \frac{ACC\_Q\_x}{2^{40}} [VARh]$$

$$S_x = \frac{K_{Ix}}{2^{10}} \times \frac{K_{Vx}}{2^{10}} \times \frac{1}{3600 \times f_s} \times \sqrt{\frac{ACC\_I\_x}{2^{40}}} \times \sqrt{\frac{ACC\_V\_x}{2^{40}}} [VAh]$$

$$P_{x_F} = \frac{K_{Ix}}{2^{10}} \times \frac{K_{Vx}}{2^{10}} \times \frac{1}{3600 \times f_s} \times \frac{ACC\_P\_x\_F}{2^{40}} [Wh]$$

$$Q_{x_F} = \frac{K_{Ix}}{2^{10}} \times \frac{K_{Vx}}{2^{10}} \times \frac{1}{3600 \times f_s} \times \frac{ACC\_Q\_x\_F}{2^{40}} [VARh]$$

$$S_{x_F} = \frac{K_{Ix}}{2^{10}} \times \frac{K_{Vx}}{2^{10}} \times \frac{1}{3600 \times f_s} \times \sqrt{\frac{ACC\_I\_x\_F}{2^{40}}} \times \sqrt{\frac{ACC\_V\_x\_F}{2^{40}}} [VAh]$$

Where, x = [A, B, C] and:

- $f_s$  = 4000 Hz is the output integration sample rate
- $P_x$  is active power of all harmonics of phase x
- $Q_x$  is reactive power of all harmonics
- $S_x$  is apparent power of phase x
- $P_{x_F}$  is active power of fundamental harmonic

- $Q_{x_F}$  is reactive power of fundamental harmonic
- $S_{x_F}$  is fundamental apparent power of phase x
- $ACC\_P\_x$  is the accumulated active power quantity for all harmonics
- $ACC\_Q\_x$  is the accumulated reactive power quantity for all harmonics
- $ACC\_P\_x\_F$  is the accumulated active power quantity for fundamental harmonic
- $ACC\_Q\_x\_F$  is the accumulated reactive power quantity for fundamental harmonic
- $ACC\_I\_x$  is the accumulated fundamental and all harmonics current quantity
- $ACC\_V\_x$  is the accumulated fundamental and all harmonics voltage quantity
- $ACC\_I\_x\_F$  is the accumulated fundamental harmonic current quantity
- $ACC\_V\_x\_F$  is the accumulated fundamental harmonic voltage quantity

### 3.5.4. Average Active and Reactive Power

Average active and reactive power over the integration period may be calculated directly from the metrology output registers for power of all harmonics and power of the fundamental harmonic:

$$P_{x\_Watts} = \frac{K_{Ix}}{2^{10}} \times \frac{K_{Vx}}{2^{10}} \times \frac{ACC\_P\_x}{N \times 2^{40}} [W]$$

$$Q_{x\_VARs} = \frac{K_{Ix}}{2^{10}} \times \frac{K_{Vx}}{2^{10}} \times \frac{ACC\_Q\_x}{N \times 2^{40}} [VAR]$$

$$P_{x_F\_Watts} = \frac{K_{Ix}}{2^{10}} \times \frac{K_{Vx}}{2^{10}} \times \frac{ACC\_P\_x\_F}{N \times 2^{40}} [W]$$

$$Q_{x_F\_VARs} = \frac{K_{Ix}}{2^{10}} \times \frac{K_{Vx}}{2^{10}} \times \frac{ACC\_Q\_x\_F}{N \times 2^{40}} [VAR]$$

Where, x = [A, B, C] and:

- $N$  is the number of samples in the integration period
- $P_{x\_Watts}$  is the average active power of all harmonics of phase x
- $Q_{x\_VARs}$  is the average reactive power of all harmonics
- $P_{x_F\_Watts}$  is the average active power of fundamental harmonic
- $Q_{x_F\_VARs}$  is the average reactive power of fundamental harmonic
- $ACC\_P\_x$  is the accumulated active power quantity for all harmonics
- $ACC\_Q\_x$  is the accumulated reactive power quantity for all harmonics
- $ACC\_P\_x\_F$  is the accumulated active power quantity for fundamental harmonic
- $ACC\_Q\_x\_F$  is the accumulated reactive power quantity for fundamental harmonic

### 3.5.5. Average Apparent Power

Average apparent power over the integration period may be calculated directly from the current and voltage RMS values, as defined in IEEE® 1459:

$$S_{x\_VAs} = I_{x\_rms} \times V_{x\_rms} [VA]$$

$$S_{x_F\_VAs} = I_{x_1\_rms} \times V_{x_1\_rms} [VA]$$

Where, x = [A, B, C] and:

- $S_{x\_VAs}$  is the average apparent power of phase x
- $S_{x_F\_VAs}$  is the average fundamental apparent power of phase x



- $I_{X_{rms}}$  is the fundamental and all harmonics current RMS value
- $V_{X_{rms}}$  is the fundamental and all harmonics voltage RMS value
- $I_{X1_{rms}}$  is the fundamental harmonic current RMS value
- $V_{X1_{rms}}$  is the fundamental harmonic voltage RMS value

### 3.5.6. Vector Power Quantities

Here are examples of some of the possible vector power quantities that may be computed (note that there are multiple definitions for vector power quantities, and the symbols used can vary, such as "U" and "S"):

$$U_x = \sqrt{(P_x)^2 + (Q_x)^2 + (D_x)^2}$$

$$S_x = \sqrt{(P_x)^2 + (Q_x)^2}$$

$$D_x = \sqrt{(U_x)^2 - (S_x)^2}$$

$$F_x = \sqrt{(Q_x)^2 + (D_x)^2}$$

$$N_x = \sqrt{(U_x)^2 - (Q_x)^2}$$

$$U_{aa} = \sum_{x=\{A,B,C\}} U_x$$

$$U_{va} = \sqrt{\left(\sum_{x=\{A,B,C\}} P_x\right)^2 + \left(\sum_{x=\{A,B,C\}} Q_x\right)^2 + \left(\sum_{x=\{A,B,C\}} D_x\right)^2}$$

Where,  $x = [A, B, C]$  and:

- $U_x$  is apparent power of all harmonics of phase x
- $S_x$  is phasor power, all harmonics
- $D_x$  is distortion power, all harmonics
- $F_x$  is fictitious power, all harmonics
- $N_x$  is nonreactive power, all harmonics
- $U_{aa}$  is system arithmetic apparent power, all harmonics
- $U_{va}$  is system vector apparent power, all harmonics

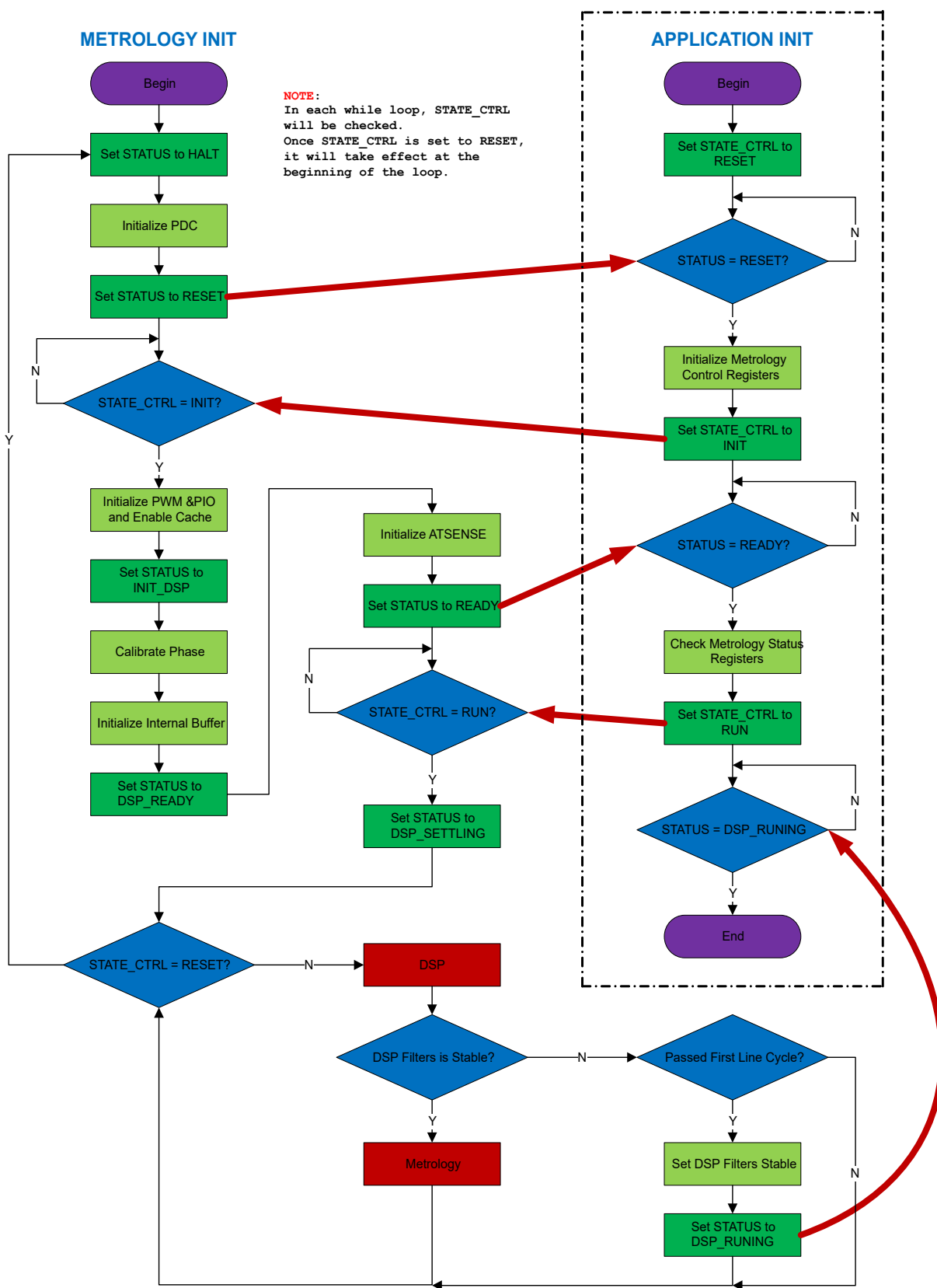
## 4. Interface between Metrology and Application

### 4.1. Interface in Initialization Stage

Application Initialization Sequence:

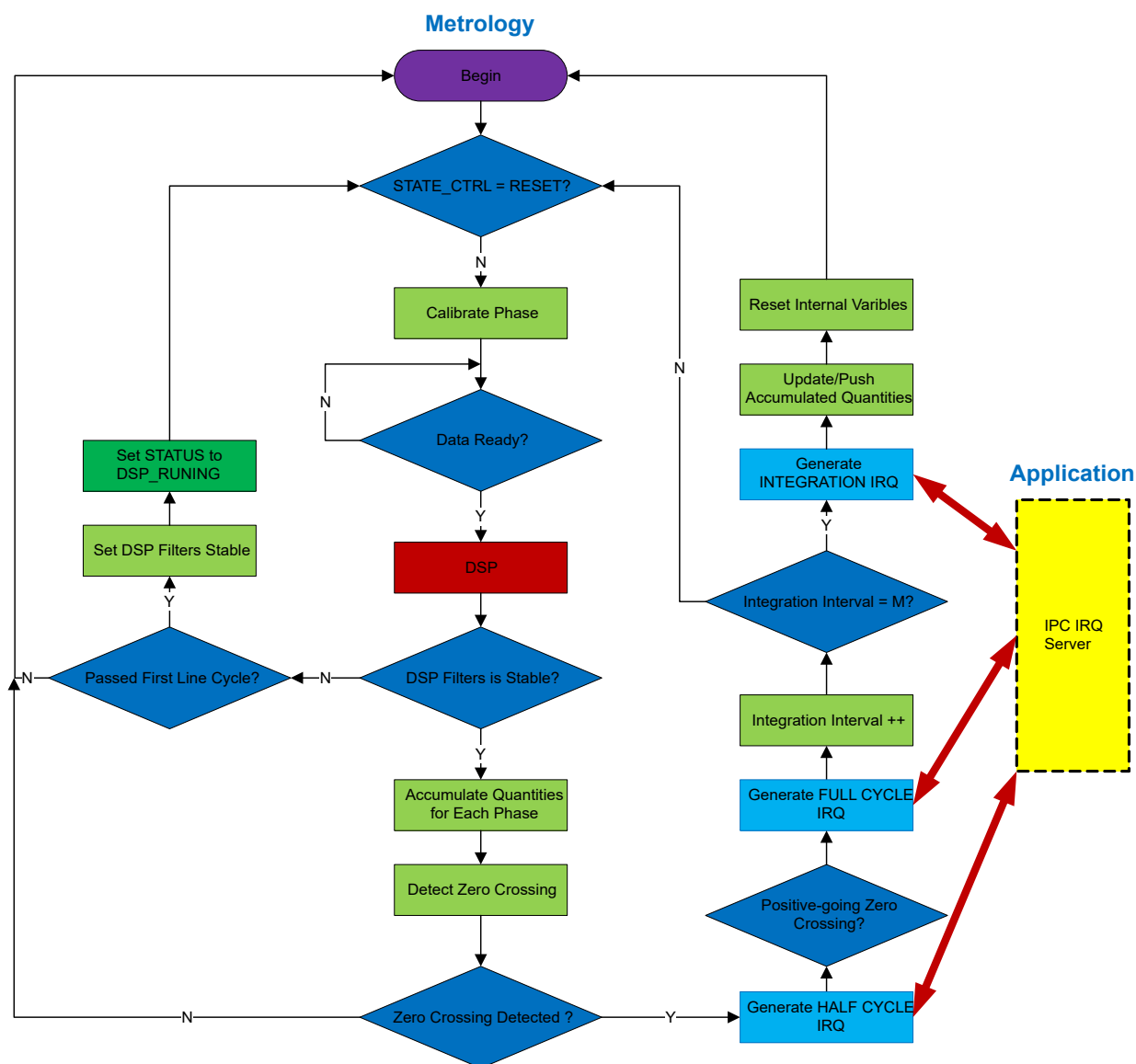
1. Change the [STATE\\_CTRL](#) register to RESET.
2. Wait until Metrology [STATUS](#) changed to RESET or wait until the interrupt is generated: IPC\_INIT\_IRQ.
3. Initialize all other Metrology Control Registers.  
**Note:** The [STATE\\_CTRL](#) register must be initialized to zero.
4. Change the [STATE\\_CTRL](#) register to RUN.
5. Wait until Metrology [STATUS](#) changed to DSP\_RUNNING.

Figure 4-1. Metrology Initialization Flowchart



## 4.2. Interrupts in Metrology Stage

Figure 4-2. Metrology Interrupts Flowchart



The application code can disable any IPC interrupts it does not need.

When an IPC IRQ interrupt arrives, the application code first determines which kind of interrupt occurred, and, then, it checks related Metrology Status Registers and executes its specific handler.

IPC interrupt is defined as the following:

31	30	29	28	27	26	25	24
—	—	—	—	—	PULSE2_IRQ	PULSE1_IRQ	PULSE0_IRQ
23	22	21	20	19	18	17	16
—	—	—	INIT_IRQ	—	—	—	STATUS_IRQ
15	14	13	12	11	10	9	8
—	—	—	RZC_IRQ	—	—	—	—
7	6	5	4	3	2	1	0

CREEP_IRQ	—	HALF_CYCLE_I RQ	FULL_CYCLE_I RQ	—	—	—	INTEGRATION _IRQ
-----------	---	--------------------	--------------------	---	---	---	---------------------

The `sef` lib provided by Microchip can be used to set this register:

- **PULSE0\_IRQ, PULSE1\_IRQ, PULSE2\_IRQ: Pulse Interrupts**

These interrupts are generated immediately after their respective pulse has computationally committed to be generated, but not necessarily occurred.

- **INIT\_IRQ: Initialization Requirement Interrupt**

This interrupt is used to inform the application code to initialize the metrology control registers and the `ACC_T0`, `ACC_T1` and `ACC_T2` if necessary. It can work with handshake enable.

- **STATUS\_IRQ: STATUS Update Interrupt**

This interrupt is used to inform the application code of change(s) in priority status bit(s). This feature is not implemented.

- **RZC\_IRQ: Raw Zero Crossing Interrupt**

This interrupt is generated on zero-crossings using the unfiltered “raw” 16 KHz data stream of the selected direction and selected voltage channel.

- **CREEP\_IRQ: CREEP Detection Interrupt**

This interrupt is used to inform the application code of detection of a creep condition. This feature is not implemented.

- **HALF\_CYCLE\_IRQ: Half Line Cycle Interrupt**

This interrupt is generated every half line cycle. It means that swell and sag flags were updated. Unlike the `RZC_IRQ`, the `HALF_CYCLE_IRQ` uses the 4 KHz narrowband filtered voltage channels and exhibit a deterministic but frequency-dependent phase delay.

- **FULL\_CYCLE\_IRQ: Line Cycle Interrupt**

This interrupt is generated every full line cycle. It means that the frequency and accumulated energy associated with pulse were updated. Unlike the `RZC_IRQ`, the `FULL_CYCLE_IRQ` uses the 4 KHz narrowband filtered voltage channels and exhibits a deterministic but frequency-dependent phase delay.

- **INTEGRATION\_IRQ: Integration Period Interrupt**

This interrupt is used to inform the application code that the whole integration period finishes. It means that all accumulated quantities and status N were updated.

## 5. Annex. Meter Forms

The service type determines what meter form is being implemented and how the Metrology DSP core interprets and processes the ADC values.

**Table 5-1.** Service Types

TYPE	Service Type		Elements	V inputs [Voltage Channels]	#I inputs [Current Channels]	P/S
0	Three-phase 4-wire Wye (3-element)	3P4WY_3E_3V3I	3	3 [v1, v2, v3]	3 [i1,i2,i3]	P
1	Three-phase 4-wire Delta (3-element)	3P4WD_3E_3V3I	3	3 [v1, v2, v3]	3 [i1,i2,i3]	P
2	Three-phase 4-wire Wye (2-½ element) †1	3P4WY_2p5E_2V3I	2 1/2	2 [v1, v2, v3]	3 [i1,i2,i3]	P
3	Three-phase 4-wire Delta (2-element) †2	3P4WD_2E_3V2I	2	3 [v1, v2, v3]	2 [i1,i3]	P
4	Three-phase 3-wire Delta (2-element)	3P3WD_2E_2V2I	2	2 [v1, v3]	2 [i1,i3]	P
5	Two-phase 3-wire Network (2 element) †3	2P3W_2E_2V2I	2	2 [v1, v3]	2 [i1,i3]	P
6	Single-phase 3-wire (1-½ element) †4	1P3W_1p5E_1V2I	1 1/2	1 [v1]	2 [i1,i3]	P
7	Single-phase 2-wire (1 element)	1P2W_1E_1V1I	1	1 [v1]	1 [i1]	P/S
8	Single-phase 3-wire (1 element) †5	1P3W_1E_2V1I	1	2 [v1, v3]	1 [i1]	P

The next chapters show the configuration for each Service Type.

†1 For the Three-phase 4-wire Wye 2-½ element meter, any one phase voltage may be selected to be the missing phase, and the missing voltage will be internally imputed from the other 2 phase voltages.

†2 For the Three-phase 4-wire Delta 2 element meter, one current sensor is used to measure the collective current of two phases, (IA-IB). All phase voltages VA, VB and VC are measured.

†3 For the Two-phase 3-wire 2 element meter, three common service types with two separate voltage phases and two separate currents may be metered by this mathematically identical service type. These are commonly known as:

- Two-phase 3-wire Network (2p3WN)
- Single-phase 3-wire 2 element (1p3W\_2E)
- Two-phase 5-wire (2p5W) with 2 current sensors each used to measure the collective currents of (IA-IA') and (IC-IC')

†4 For the Single-phase 3-wire 1-½ element meter where only one phase-phase voltage, VAC, is measured but 2 current elements are measured.

†5 For the Single-phase 3-wire 1 element meter where two individual phase voltages, VA & VC, are measured but only one current element is measured.

**METER\_TYPE** contains all the possibilities for the Service Type available and their configurations.

Figure 5-1. Meter Forms Summary

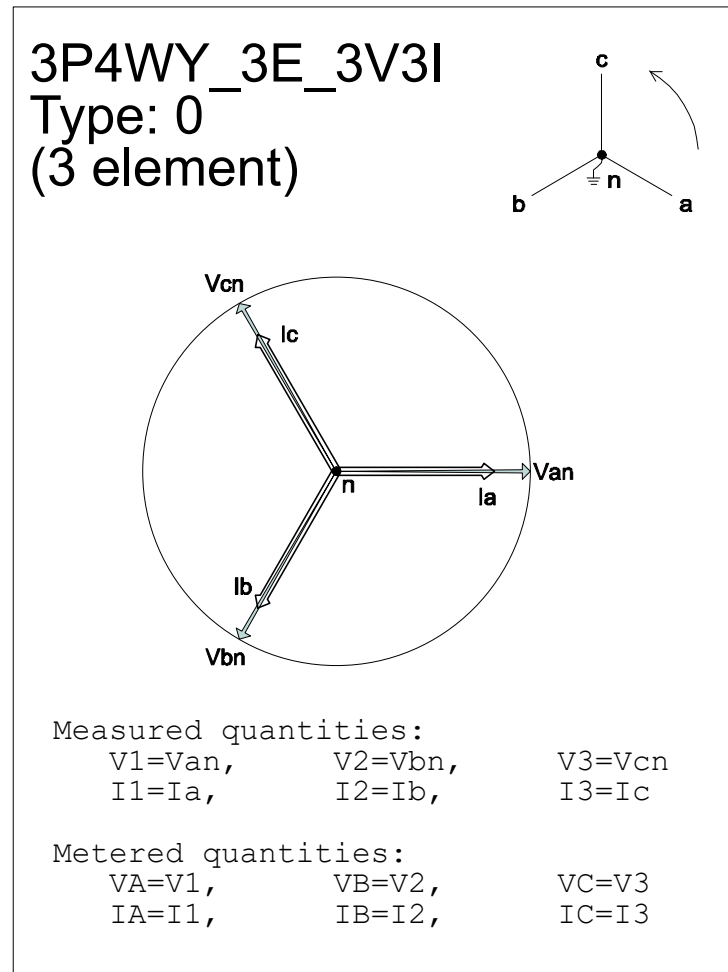
<p><b>3P4WY_3E_3V3I</b> Type: 0 (3 element)</p> <p>Measured quantities:  <math>V1=Van</math>, <math>V2=Vbn</math>, <math>V3=Vcn</math>  <math>I1=Ia</math>, <math>I2=Ib</math>, <math>I3=Ic</math></p> <p>Metered quantities:  <math>VA=V1</math>, <math>VB=V2</math>, <math>VC=V3</math>  <math>IA=I1</math>, <math>IB=I2</math>, <math>IC=I3</math></p>	<p><b>3P4WD_3E_3V3I</b> Type: 1 (3 element)</p> <p>Measured quantities:  <math>V1=Van</math>, <math>V2=Vbn</math>, <math>V3=Vcn</math>  <math>I1=Ia</math>, <math>I2=Ib</math>, <math>I3=Ic</math></p> <p>Metered quantities:  <math>VA=V1</math>, <math>VB=V2</math>, <math>VC=V3</math>  <math>IA=I1</math>, <math>IB=I2</math>, <math>IC=I3</math></p>	<p><b>3P3WY_2.5E_2V3I</b> Type: 2 (2-1/2 element)</p> <p>Measured quantities:  <math>V1=Van</math>, <math>V2=Vbn</math>, <math>V3=Vcn</math>  <math>I1=Ia</math>, <math>I2=Ib</math>, <math>I3=Ic</math></p> <p>Metered quantities:  <math>VA=V1</math>, <math>VB=-(V1+V3)</math>, <math>VC=V3</math>  (*or any one missing voltage phase)  <math>IA=I1</math>, <math>IB=I2</math>, <math>IC=I3</math></p> <p>This is a Non-Blondel metering solution.</p>	<p><b>3P4WD_2E_3V2I</b> Type: 3 (2 element)</p> <p>Measured quantities:  <math>V1=Van</math>, <math>V2=Vbn</math>, <math>V3=Vcn</math>  <math>I1=Ia-Ib</math>, <math>I2=Ib</math>, <math>I3=Ic</math></p> <p>Metered quantities:  <math>VA=V1</math>, <math>VB=V2</math>, <math>VC=V3</math>  <math>IA=I1/2</math>, <math>IB=-I1/2</math>, <math>IC=I3</math></p> <p>This is a Non-Blondel metering solution.</p>
<p><b>3P3WD_2E_2V2I</b> Type: 4 (2 element)</p> <p>Measured quantities:  <math>V1=Vab</math>, <math>V2=Vcb</math>, <math>V3=Vcb</math>  <math>I1=Ia</math>, <math>I2=Ib</math>, <math>I3=Ic</math></p> <p>Metered quantities:  <math>VA=V1</math>, <math>VB=0</math>, <math>VC=V3</math>  <math>IA=I1</math>, <math>IB=0</math>, <math>IC=I3</math></p>	<p><b>2P3W_2E_2V2I (2P3WN, 2P5W, 1P3W2E)</b> Type: 5 (2 element)</p> <p>Measured quantities:  <math>V1=Van</math>, <math>V2=Vbn</math>, <math>V3=Vcn</math>  <math>I1=Ia</math>, <math>I2=Ib</math>, <math>I3=Ic</math></p> <p>Metered quantities:  <math>VA=V1</math>, <math>VB=0</math>, <math>VC=V3</math>  <math>IA=I1</math>, <math>IB=0</math>, <math>IC=I3</math></p> <p>Note: for 2P5W  <math>I1=Ia-Ia'</math>  <math>I3=Ic-Ic'</math></p>	<p><b>1P3W_1.5E_1V2I</b> Type: 6 (1-1/2 element)</p> <p>Measured quantities:  <math>V1=Vac</math>, <math>V2=Vbn</math>, <math>V3=Vcn</math>  <math>I1=Ia</math>, <math>I2=Ib</math>, <math>I3=Ic</math></p> <p>Metered quantities:  <math>VA=V1/2</math>, <math>VB=0</math>, <math>VC=-V1/2</math>  <math>IA=I1</math>, <math>IB=0</math>, <math>IC=I3</math></p> <p>This is a Non-Blondel metering solution.</p>	<p><b>1P2W_1E_1V1I</b> Type: 7 (1 element)</p> <p>Measured quantities:  <math>V1=Van</math>, <math>V2=Vbn</math>, <math>V3=Vcn</math>  <math>I1=Ia</math>, <math>I2=Ib</math>, <math>I3=Ic</math></p> <p>Metered quantities:  <math>VA=V1</math>, <math>VB=0</math>, <math>VC=0</math>  <math>IA=I1</math>, <math>IB=0</math>, <math>IC=0</math></p>
<p><b>1P3W_1E_2V1I</b> Type: 8 (1 element)</p> <p>Measured quantities:  <math>V1=Van</math>, <math>V2=Vbn</math>, <math>V3=Vcn</math>  <math>I1=Ia-Ic</math></p> <p>Metered quantities:  <math>VA=V1</math>, <math>VB=0</math>, <math>VC=V3</math>  <math>IA=I1/2</math>, <math>IB=0</math>, <math>IC=-I1/2</math></p> <p>This is a Non-Blondel metering solution.</p>			

## 5.1. Service Type 0 – 3P4WY\_3E\_3V3I

Metering form 3-Phase 4-Wire WYE, 3-Elements, 3-Voltages, 3-Currents

This is the default metrology metering form.

Figure 5-2. Service Type 0 – 3P4WY\_3E\_3V3I



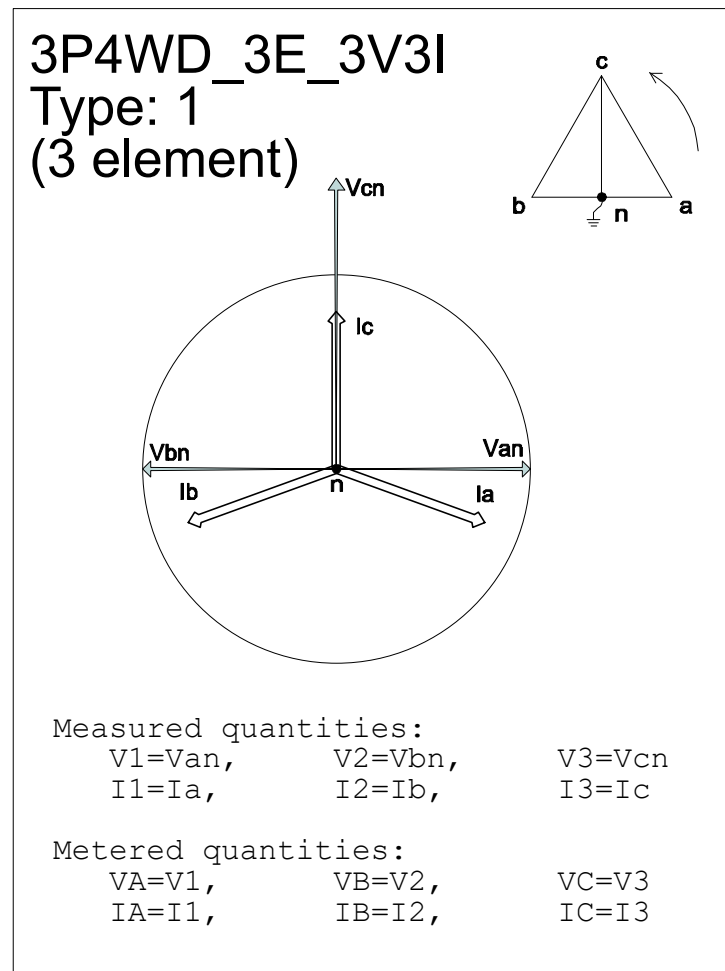
In the most straight-forward, default non-transformational processing, metering with form type:0 is mathematically the equivalent to metering with form type:1. However, as expected, differences would be evident in different reported results for phase-phase voltage values as well as phasing between the voltage and current channels.



## 5.2. Service Type 1 – 3P4WD\_3E\_3V3I

Metering form 3-Phase 4-Wire DELTA, 3-Elements, 3-Voltages, 3-Currents

Figure 5-3. Service Type 1 – 3P4WD\_3E\_3V3I



In the most straight-forward, default non-transformational processing, metering with form type:1 is mathematically the equivalent to metering with form type:0. However, as expected, differences would be evident in different reported results for phase-phase voltage values as well as phasing between the voltage and current channels.

### Dto4WY\_TRANSFORM EQUATIONS:

The DtoY\_TRANSFORM option enables the following alternate transform equations:

- $V_A = V1 - V3/3$
- $V_B = V2 - V3/3$
- $V_C = (2/3)V3$

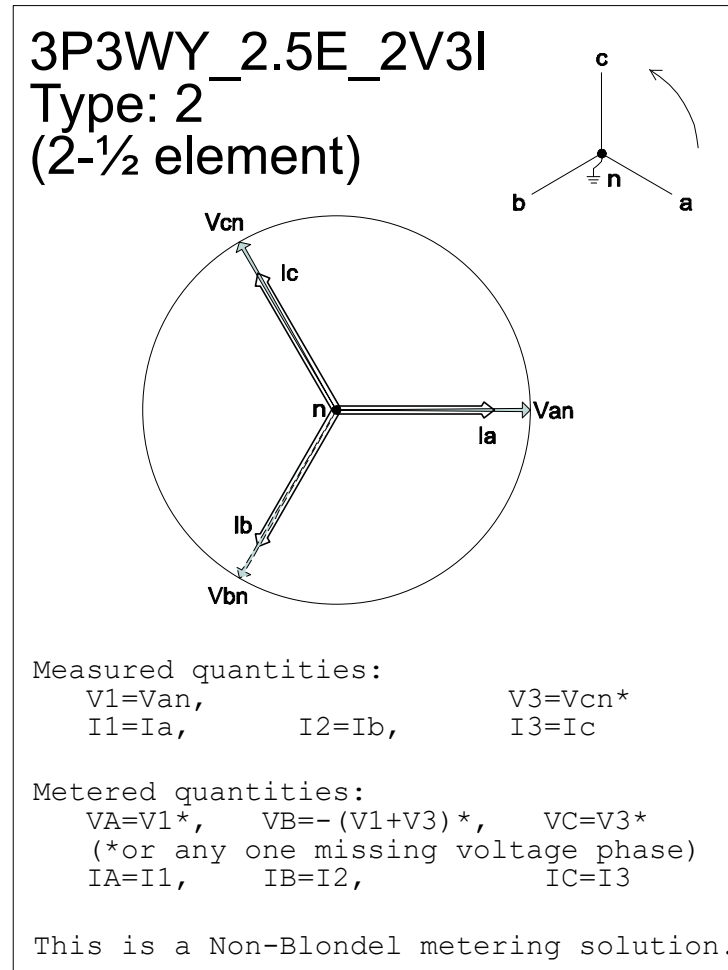
**Note:** Transforms may introduce metering artifacts in the case of non-Blondel and unbalanced situations.

### 5.3. Service Type 2 – 3P4WY\_2.5E\_2V3I

Meter form 3-Phase 3-Wire WYE, 2½-Elements, 2-Voltages, 3-Currents

Use this meter form type to mathematically generate any one missing voltage phase for a 3-wire WYE 2½ element service.

Figure 5-4. Service Type 2 – 3P4WY\_2p5E\_2V3I



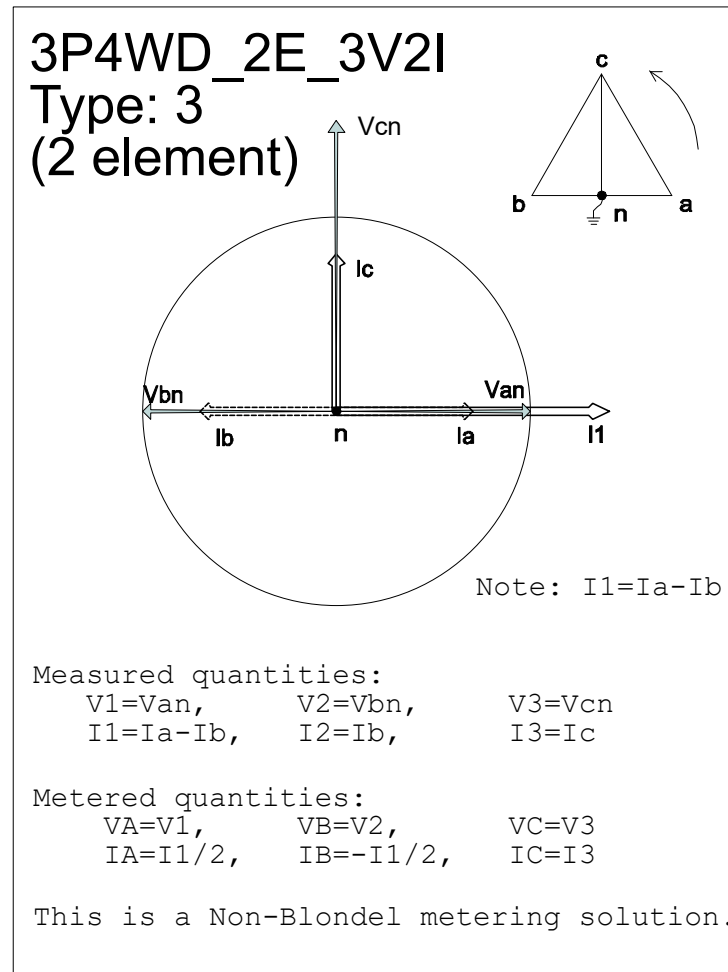
To minimize lost revenue, this meter form type may be dynamically selected to generate any one missing phase potential when detecting a dropped phase voltage of a 4-wire WYE 3-element service.

### 5.4. Service Type 3 – 3P4WD\_2E\_3V2I

3-Phase 4-Wire DELTA, 2-Elements, 3-Voltages, 2-Currents

Use this meter form type to mathematically generate balanced currents for Phase-A and Phase-B from a single shared current sensor for the lighting load phases.

Figure 5-5. Service Type 3 – 3P4WD\_2E\_3V2I



#### Dto4WY\_TRANSFORM EQUATIONS:

The DtoY\_TRANSFORM option enables the following alternate transform equations:

- $V_A = V1 - V3/3$   $I_A = I1/2 - I3/2$
- $V_B = V2 - V3/3$   $I_B = -I2/2 - I3/2$
- $V_C = (2/3)V3$

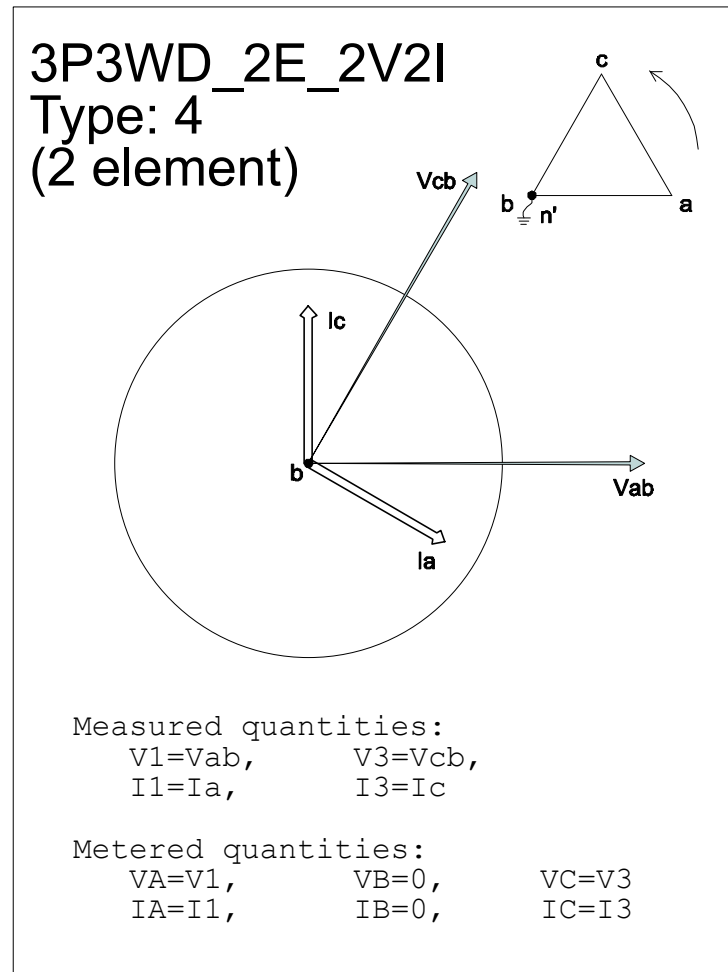
**Note:** Transforms may introduce metering artifacts in the case of non-Blondel and unbalanced situations.

### 5.5. Service Type 4 – 3P3WD\_2E\_2V2I

3-Phase 3-Wire DELTA, 3-Elements, 2-Voltages, 2-Currents

Use this meter form type to meter the typical 3-phase 3-wire delta 2 element service.

Figure 5-6. Service Type 4 – 3P3WD\_2E\_2V2I



In the most straight-forward, default non-transformational processing, metering with form type:4 is mathematically the equivalent to metering with form type:5. However, as expected, differences would be evident in different reported results for phase-phase voltage values as well as phasing between the voltage and current channels.

#### Dto4WY\_TRANSFORM EQUATIONS:

The DtoY\_TRANSFORM option enables the following alternate transform equations:

- $VA = (2/3)V1 - V3/3$
- $VB = -(V1 + V3)/3$   $IB = -(I1 + I3)$
- $VC = (2/3)V3 - V1/3$

**Note:** Transforms may introduce metering artifacts in the case of non-Blondel and unbalanced situations.

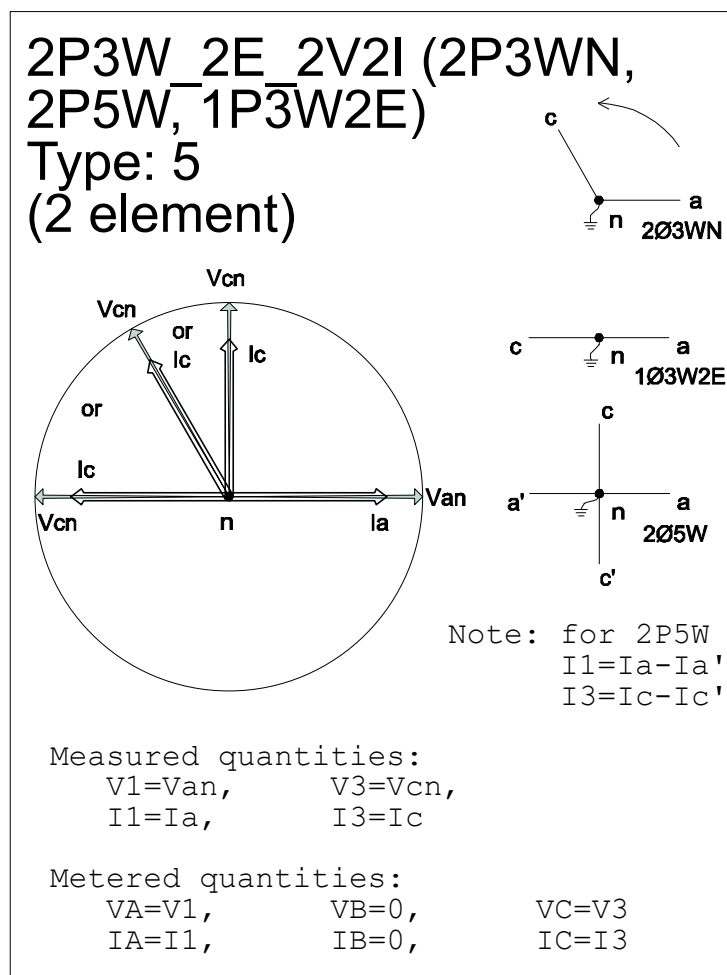
## 5.6. Service Type 5 – 2P3W\_2E\_2V2I

2-Phase 3-Wire NETWORK, 2-Elements, 2-Voltages, 2-Currents

Use this meter form type when metering any 2-Phase service with two phases of voltage measurement, each with its own current measurement. Mathematically, this makes three seemingly different services: 2-Phase 3-Wire Network, 2-Phase 5-Wire, and the “1-Phase” 3-Wire 2-Element

meter forms all mathematically equivalent, except for the results reported for phase-phase voltages and voltage-current phasing.

**Figure 5-7. Service Type 5 – 2P3W\_2E\_2V2I**



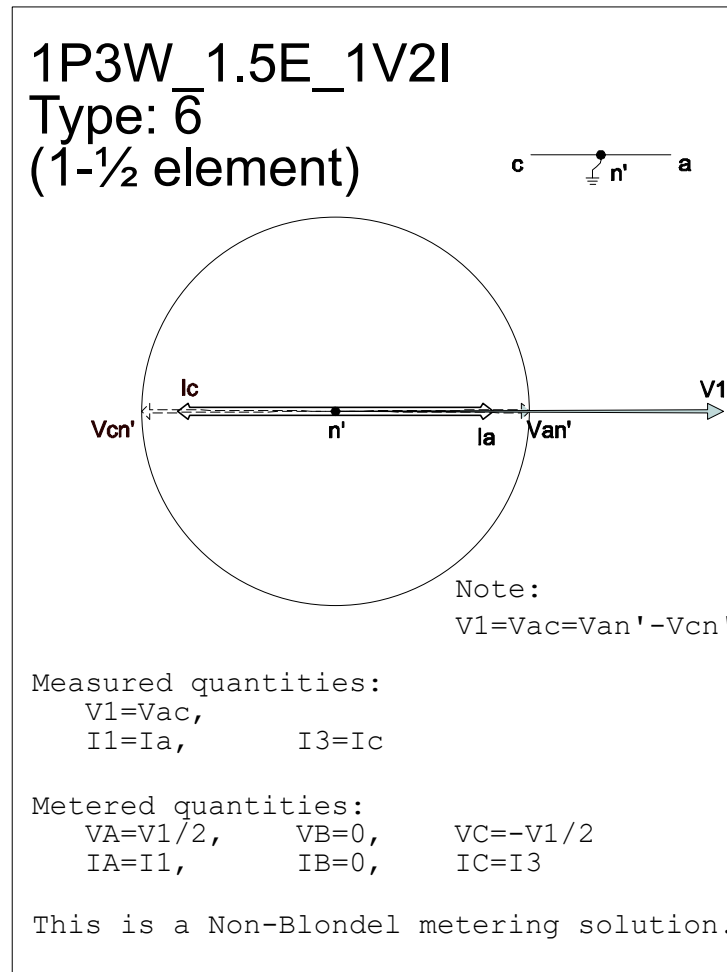
In the most straightforward, default non-transformational processing, metering with form type:5 is mathematically the equivalent to metering with form type:4. However, as expected, differences would be evident in different reported results for phase-phase voltage values as well as phasing between the voltage and current channels.

## 5.7. Service Type 6 – 1P3W\_1.5E\_1V2I

1-Phase 3-Wire, 1½-Elements, 1-Voltage, 2-Currents

Use this meter form type when metering a single-phase application using a single phase-phase voltage sensor, but two separate current measuring elements. In this application, it would be expected that the meter is "hot" with the metrology not explicitly connected to an external neutral reference.

Figure 5-8. Service Type 6 – 1P3W\_1p5E\_1V2I

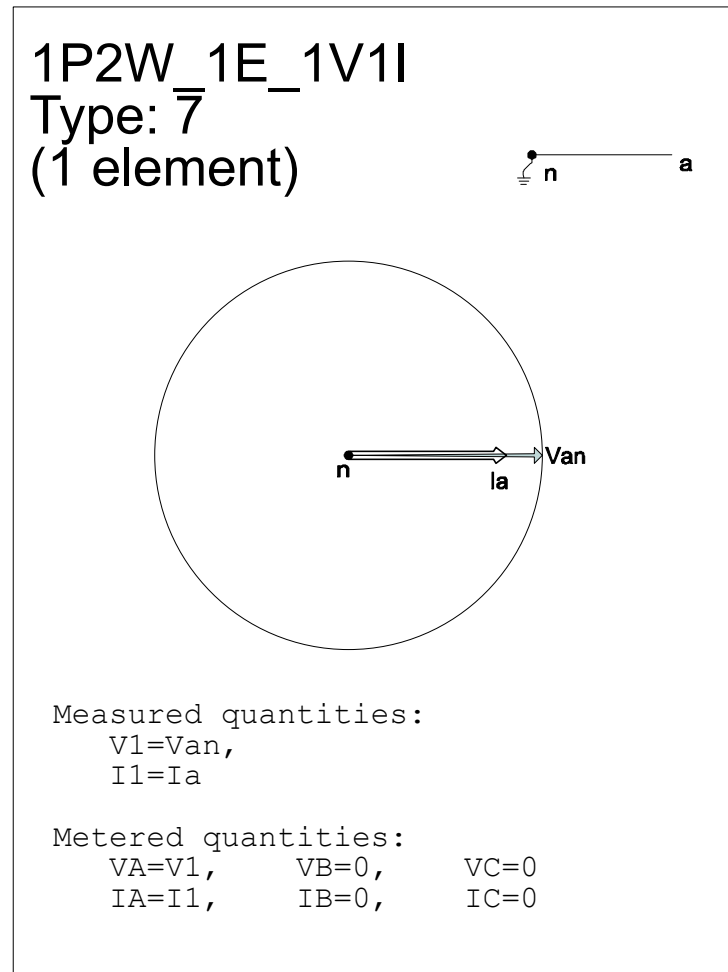


## 5.8. Service Type 7 – 1P2W\_1E\_1V1I

1-Phase 2-Wire, 1-Element, 1-Voltage, 1-Current

Use this meter form type when metering a single-phase metering application with one voltage and one current.

Figure 5-9. Service Type 7 – 1P2W\_1E\_1V1I

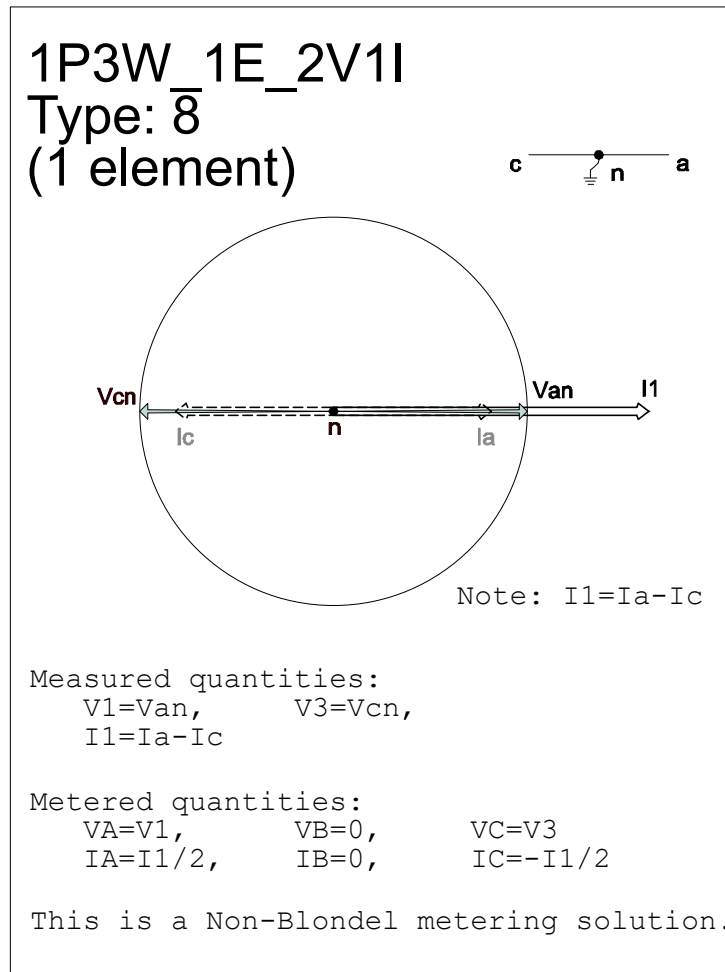


## 5.9. Service Type 8 – 1P3W\_1E\_2V1I

1-Phase 3-Wire, 1-Element, 2-Voltages, 1-Current

Use this meter form type when metering a single-phase application using a single shared current sensor but two separate phase voltage measurement inputs 180° out of phase.

Figure 5-10. Service Type 8 – 1P3W\_1E\_2V1I





## 6. References

- ATSENSE-101/ATSENSE-301(H) Multi-Channel Sigma-Delta Analog Front End (*DS60001524*)
- Microchip PIC32CXMTx Metrology User Guide (*DS50003460*)

## 7. Revision History

### Revision E - 06/2025

Document	<ul style="list-style-type: none"> <li>• Metrology library version v3.3.00.</li> <li>• Apparent energy has been integrated as a source for metrology pulses.</li> <li>• The <a href="#">Metrology Interface Definition</a> section provides detailed information regarding the sizes and addresses of the register blocks.</li> <li>• Updated Index and added Address column in the following tables: <a href="#">Table 3-2</a>, <a href="#">Table 3-4</a>, <a href="#">Table 3-5</a>, and <a href="#">Table 3-6</a>.</li> <li>• Added Reset Value = 0 in all Registers.</li> <li>• Updated start address in <a href="#">Metrology Status Registers</a>, <a href="#">Accumulated Output Quantities</a>, and <a href="#">Harmonic Analysis Output Quantities</a> sections.</li> <li>• Added new control registers <a href="#">S_K_t</a>, <a href="#">CREEP_THRESHOLD_S</a>, and <a href="#">POWER_OFFSET_S</a>.</li> <li>• The control register <a href="#">FEATURE_CTRL</a> now includes a new flag, <a href="#">CREEP_S_EN</a>, and the flag, <a href="#">SYNCH</a>, changed the name from "Active Voltage Channel Selection" to "Dominant Voltage Channel Selection".</li> <li>• The control register <a href="#">PULSEx_CTRL</a> has been modified to support the new functionalities related to apparent power pulsing capabilities.</li> <li>• The control register <a href="#">POWER_OFFSET_CTRL</a> now includes a new flag, <a href="#">S_OFFSET_PUL</a>.</li> <li>• Added Warning in <a href="#">HARMONIC_CONTROL</a>, <a href="#">CAL_M_Ix</a>, and <a href="#">CAL_M_Vx</a> registers.</li> <li>• The status register <a href="#">STATE_FLAG</a> now includes a new flag, <a href="#">CREEP_DET_S</a>, and the flag, <a href="#">TIMING_Vx</a>, changed the name from "Active Voltage Channel" to "Dominant Voltage Channel".</li> <li>• The status register <a href="#">FREQ</a> changed the name from "Active Line Voltage Fundamental Harmonic Frequency" to "Dominant Line Voltage Fundamental Harmonic Frequency".</li> <li>• Added Note in <a href="#">FREQ</a>, and <a href="#">FREQ_Vx</a> registers.</li> <li>• Added an example for calculating the phase shift between voltages by applying the Law of Cosines in <a href="#">V_AB/V_BC/V_CA/V_AB_F/V_BC_F/V_CA_F</a> register.</li> <li>• Added VAh unit in <a href="#">ACC_T0</a>, <a href="#">ACC_T1</a>, and <a href="#">ACC_T2</a> in <a href="#">Table 3-5</a> and in <a href="#">ACC_T0/ACC_T1/ACC_T2</a> register.</li> <li>• Changed <a href="#">sQ13.8</a> by <a href="#">sQ13.18</a> in <a href="#">Harmonic Analysis Output Quantities</a> section.</li> <li>• Updated the first paragraph in <a href="#">THD</a> section.</li> <li>• Updated <a href="#">Energy/Quadergy</a>, and <a href="#">Vector Power Quantities</a> sections.</li> <li>• Added <a href="#">Average Apparent Power</a> section.</li> </ul>
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## Revision D - 12/2024

Document	<ul style="list-style-type: none"> <li>• Metrology library version v3.2.00.</li> <li>• The library is able to compute up to 31 harmonic orders simultaneously.</li> <li>• Functionality in FEATURE_CTRL0 and FEATURE_CTRL1 has been unified in FEATURE_CTRL0.</li> <li>• FEATURE_CTRL1 was renamed to HARMONIC_CTRL. This register is used to enable the harmonic computation and for selecting the desired harmonics orders to be calculated.</li> <li>• STATE_FLAG.HARMONIC_m_CONF[7:0] field was removed.</li> <li>• HARMONIC output registers increased to 434 registers. The format changes. The values are not scaled with K_L_x and K_V_x registers.</li> <li>• PU (Pull-Up) and OPD (Open-Drain) features removed from pulse control registers, as these functionalities are not available while under PWM peripheral control.</li> <li>• Added a protection mechanism to avoid the issue that sometimes happened when the library was incorrectly configured to pulse all the energy being applied. The improper configuration occurred when the configured meter constants and pulse widths generated a pulse rate not supported, when applying energies above a threshold. The effect was that sometimes the library was not working properly, affecting the accuracy of the measurements.</li> <li>• In previous version, the metrology library disabled the watchdogs. Now the watchdog control register is not written.</li> </ul>
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## Rev C - 03/2024

Document	<ul style="list-style-type: none"> <li>• Metrology library version v3.1.02.</li> <li>• Pulse algorithm changed to support testing inter-harmonics in the current circuits (burst fired waveform test, as defined in IEC62052-11:2021) using the pulses.</li> <li>• Added counters for the number of pulses issued in the three pulse outputs. The counters are shown in the status registers 25, 26 and 27.</li> <li>• Corrected a bug that in certain circumstances could generate unexpected pulses when transitioning from a high pulse rate to a very low or zero pulse rate.</li> <li>• Included a clarification regarding the maximum metrology pulse rate.</li> </ul>
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## Rev B - 10/2023

Document	<ul style="list-style-type: none"> <li>• Changed name of document from "<i>Microchip PIC32CXMTx Metrology Data Sheet</i>" to "<i>PIC32CXMTx Metrology Reference Guide</i>".</li> <li>• Metrology library version v3.1.00.</li> <li>• Metrology pulses peripheral clock rate increased to 7.424 MHz.</li> <li>• Pulse algorithm improved.</li> <li>• Bug affecting the frequency measurements corrected. In previous versions, the frequency of the non-dominant phases was not accurate.</li> <li>• Maximum metrology pulse rate increased to 1800 pulses/sec.</li> </ul>
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## Rev A - 12/2022

Document	<ul style="list-style-type: none"> <li>• Initial release.</li> <li>• Metrology library version v3.0.0b.</li> </ul>
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