MM256K DRAM
Technical Reference Manual

MORROW DESIGNS

MM256K Board
Technical Reference Manual

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1. INTRODUCTION

Morrow Designs' MM256K board provides 256 kilobytes of fast, dynamic memory for IEEE-696 S-100 computer systems. The board is compatible with IEEE-696 S-100 boards, including the 6 MHz Z80B.

The MM256K significantly increases the amount of memory available for multi-user systems, such as the Morrow Designs' Micronix Operating System, and thereby decreases the amount of additional hardware originally required for these system.

You'll find the board easy to use and install. There are no switches to set, and only one set of jumpers, which set the board's memory address.

The board uses reliable 64 Kbit RAM chips that draw little power. We think you'll find the MM256K board to be an efficient and economical addition to your system.

1.1. Hardware Features

The MM256K board offers the following features:

1. The memory in the MM256K board can be located on any 256K boundary, and comes factory set as the first 256K in your system.

2. The board is fully compatible with extended addressing, and handles 8- or 16-bit data transfers.

3. You do not have to worry about the refresh cycle on the MM256K board since the board generates an automatic wait state if your computer asks for information during a memory refresh. This means that all of your software works without modification.

4. The MM256K board is designed to work without wait states with microprocessors that run at 6 MHz or less, such as the Morrow Designs MPZ80 CPU. Wait states are generated automatically with CPU's running at faster rates (up to 10 MHz). A parity checking option is also available for the MM256K board.

1.2. Manual Organization

This manual has been designed for all users of the MM256K board. Chapter 2 generally describes the board's functions and its settings as shipped from the factory. Chapter 3 covers board installation, and all users are advised to read this chapter before installing the MM256K board.

Chapter 4 covers maintenance and chip replacement, Chapter 5 contains special application notes concerning traces on the board, and Chapter 6 is the theory of operation of the board.

Users installing the MM256K board in a non-Morrow Designs system should read through Chapters 5 and 6 before installing the boards in their systems. The appendix contains technical specifications, schematics, and a parts list for the board.

2. BOARD OVERVIEW

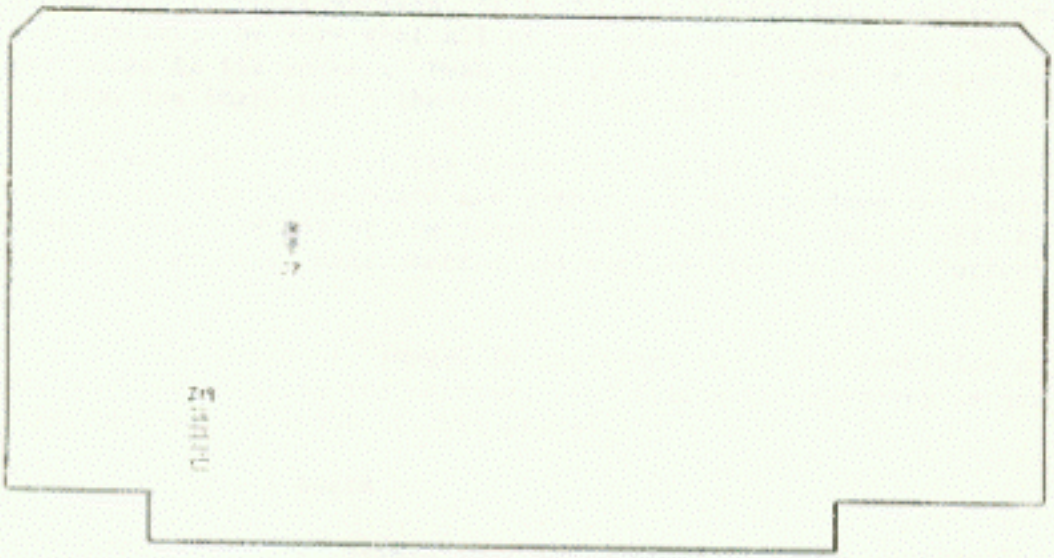
The MM256K board adds 256K of dynamic memory to any IEEE/696 (S-100) system. There are two user-configurable sets of jumpers, which allow you to change the beginning address of the board and the refresh cycle.

2.1. Factory Jumper Settings

Your MM256K board comes ready to install in a Morrow Designs Decision 1 system which contains no memory. The board will provide 256K of memory, starting at address 00000H. It is also set to perform its internal memory refresh cycles after each read operation.

The board initially comes with a jumper connector on the top two pins of jumper J7, and all pairs of pins connected on jumper J19:

Table 2-1: Factory Settings for Jumpers



(On some boards jumper J7 may be directly soldered on the board rather than having jumper posts.)

The next section discusses the base address of the board. Changing the factory-set values of the jumpers is discussed in Chapter 5.

2.2. Factory Set Memory Address

The board comes set for use between 0 and 256K, with all six pairs of jumper pins connected. The MX256K board can be used as memory that begins at any 256K boundary in the available 16 Megabyte region. This means that it can be used as memory locations 0-256K, 256K-512K, etc. See Chapter 5 for instructions on changing the base address of the board.

3. BOARD INSTALLATION

All computer boards must be handled with care, since the components on them can be damaged by bending or bumping. Also, the RAM chips in the chip sockets can come loose if the board is mishandled.

You should also be especially careful of static electricity when you handle the MM256K board, since the memory chips are susceptible to damage from static. Discharge any static that has built up on your body by touching an electrically grounded piece of metal (such as a cold water pipe or the screw on an electrical outlet) before handling the board.

3.1. Inspecting the Board

Inspect the MM256K board for shipping damage. Be sure that the traces (the foil leads on the front and back of the board) are not scratched, and that all of the capacitors (the blue, green, and red components on the board) are intact.

Check that the RAM chips in the top two rows of the board are seated in their sockets. If a RAM chip is not fully seated in its socket, be sure that all of the pins of the chip are above the holes in its socket. Push gently on the end that is sticking up from the board until the chip is flat against the socket.

Also, be sure that the black rectangular jumper connectors that stand above the board are pushed all the way down on their jumper pins. If any of the jumper connectors have fallen off the board, read the next section and replace them on the correct pins.

If the board is damaged in shipping, note the condition on the waybill, notify the carrier, and follow the Warranty Return Procedure in the front of this manual.

3.2. Seating the board

Once your are certain that the jumpers are set correctly, install the board in your system. Make sure that your computer is not plugged in. **Do not install or handle this board with the system plugged in, as this may cause damage to the board components.**

Slide the board in any free slot on the mainframe, making sure the component side of the board is facing the same direction as the component side of the other boards in your system. Gently push the top of the board so that the bottom section fits snugly into the connector on the mainframe bus.

Your computer is now ready to operate with the MM256K board. If you need to remove the board, pull gently on the top of the board and rock it to loosen it from the mainframe, then simply pull up on the board.

4. MAINTENANCE

The MM256K board requires no maintenance other than the usual maintenance you perform on your computer.

If your computer system reports that there is a bad byte of RAM memory on the board, use the following table to determine which chip contains the bad memory:

Table 4-1: Locating Bad Memory Chips

Address	Byte type	Bit within byte							
		0	1	2	3	4	5	6	7
0-128K	Even bytes	U1	U2	U3	U4	U5	U6	U7	U8
	Odd bytes	U13	U14	U15	U16	U17	U18	U19	U20
128-256K	Even bytes	U21	U22	U23	U24	U25	U26	U27	U28
	Odd bytes	U32	U33	U34	U35	U36	U37	U38	U39

On your MM256K board, chips U1-U8 are in the upper left corner, chips U13-U20 in the upper right corner, chips U21-U28 on the left side of the second row, and chips U32-U39 on the right side of the second row.

For example, if the memory test on your computer tells you that bit 4 of byte 193455 is bad, that means that RAM chip U36 needs to be replaced (since it is an odd byte between 128-256K). If you have a bad RAM chip, call your Morrow Designs dealer with the above information.

5. SPECIAL APPLICATION NOTES

These notes will help you make changes to the operation of your MM256K board. You can change the base address and refresh cycle of the board simply by changing the jumper connectors. Other changes, which require you to cut traces on the board, are described in section 5.2.

5.1. Setting the Jumpers

Jumpers allow you to change some of the settings on your MM256K board. There are two sets of jumper pins on the MM256K board. These are the copper pins protruding above the board, some with black rectangular jumper connectors on them.

To connect two jumper pins, place the black jumper connector over the pins with the silver end up. Be sure that the pins fit into the black holes on the bottom of the connector. Slide the connector all the way down the jumper pins.

To disconnect two pins, simply remove the jumper connector. Save the jumper connector, since you may want to change the jumper setting later.

5.1.1. Base Address Jumper - J19

The MM256K board can be addressed at any 256K boundary of memory within the 16-megabyte address space. To change the base address of the board, change the jumper connections in J19 (located 2 inches from the left near the bottom of the MM256K board). There are six pairs of jumper pins, which represent the bits of the 256K segment address of the board. An address bit of 1 corresponds to an unconnected jumper, and an address bit of 0 corresponds to a connected jumper.

The top pair of pins represent the lowest order bit of the address, the next pair down represent the next bit, etc. With the default of all pairs connected, the 256K segment address is 000000. To indicate the board is used for the second bank of 256K (256-512K), the 256K segment address is 000001, and all pairs of pins are connected except the top pair.

The following illustrate the addressing scheme:

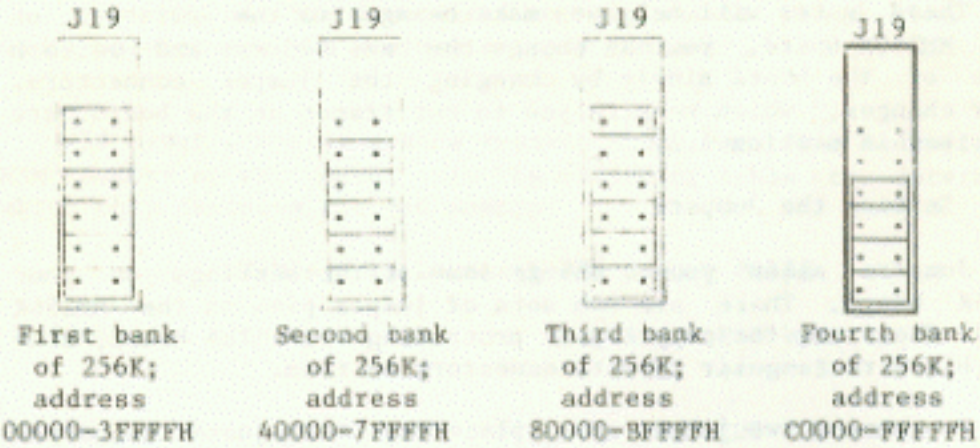


Fig. 5-1: Example Address Settings of J19

5.1.2. Refresh Cycle - J7

This set of jumper pins, located 2.5 inches from the top and 3 inches from the left side of the board, specifies whether to do a refresh after a read cycle or after an sM1 fetch (S-100 pin 44). The board comes set for refresh after read. Note that on some boards this jumper header is replaced with a wire soldered on the board.

To change the refresh cycle, change the jumper connections on J7. Connecting the top and middle pins sets the board for refresh after read; connecting the middle and bottom pins sets the board for refresh after sM1 fetch. For faster processors, such as the 8086 and 68000, set the board for refresh after sM1.

Refresh after read Refresh after sM1

Fig. 5-2: Settings of J7

5.2. Traces and Jumper Options

The following lists the artwork traces used on the MM256K board to set certain functions and features that may be required in certain custom applications. All of the jumpers described in this chapter are implemented in hardware by traces on either the front or back of the MM256K board, or by jumper wires soldered directly on the board.

Note: This list is for your information only. Any traces cut, or jumpers installed, by anyone other than Morrow Designs automatically voids the warranty of the board.

5.2.1. Row Refresh for 16K vs. 64K RAM Chips - J2

This trace, located 1.75 inches from the top and 4 inches from the right side of the board, specifies whether to access RAM as 256 rows by 256 columns. The default, with the trace connected, causes all 256 rows to be accessed. With the jumper removed, only 128 rows by 128 columns are available; this option is used with 16K RAM chips. The MM256K board works with standard 64K RAM chips made by Texas Instruments, Intel, NEC, Hitachi, and other manufacturers.

5.2.2. RAM Transposition - J8

This set of traces, located 3 inches from the top and 1.5 inches from the left side of the board, specifies the mapping between the 64K physical segments and the logical segments of memory. There are 24 pads in J8. The default configuration for J8 is:

Fig. 5-3: Default Configuration of J8

Each of the four physical 64K segments of chips can be used as any logical segment of memory. To do this, the following jumpers must be connected:

Table 5-1: Address Mapping with J8

Logical memory segment	Jumper pads connected	Chips addressed
Even bytes of 0-128K	1-2 *	U1-U8 *
	7-8	U13-U20
	13-14	U21-U28
	19-20	U32-U39
Odd bytes of 0-128K	4-5	U1-U8
	10-11 *	U13-U20 *
	16-17	U21-U28
	22-23	U32-U39
Even bytes of 128-256K	2-3	U1-U8
	8-9	U13-U20
	14-15 *	U21-U28 *
	20-21	U32-U39
Odd bytes of 128-256K	5-6	U1-U8
	11-12	U13-U20
	17-18	U21-U28
	23-24 *	U32-U39 *

The default configuration, shown by asterisks in the table, is that even bytes of 0-128K are chips U1-U8, odd bytes of 0-128K are chips U13-U20, even bytes of 128-256K are chips U21-U28, and odd bytes of 128K-256K are chips U32-U39.

For example, to use the MM256K board as a 128K memory board, and only access the U21-U28 and U32-U39 chips, you would disconnect all of the current jumpers, and connect pads 13-14 and 22-23.

5.2.3. Phantom Segments - J9 and J10

This set of traces, located 3 inches from the top and 2.25 inches from the left side of the board, determines which 64K segments will be inaccessible when the PHANTOM* line (S-100 pin 67) is low. The default is that all segments respond to PHANTOM*.

Systems which do not support PHANTOM* must drive S-100 pin 67 high to insure correct operation of the MM256K board.

Fig. 5-4: Default Configuration of J9 and J10

Table 5-2: Enable PHANTOM* with J9 and J10

Addresses	PHANTOM* enabled for bank	PHANTOM* disabled for bank
0K - 64K	J9 2-3	J9 1-2
64K - 128K	J10 2-3	J10 1-2
128K - 192K	J9 4-5	J9 5-6
192K - 256K	J10 4-5	J10 5-6

5.2.4. Delayed pSTVAL* - J13

This set of traces, located 3 inches from the top and 3.5 inches from the left side of the board, determines whether to take the signal from the pSTVAL* line (S-100 pin 25) or to use a built in delay from the rising edge of pSYNC (S-100 pin 76). This option would be used in systems which do not generate the pSTVAL* signal. The default (with pads 3-4 connected), is to use pSTVAL.

Fig. 5-5: Default Configuration of J13

5.2.5. Early sM1 Start - J16

This set of traces, located 3.25 inches from the top and 4 inches from the right side of the board, specifies whether to start a memory read cycle on sM1 (opcode fetch), or on sMEMR (memory read operation). The default, pads 2-3 connected, starts a memory cycle with sMEMR (S-100 pin 47).

The Morrow MPZ80 CPU does not put out an early sM1 status, and thus does not care which pads are connected on this jumper. Connect pads 1-2 if you are using another CPU board, and the board puts out an early sM1 status; this will decrease the instruction fetch access times on the MM256K board.

Fig. 5-6: Default Configuration of J16

5.2.6. Parity Error Notification - J17

This set of traces, located 3.75 inches from the top and 2.5 inches from the right side of the board, determines how to notify the host on the bus of a parity error. Since parity is not checked by the MM256K board, this jumper is not connected.

Connect pads 1-2 to pull VI4* line (S-100 pin 8) low on a parity error. Connect pads 3-4 to pull ERROR* line (S-100 pin 98) low on a parity error.

Fig. 5-7: Default Configuration of J17

5.2.7. 16K vs. 64K RAM Chips - J18

This set of traces, located 4 inches from the top and 1.75 inches from the left side of the board, specifies that the MM256K board uses 64K RAM chips.

Fig. 5-8: Default Configuration of J18

5.2.8. 8- or 16-Bit Data Path - J22

This set of traces, located 4.25 inches from the top and 4 inches from the left side of the board, determines whether the MM256K board responds to the sXTRQ* line (S-100 pin 58) to determine if the memory cycle is 8 or 16 bits. The default (pads 1-2 connected) causes the board to perform 8- or 16-bit operations according to the sXTRQ* line.

Systems which do not support the sXTRQ* line must drive S-100 pin 58 high to insure correct 8-bit operation of the MM256K board.

With pads 2-3 connected, the board always uses a 16-bit data path, regardless of sXTRQ*. With pads 1-2-3 all disconnected, the board always uses an 8-bit data path, regardless of sXTRQ*.

Fig. 5-9: Default Configuration of J22

5.2.9. RAM Refresh - J23

This set of traces, located 4.25 inches from the top and 4.5 inches from the left side of the board, determines whether the MM256K board uses pHLDA, sHLTA, and pWAIT signals for RAM refresh. The default, pads 1-2 and 4-5 connected, complies with the IEEE 696/S-100 standard, which is to generate a refresh during sHLTA.

To use the old S-100 pWAIT signal (S-100 pin 27), which was used before the IEEE standard, instead of the sHLTA line (S-100 pin 48) for memory refresh operations, pads 4-5 must be

disconnected and pads 5-6 must be connected.

The current IEEE/696 standard designates pin 27 (formerly pWAIT) as reserved for future use (RFU). This jumper option is only for backwards compatibility with pre-standard systems.

Fig. 5-10: Default Configuration of J23

6. THEORY OF OPERATION

The MM256K memory board follows the IEEE 696/S-100 standard for memory boards. The descriptions in this chapter give more information about how signals are handled on the board. You are encouraged to read the IEEE 696/S-100 standard for more information on the interaction between the board and the S-100 bus. This section assumes that the reader has chip-level experience with TTL-based systems.

6.1. Extended Addressing

S-100 address lines A18 through A23 select the MM256K board, A0 and A17 select the 64K bank on the board (A0 is the low bit, A17 is the high bit), and A1 through A16 select the memory location on the board.

The following table illustrates the address lines and corresponding pins used in memory addressing:

Table 6-1: S-100 Pins for Addressing Memory

Line	Pin	Line	Pin	Line	Pin	Line	Pin
A0	79	A6	82	A12	33	A18	15
A1	80	A7	83	A13	85	A19	59
A2	81	A8	84	A14	86	A20	61
A3	31	A9	34	A15	32	A21	62
A4	30	A10	37	A16	16	A22	63
A5	29	A11	87	A17	17	A23	64

The address of the board may be modified by J19, and the logical order of the four banks of memory may be modified by J8. When the board address matches the current bus address, the MM256K signal -ADDR MTCH (U68-19) goes low.

6.2. Using PHANTOM*

When the PHANTOM* line (S-100 pin 67) is low, all blocks of memory are deselected, and cannot be read or written to. This is used for master CPU's or memory mapped devices which have ROM addressed at overlapping addresses with the MM256K board.

The use of PHANTOM* may be modified by J9 and J10. The default of the MM256K is to deselect all four banks on a PHANTOM* signal.

6.3. Data Modes

The MM256K can transfer 8- or 16-bit data. The data path is determined by J22, which can force 8-bit or 16-bit operations exclusively, or allow sXTRQ* (S-100 pin 58) to determine the path size. The default is to use the sXTRQ* line.

If the sXTRQ* line is being used, the size of the data path is specified by the MM256K signals +WORD or +BYTE just before the falling edge of pSYNC (S-100 pin 76).

8-bit operations can be mixed using the sXTRQ* line. During a 16-bit read operation, data written with an 8-bit write with A0 set low will appear in the lower byte.

6.3.1. 8-Bit Data

Following the IEEE 696/S-100 standard, the MM256K board reads the A0 address line to determine which byte of the data word is used in read and write functions. Internally, the MM256K board always operates with 16-bit words. Thus, the RAM is organized as 2 rows of 16 chips, each chip corresponding to a data bit. For read operations, +BYTE is used with address bit A0 to determine which 8 bits are to be gated onto the DI bus.

6.3.2. 16-Bit Data

The IEEE 696/S-100 standard describes how 16-bit transfers are bi-directional, using both bytes in the path for data, and multiplexing the DI and DO buses into the DI/O bus.

6.3.3. Gating the Data

The registers listed below are set based on the type of operation (read or write) and the data path (8- or 16-bit).

Table 6-2: Gating Signals

Transfer Type	Data Lines Used	+RD	-GDI0	-GDI1	-GDI2	-GDO0	-GDO1	-LDI	-SEL LOW
16 bit read	DATA0-DATA15	H	H	H	H	L	L	L	H
16 bit write	DATA0-DATA15	L	L	H	L	H	H	H	X
8 bit read low byte	DATA8-DATA15	H	H	H	H	L	H	L	L
8 bit read high byte	DATA8-DATA15	H	H	H	H	L	H	L	H
8bit write low byte	DATA0-DATA7	L	L	H	H	H	H	H	X
8bit write high byte	DATA0-DATA7	L	L	L	H	H	H	H	X

H=high L=low X=undefined

6.4. Memory Operations

When the card address matches the S-100 bus address on lines A18 through A23, the MM256K signal -BD SELECT (U56-6) is set low. This is the only time that a read or write can take place.

Read and write operations are arbitrated during refresh cycles, since the MM256K signal +WAIT REQ (U42) sets the RDY line (S-100 pin 72) low during refresh. Normally, only one wait state is needed to complete the refresh cycle in progress. After the refresh completes, the pending read or write operation begins.

6.4.1. Read Cycle

The READ register (U58-9) is set when sMEMR (S-100 pin 47) is active (high) and the CPU is not halted; it is set on the negative edge of pSTVAL* (S-100 pin 25) during pSYNC (S-100 pin 76).

If a refresh is in progress, it is completed, and -RASI (U47-8) control signal is sent to the 2964B memory controller (U11-3). The timing chain is also begun. -RAS0 or -RAS1 is driven to the row of RAM selected by line A17 (S-100 pin 17). The timing chain generates signals to enable the column addresses and generate -CAS0 or -CAS1.

The data is sent to the bus when it is valid, and is latched just before -CAS0 or -CAS1 becomes inactive. Data is held on the bus until pDBIN (S-100 pin 78) goes low (inactive).

6.4.2. Write Cycle

The WRITE register (U58-5) is set when sWO* (S-100 pin 97) is low, the CPU is not halted, and sOUT (S-100 pin 45) is not active (low); it is set on the leading edge of pWR* (S-100 pin 77).

The timing chain begins, the -RASI control signal generates WE0 and WE1 signals, and the appropriate lines on the bus are read when -CAS0 or -CAS1 is active.

6.4.3. Refresh Cycle

Row refresh operations occur approximately every 14 microseconds. On the MM256K board, a refresh is done after each read cycle (this may be modified by J7). The timer for refresh is clocked by the trailing edge of pSYNC (S-100 pin 76). The MM256K board performs RAS-only refresh cycles.

Read and write operations cannot be performed during refresh cycles, since +WAIT REQ (U42) sets the RDY line (S-100 pin 72) low during refresh. Normally, only one wait state is needed for refreshing. You can minimize the number of wait states by matching the speed of the board's delay line (U45) to the speed of the CPU and the dynamic RAM chips.

The MM256K board will refresh even if the CPU on the bus is halted. The board monitors sHLTA or pWAIT (depending on the setting of J23), as well as RESET*, POC*, and pRDY (S-100 pins 48, 27, 72, 75, and 99), and if a refresh is needed, it is activated by -RFSH (U42-2).

Under normal conditions, the timing cycle starts and the refresh addresses are enabled. Each of the 256 row addresses is refreshed sequentially by the dynamic RAM controller chip, which may be modified by J2. After a short delay, -RASI is generated and sent to the memory.

-RASI will stay active for slightly more than 200 nanoseconds, which is the minimum required pulse width. +RFSH (U62-11) is held longer (about 360 nanoseconds) so that the RAMs can precharge between the refresh RAS and the RAS of the next read cycle.

A. TECHNICAL SPECIFICATIONS

Power Requirements:

- Input voltage
  - 8.0V unregulated, 7.0V minimum
  - 25V maximum instantaneous
- Input current
  - .98A typical, 1.12A max

Memory:

- 256K x 8, or 128K x 16
- Extended addressing on 256K boundaries
- Access time from pSTVAL*
  - 150 nanoseconds typical
  - 225 nanoseconds maximum
- Read cycle time
  - 550 nanoseconds minimum with refresh
  - 350 nanoseconds minimum read cycle
- Write cycle time
  - 350 nanoseconds minimum

S-100 interface:

- Input loading:
  - All input signals are received by buffer devices, and are loaded by not more than one LS TTL input load each (.4 mA maximum load at .4 V), except sXTRQ*, which is loaded by .4 mA typical (.6 mA maximum).
- Output drive:
  - All three-state outputs are driven by bus drivers equivalent to 74LS373 buffer drivers. All open collector outputs are driven by 7438 or 74S38 TTL devices (with 10K ohm pull-up resistor to +5VDC for RDY and ERROR*).

The MM256K board fully complies with IEEE 696/S-100 standard. It is guaranteed to run with master CPU's up to 6 MHz. A board with parity option will also be available.