

Test: CLAT-1

Course Code & Title: 18ECC303J& COMPUTER COMMUNICATION NETWORK

Year & Sem: III & VI

Date: 20.02.2023

Time: 12:30 to 1:30 PM

Max. Marks: 25

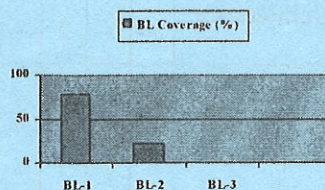
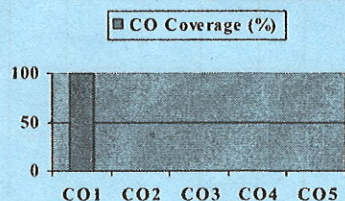
Course Articulation Matrix:

CO	18ECC303J - Computer Communication Networks Course Outcomes (COs)	Program Outcomes (POs)														
		Graduate Attributes												PSO		
		1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
1	Express the basic services and concepts related to internetworking.	-	-	-	-	-	-	3	-	-	-	-	2	-	-	-
2	Define the basic OSI model architecture and its lower layer functions.	-	-	2	-	-	-	1	-	-	-	-	-	-	-	3
3	Apply the various Network Layer concepts, mechanisms and protocols.	-	-	3	-	-	1	2	-	-	-	-	-	-	-	-
4	Analyze the services and techniques of Transport Layer.	-	-	-	-	-	-	2	-	-	-	-	-	-	-	3
5	Produce the various services and protocols in Application Layer.	-	-	2	-	-	-	-	-	-	-	-	-	-	-	3
6	Evaluate the various Networking concepts and Routing protocols.	-	-	-	-	1	-	-	-	-	-	-	2	-	-	3

Q. No	PART – A (5 X 1 = 5 Marks) Answer all the questions	Mark	BL	CO	PO
1	The maximum payload length in IEEE 802.3 frame is _____ Bytes. a. 45 b. 3200 <input checked="" type="checkbox"/> c. 1500 d. 8190	1	1	1	7
2	Number of full duplex links required in ring topology to connect 'N' nodes is a. N <input checked="" type="checkbox"/> b. N-1 c. 2N d. N/2	1	2	1	7
3	_____ layer provides process to process delivery. a. Physical b. Data link c. Network <input checked="" type="checkbox"/> d. Transport	1	1	1	7
4	Main difference between synchronous and asynchronous transmission a. Band width required is different b. Pulse height is different <input checked="" type="checkbox"/> c. Clocking is derived from the data in synchronous transmission d. Clocking is mixed with data in asynchronous transmission	1	1	1	7
5	A _____ is a set of rules that governs the communication. a. Standard <input checked="" type="checkbox"/> b. Protocol c. Server d. RFCs	1	1	1	7

PART -B (2 X 4 = 8 Marks)					
Answer Any two questions					
6	Compare Datagram packet switching and Virtual circuit switching networks. <i>(Any 2 pls)</i>	4	2	1	7
7	Explain the function of Data link layer and Network layer in OSI model.	4	1	1	7
8	Discuss the 10 Base 5 implementation of Ethernet with a neat diagram.	4	2	1	7
PART - C (1 X 12 =12 Marks)					
Answer Either or Question					
9	i. With a neat timing diagram, explain the delay caused in the three phases of Circuit switching. ii. Draw the frame format of FDDI, name the fields in it.	8	1	1	7
10	i. Discuss the star, ring network topologies with their advantages and disadvantages ii. Compare LAN and MAN	4			
		8	1	1	7
		4			

Course Outcome (CO) and Bloom's level (BL) Coverage in Questions



Name of the Student:

Approved by the Course Coordinator
Register No.:

Part- A (5 x 1= 5 Marks)					
Q. No	CO	PO	Maximum Marks	Marks Obtained	Total
1	CO1	7	1		
2	CO1	7	1		
3	CO1	7	1		
4	CO1	7	1		
5	CO1	7	1		
Part- B (2 x 4= 8 Marks)					
6	CO1	7	4		
7	CO1	7	4		
8	CO1	7	4		
Part – C (1 X 12 = 12 marks)					
9	CO1	7	12		
10	CO1	7	12		

CO	Maximum	Marks
1	41	
Total	41	

PO	Maximum	Marks
7	41	
Total	41	

Signature of the Question paper setter

Academic Advisor