Let's consider the probabilities $P(1/0)$ and $P(0/1)$, assuming that no photons have been received with bit 0 and one photon has been received with bit 1. The probability of identifying a bit as 1 when bit 0 arrives as $P(1/0)$ is zero because no photons have been received in this case. The probability of identifying a bit as 0 when bit 1 arrives is equal to $P(0) = \exp(-N_p)$ because $n = 0$. Refer again to the definition of BER given in Formula 11.48. In this case, BER is given by [1]

$$\text{BER} = 0.5[P(1/0) + P(0/1)] = 0.5\exp(-N_p) \tag{11.68}$$

So, a plain exponent represents the dependence of BER on the absolute minimal number of photons necessary to detect a bit. Since this relationship determines the absolute minimum of N_p, it is called the *quantum limit*. If one photon is received, BER is 0.18 (which means that 18 out of 100 bits received are interpreted incorrectly); if $N_p = 10$, BER is 2.27×10^{-5}. You can continue to calculate these numbers. For $N_p = 20$, BER $= 1.03 \times 10^{-9}$. Remember, BER $= 10^{-9}$ is considered the minimum acceptable bit-error rate in modern fiber-optic communications systems. The quantum limit for BER $= 10^{-12}$ is $N_p = 26$. (You may, in your work, come across quantum limit calculated in terms of average number of photons per bit (N_p^*), which is equal to $N_p/2$. So don't be confused if you see $N_p^* = 10$ for BER $= 10^{-9}$.)

Wrestling with quantum limit may seem to you to be an academic exercise, but it is not. In calculating the power budget of a fiber-optic communications system, the designer usually has to know how far (or how close) his or her system is from its quantum limit. This is another measure of system quality. For more information on this concept, see reference [9] at the end of this chapter.

11.4 RECEIVER UNITS

A receiver is a unit that converts an optical input signal into an appropriately formatted electric output signal. Since we are concentrating here on digital transmission, we can say that a receiver converts a stream of light pulses into a stream of electric pulses capable of driving the electronics that follow in the system. (See the general diagram of a fiber-optic communications system in Figure 1.4.)

As we have already seen with transmitters, the light source—either an LED or a laser diode—is the heart of these devices, but the properties of a transmitter depend also on the characteristics of its electronics and its packaging. The same holds true for receivers. Photodiodes determine the major features of the devices but even an ideal PD cannot make an ideal receiver. We need good electronics, packaging, and design in order to make a good device. In other words, a high-quality photodiode is the only condition necessary to attain a high-quality receiver. The output signal emanates from the entire receiver, not just from its photodiode. At this point, aware of how a photodiode works and fully cognizant of its characteristics, we will discuss the receiver unit in detail.

It is suggested that you reread Section 10.4, "Transmitters," because both units—transmitter and receiver—have much in common in terms of design approach, operation with a signal, and practical application. What's more, such matters as packaging, printed circuit board layout, reliability, testing, and troubleshooting are almost identical and so they will not be repeated in this section.

Functional Block Diagram and Typical Circuits of a Receiver

Block diagram Many types of receivers are used in modern fiber-optic communications systems. They differ in their architecture and in the components they use; however, most of them have very much in common functionally. A typical functional block diagram of a receiver is shown in Figure 11.16.

To refresh your memory as to what a receiver looks like, refer again to Figure 1.7, where two types of receiver units—DIP and butterfly—are shown. To see what a receiver board popu-

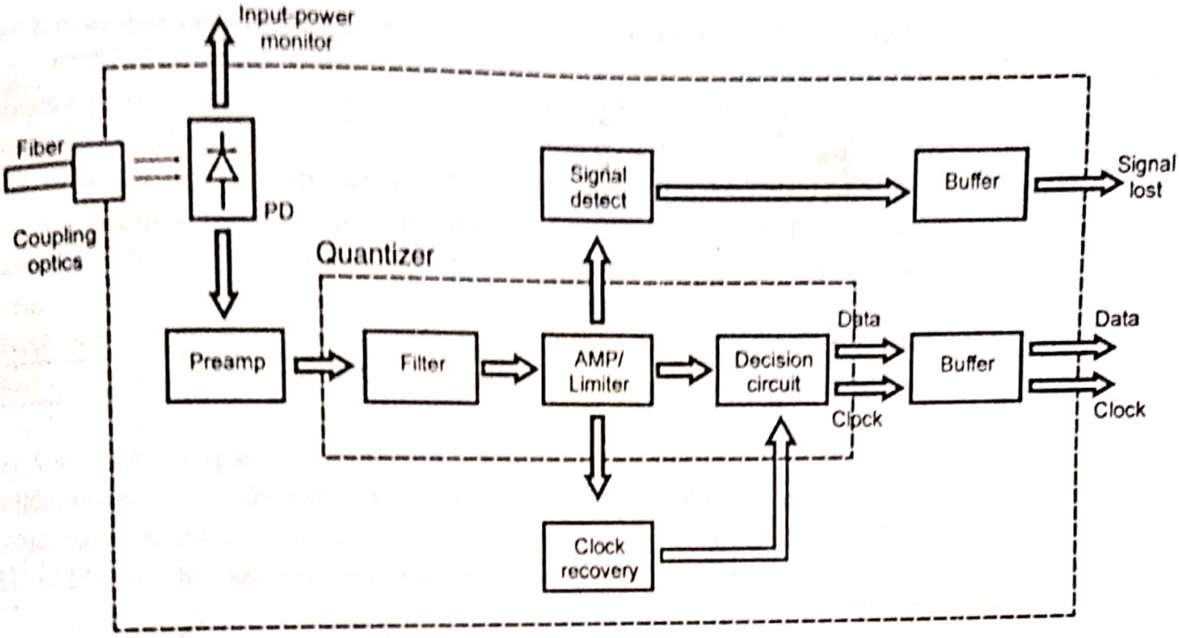

Figure 11.16 Functional block diagram of a receiver. *(Adapted with permission from Opto Electronic Products by Ericsson Microelectronics AB, Stockholm, Sweden.)*

lated with IC chips and discrete components looks like, see Figure 10.40. (Even though Figure 10.40 exhibits a transmitter assembly, the physical appearance of both units is very similar.)

Light from an optical fiber passes through coupling optics and falls on the sensitive area of a photodiode. (A detailed discussion of coupling optics is presented in Chapter 9; additional discussion can be found in Section 11.2.) A photodiode (PD) converts light into photocurrent. This photocurrent is converted into voltage and amplified by a preamplifier, denoted as "Preamp" in Figure 11.16. The output voltage from the preamplifier enters a block (usually called a "quantizer") whose output is data and clock signals in an appropriate format. (This block will be discussed shortly.) The data and clock signals then enter a buffer, which converts them into ECL-compatible signals capable of driving the succeeding digital circuitry. Thus, the input of a receiver is an optical signal and the output is the electric voltage in a specific format with specific electrical characteristics. Now let's look at the components of a receiver in detail.

Optical front end A photodiode along with the preamplifier linked to it is called the receiver's *optical front end.* The function of this section is to convert light into electric voltage of the required amplitude. This is done in two steps: First, the photodiode converts light into photocurrent; secondly, the preamplifier converts the photocurrent into voltage, amplifies the signal, and presents it to a quantizer. A receiver's photodiode can be chosen from a variety of commercially available devices. The critical concern in the design of an optical front end is choosing the right electronic amplifier.

You will recall that the load resistance (R_L) of a photodiode plays a very important role in both noise and bandwidth considerations. On the one hand, thermal noise, which is the dominant component of noise current in *p-i-n* PDs, is inversely dependent on the load resistance. This is why load resistance appears in all the major formulas determining SNR and BER as a function of the sensitivity of a photodiode. (See Formulas 11.30, 11.38, and 11.65.)

It is important to underscore one more effect of R_L. As with thermal noise, a photodiode's sensitivity is also inversely dependent on load resistance. (See Formula 11.64.) Hence, to decrease thermal noise (and increase the photodiode's sensitivity), we need to increase the load resistance. Nothing could work better in achieving this goal than connecting a photodiode directly to an amplifier because the input impedance of an electronic amplifier is very high (usually on the order of units of MΩ). This connection is known as *high-impedance design* and its equivalent circuit is shown in Figure 11.17(a).

On the other hand, the bandwidth of a photodiode is inversely proportional to load resistance, as Formula 11.13 shows. (In that formula we considered a PD's junction resistance [R_{in}] as the load resistance.) Thus, to increase the bandwidth of a receiver, we need to decrease the load resistance. The upshot: *There is a trade-off between bandwidth and noise (sensitivity) of a receiver* and the right design is determined by the load resistance of the photodiode.

Keep in mind that a preamp must not only amplify the signal but also convert current into voltage. The latter function is performed by an amplifier with negative feedback. Thus, another connection between a PD and a preamp—a so-called *transimpedance design*—is used in optical front ends. This design is shown in Figure 11.17(b).

Input impedance of an electronic amplifier with negative feedback is called *transimpedance* (R_t); this is the actual load resistance for a photodiode. Transimpedance is the function of the amplifier's gain (A) and feedback resistor (R_F). A designer can vary these two parameters to obtain the desired value of R_L, which is usually on the order of tens of kΩ. The output voltage of this preamp is given by

$$V_{out} = I_p R_t, \tag{11.69}$$

where I_p is the photocurrent produced by the photodiode, and $R_t = R_L$, again, is the transimpedance of the preamp with negative feedback.

The transimpedance design is the most common type you will meet in the field. In nearly every commercial receiver's data sheet, you will find the term *transimpedance amplifier*, which means an amplifier with negative feedback.

A photodiode is usually integrated with a transimpedance amplifier in a component called a *PINAMP*. When a preamp is linked to field-effect-transistor (FET) circuitry, the front-end unit is called a *PINFET*. Typical characteristics of such an optical front end can be found in [14].

But even the transimpedance design itself cannot satisfy a variety of requirements that receivers must meet in today's applications. One important new characteristic of a receiver that is critical in fiber-optic-network applications is the *dynamic range* which *is the difference between the highest and the lowest input signals at which a preamp can operate*. The dynamic range of a receiver is measured in dB and its typical values vary from 35 to 45 dB.

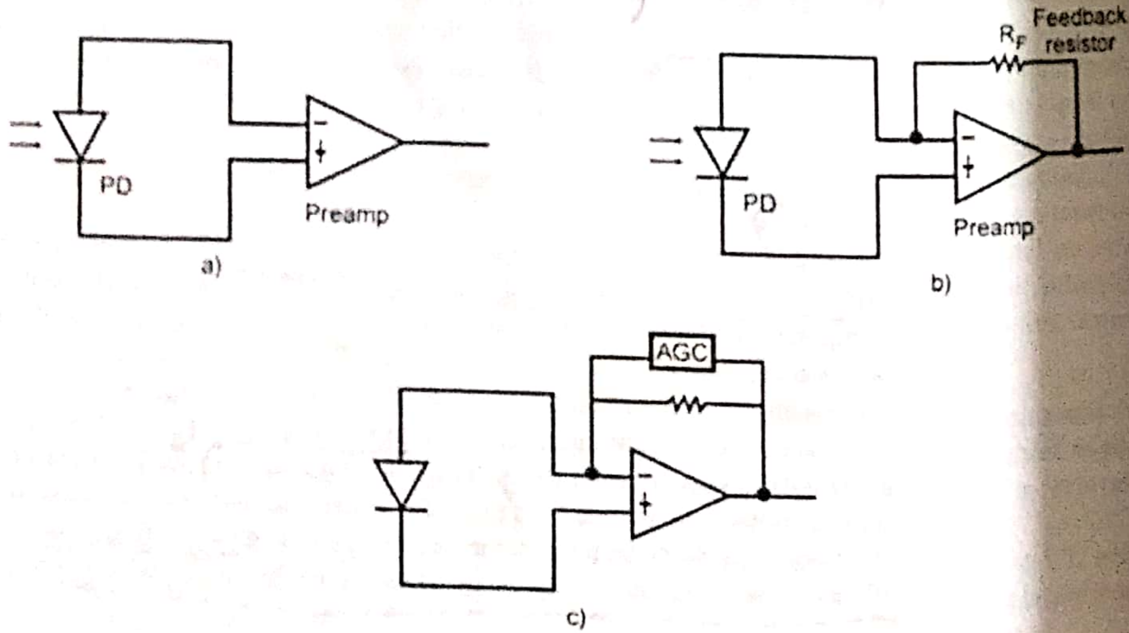

Figure 11.17 Equivalent circuits of an optical front end: (a) High-impedance design; (b) transimpedance design; (c) transimpedance design with automatic gain control (AGC).

In fiber-optic networks, the input signal can fluctuate widely. A transimpedance amplifier has a much wider dynamic range than a high-impedance one. This is because a preamp's output voltage is proportional to its input impedance, as Formula 11.69 states, and this value for a transimpedance design is much smaller than for a high-impedance design. But this is still not enough. To further increase the dynamic range of a transimpedance preamp, manufacturers include *automatic-gain-control (AGC)* circuitry in the feedback loop, as Figure 11.17(c) shows. This circuitry, as the name implies, controls the amplifier gain to keep the output voltage stable; this means the transimpedance (R_Z) is also varied, so that it is high at a low-input signal and it is low at a high-input signal. This is how a preamp can handle an input signal in a wide dynamic range.

To conclude, an optical front end is the first stage of a receiver. It accepts an optical signal and presents amplified voltage to the next block—the quantizer.

Quantizer A quantizer typically includes three components: a noise filter, a power amplifier/limiter, and a decision circuit.

The *noise filter* improves the signal-to-noise ratio or, ultimately, the receiver's sensitivity, as was mentioned in Section 11.3. The design consideration for a noise filter centers on the bandwidth requirements. For example, in designing an optical front end, a manufacturer wants to achieve maximum bandwidth to, obviously, increase the sales potential of the device. But this has a negative side for the user. Specific applications probably don't need all the bandwidth available. We have already pointed out, remember, that noise is directly dependent on bandwidth so that excess bandwidth contributes to additional noise. This, in turn, reduces a receiver's sensitivity.

Consider this situation: Assume your network operates at BR = 155.520 Mbit/s, which is an OC-3 signal in the SONET standard. When converting the bandwidth (BW) and bit rate (BR) for a receiver, the rule of thumb is this: BW ~ 0.7BR. Hence, the required bandwidth is equal to approximately 109 MHz. You have on hand an MF-432 PIN photodiode, whose data sheet was discussed in Section 11.2. This PD has a bandwidth of 2.5 GHz. Thus, for our network, whose BR = 155.52 Mbit/s, we can use a low-pass noise filter to restrict the bandwidth of the receiver to 109 MHz. By restricting bandwidth, a noise filter also reduces *intersymbol interference (ISI).*

You can purchase a receiver for a specific application with a pre-installed filter or you might customize the filter. In the latter case, the manufacturer usually provides you with a circuit, a table of suggested values of capacitors, and an inductance to build an L-C noise filter according to your application. Needless to say, a noise filter is an optional component and some receivers, to keep their cost down, don't contain it.

An *amplifier/limiter* provides power amplification of a signal obtained from a preamp through the noise filter. Amplification is necessary to attain a signal with enough power to drive the decision circuit. (Remember, the preamp is the voltage amplifier.) If the amplified signal is high enough, this circuit clips the signal—thus the name "limiter." In other words, the gain of this amplifier is a function of the amplitude of the input signal: the larger the amplitude, the less the gain. This power amplifier can also include automatic gain control—the circuit we discussed above. This unit might also include an *equalizer* with a specific gain-versus-frequency characteristic to correct any bandwidth-caused signal distortion.

The *decision circuit* is the unit that determines the logical meaning of the received signal. Typically, this is a comparator driven by the input signal. The basic circuit is shown in Figure 11.18(a). When the received signal is above threshold, the comparator's output is high. This means the decision is made that this signal carries logic HIGH, or 1. When the signal is lower than threshold, the comparator's output is low. This means the decision is made that the received signal carries logic LOW, or 0. (See Figure 11.18[b].)

An electric signal representing a bit varies over even a single-bit time interval, as Figure 11.13 shows. The question is, when do you want to take a sample of data (v_{ins}) to compare with threshold voltage (v_{th})? Obviously, it is better to take such samples in the middle of each bit, where the probability of having the best sample is the highest. (See Figure 11.18[c].) Thus, the

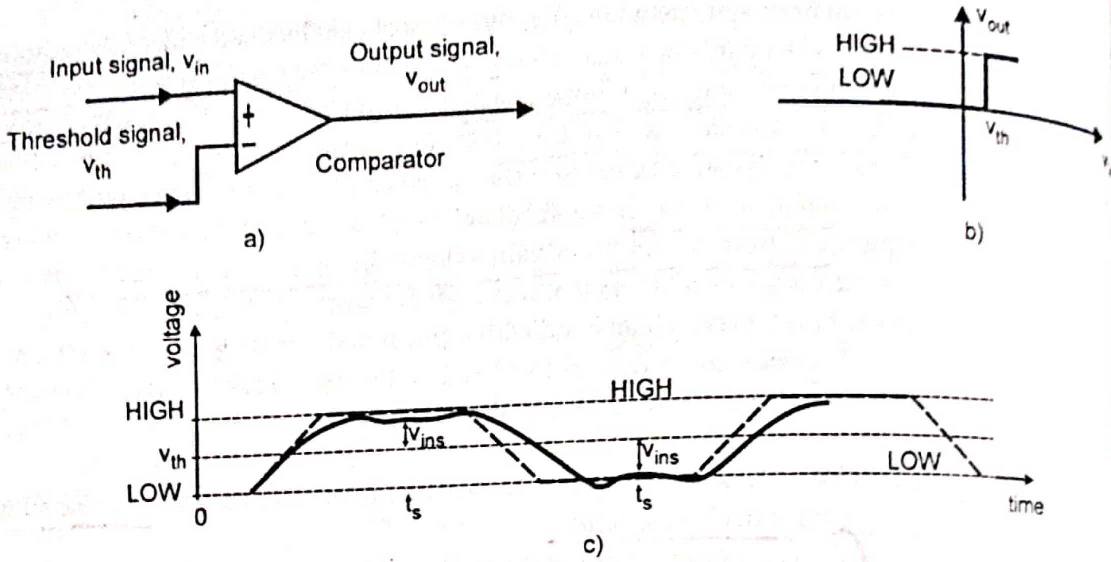

Figure 11.18 Principle of operation of a decision circuit: (a) Basic circuit; (b) comparator output; (c) decision-making process.

need for precise timing of the signal arises. If your circuit makes a mistake in determining this midpoint of bit time (t_s), the probability of error increases. Incidentally, an eye diagram helps in finding the best position for t_s; this is where an eye diagram is opened to its maximum.

We need to emphasize that a comparator works with voltages, although, in our theoretical considerations, we did indeed describe decision-making techniques in terms of currents. (See Formulas 11.52, 11.53, and 11.65.) This is because in Section 11.3 we dealt with a photodiode itself but, in this section, we are considering the entire receiver unit. To convert photocurrent (I_p) into voltage, we need to multiply I_p by some impedance (Z_{cas}) representing a cascade of transformations that photocurrent experiences before entering a comparator. In short, we need to consider the transformation of an optical input signal into voltage entering a comparator (v_{inc}) through the convolution integral. This would lead to our obtaining a transform function of the circuit performing this transform, including all noise sources. Such an approach is proposed in reference [9]. Instead of developing this theory, we will simply rely on a practical engineering approach: Measured voltage (v_{inc}) includes all the transformations from an optical signal to the input of a comparator.

The critical problem in designing a decision-making circuit is what signal should be used as the threshold (reference). Since this design is so crucial in the consideration of a receiver, we have set aside a separate subsection (pages 484–489) to discuss it.

Buffers A *buffer* transfers a logic signal from the input to the output unchanged but reshapes the electrical form of this signal. Typically, this is an emitter-follower circuit. In this case, a buffer provides output in ECL-compatible format. (For more on buffers, see Section 10.4.) A receiver can contain several buffers, as Figure 11.16 illustrates.

Clock recovery *Clock recovery* extracts timing information from the data stream and helps the decision circuit to generate clean and reshaped differential DATA and NON-DATA outputs.

You may ask why we need this circuit. As you know, synchronous digital circuits work under control of a clock signal. This timing signal must be the same at the transmitter and receiver ends to synchronize all operations. In our case, for example, we need to take a sample of data entering a comparator (v_{ins}) and compare it with the threshold voltage (v_{ins}) exactly in the middle of a bit, as Figure 11.18(c) shows. But bit timing is determined by the transmitter clock. If the receiver clock has a different time, we'll experience a data-sampling error. This error will lead to an error in determining the meaning of the received signal's logic; in other words, it will increase the bit-error rate.

The clock signal is produced by a frequency generator. Since the frequency stability of such a generator is finite (even though it is on the order of 10^{-6} and higher for practical miniature circuits), two generators will inevitably have a significant clock discrepancy over their operating time. Let's consider a popular crystal (quartz) generator [15]: Its typical stability is about 25 parts per million. This means that at 20 MHz the oscillator's frequency can vary up to ± 25 Hz. Therefore, two such generators, one in the transmitter and the other in the receiver, can have a frequency difference up to 50 Hz, producing an unacceptable BER.

The only way to ensure the same time frame along a transmission path is to have the data itself carry a timing signal. This is done by using specific line codes, a topic discussed in Chapter 8. For now, we only need to understand that the typical non-return-to-zero (NRZ) code shown in Figure 11.18 does not carry timing information in explicit form. Therefore, a special measure has to be taken to extract a clock signal from the data. This is accomplished by a clock-recovery circuit.

The principle of operation of this circuit can be seen in Figure 11.19. A *voltage-controlled oscillator (VCO)* generates approximately the same frequency as a transmitter generator. A phase of received data is compared with the phase of a signal generated by the VCO and their difference is converted by a low-pass filter into a dc signal. This signal makes the VCO change its frequency in order to eliminate any discrepancy between received and generated frequencies. (Frequency, as pointed out previously, is the derivative of a phase.) The corrected frequency signal—the clock signal in Figure 11.19—controls the operation of the decision circuit.

If you have some background in electronics, you may at this point say, "Wait a minute. In a sense, Figure 11.19 shows a typical *phase-locked-loop (PLL) circuit*, does it not?" Yes, indeed. This is a typical phase-locked loop and many receivers' data sheets refer to the clock-recovery circuit as simply a PLL circuit. The key feature of this digital circuit is that it compares the edge transitions of the data and the VCO pulses, which we referred to as the "phase comparison." Not all receivers contain clock-recovery circuits. These circuits are also available as stand-alone units [16].

Signal detect *Signal detect* is essentially an alarm circuit. It monitors the level of the incoming signal and generates a logic LOW signal when the signal-to-noise ratio is not sufficient. The output of this circuit is a logical flag, which indicates when the level of the input signal drops below the acceptable (threshold) level. Suppose the input signal hovers around the threshold level. In this case, the flag signal will toggle between HIGH and LOW, making you nervous because you don't know whether you should take some kind of action or just wait until the alarm becomes steady. To prevent this situation, a signal-detect circuit generates an alarm signal only when the increasing input signal rises a certain level above the threshold. When the input signal decreases, the detect circuit waits until the signal drops below threshold to a certain predetermined level. In other words, the signal-detect circuit works with hysteresis, which is usually on the order of 1.5 dB.

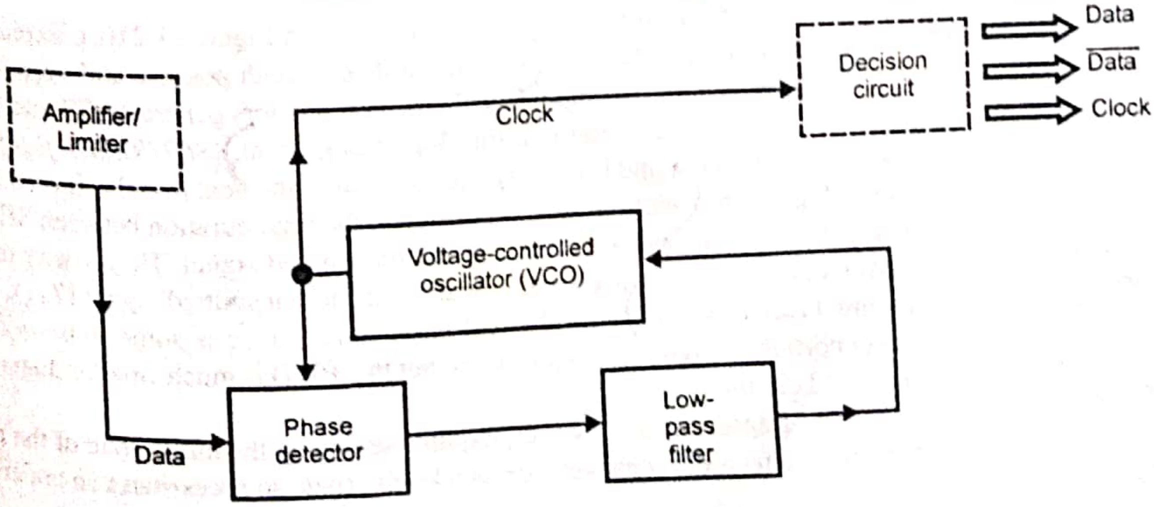

Figure 11.19 Typical clock-recovery circuit.

Monitoring circuits Look again at Figure 11.16. Notice the two monitoring circuits in the typical receiver. The first, monitoring the voltage drop produced by photocurrent flowing through a resistor, allows the engineer to keep tabs on input power. The second, a flag signal from a signal-detect circuit, watches for a possible signal-lost situation.