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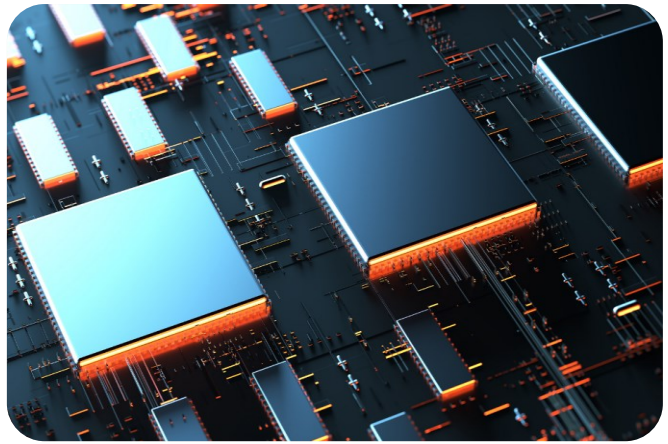
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
MKCE

MULTI FAULT MULTI-LAYER DIAGNOSIS FOR FAULT-TOLERANT NETWORKS-ON-CHIP



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INTRODUCTION

- The continuous evolution of new application has become the reason of the invention of some new processor, memory and accelerator cores.
- Moreover, the fast development and improvement of computation and the complexity of communication have caused the invention of the scalability-centered paradigms.

PROBLEM STATEMENT

- Recently, NOC reliability research has made significant strides and has developed a suite of canonical approaches to improve failure resistance including the use of redundant components and logic for self-repair at the circuit layer, redundant wires and error correction codes at the data layer, and reconfiguration and fault-tolerant routing algorithms at the network layer.

OBJECTIVE

- In order to tolerate faults that emerge in operating Networks-on-Chip, diagnosis techniques are employed for fault detection and localization.
- On various network layers, diverse diagnosis methods can be employed which differ in terms of their impact on network performance (e.g., by operating concurrently versus pre-empting regular network operation) and the quality of diagnostic results.

EXISTING SYSTEM

- As the complexity of designs increases and technology scales down into the deep-submicron domain, the probability of malfunctions and failures in the networks-on-chip (NOCs) components increases.
- Networks-on-Chip constitute the interconnection architecture of future, massively parallel multiprocessors that assemble hundreds to thousands of processing cores on a single chip.

PROPOSED SYSTEM

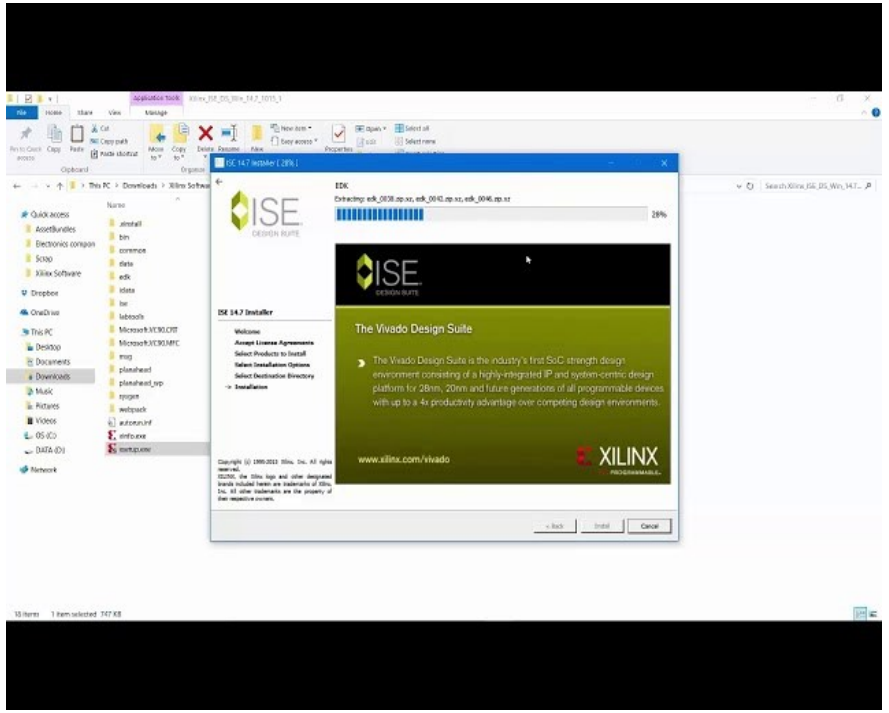
- Networks-on-chip are inherently fault tolerant or at least gracefully degradable as both, connectivity and amount of resources, provide some useful redundancy.
- These properties can only be exploited extensively if test and diagnosis techniques support fault detection and error containment in an optimized way.

COMPARISION

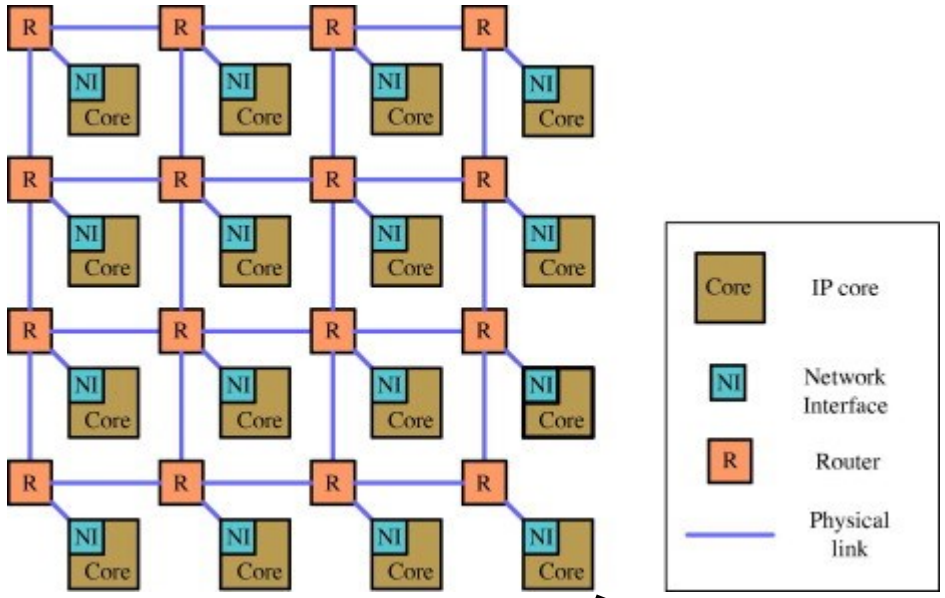
S.No	Paper	Methodology	Merits/demerits
1	Fault-tolerant networks-on-chip routing with coarse and fine-grained look-ahead	novel adaptive routing algorithms, namely coarse and fine-grained (FG) look-ahead algorithms	higher throughput and scalability
2	A unified test and fault-tolerant multicast solution for network-on-chip designs	fault-free routers/links	Performance degradation
3	Simple fault-tolerant method to balance load in network-on-chip	Multi Router Fault tolerant (LBMF) routing method	Low Power
4	Reliability assessment of fault tolerant routing algorithms in networks-on-chip: An analytic approach	Efficient fault adaptive routing algorithms	Energy efficient System
5	Fault Tolerant Deadlock-Free Adaptive Routing Algorithms for Hexagonal Networks-on-Chip	hexagonal on-chip network topology	Proposed method in reducing test time.

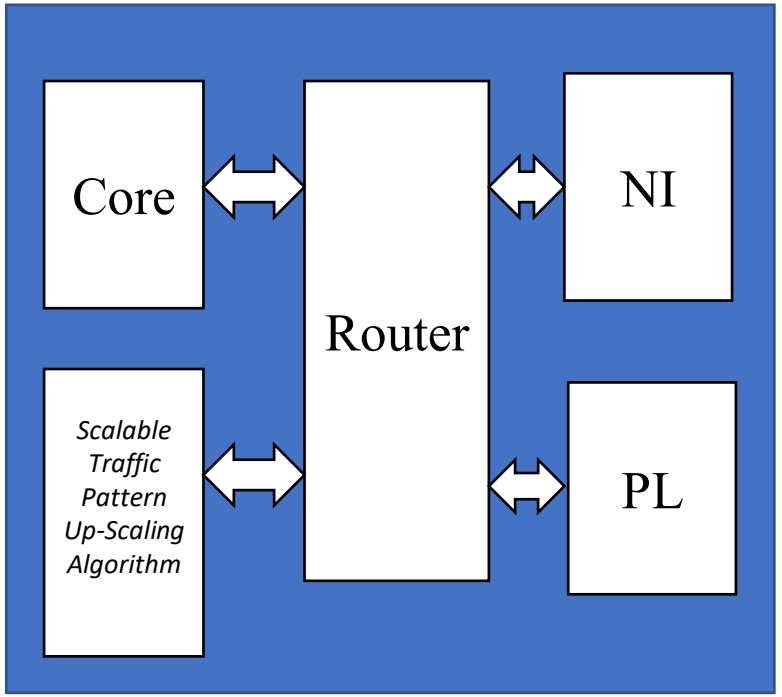
TOOL USED

- Xilix 14.7

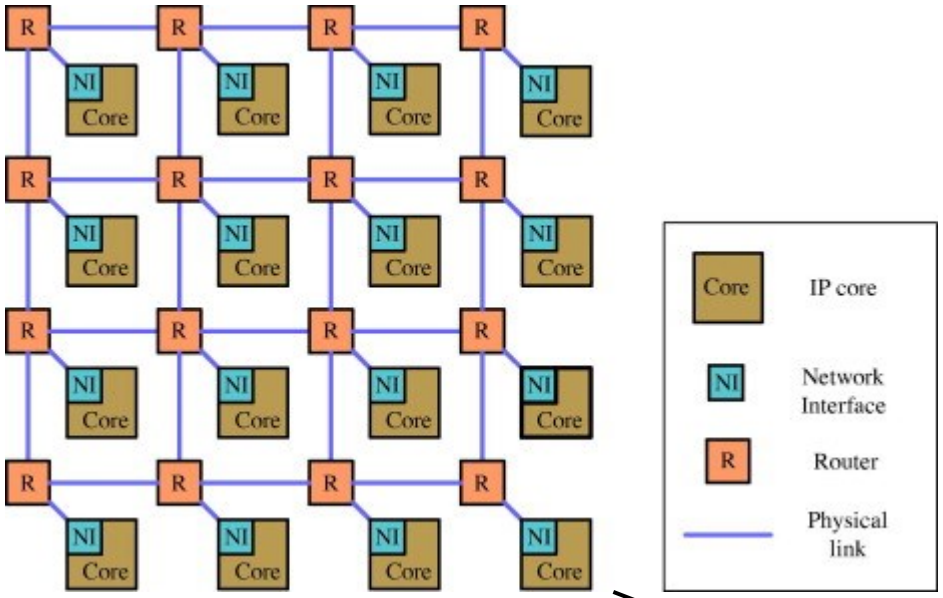


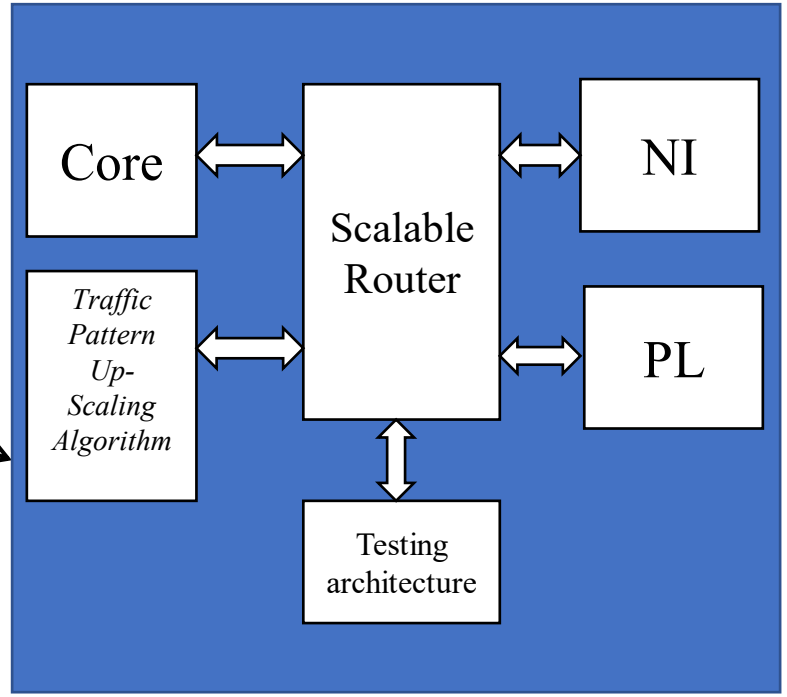
BASE BLOCK DIAGRAM





PROPOSED BLOCK DIAGRAM



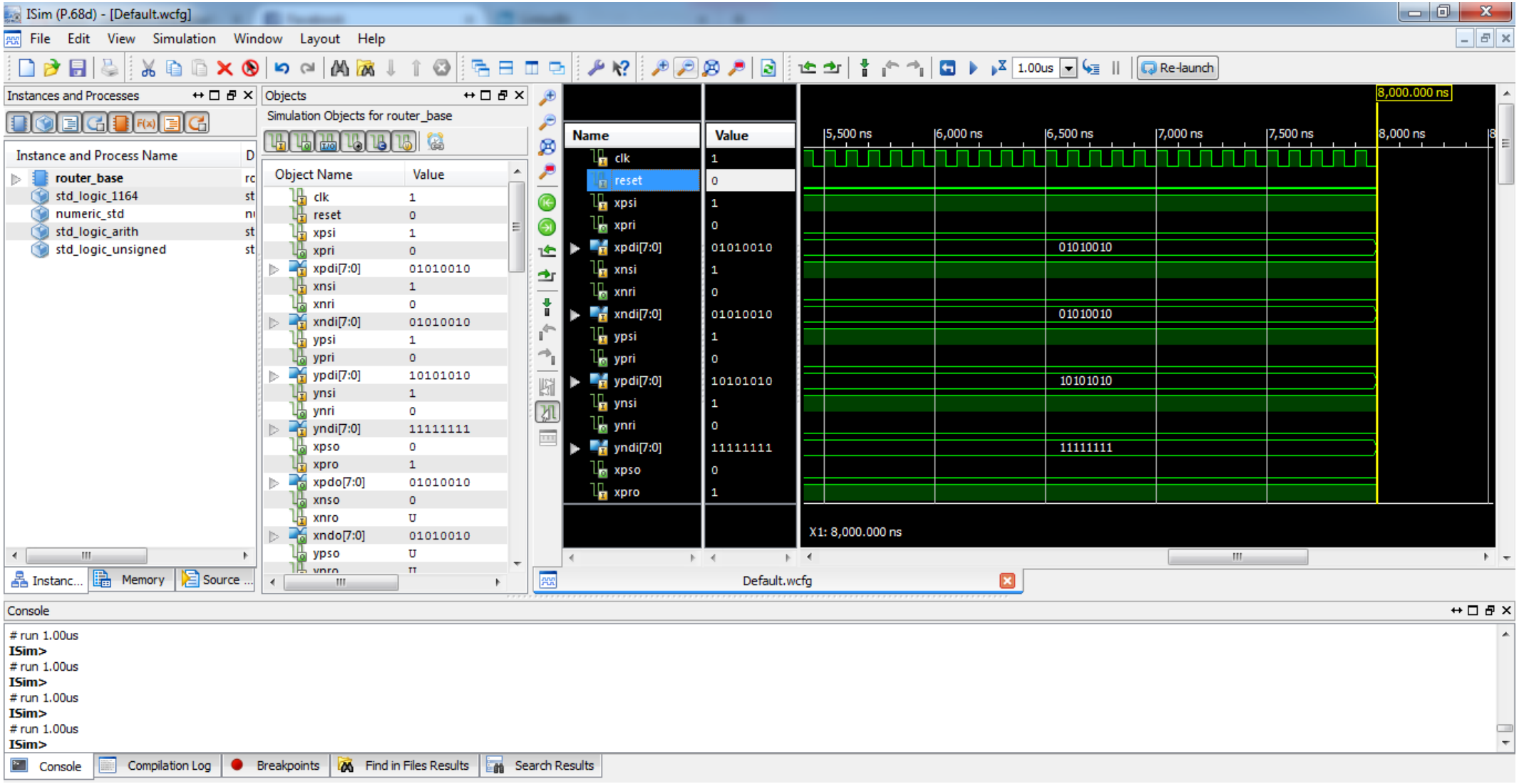


Modules

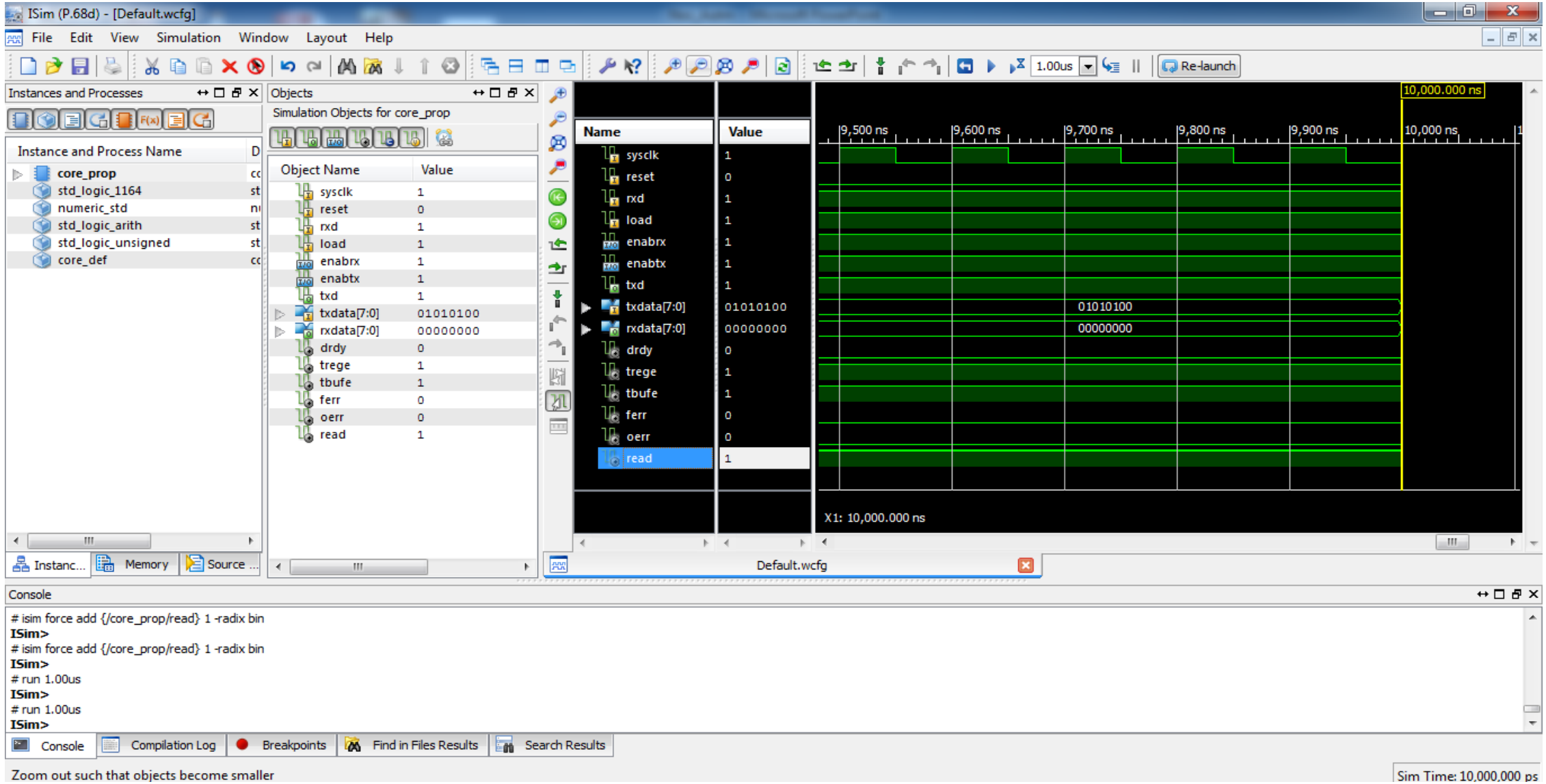
- Network on Chip (NoC)
  - Router
  - Network interface (NI)
  - Core
  - Physical Link (PL)
  - Scalable Traffic Pattern Up-Scaling Algorithm
- Fuzzy based Traffic Regulation Unit (F-TRU)
- Testing Architecture

SIMULATION RESULTS

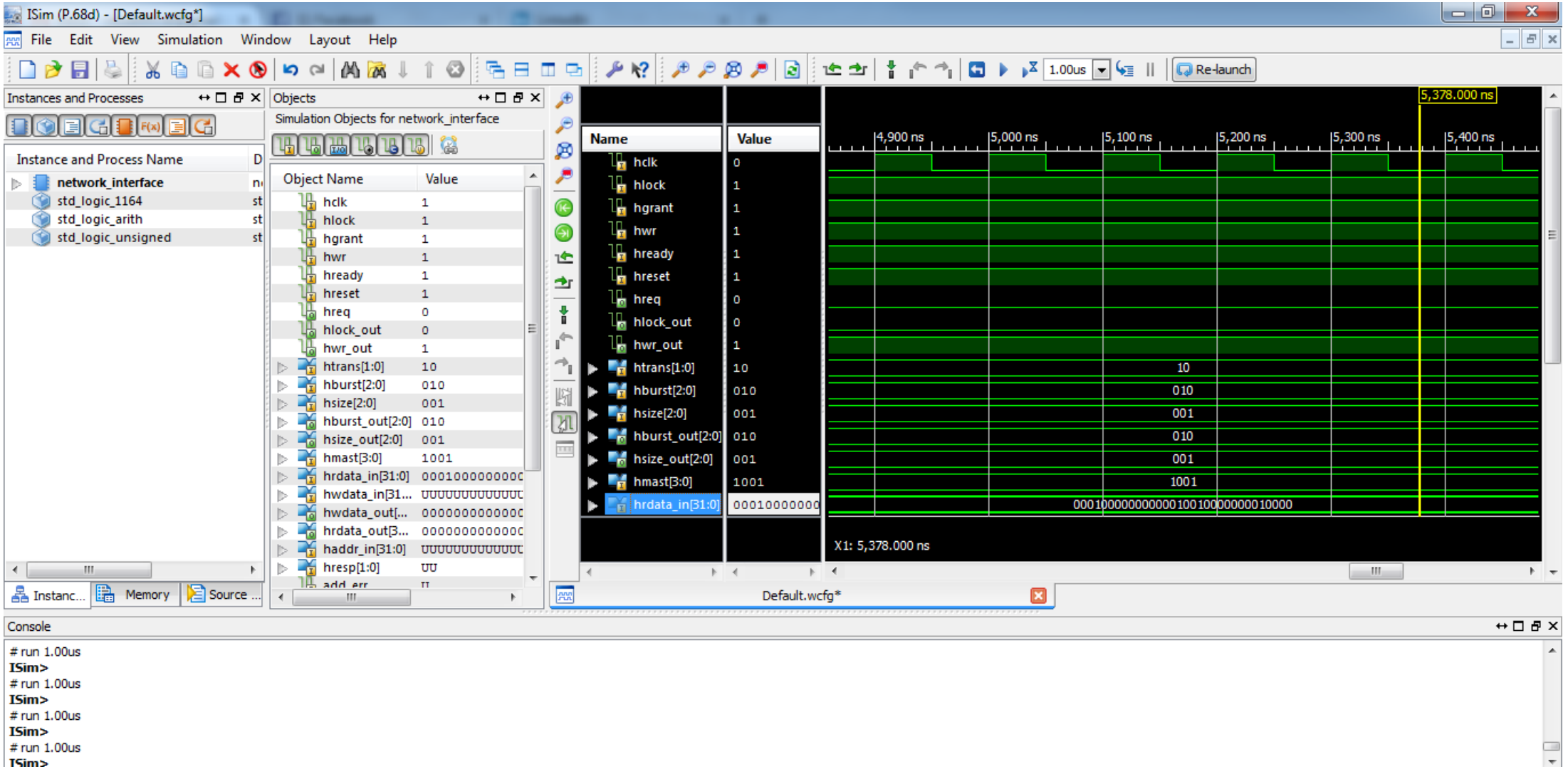
Router


ISim (P.68d) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
router_base
std_logic_1164
numeric_std
std_logic_arith
std_logic_unsigned
Objects
Simulation Objects for router_base
Object Name Value
clk 1
reset 0
xpsi 1
xpri 0
xpdi[7:0] 01010010
xnsi 1
xnri 0
xndi[7:0] 01010010
ypsi 1
ypri 0
ypdi[7:0] 10101010
ynsi 1
ynri 0
yndi[7:0] 11111111
xpso 0
xpro 1
xpdo[7:0] 01010010
xnso 0
xnro U
xndo[7:0] 01010010
ypso U
Name
Value
5,500 ns
6,000 ns
6,500 ns
7,000 ns
7,500 ns
8,000 ns
8,000.000 ns
X1: 8,000.000 ns
Default.wcfg
Console
run 1.00us
ISim>
run 1.00us
ISim>
run 1.00us
ISim>
run 1.00us
ISim>
Compilation Log
Breakpoints
Find in Files Results
Search Results

CORES


ISim (P.68d) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
core_prop
std_logic_1164
numeric_std
std_logic_arith
std_logic_unsigned
core_def
Objects
Simulation Objects for core_prop
Object Name Value
sysclk 1
reset 0
rxd 1
load 1
enabrx 1
enabtx 1
txd 1
txdata[7:0] 01010100
rxdata[7:0] 00000000
drdy 0
trege 1
tbufe 1
ferr 0
oerr 0
read 1
Name Value
10,000.000 ns
9,500 ns 9,600 ns 9,700 ns 9,800 ns 9,900 ns 10,000 ns
X1: 10,000.000 ns
Instanc... Memory Source ...
Default.wcfg
Console
isim force add {/core_prop/read} 1 -radix bin
ISim>
isim force add {/core_prop/read} 1 -radix bin
ISim>
run 1.00us
ISim>
run 1.00us
ISim>
Console Compilation Log Breakpoints Find in Files Results Search Results
Zoom out such that objects become smaller
Sim Time: 10,000,000 ps

NI


ISim (P.68d) - [Default.wcfg*]
File Edit View Simulation Window Layout Help
Re-launch
1.00us
Instances and Processes
Instance and Process Name
network_interface
std_logic_1164
std_logic_arith
std_logic_unsigned
Objects
Simulation Objects for network_interface
Object Name
Value
hclk 1
hlock 1
hgrant 1
hwr 1
hready 1
hreset 1
hreq 0
hlock_out 0
hwr_out 1
htrans[1:0] 10
hburst[2:0] 010
hsize[2:0] 001
hburst_out[2:0] 010
hsize_out[2:0] 001
hmast[3:0] 1001
hrdata_in[31:0]
hwdata_in[31...
hwdata_out[...
hrdata_out[3...
haddr_in[31:0]
hresp[1:0]
Name
Value
4,900 ns
5,000 ns
5,100 ns
5,200 ns
5,300 ns
5,400 ns
5,378.000 ns
X1: 5,378.000 ns
Instanc...
Memory
Source ...
Default.wcfg*
Console
run 1.00us
ISim>
run 1.00us
ISim>
run 1.00us
ISim>
run 1.00us
ISim>

Base Area @ 130 slices

- Design Overview
  - Summary
  - IOB Properties
  - Module Level Utilization
  - Timing Constraints
  - Pinout Report
  - Clock Report
  - Static Timing
- Errors and Warnings
  - Parser Messages
  - Synthesis Messages
  - Translation Messages
  - Map Messages
  - Place and Route Messages
  - Timing Messages
  - Bitgen Messages
  - All Implementation Messages
- Detailed Reports
  - Synthesis Report
  - Translation Report
  - Map Report
  - Place and Route Report
  - Post-PAR Static Timing Report
  - Power Report
  - Bitgen Report

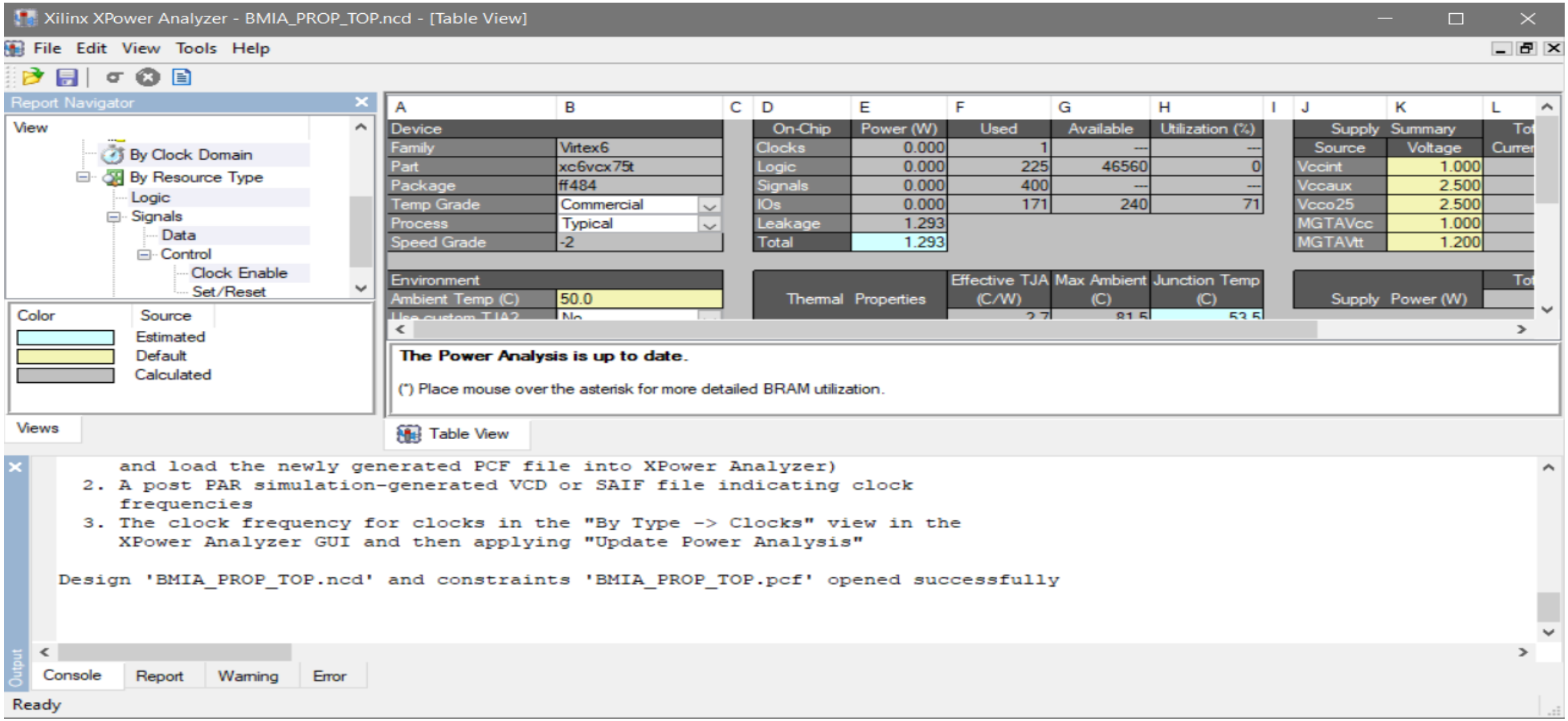
Design Properties
- [ ] Enable Message Filtering

Optional Design Summary Contents
- [ ] Show Clock Report
- [ ] Show Failing Constraints
- [ ] Show Warnings
- [ ] Show Errors

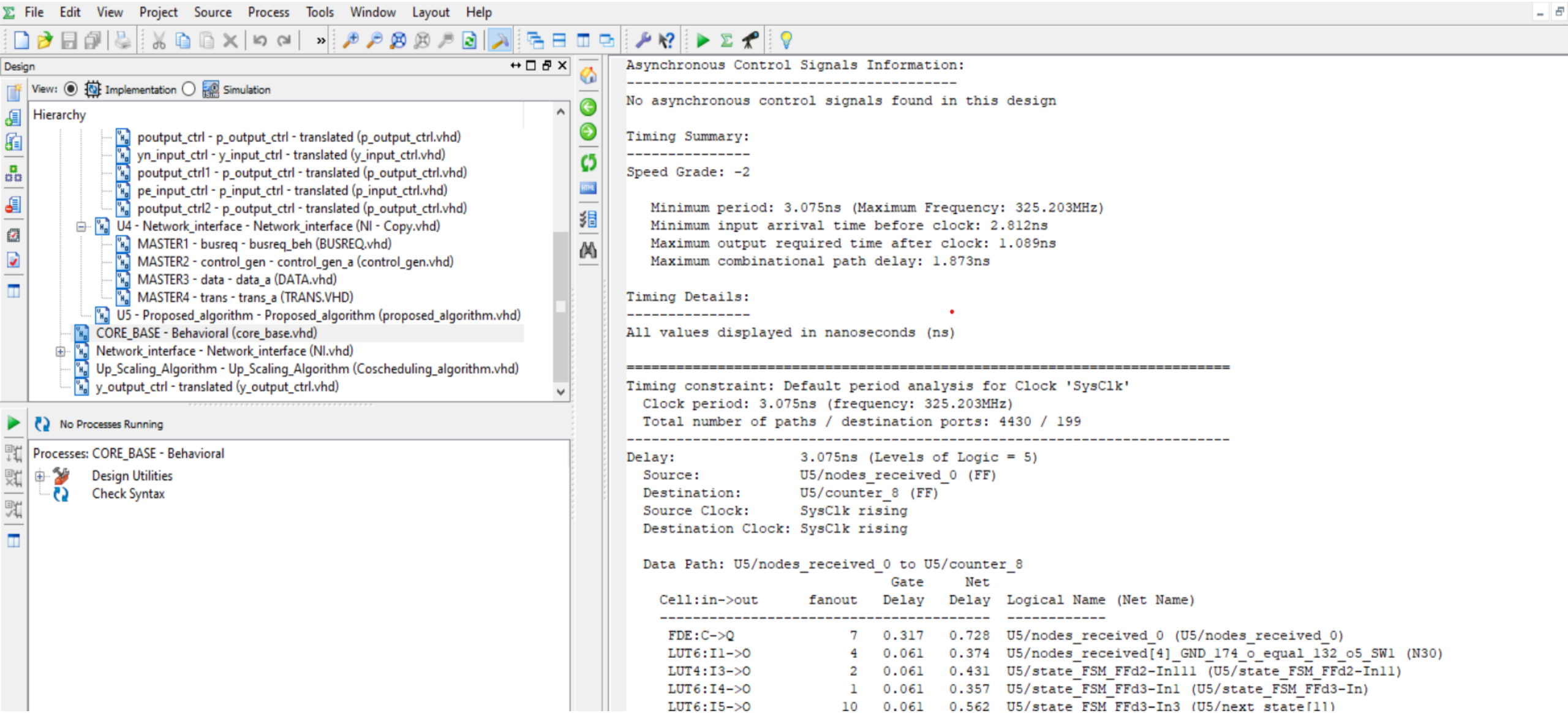
BMIA_PROP_TOP Project Status			
Project File:	NoC_Project.xise	**Parser Errors:**	No Errors
Module Name:	BMIA_PROP_TOP	**Implementation State:**	Placed and Routed
Target Device:	xc6vcx75t-2ff484	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	391 Warnings (0 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	130	93,120	1%	
Number used as Flip Flops	130			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	225	46,560	1%	
Number used as logic	223	46,560	1%	
Number using O6 output only	145			
Number using O5 output only	13			
Number using O5 and O6	65			
Number used as ROM	0			
Number used as Memory	0	16,720	0%	
Number used exclusively as route-thrus	2			
Number with same-slice register load	0			
Number with same-slice carry load	2			
Number with other load	0			
Number of occupied Slices	114	11,640	1%	

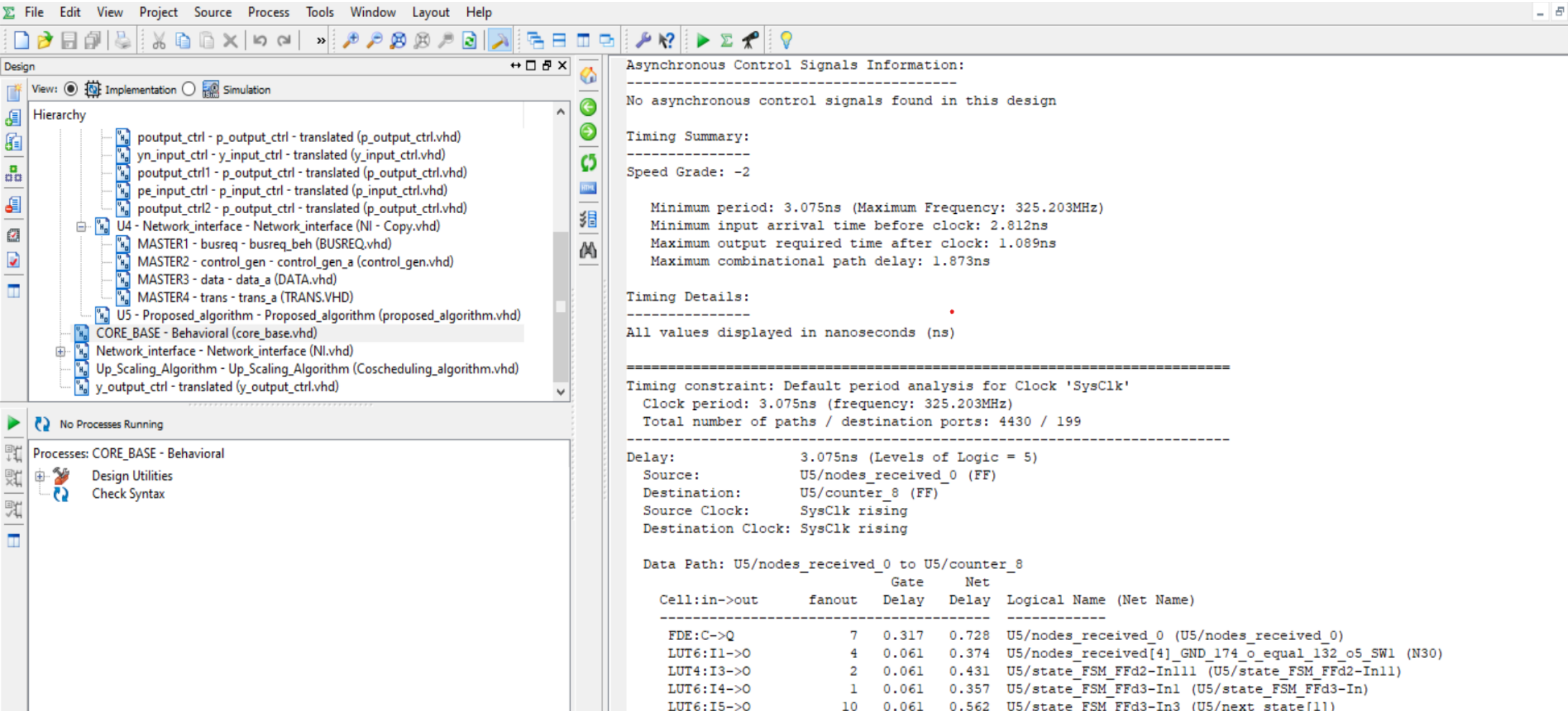
Base Power @ 71%(1.293W)



Base Speed @ 350MHz



Base Latency @ 3.025ns.



CONCLUSION

❖The proliferation of multi-core and many-core chips for performance scaling is making the Network-on-Chip (NOC) occupy a growing amount of silicon area spanning several metal layers.

- To this end, we propose a Permanent Fault Tolerant Router (PFTR) that is capable of tolerating multiple permanent faults in the pipeline. PFTR is designed by making architectural modifications to individual pipeline stages of the baseline NoC router.

REFERENCE

[1] Intel Xeon Phi Coprocessor, visited March 2015. [Online]. Available: https://software.intel.com/de-de/mic-developer

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[4] S. Borkar, “Designing reliable systems from unreliable components: the challenges of transistor variability and degradation,” IEEE Micro, vol. 25, no. 6, pp. 10–16, 2005.

[5] J. Lienig, “Electromigration and its impact on physical design in future technologies,” in Proc. of ACM Int’l Symp. on Physical Design (ISPD), 2013, pp. 33–40.


Thank
you