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MULTI FAULT MULTI-LAYER DIAGNOSIS FOR FAULT-TOLERANT NETWORKS-ON-CHIP

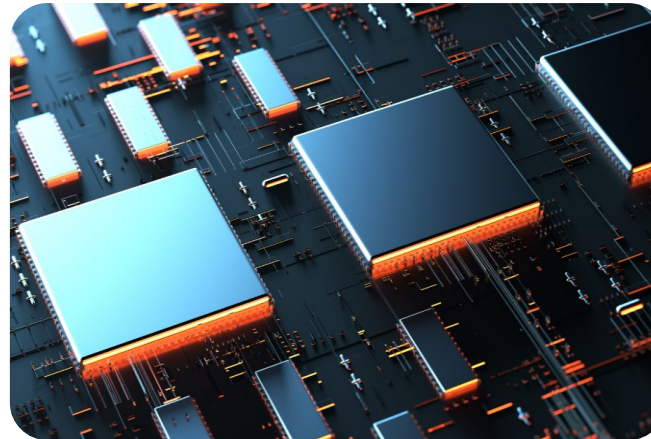
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INTRODUCTION

- ❖ The continuous evolution of new application has become the reason of the invention of some new processor, memory and accelerator cores.
- ❖ Moreover, the fast development and improvement of computation and the complexity of communication have caused the invention of the scalability-centered paradigms.

PROBLEM STATEMENT

❖ Recently, NOC reliability research has made significant strides and has developed a suite of canonical approaches to improve failure resistance including the use of redundant components and logic for self-repair at the circuit layer, redundant wires and error correction codes at the data layer, and reconfiguration and fault-tolerant routing algorithms at the network layer.

OBJECTIVE

- ❖ In order to tolerate faults that emerge in operating Networks-on-Chip, diagnosis techniques are employed for fault detection and localization.
- ❖ On various network layers, diverse diagnosis methods can be employed which differ in terms of their impact on network performance (e.g., by operating concurrently versus pre-empting regular network operation) and the quality of diagnostic results.

EXISTING SYSTEM

- ❖ As the complexity of designs increases and technology scales down into the deep-submicron domain, the probability of malfunctions and failures in the networks-on-chip (NOCs) components increases.
- ❖ Networks-on-Chip constitute the interconnection architecture of future, massively parallel multiprocessors that assemble hundreds to thousands of processing cores on a single chip.

PROPOSED SYSTEM

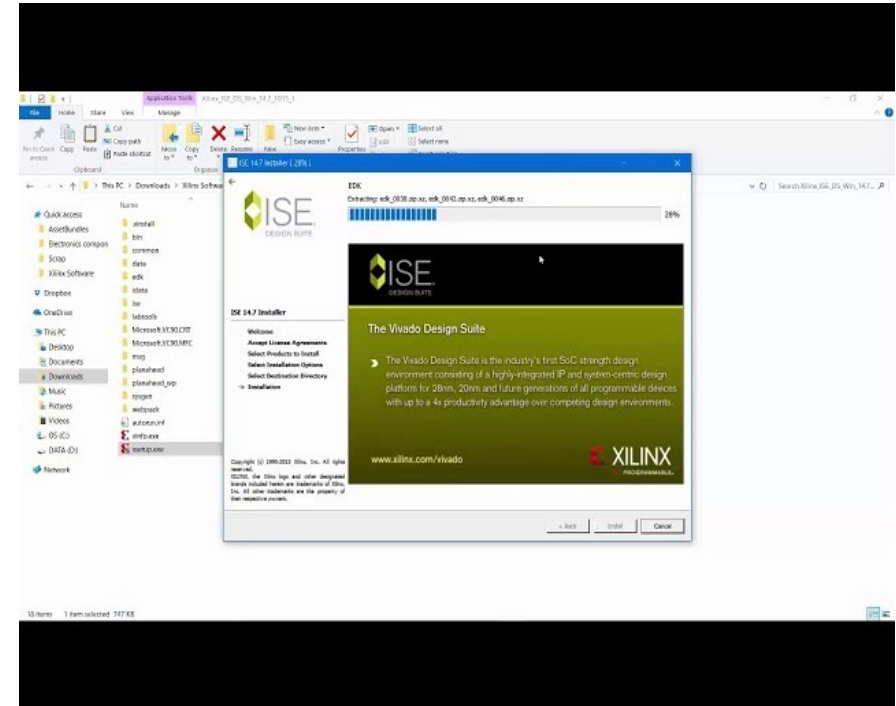
- ❖ Networks-on-chip are inherently fault tolerant or at least gracefully degradable as both, connectivity and amount of resources, provide some useful redundancy.
- ❖ These properties can only be exploited extensively if test and diagnosis techniques support fault detection and error containment in an optimized way.

COMPARISION

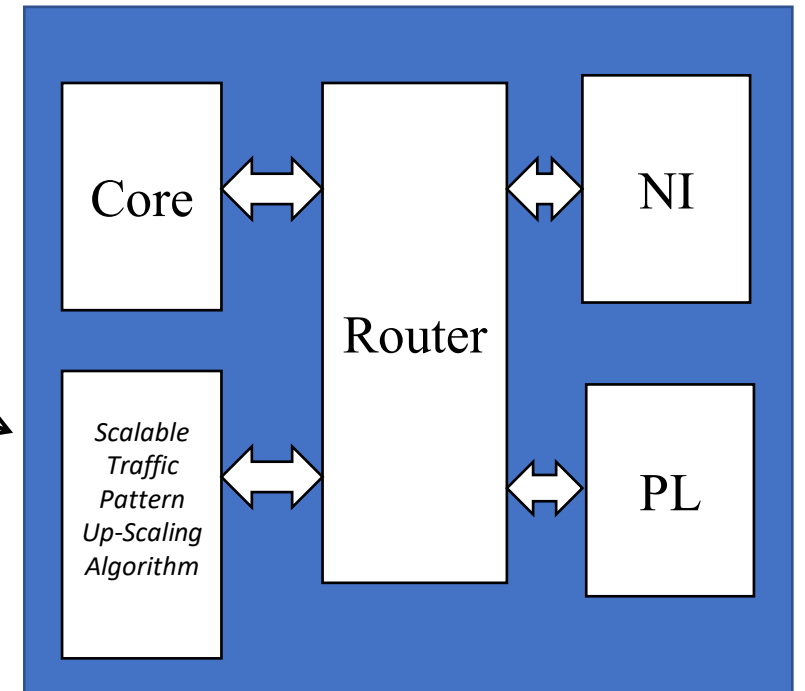
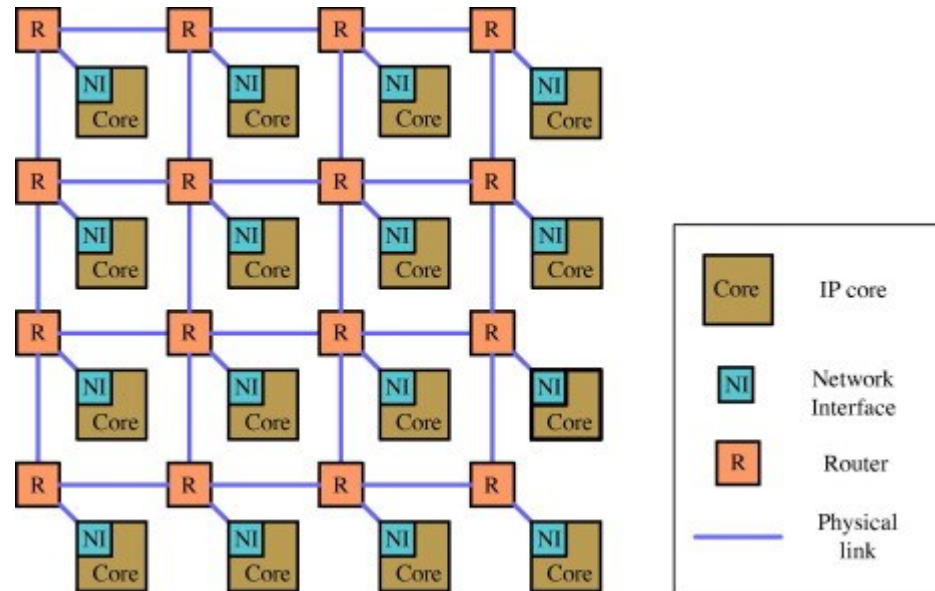
S.No	Paper	Methodology	Merits/demerits
1	Fault-tolerant networks-on-chip routing with coarse and fine-grained look-ahead	novel adaptive routing algorithms, namely coarse and fine-grained (FG) look-ahead algorithms	higher throughput and scalability
2	A unified test and fault-tolerant multicast solution for network-on-chip designs	fault-free routers/links	Performance degradation
3	Simple fault-tolerant method to balance load in network-on-chip	Multi Router Fault tolerant (LBMF) routing method	Low Power
4	Reliability assessment of fault tolerant routing algorithms in networks-on-chip: An analytic approach	Efficient fault adaptive routing algorithms	Energy efficient System
5	Fault Tolerant Deadlock-Free Adaptive Routing Algorithms for Hexagonal Networks-on-Chip	hexagonal on-chip network topology	Proposed method in reducing test time.

TOOL USED

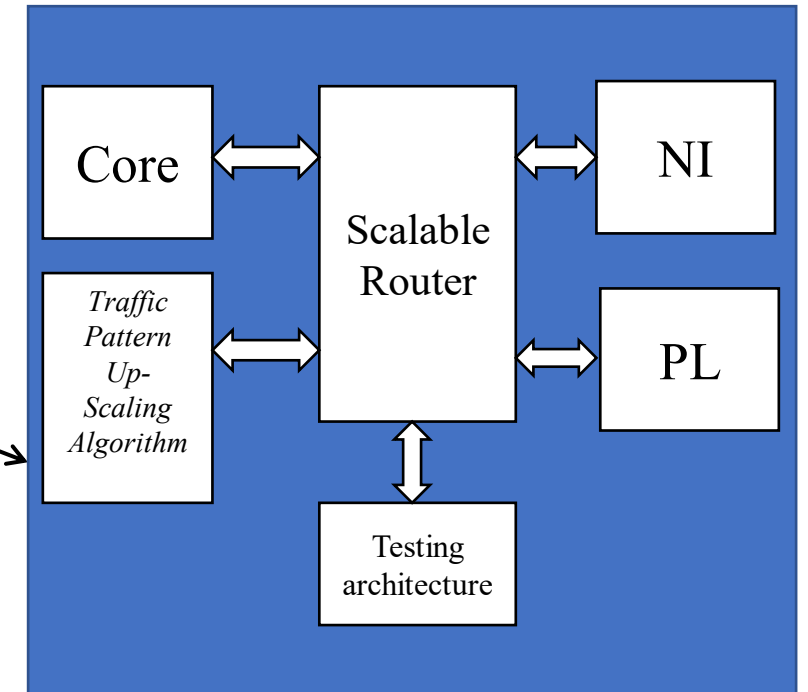
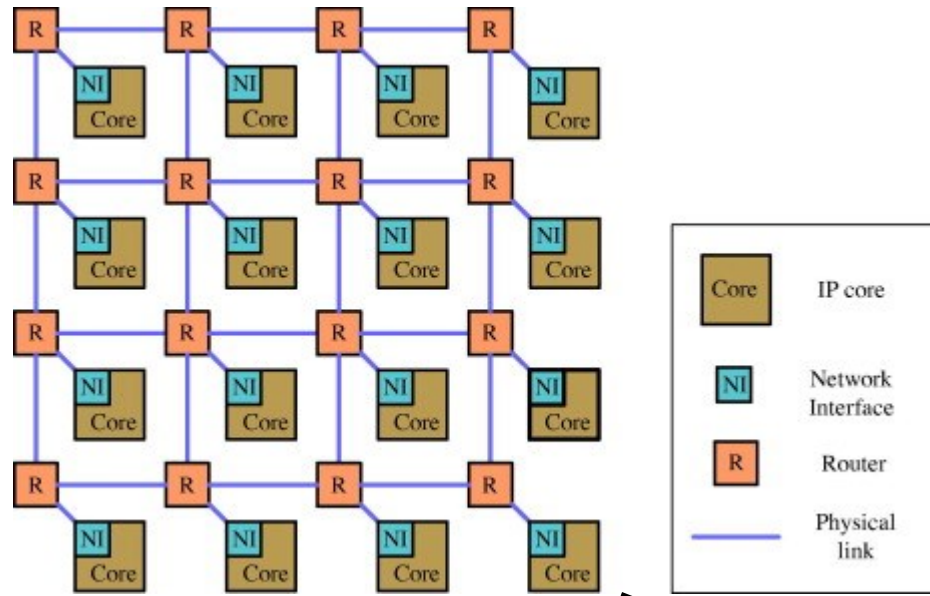
❖ Xilinx 14.7



BASE BLOCK DIAGRAM



PROPOSED BLOCK DIAGRAM

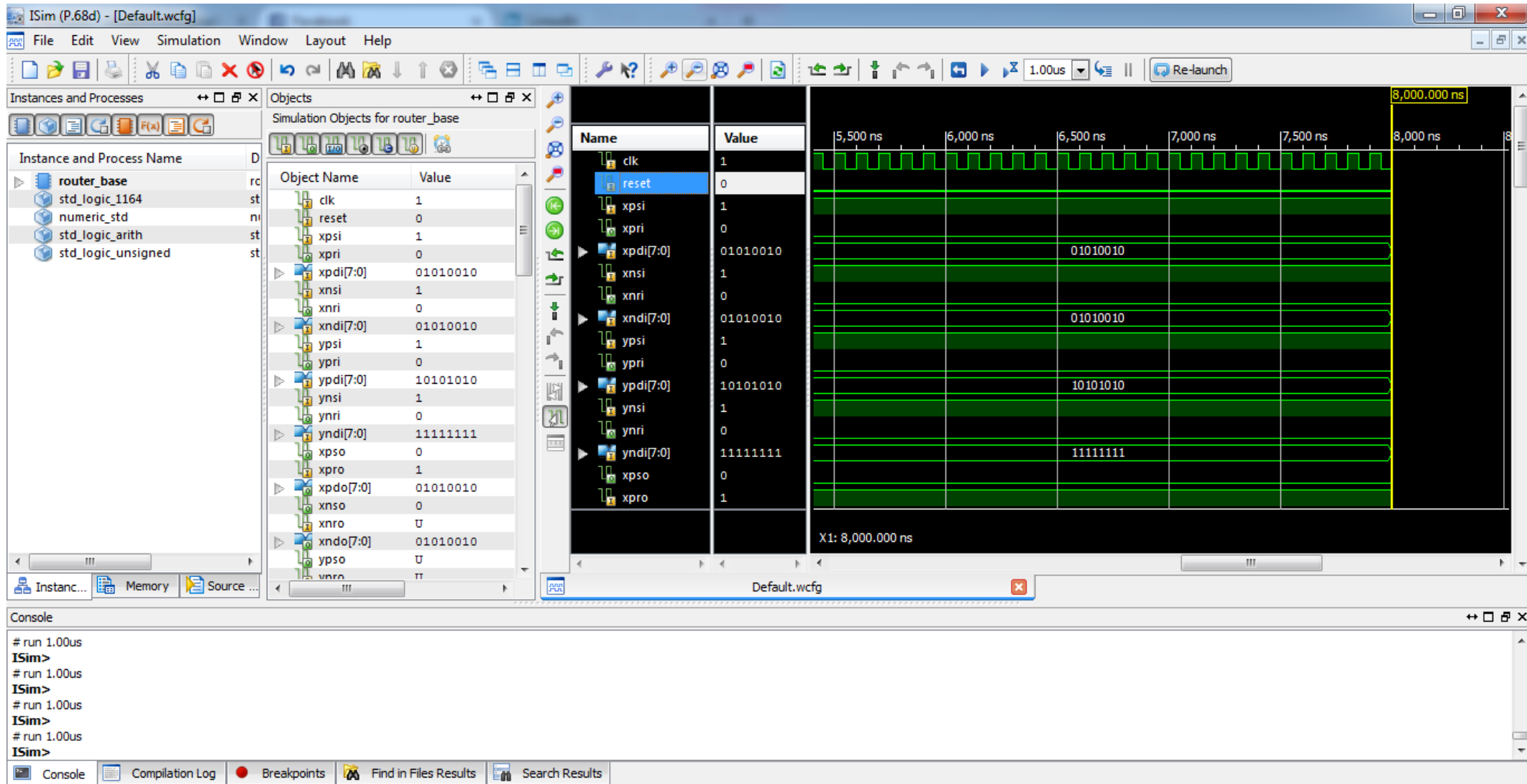


Modules

- Network on Chip (NoC)
 - Router
 - Network interface (NI)
 - Core
 - Physical Link (PL)
 - Scalable Traffic Pattern Up-Scaling Algorithm
- Fuzzy based Traffic Regulation Unit (F-TRU)
- Testing Architecture

SIMULATION RESULTS

Router



CORES

ISim (P.68d) - [Default.wcfg]

File Edit View Simulation Window Layout Help

Instances and Processes

Instance and Process Name

- core_prop
- std_logic_1164
- numeric_std
- std_logic_arith
- std_logic_unsigned
- core_def

Objects

Simulation Objects for core_prop

Object Name	Value
sysclk	1
reset	0
rxd	1
load	1
enabrx	1
enabtx	1
txd	1
txdata[7:0]	01010100
rxdata[7:0]	00000000
drdy	0
trege	1
tbufe	1
ferr	0
oerr	0
read	1

Name Value

Name	Value
sysclk	1
reset	0
rxd	1
load	1
enabrx	1
enabtx	1
txd	1
txdata[7:0]	01010100
rxdata[7:0]	00000000
drdy	0
trege	1
tbufe	1
ferr	0
oerr	0
read	1

Timing Diagram: 9,500 ns to 10,000 ns. X1: 10,000.000 ns.

Console

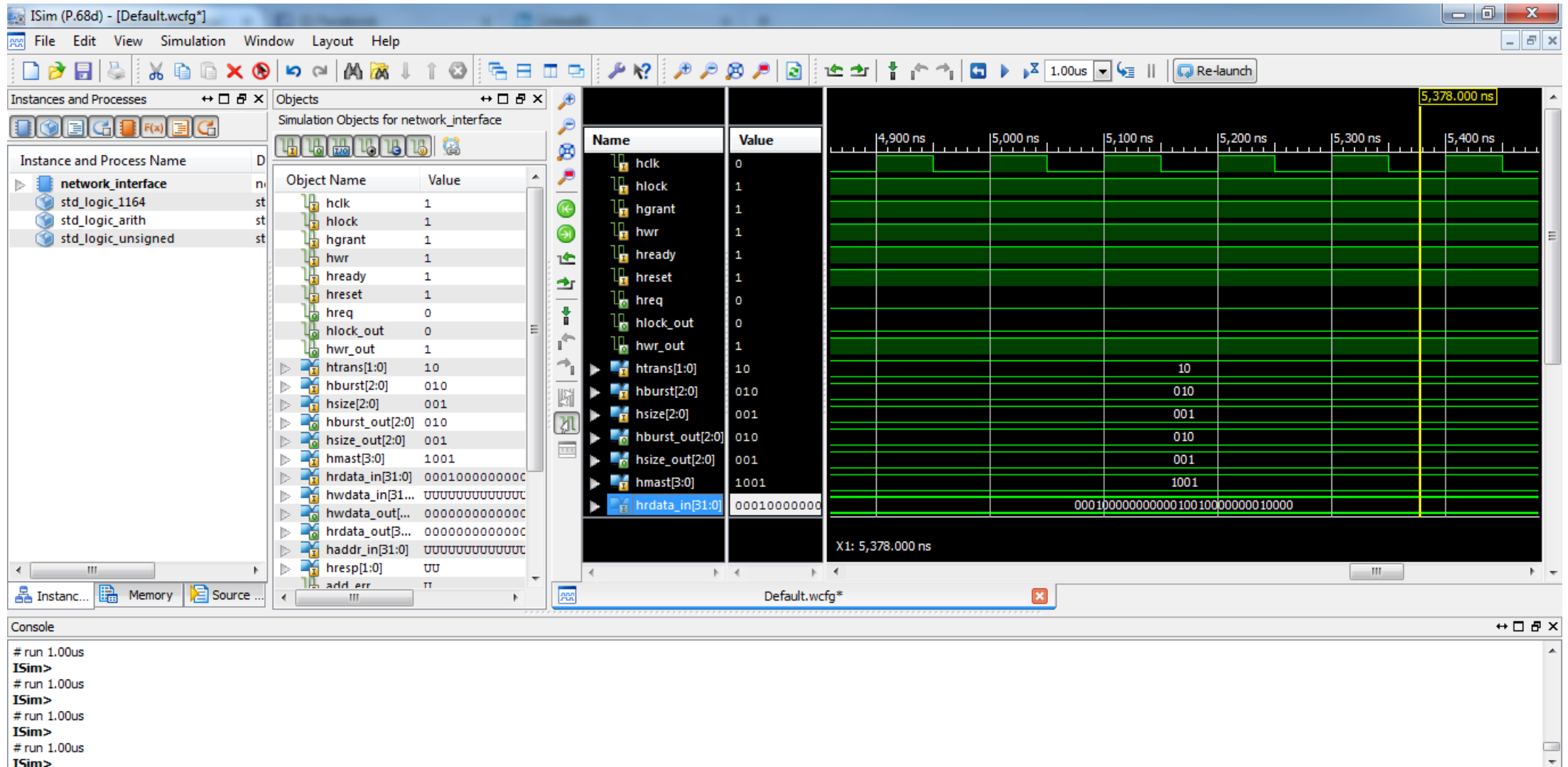
```
# isim force add {/core_prop/read} 1 -radix bin
ISim>
# isim force add {/core_prop/read} 1 -radix bin
ISim>
# run 1.00us
ISim>
# run 1.00us
ISim>
```

Console Compilation Log Breakpoints Find in Files Results Search Results

Zoom out such that objects become smaller

Sim Time: 10,000,000 ps

NI



Base Area @ 130 slices

Design Overview
Summary
IOB Properties
Module Level Utilization
Timing Constraints
Pinout Report
Clock Report
Static Timing
Errors and Warnings
Parser Messages
Synthesis Messages
Translation Messages
Map Messages
Place and Route Messages
Timing Messages
Bitgen Messages
All Implementation Messages
Detailed Reports
Synthesis Report
Translation Report
Map Report
Place and Route Report
Post-PAR Static Timing Report
Power Report
Bitgen Report

- Design Properties
- ☐ Enable Message Filtering
- Optional Design Summary Contents
- ☐ Show Clock Report
 - ☐ Show Failing Constraints
 - ☐ Show Warnings
 - ☐ Show Errors

BMIA_PROP_TOP Project Status			
Project File:	NoC_Project.xise	Parser Errors:	No Errors
Module Name:	BMIA_PROP_TOP	Implementation State:	Placed and Routed
Target Device:	xc6vx75t-2ff484	• Errors:	No Errors
Product Version:	ISE 14.7	• Warnings:	391 Warnings (0 new)
Design Goal:	Balanced	• Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	All Constraints Met
Environment:	System Settings	• Final Timing Score:	0 (Timing Report)

Device Utilization Summary					
Slice Logic Utilization	Used	Available	Utilization	Note(s)	
Number of Slice Registers	130	93,120	1%		
Number used as Flip Flops	130				
Number used as Latches	0				
Number used as Latch-thrus	0				
Number used as AND/OR logics	0				
Number of Slice LUTs	225	46,560	1%		
Number used as logic	223	46,560	1%		
Number using O6 output only	145				
Number using O5 output only	13				
Number using O5 and O6	65				
Number used as ROM	0				
Number used as Memory	0	16,720	0%		
Number used exclusively as route-thrus	2				
Number with same-slice register load	0				
Number with same-slice carry load	2				
Number with other load	0				
Number of occupied Slices	114	11,640	1%		

Base Power @ 71%(1.293W)

Xilinx XPower Analyzer - BMIA_PROP_TOP.ncd - [Table View]

File Edit View Tools Help

Report Navigator

View

- By Clock Domain
- By Resource Type
 - Logic
 - Signals
 - Data
 - Control
 - Clock Enable
 - Set/Reset

Color Source

- Estimated
- Default
- Calculated

A	B	C	D	E	F	G	H	I	J	K	L
Device		On-Chip	Power (W)	Used	Available	Utilization (%)			Supply	Summary	Total
Family	Virtex6	Clocks	0.000	1	---	---			Source	Voltage	Current
Part	xc6vcx75t	Logic	0.000	225	46560	0			Vccint	1.000	
Package	ff484	Signals	0.000	400	---	---			Vccaux	2.500	
Temp Grade	Commercial	IOs	0.000	171	240	71			Vcco25	2.500	
Process	Typical	Leakage	1.293						MGTAVcc	1.000	
Speed Grade	-2	Total	1.293						MGTAVtt	1.200	
Environment		Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)				Supply	Power (W)	Total
Ambient Temp (C)	50.0		2.7	81.5	53.5						
Use custom TJA?	No										

The Power Analysis is up to date.

(*) Place mouse over the asterisk for more detailed BRAM utilization.

Views

Table View

and load the newly generated PCF file into XPower Analyzer)

2. A post PAR simulation-generated VCD or SAIF file indicating clock frequencies
3. The clock frequency for clocks in the "By Type -> Clocks" view in the XPower Analyzer GUI and then applying "Update Power Analysis"

Design 'BMIA_PROP_TOP.ncd' and constraints 'BMIA_PROP_TOP.pcf' opened successfully

Output

Console Report Warning Error

Ready

Base Speed @ 350MHz

The screenshot displays a digital logic design tool interface. The left pane shows the project hierarchy with components like `poutput_ctrl`, `yn_input_ctrl`, `U4 - Network_interface`, and `U5 - Proposed_algorithm`. The right pane shows the timing analysis results for the clock 'SysClk'.

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -2

Minimum period: 3.075ns (Maximum Frequency: 325.203MHz)
Minimum input arrival time before clock: 2.812ns
Maximum output required time after clock: 1.089ns
Maximum combinational path delay: 1.873ns

Timing Details:

All values displayed in nanoseconds (ns)

=====
Timing constraint: Default period analysis for Clock 'SysClk'
Clock period: 3.075ns (frequency: 325.203MHz)
Total number of paths / destination ports: 4430 / 199
=====

Delay: 3.075ns (Levels of Logic = 5)

Source: U5/nodes_received_0 (FF)
Destination: U5/counter_8 (FF)
Source Clock: SysClk rising
Destination Clock: SysClk rising

Data Path: U5/nodes_received_0 to U5/counter_8

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
FDE:C->Q	7	0.317	0.728	U5/nodes_received_0 (U5/nodes_received_0)
LUT6:I1->O	4	0.061	0.374	U5/nodes_received[4]_GND_174_o_equal_132_o5_SW1 (N30)
LUT4:I3->O	2	0.061	0.431	U5/state_FSM_FFd2-In111 (U5/state_FSM_FFd2-In111)
LUT6:I4->O	1	0.061	0.357	U5/state_FSM_FFd3-In1 (U5/state_FSM_FFd3-In1)
LUT6:I5->O	10	0.061	0.562	U5/state_FSM_FFd3-In3 (U5/next state[11])

Base Latency @ 3.025ns.

The screenshot displays a digital logic design tool interface. The left pane shows a hierarchy of components, including control units, a network interface, and a proposed algorithm. The right pane shows the timing analysis results for the design.

Design Hierarchy:

- View: Implementation
- Hierarchy:
 - poutput_ctrl - p_output_ctrl - translated (p_output_ctrl.vhd)
 - yn_input_ctrl - y_input_ctrl - translated (y_input_ctrl.vhd)
 - poutput_ctrl1 - p_output_ctrl - translated (p_output_ctrl.vhd)
 - pe_input_ctrl - p_input_ctrl - translated (p_input_ctrl.vhd)
 - poutput_ctrl2 - p_output_ctrl - translated (p_output_ctrl.vhd)
 - U4 - Network_interface - Network_interface (NI - Copy.vhd)
 - MASTER1 - busreq - busreq_beh (BUSREQ.vhd)
 - MASTER2 - control_gen - control_gen_a (control_gen.vhd)
 - MASTER3 - data - data_a (DATA.vhd)
 - MASTER4 - trans - trans_a (TRANS.VHD)
 - U5 - Proposed_algorithm - Proposed_algorithm (proposed_algorithm.vhd)
 - CORE_BASE - Behavioral (core_base.vhd)
 - Network_interface - Network_interface (NI.vhd)
 - Up_Scaling_Algorithm - Up_Scaling_Algorithm (Coscheduling_algorithm.vhd)
 - y_output_ctrl - translated (y_output_ctrl.vhd)

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -2

Minimum period: 3.075ns (Maximum Frequency: 325.203MHz)
Minimum input arrival time before clock: 2.812ns
Maximum output required time after clock: 1.089ns
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Timing Details:

All values displayed in nanoseconds (ns)

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Destination: U5/counter_8 (FF)
Source Clock: SysClk rising
Destination Clock: SysClk rising

Data Path: U5/nodes_received_0 to U5/counter_8

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
FDE:C->Q	7	0.317	0.728	U5/nodes_received_0 (U5/nodes_received_0)
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LUT4:I3->O	2	0.061	0.431	U5/state_FSM_FFd2-In111 (U5/state_FSM_FFd2-In111)
LUT6:I4->O	1	0.061	0.357	U5/state_FSM_FFd3-In1 (U5/state_FSM_FFd3-In)
LUT6:I5->O	10	0.061	0.562	U5/state_FSM_FFd3-In3 (U5/next state[11])

CONCLUSION

- ❖ The proliferation of multi-core and many-core chips for performance scaling is making the Network-on-Chip (NOC) occupy a growing amount of silicon area spanning several metal layers.
- To this end, we propose a Permanent Fault Tolerant Router (PFTR) that is capable of tolerating multiple permanent faults in the pipeline. PFTR is designed by making architectural modifications to individual pipeline stages of the baseline NoC router.

REFERENCE

- [1] Intel Xeon Phi Coprocessor, visited March 2015. [Online]. Available: <https://software.intel.com/de-de/mic-developer>
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- [3] W. Dally and B. Towles, “Route packets, not wires: on-chip interconnection networks,” in Proc. of Design Automation Conf. (DAC), 2001, pp. 684–689.
- [4] S. Borkar, “Designing reliable systems from unreliable components: the challenges of transistor variability and degradation,” IEEE Micro, vol. 25, no. 6, pp. 10–16, 2005.
- [5] J. Lienig, “Electromigration and its impact on physical design in future technologies,” in Proc. of ACM Int’l Symp. on Physical Design (ISPD), 2013, pp. 33–40.

*Thank
you*

