NTUEE DCLAB

Quartus Installation & Design Flow

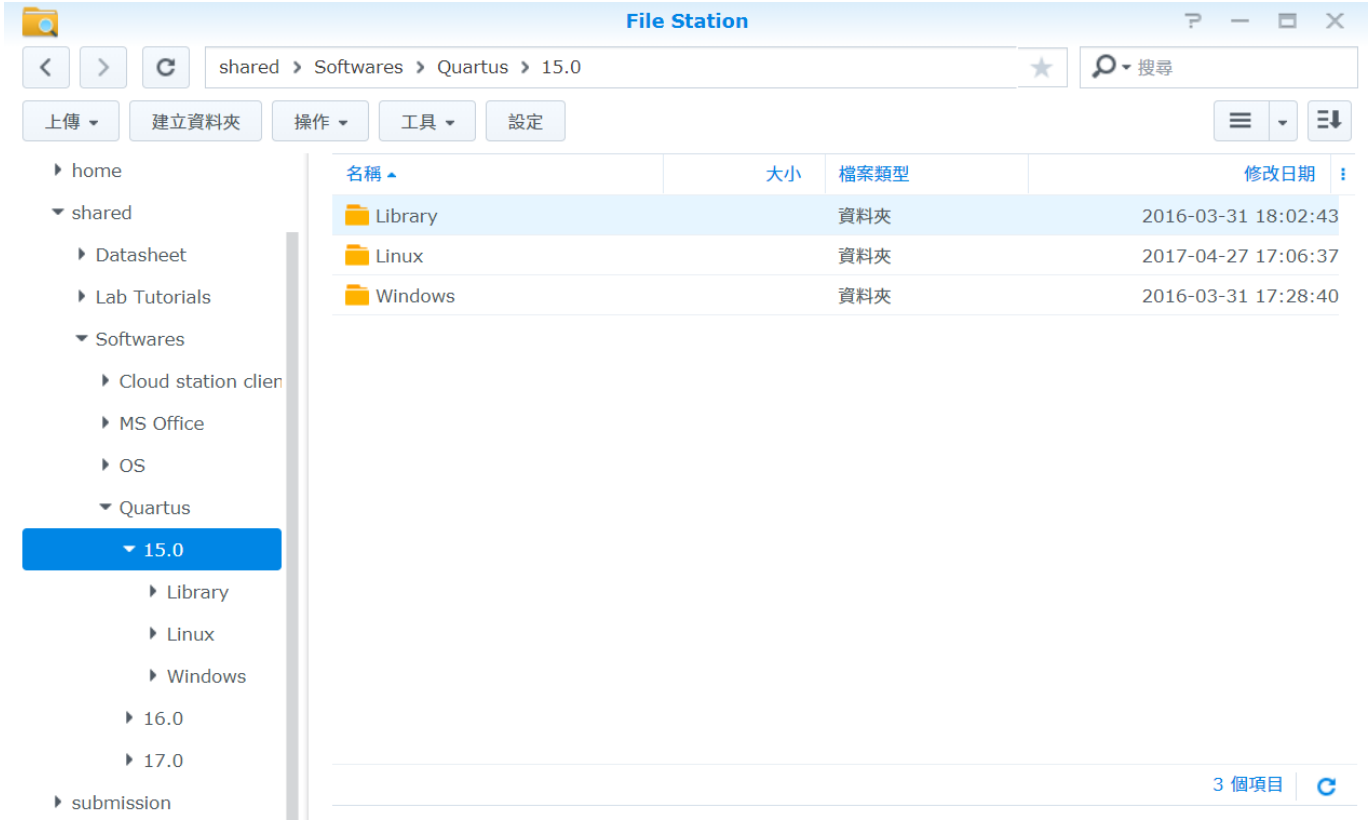
Graduate Institute of Electronics Engineering
National Taiwan University

Outline

- Quartus installation
  - Install devices
  - License setup
  - Install USB driver
- Quartus design flow
  - Create new project
  - Import qsf
- Put your code to FPGA
  - Compile and program
- Debugging and compiling FAQ

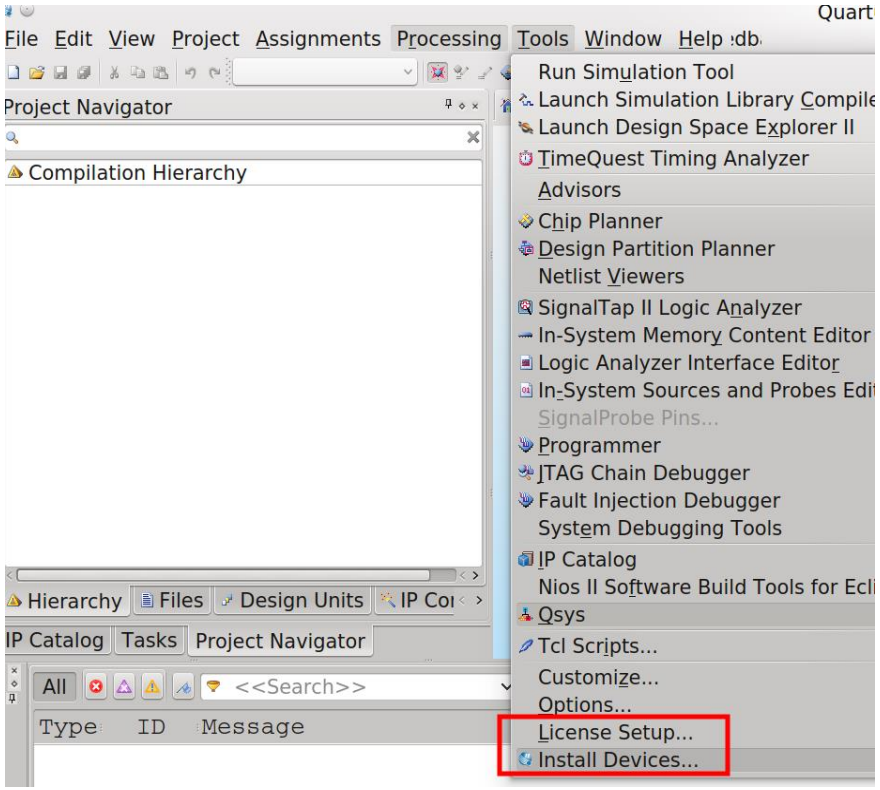
Download & Run Installer

- Download library and installation files
  - Register and download from Altera website
  - Or download from DCLab NAS



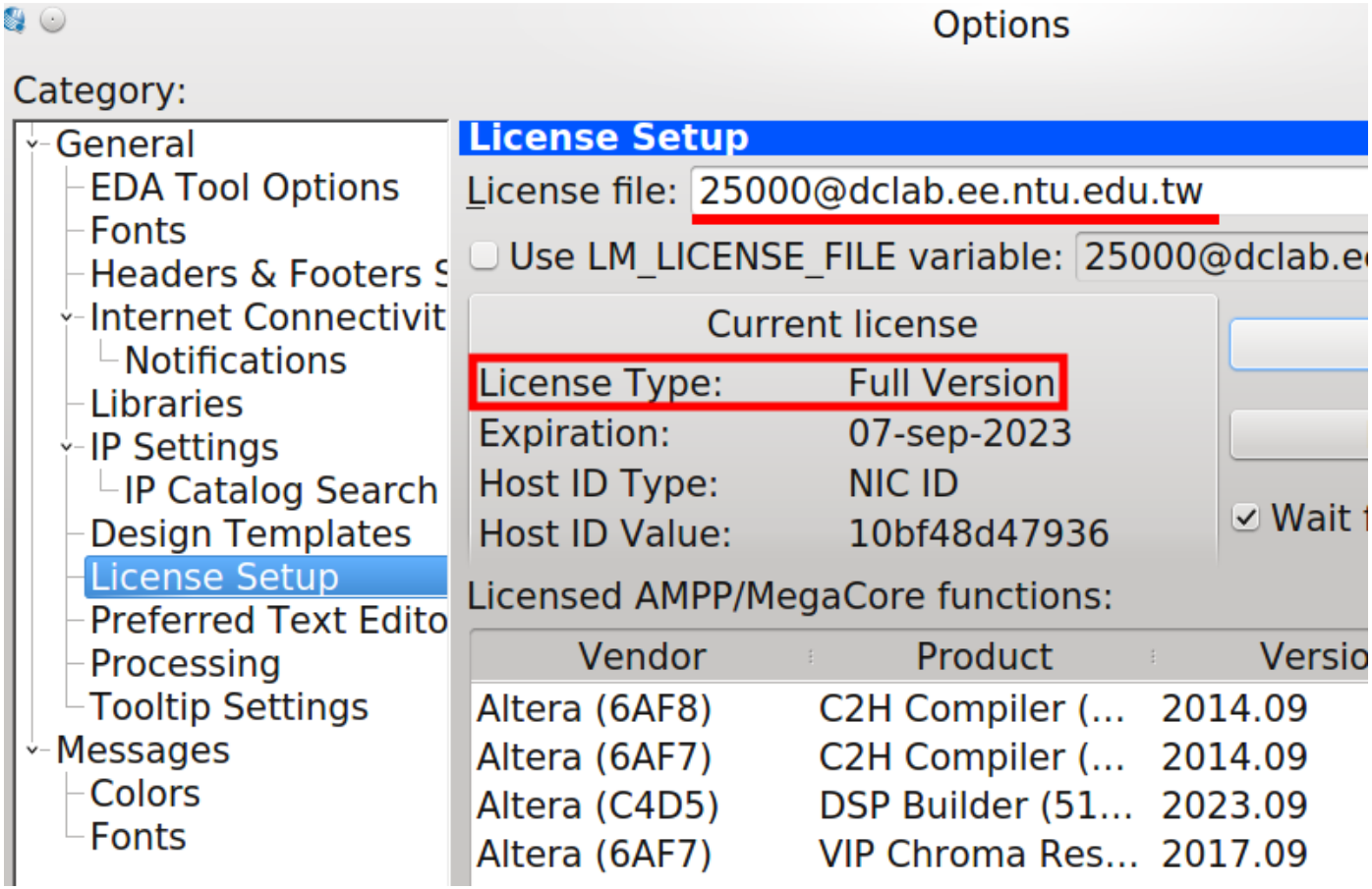
Install Devices

- Tools -> Install Devices
- Choose the library (qdz files) you downloaded
  - Note that DE2-155 belongs to Cyclone IV family



License Setup

- Tools -> License Setup
- This is only available when you are using NTU IP



Install USB Driver for Windows

- The driver is under drivers/usb-blaster/ directory under Quartus installation path
- Plus the USB cable and open following path
  - 我的電腦 -> (右鍵)內容 -> 硬體 -> 裝置管理員
- Choose your device and the driver from the directory

Install USB Driver for Linux

- Create /etc/udev/rules.d/51-usbblaster.rules, then reboot

```
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6001", MODE="0666"
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6002", MODE="0666"
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6003", MODE="0666"
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6010", MODE="0666"
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6810", MODE="0666"
```

- Check the installation
  - Run the library jtagd in bin/directory under Quartus installation path

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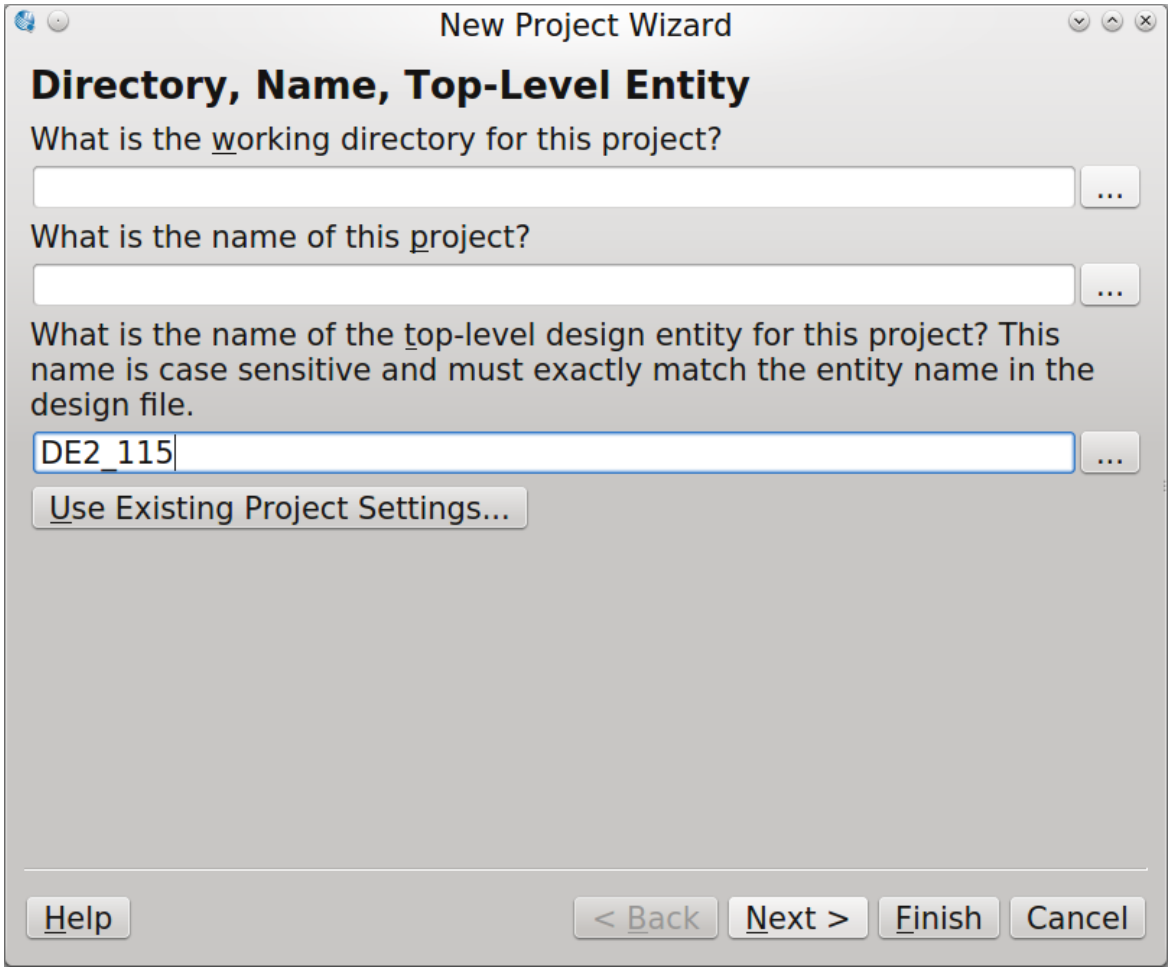
Create New Project

- File -> New Project Wizard
- The name of the top-level design is “DE2_115”

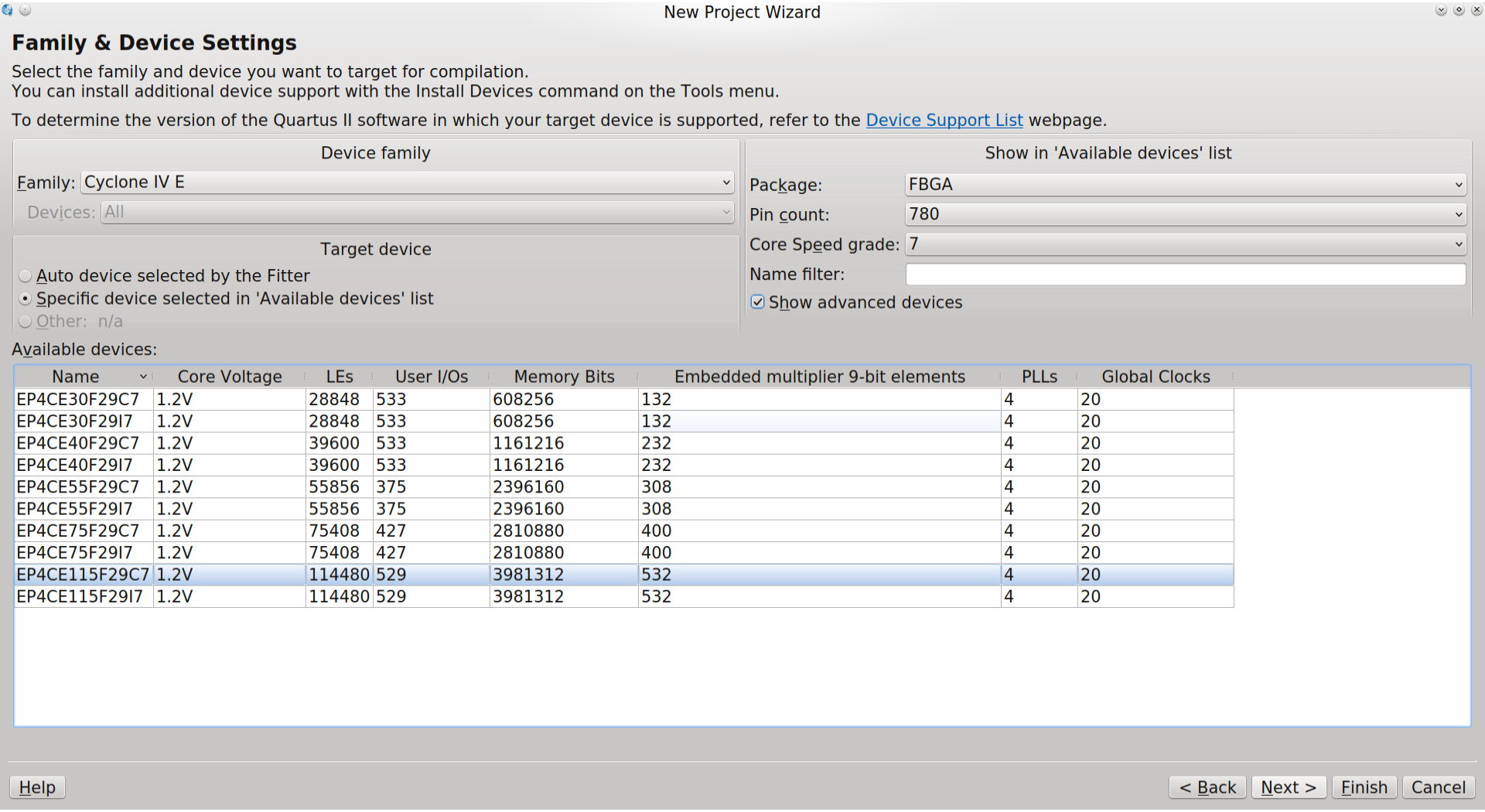


Add Files

- Add files
  - *.sv
  - *.sdc

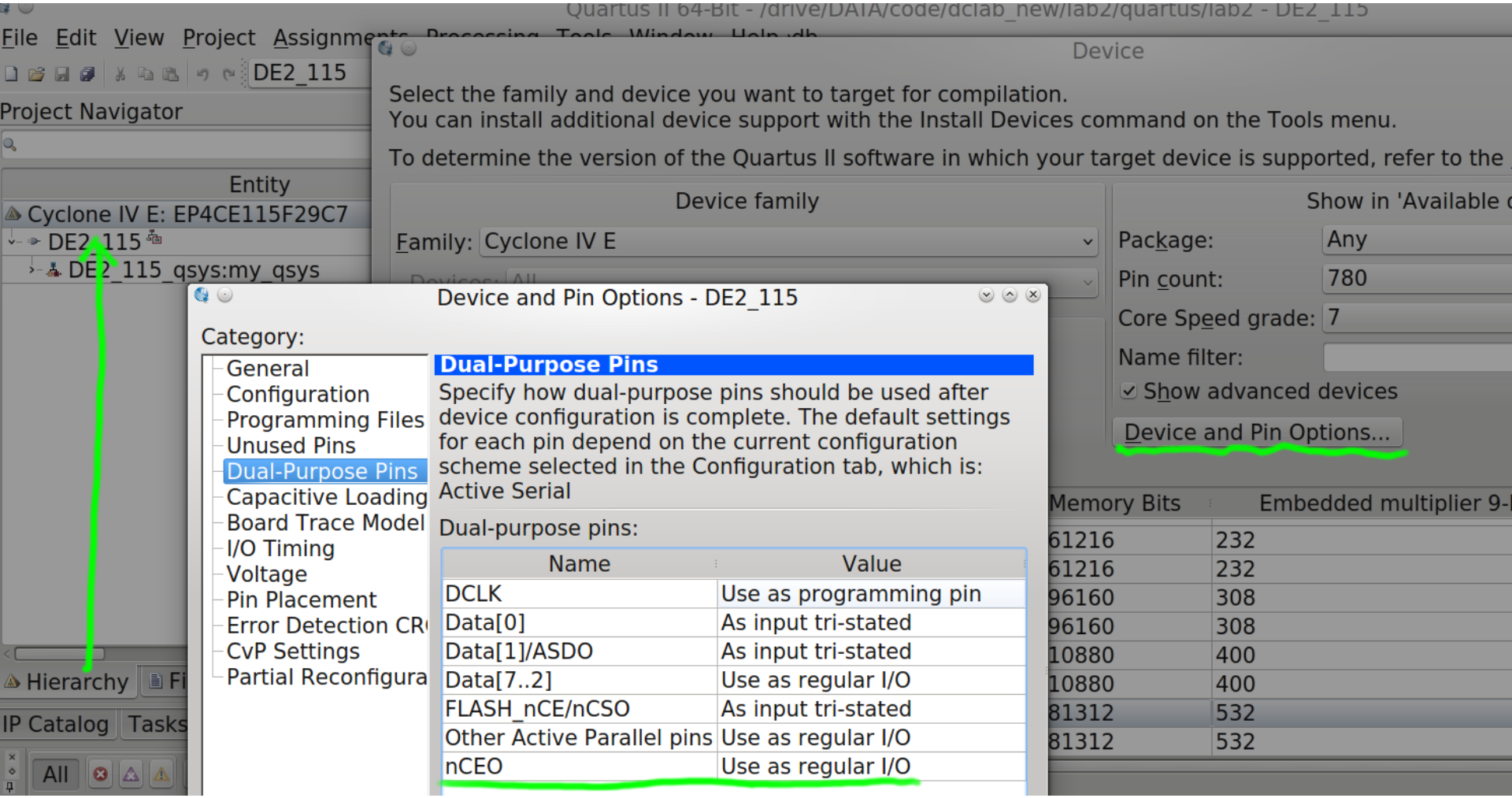
Set the Device

- Select EP4CE115F29C7



A Subtle Configuration

- Some error might occur if this step is skipped



Import qsf

- Assignment -> Import Assignments
  - Select the given qsf file

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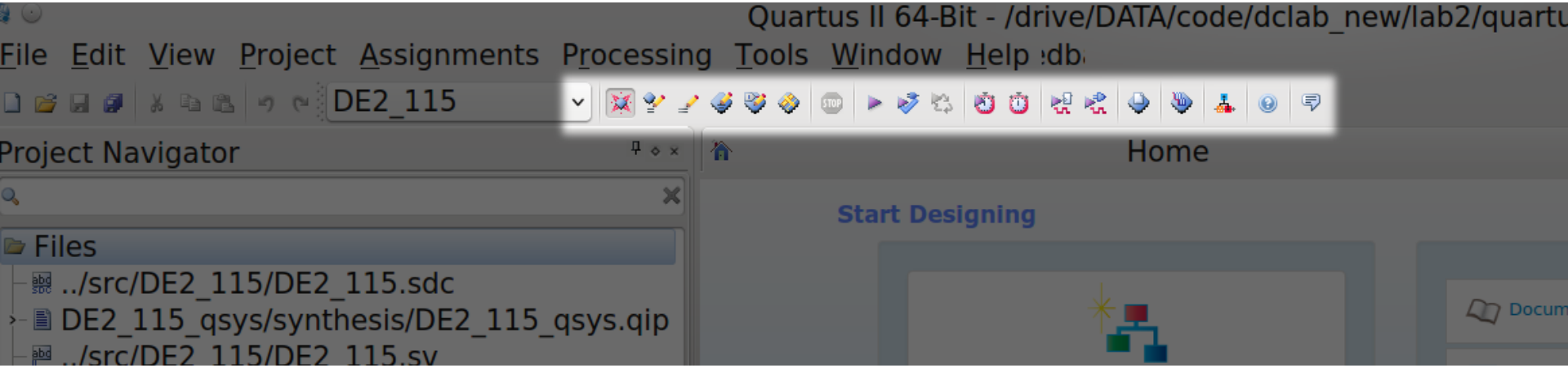
Compile Your Code

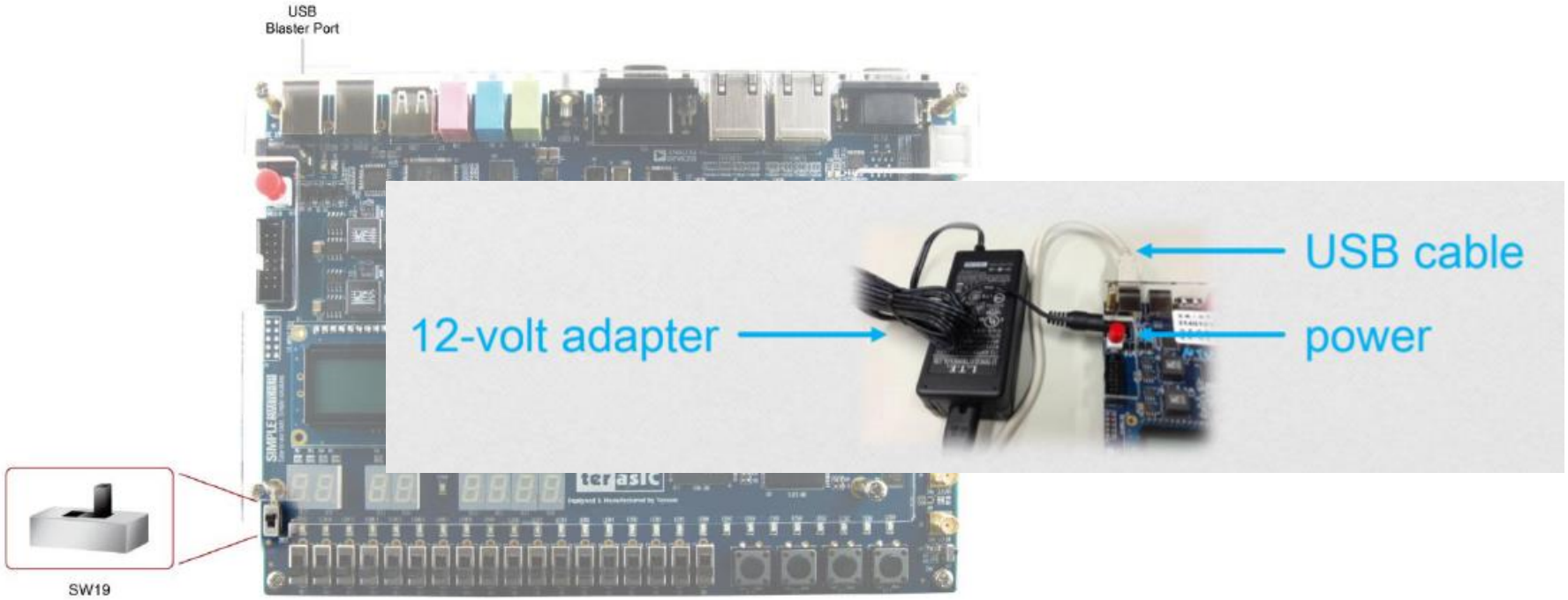
- Press “Ctrl+L” or the purple play button
  - Converts the code to the format that FPGA recognizes
  - Including synthesis, place and route, fitting, etc.
  - Generates a sof file



- Check if there are errors or warnings
  - Modify your code if necessary

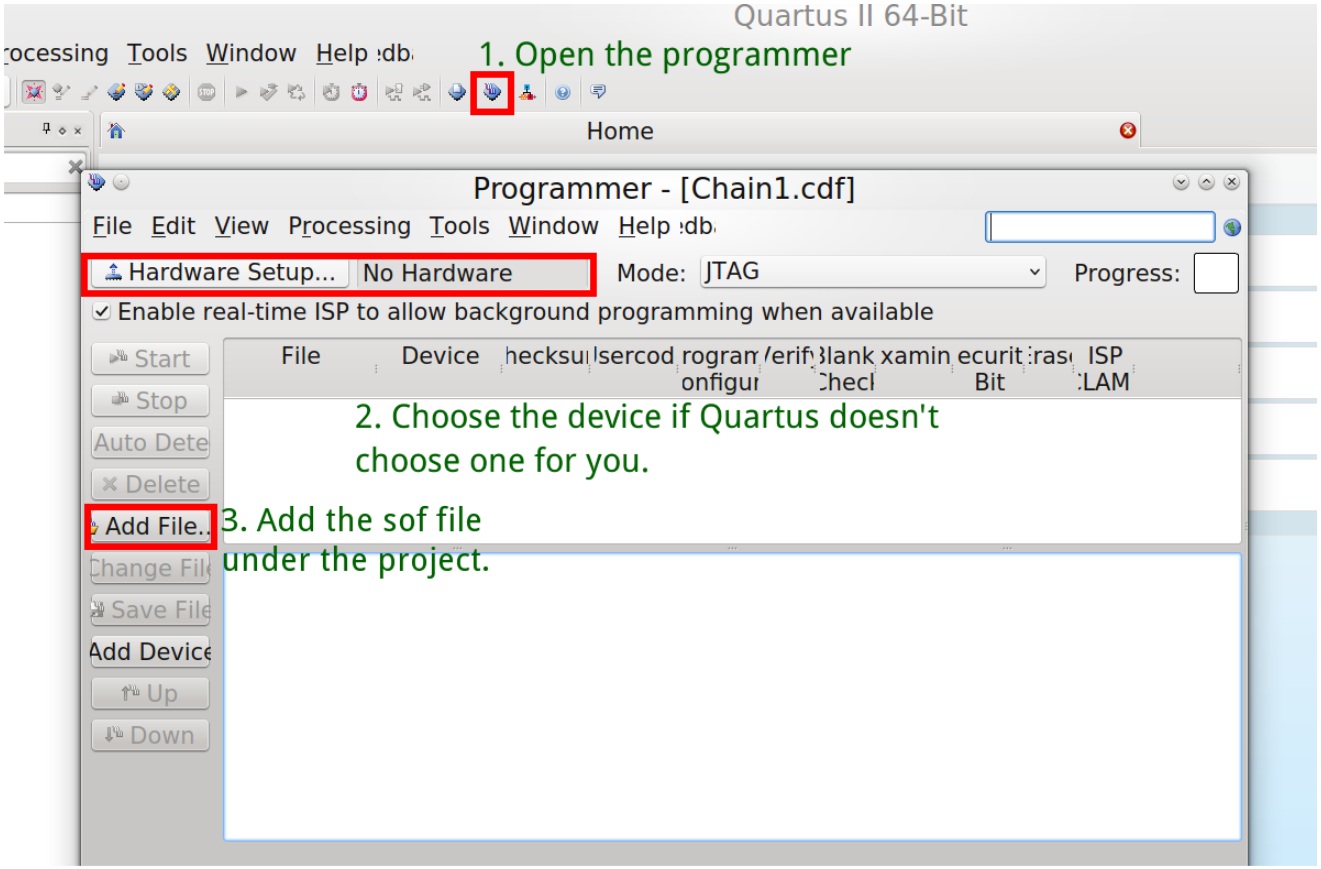
Before Programming FPGA

- Make sure
  - Blaster USB cable is connected
  - Power of FPGA is on
  - The switch on the bottom left is set to RUN



Program the FPGA

- Hardware Setup -> Add File -> Run -> Success



- If you prefer CLI, check this link

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My Verilog Pass Simulation but Don't Work on FPGA

- Some code can not be compiled to hardware
  - Modify your code if there is any **WARNING** about *Combinational Loop* or *Inferred Latch*

- Common warnings/errors of code that is not synthesizable
  - 22011 Combinational Loop
  - 22013 Asynchronous Loop
  - 22014 Synchronous Loop
  - 22051 (Verilog) Generated Reset
  - 22052 (Verilog) Generated Clock
  - 22082 Port Not Connected
  - 23003 Inferred Latch
  - 23006 (Verilog) Incomplete Case Expression with Default Clause
  - 23007 (Verilog) Case Statement Not Fully Specified
  - 25001 Signal with No Driver