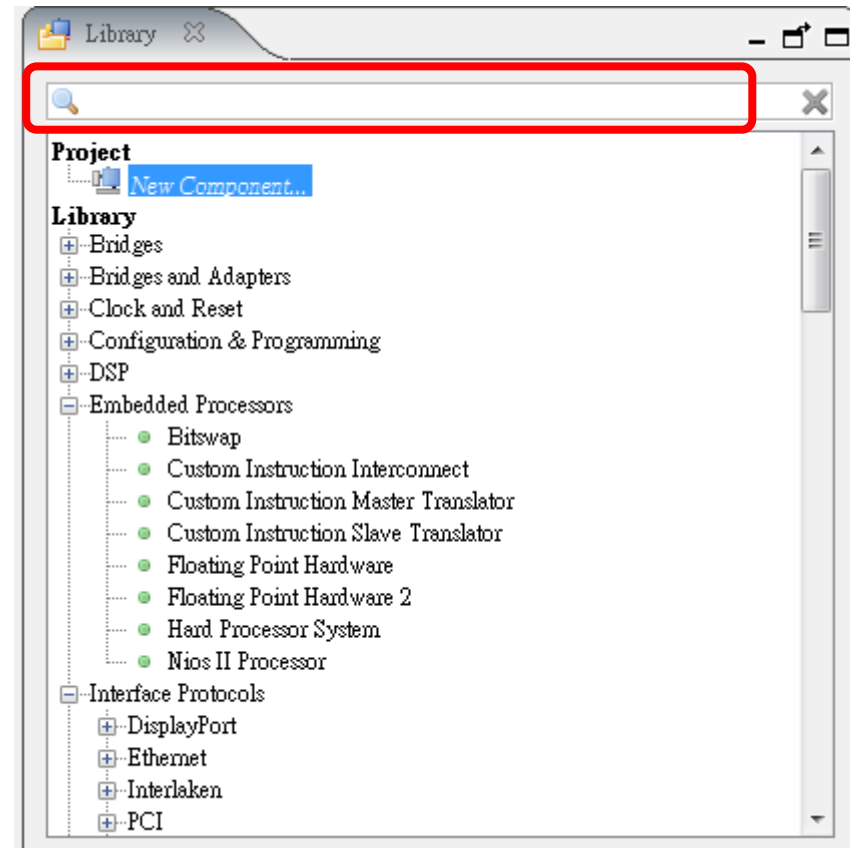


Lab 2 Qsys Tutorial

IPs in this lab

- Altera IPs
 - Avalon ALTPLL
 - UART (RS-232 Serial Port)
- Custom module
 - RSA Avalon-MM master interface module



IP configuration – Avalon ALTPLL

MegaWizard Plug-In Manager [page 1 of 11]

ALTPLL

1 Parameter Settings **2** PLL Reconfiguration **3** Output Clocks **4** EDA

General/Modes > Inputs/Lock > Bandwidth/SS > Clock switchover >

ALTPLL1437830806730229

Clk	Ratio	Ph (dg)	DC (%)
c0	1/1	0.00	50.00

Cyclone IV GX

Currently selected device family: Cyclone IV GX

☒ Match project/default

Able to implement the requested PLL

General

Which device speed grade will you be using? Any

☐ Use military temperature range devices only

What is the frequency of the inclk0 input? 50.0 MHz

☐ Set up PLL in LVDS mode

Data rate: (Not Available) Mbps

PLL Type

Which PLL type will you be using?

☐ Fast PLL ☐ Enhanced PLL ☒ Select the PLL type automatically

Operation Mode

How will the PLL outputs be generated?

☒ Use the feedback path inside the PLL

☒ In normal mode

☐ In source-synchronous compensation Mode

☐ In zero delay buffer mode

☐ Connect the fbmimic port (bidirectional)

☐ With no compensation

☐ Create an 'fbmimic' input for an external feedback (External Feedback Mode)

Which output clock will be compensated for? c0

Cancel < Back Next > Finish

IP configuration – Avalon ALTPLL

MegaWizard Plug-In Manager [page 6 of 11]

ALTPLL

1 Parameter Settings 2 PLL Reconfiguration 3 Output Clocks 4 EDA

clk c0 > clk c1 > clk c2 > clk c3 > clk c4

ALTPLL1437895905829125

inclk0
areset

inclk0 frequency: 50.000 MHz
Operation Mode: Normal

Clk	Ratio	Ph (deg)	DC (%)
c0	4/5	0.00	50.00

c0
locked

Cyclone IV E

c0 - Core/External Output Clock

Able to implement the requested PLL

☒ Use this clock

Clock Tap Settings

☒ Enter output clock frequency:
☐ Enter output clock parameters:

Requested Settings

40.00000000 MHz

Actual Settings

40.000000

1 4

1 5

0.00 deg 0.00

50.00 50.00

Description

Description	Value
Primary clock VCO frequency (MHz)	6...
Modulus for M counter	12

Note: The displayed internal settings of the PLL is recommended for use by advanced users only

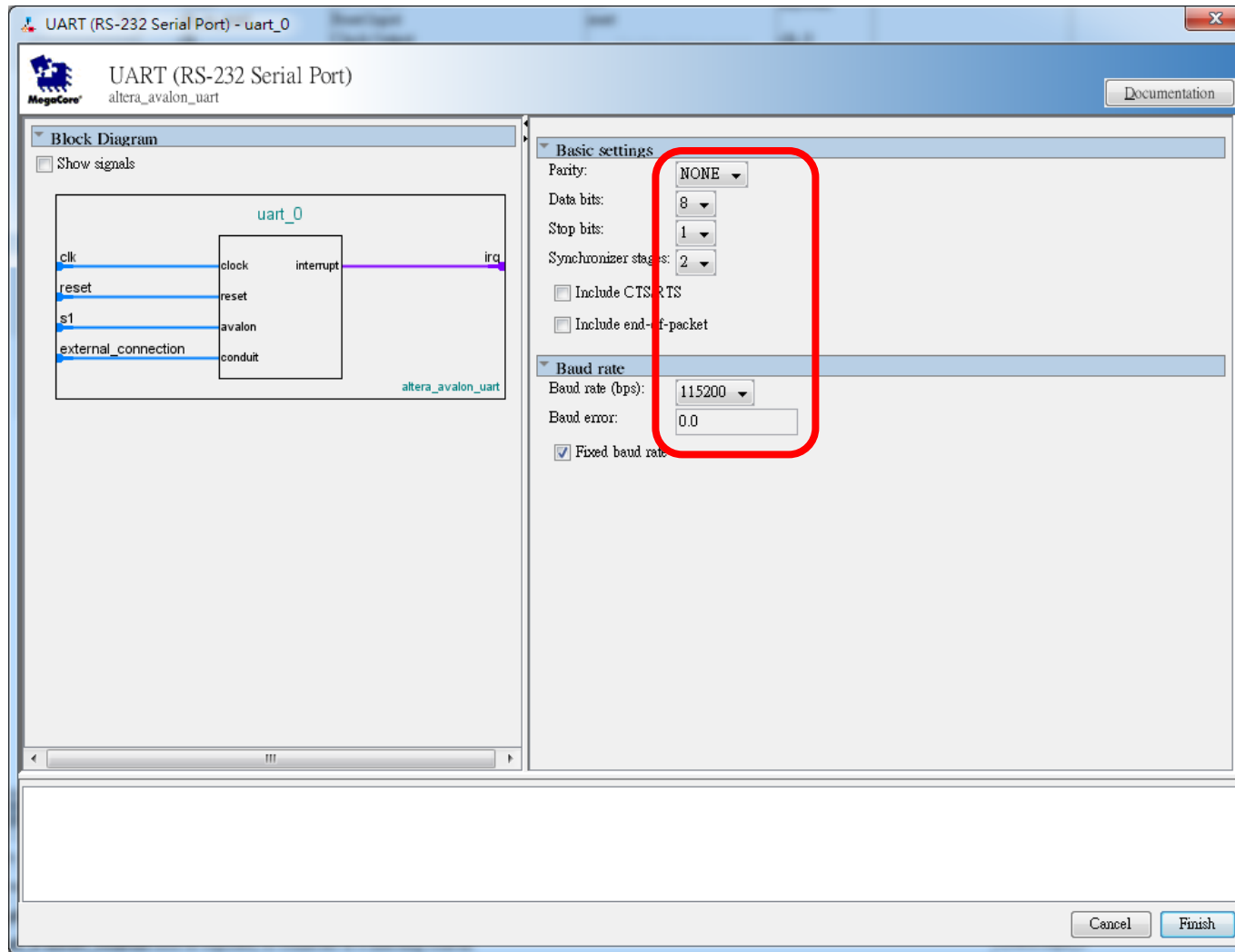
Per Clock Feasibility Indicators

c0 c1 c2 c3 c4

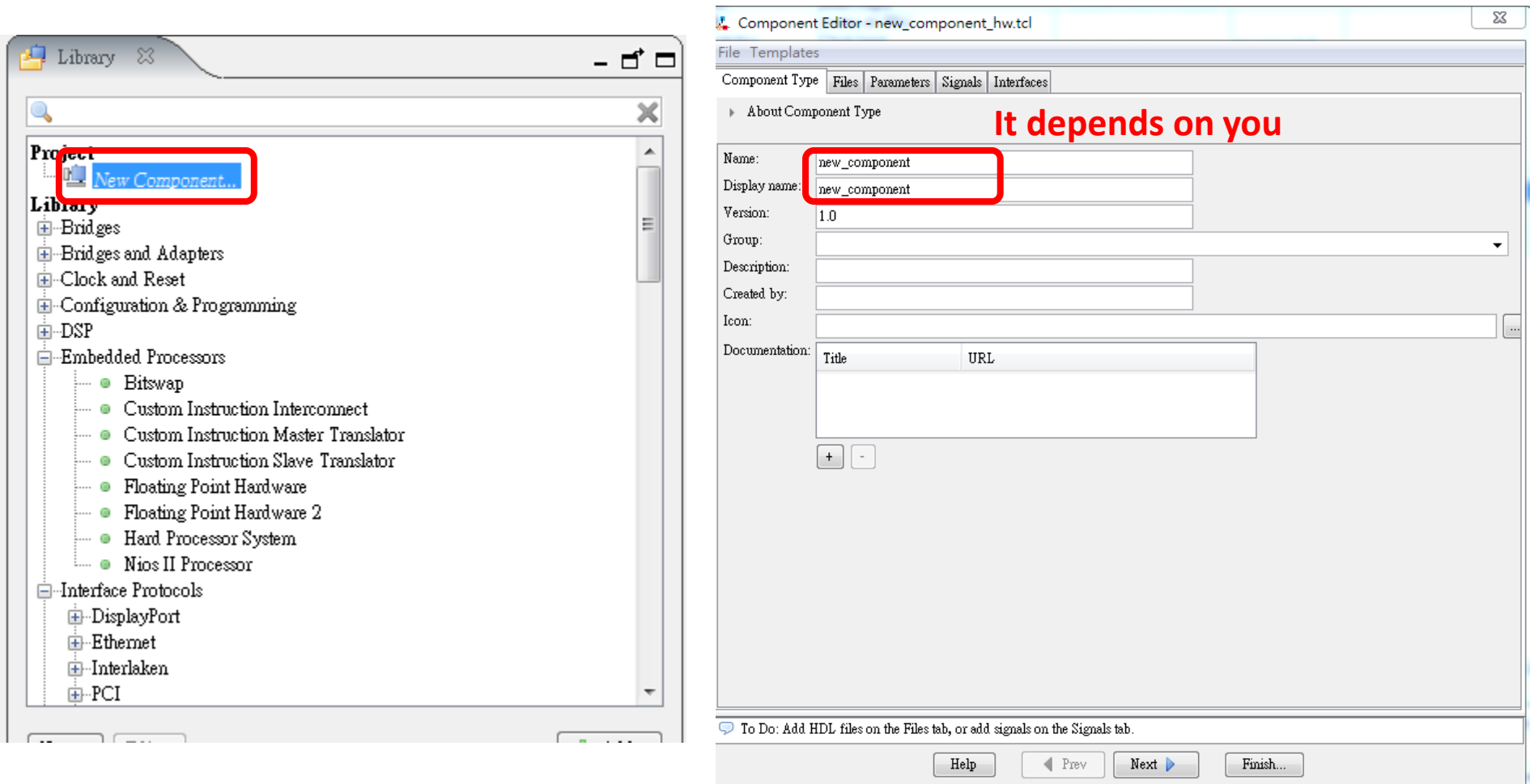
Cancel < Back Next > Finish

System clock depends on your design

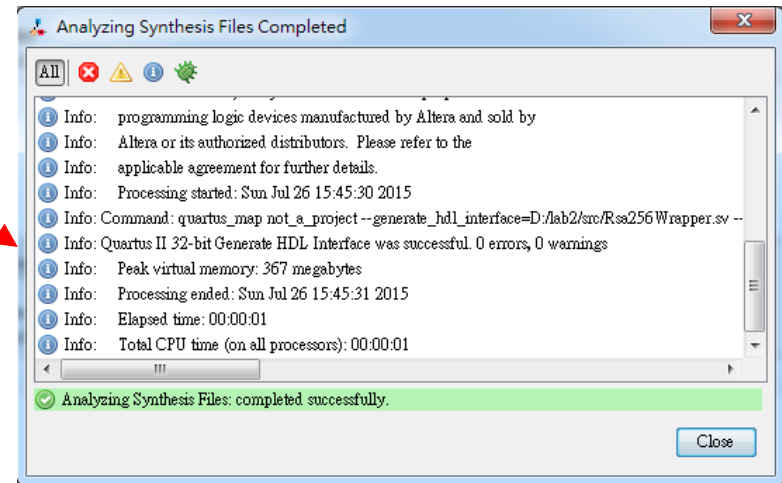
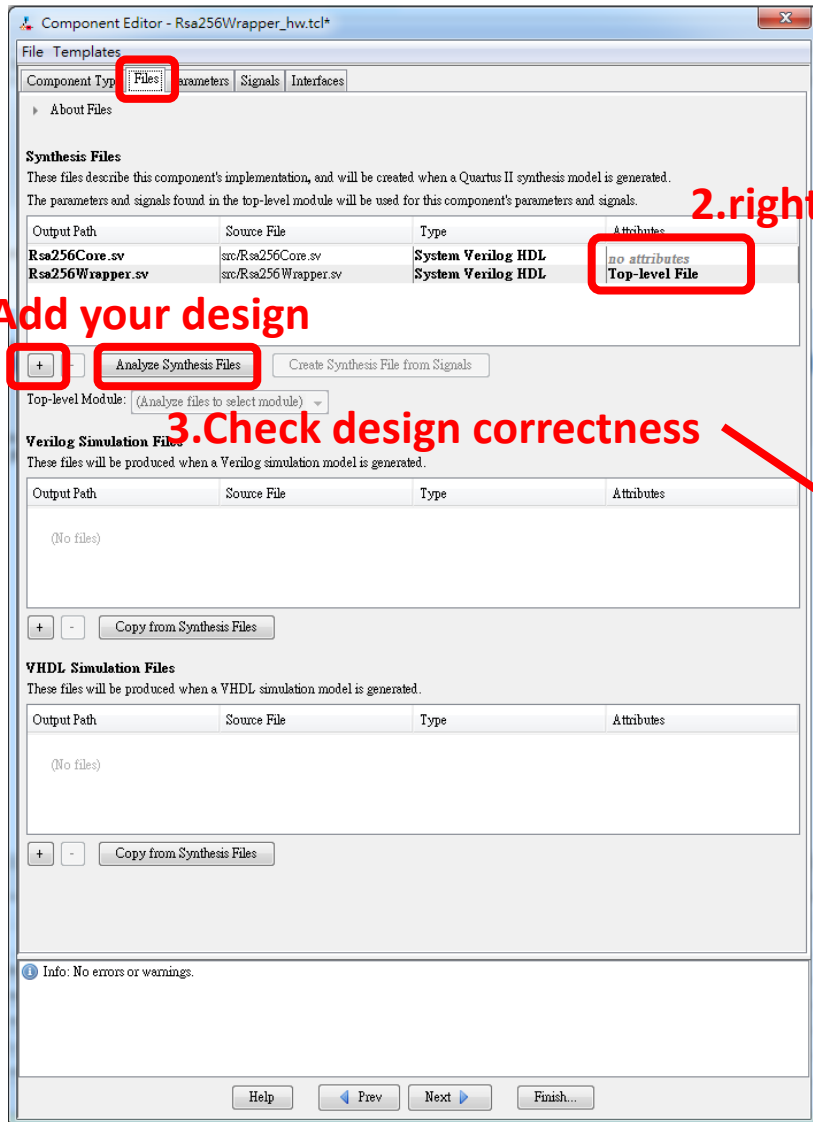
IP configuration – UART (RS232)



Add custom module to Qsys



Add custom module to Qsys



Add custom module to Qsys

Component Editor - new_component_hw.tcl

File Templates

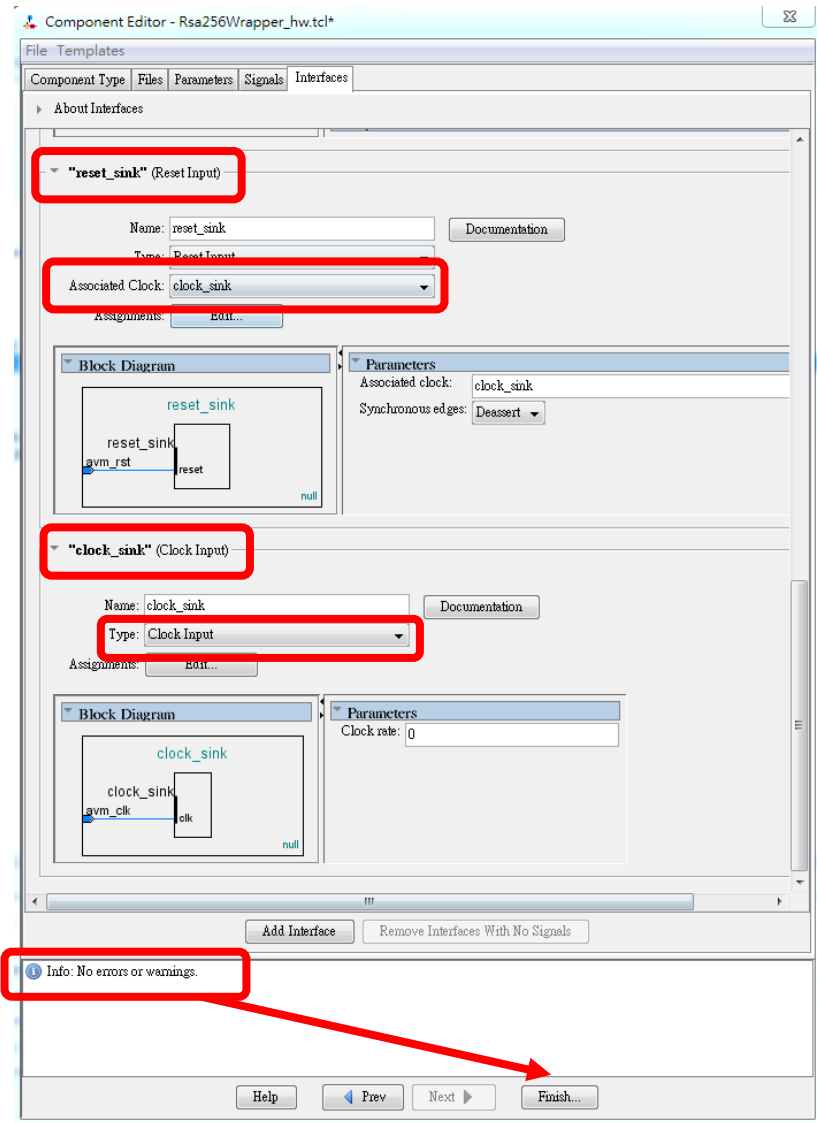
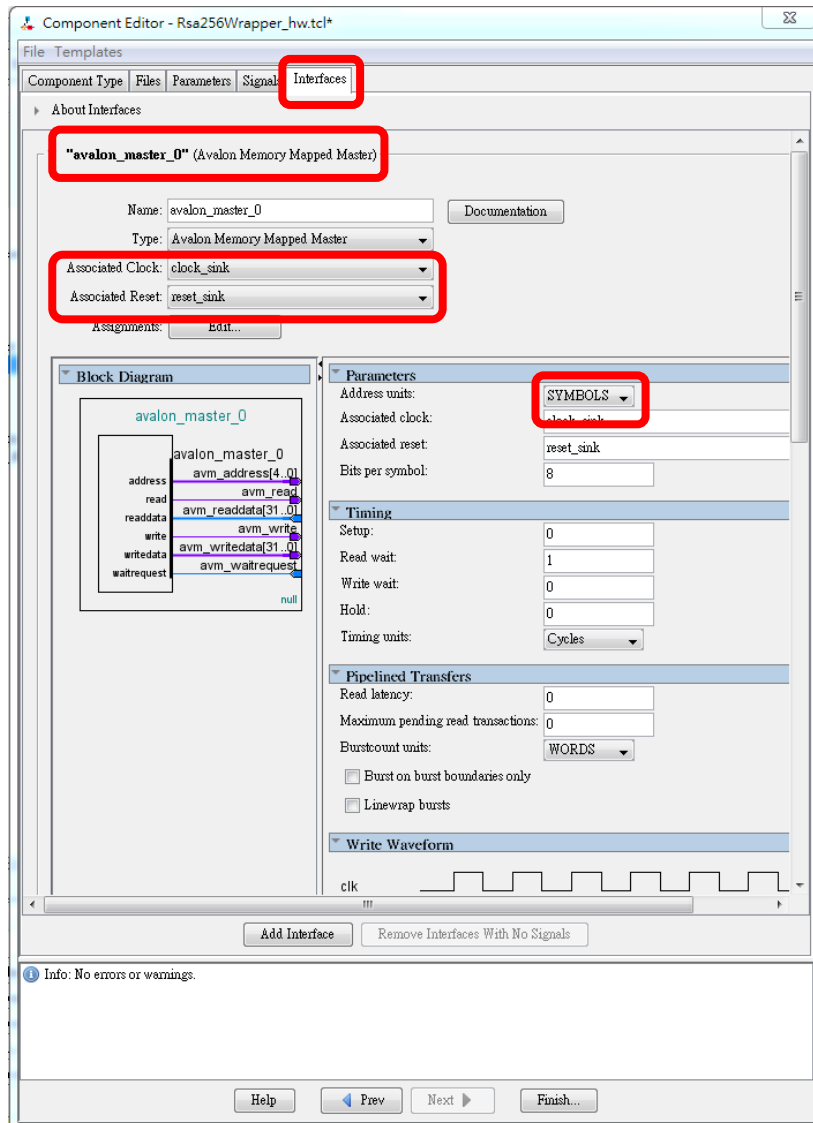
Component Type Files Parameters **Signals** Interfaces

► About Signals

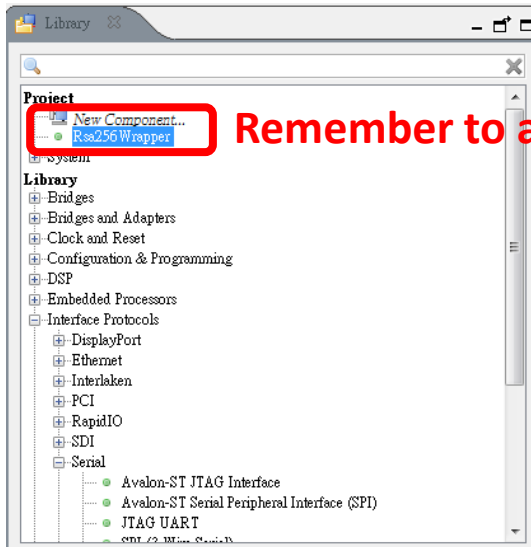
Name	Interface	Signal Type	Width	Direction
avm_rst	reset_sink	reset	1	input
avm_clk	clock_sink	clk	1	input
avm_address	avalon_master_0	address	5	output
avm_read	avalon_master_0	read	1	output
avm_readdata	avalon_master_0	readdata	32	input
avm_write	avalon_master_0	write	1	output
avm_writedata	avalon_master_0	writedata	32	output
avm_waitrequest	avalon_master_0	waitrequest	1	input

Check the interface & signal type are consistent with Avalon-MM master protocol

Add custom module to Qsys



Qsys system & connection



Remember to add your module

Signals here will be in the I/O list of the generated Qsys module

Use	Connections	Name	Description	Export	Clock	Base
<input checked="" type="checkbox"/>		clk_0	Clock Source	clk	exported	
		clk_in	Clock Input	Double-click to export	clk_0	
		clk_in_reset	Reset Input	Double-click to export		
		clk	Clock Output			
		clk_reset	Reset Output			
<input checked="" type="checkbox"/>		altp1l_0	Avalon AL TPLL			
		inclk_interface	Clock Input	Double-click to export	unconnected	
		inclk_interface_reset	Reset Input	Double-click to export	[inclk_interfa...	
		pll_slave	Avalon Memory Mapped Slave	Double-click to export	[inclk_interfa...	
		c0	Clock Output	Double-click to export	altp1l_0_c0	
		areset_conduit	Conduit	Double-click to export		
		locked_conduit	Conduit	Double-click to export		
		phasedone_conduit	Conduit	Double-click to export		
<input checked="" type="checkbox"/>		uart_0	UART (RS-232 Serial Port)			
		clk	Clock Input	Double-click to export	unconnected	
		reset	Reset Input	Double-click to export	[clk]	
		s1	Avalon Memory Mapped Slave	Double-click to export	[clk]	
		external_connection	Conduit	Double-click to export		
<input checked="" type="checkbox"/>		Rsa256Wrapper_0	Rsa256 Wrapper			
		avalon_master_0	Avalon Memory Mapped Master	Double-click to export	[clock_sink]	
		reset_sink	Reset Input	Double-click to export	[clock_sink]	
		clock_sink	Clock Input	Double-click to export	unconnected	

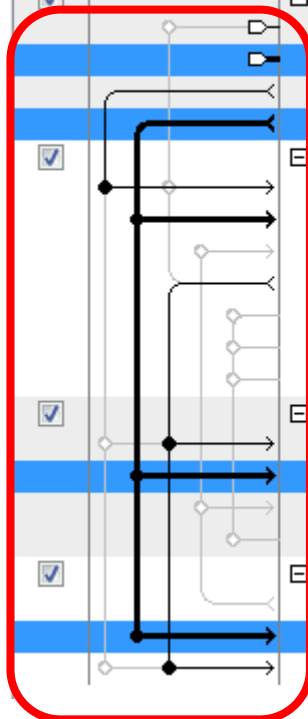
Qsys system & connection

Use	Connections	Name	Description	Export	Clock	Base
<input checked="" type="checkbox"/>		clk_0	Clock Source			
		clk_in	Clock Input	clk	exported	
		clk_in_reset	Reset Input	reset		
		clk	Clock Output	Double-click to export	clk_0	
		clk_reset	Reset Output	Double-click to export		
<input checked="" type="checkbox"/>		altpll_0	Avalon ALTPLL			
		inclock_interface	Clock Input	Double-click to export	clk_0	
		inclock_interface_reset	Reset Input	Double-click to export	[inclock_interfa...	
		pll_slave	Avalon Memory Mapped Slave	Double-click to export	[inclock_interfa...	
		c0	Clock Output	Double-click to export	altpll_0_c0	
		areset_conduit	Conduit	Double-click to export		
		locked_conduit	Conduit	Double-click to export		
		phasedone_conduit	Conduit	Double-click to export		
<input checked="" type="checkbox"/>		uart_0	UART (RS-232 Serial Port)			
		clk	Clock Input	Double-click to export	altpll_0_c0	
		reset	Reset Input	Double-click to export	[clk]	
		s1	Avalon Memory Mapped Slave	Double-click to export	[clk]	
		external_connection	Conduit	Double-click to export		
<input checked="" type="checkbox"/>		Rsa256Wrapper_0	Rsa256 Wrapper			
		avalon_master_0	Avalon Memory Mapped Master	Double-click to export	[clock_sink]	
		reset_sink	Reset Input	Double-click to export	[clock_sink]	
		clock_sink	Clock Input	Double-click to export	altpll_0_c0	

Idea of these connections:

DE2-115 clock (clk_in) is used by altpll to generate the clock (c0) for uart-rs232 & rsa module

Qsys system & connection

Use	Connections	Name	Description	Export	Clock	Base
<input checked="" type="checkbox"/>		clk_0	Clock Source			
		clk_in	Clock Input	clk	exported	
		clk_in_reset	Reset Input	reset		
		clk	Clock Output	Double-click to export	clk_0	
		clk_reset	Reset Output	Double-click to export		
<input checked="" type="checkbox"/>		altpll_0	Avalon AL TPLL			
		inclk_interface	Clock Input	Double-click to export	clk_0	
		inclk_interface_reset	Reset Input	Double-click to export	[inclk_interfa...	
		pll_slave	Avalon Memory Mapped Slave	Double-click to export	[inclk_interfa...	
		c0	Clock Output	Double-click to export	altpll_0_c0	
		areset_conduit	Conduit	Double-click to export		
		locked_conduit	Conduit	Double-click to export		
		phasedone_conduit	Conduit	Double-click to export		
<input checked="" type="checkbox"/>		uart_0	UART (RS-232 Serial Port)			
		clk	Clock Input	Double-click to export	altpll_0_c0	
		reset	Reset Input	Double-click to export	[clk]	
		s1	Avalon Memory Mapped Slave	Double-click to export	[clk]	
		external_connection	Conduit	Double-click to export		
<input checked="" type="checkbox"/>		Rsa256Wrapper_0	Rsa256 Wrapper			
		avalon_master_0	Avalon Memory Mapped Master	Double-click to export	[clock_sink]	
		reset_sink	Reset Input	Double-click to export	[clock_sink]	
		clock_sink	Clock Input	Double-click to export	altpll_0_c0	

Similarly, these connection means the reset signal from DE2-115 works as reset signal for altpll, uart-rs232, and rsa module.

Qsys system & connection

Use	Connections	Name	Description	Export	Clock	B
<input checked="" type="checkbox"/>		clk_0	Clock Source			
		clk_in	Clock Input			
		clk_in_reset	Reset Input			
		clk	Clock Output			
		clk_reset	Reset Output			
<input checked="" type="checkbox"/>		altp11_0	Avalon AL TPLL			
		inclk_interface	Clock Input			
		inclk_interface_reset	Reset Input			
		pll_slave	Avalon Memory Mapped Slave			
		c0	Clock Output			
		areset_conduit	Conduit			
		locked_conduit	Conduit			
		phasedone_conduit	Conduit			
<input checked="" type="checkbox"/>		uart_0	UART (RS-232)			
		clk	Clock Input			
		reset	Reset Input			
		s1	Avalon Memory Mapped Slave			
		external_connection	Conduit			
<input checked="" type="checkbox"/>		Rsa256Wrapper_0	Rsa256 Wrapper			
		avalon_master_0	Avalon Memory Mapped Master			
		reset_sink	Reset Input			
		clock_sink	Clock Input			

Remember to export necessary conduit signals to connect with DE2-115 pins

Master-slave pair in this lab

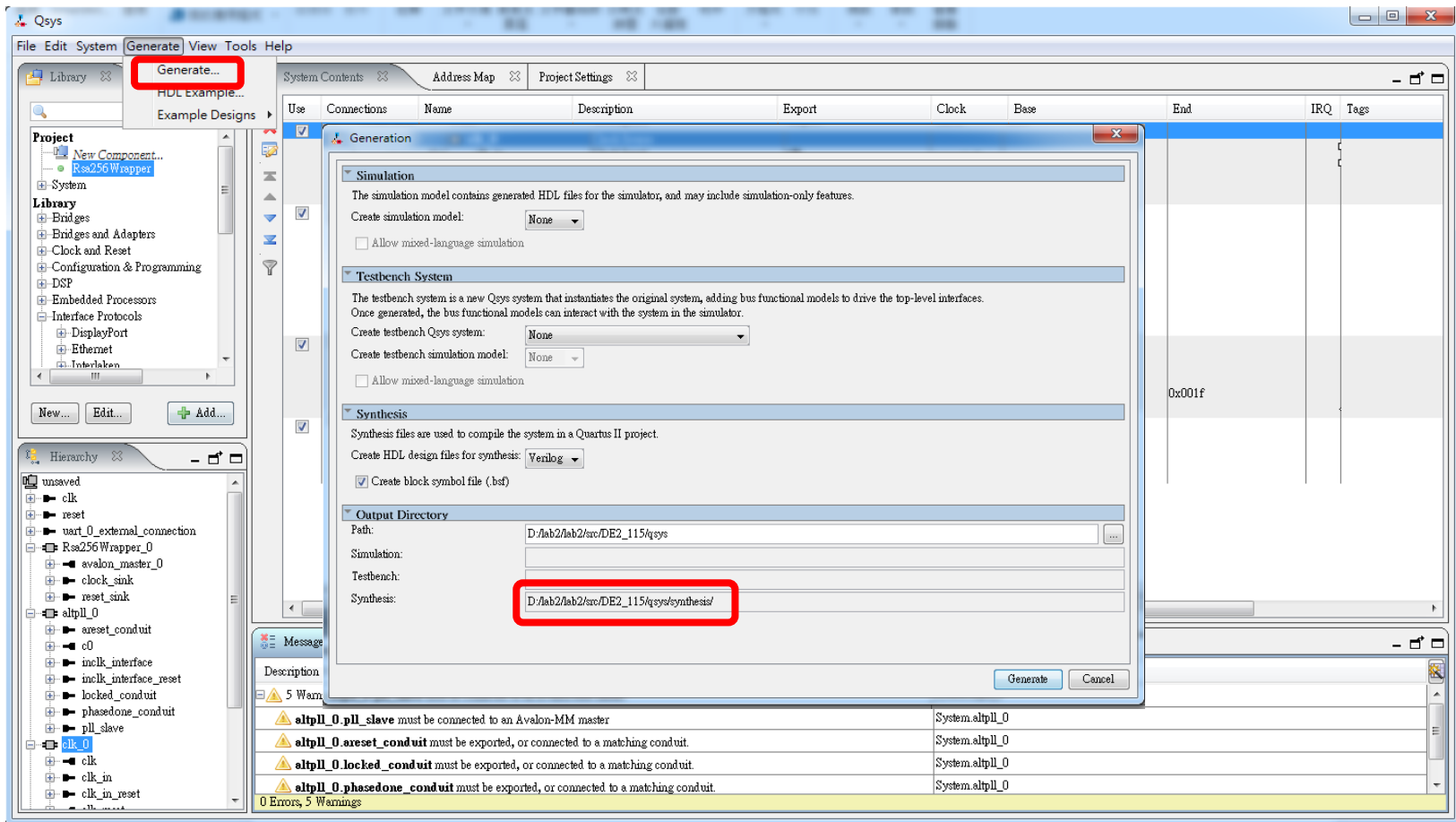
Generate Qsys module

The screenshot shows the Qsys software interface. On the left, the 'System' menu is open, and 'Assign Base Addresses' is highlighted with a red box. A red arrow points from this menu item to the 'Address Map' table. The table has columns: Name, Description, Export, Clock, Base, and End. The row for 'altpll_0_c0' has its 'Base' value '0x0000' highlighted with a red box.

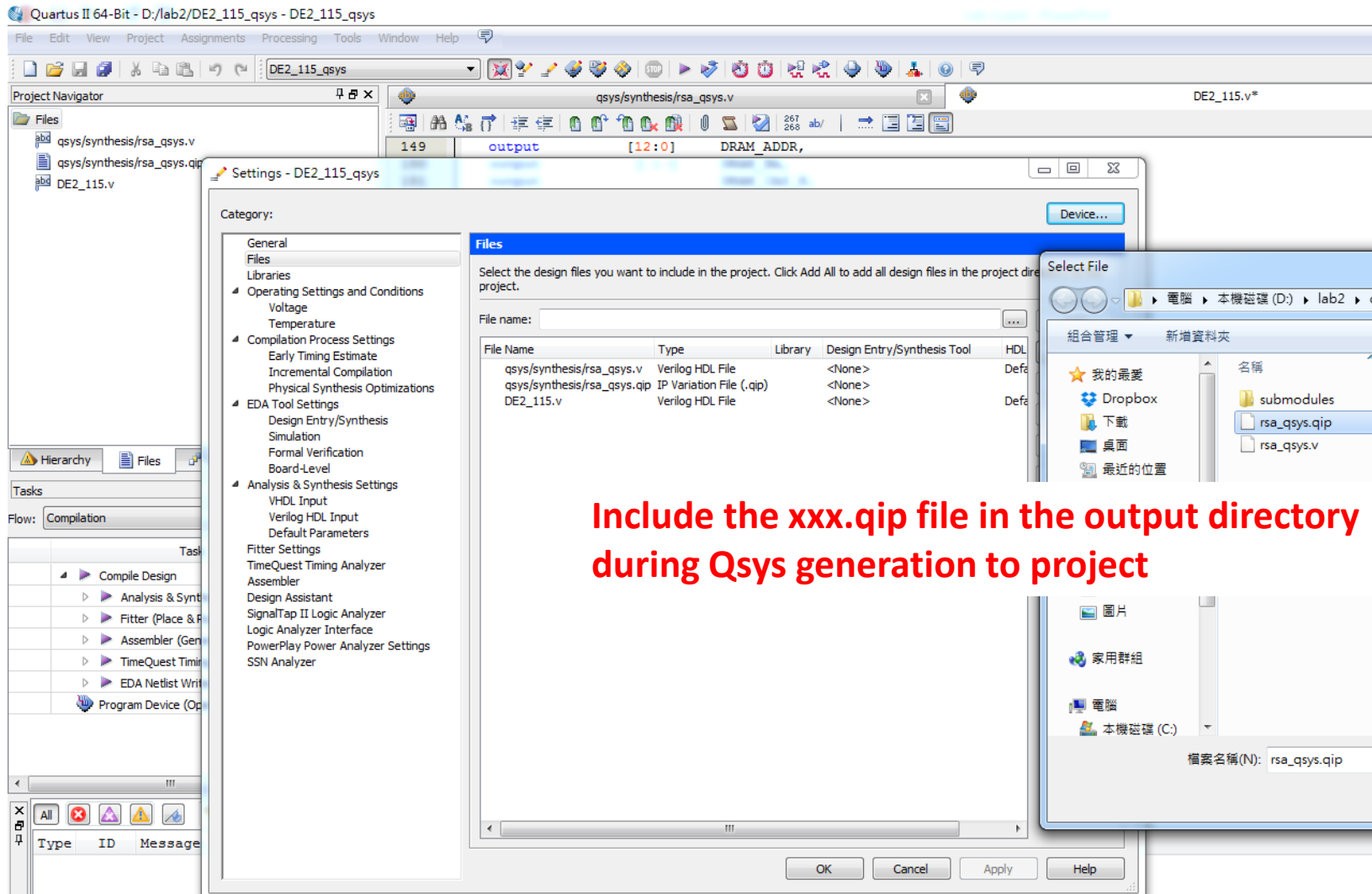
Name	Description	Export	Clock	Base	End
clk_0	Clock Source				
clk_in	Clock Input	clk	exported		
clk_in_reset	Reset Input	reset			
clk	Clock Output	Double-click to export	clk_0		
clk_reset	Reset Output	Double-click to export			
altpll_0	Avalon AL TPLL				
inclnk_interface	Clock Input	Double-click to export	clk_0		
inclnk_interface_reset	Reset Input	Double-click to export	[inclnk_interfa...		
pll_slave	Avalon Memory Mapped Slave	Double-click to export	[inclnk_interfa...		
c0	Clock Output	Double-click to export	altpll_0_c0		
areset_conduit	Conduit	Double-click to export			
locked_conduit	Conduit	Double-click to export			
phasedone_conduit	Conduit	Double-click to export			
uart_0	UART (RS-232 Serial Port)				
clk	Clock Input	Double-click to export	altpll_0_c0	0x0000	0x001f
reset	Reset Input	Double-click to export	[clk]		
s1	Avalon Memory Mapped Slave	Double-click to export	[clk]		
external_connection	Conduit	Double-click to export			
Rsa256Wrapper_0	Rsa256 Wrapper				
avalon_master_0	Avalon Memory Mapped Me				
reset_sink	Reset Input				
clock_sink	Clock Input				

MM slave will be assigned with address

Generate Qsys module



Include generated Qsys module



Instantiate Qsys module

- Finally, remember to instantiate the generate Qsys module.
 - For the module I/O, refer to xxx.v in the same directory of xxx.qip

```
`timescale 1 ps / 1 ps
module rsa_qsys (
    input wire clk_clk,           // clk.clk
    input wire reset_reset_n,     // reset.reset n
    input wire uart_0_external_connection_rxd, // uart_0_external_connection.rxd
    output wire uart_0_external_connection_txd // .txd
);
```

Use	Connections	Name	Description	Export	Clock
<input checked="" type="checkbox"/>		clk_0	Clock Source		
		clk_in	Clock Input	clk	export
		clk_in_reset	Reset Input	reset	
		clk	Clock Output	Double-click to export	clk_0
		clk_reset	Reset Output	Double-click to export	
<input checked="" type="checkbox"/>		altpll_0	Avalon ALTPLL		
		incclk_interface	Clock Input	Double-click to export	clk_0
		incclk_interface_reset	Reset Input	Double-click to export	incclk_i
		pll_slave	Avalon Memory Mapped Slave	Double-click to export	incclk_j
		c0	Clock Output	Double-click to export	altpll_0
		areset_conduit	Conduit	Double-click to export	
		locked_conduit	Conduit	Double-click to export	
		phasedone_conduit	Conduit	Double-click to export	
<input checked="" type="checkbox"/>		uart_0	UART (RS-232 Serial Port)		
		clk	Clock Input	Double-click to export	altpll_0
		reset	Reset Input	Double-click to export	clk
		sl	Avalon Memory Mapped Slave	Double-click to export	clk
		external_connection	Conduit	Double-click to export	uart_0_external_connec...
<input checked="" type="checkbox"/>		Rsa256Wrapper_0	Rsa256 Wrapper		
		avalon_master_0	Avalon Memory Mapped Master	Double-click to export	clock
		reset_sink	Reset Input	Double-click to export	clock
		clock_sink	Clock Input	Double-click to export	altpll_0

Generated module I/O should be the same as Exported signals in Qsys