

Chapter 10

Power/Clock Distribution, IO, and Packaging



關志達

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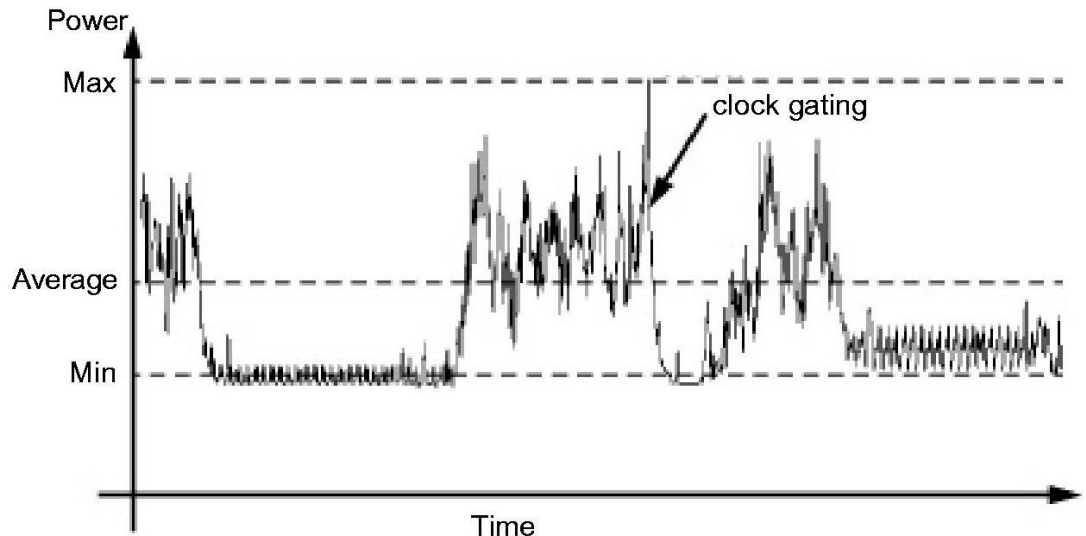


Power Distribution

- Power Distribution Network functions
 - Carry current from pads to transistors on chip
 - Maintain stable voltage with low noise
 - Provide average and peak power demands
 - Provide current return paths for signals
 - Avoid electromigration & self-heating wearout
 - Consume little chip area and wire
 - Easy to lay out

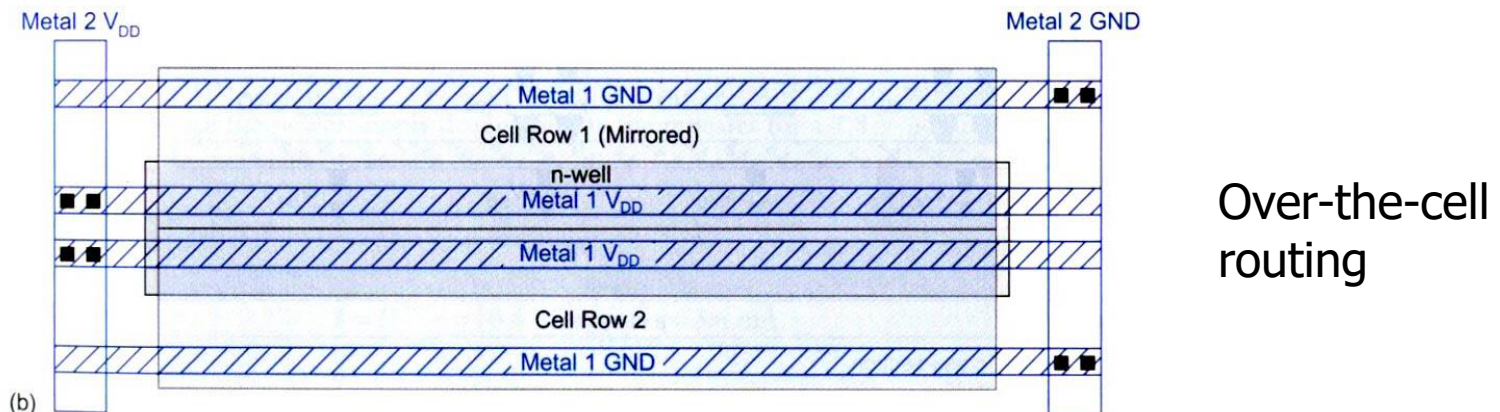
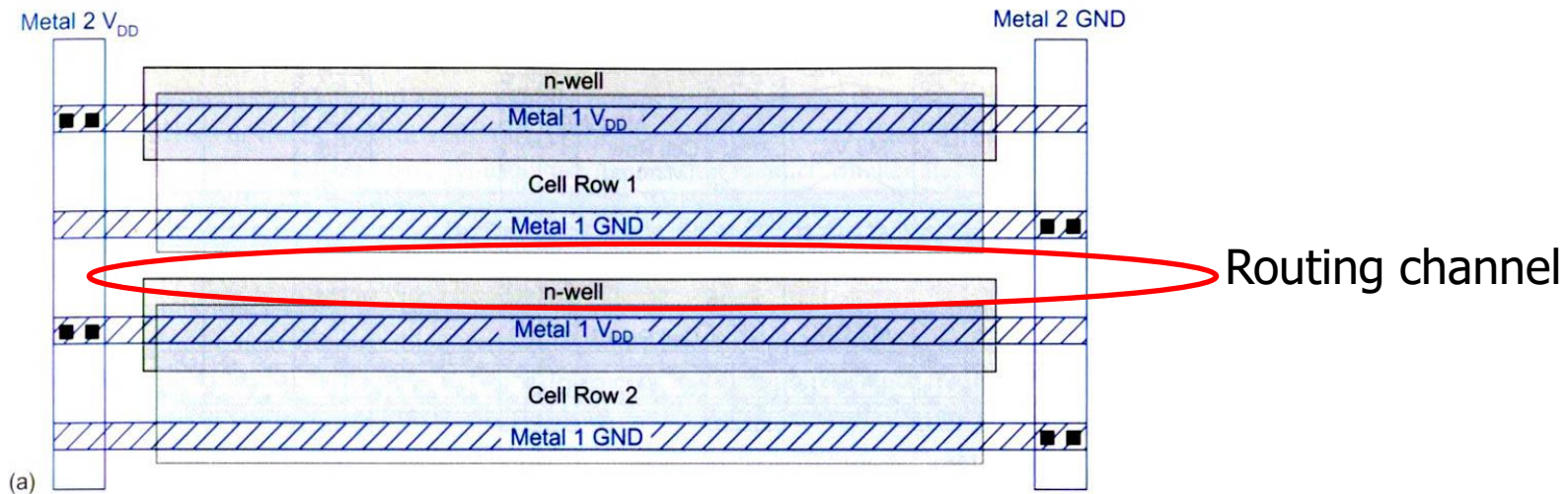
Power Requirements

- $V_{DD} = V_{DDnominal} - V_{droop}$
- Want $V_{droop} < +/- 10\%$ of V_{DD}
- Sources of V_{droop}
 - IR drops
 - di/dt noise
- I_{DD} changes drastically



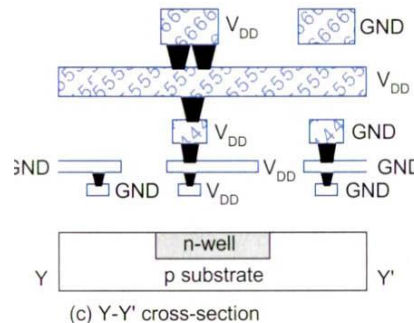
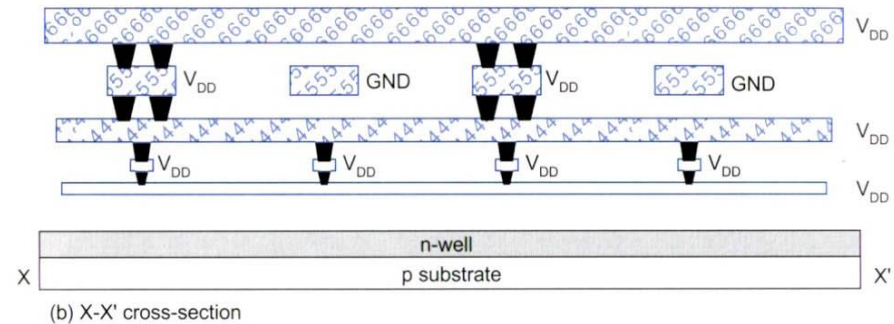
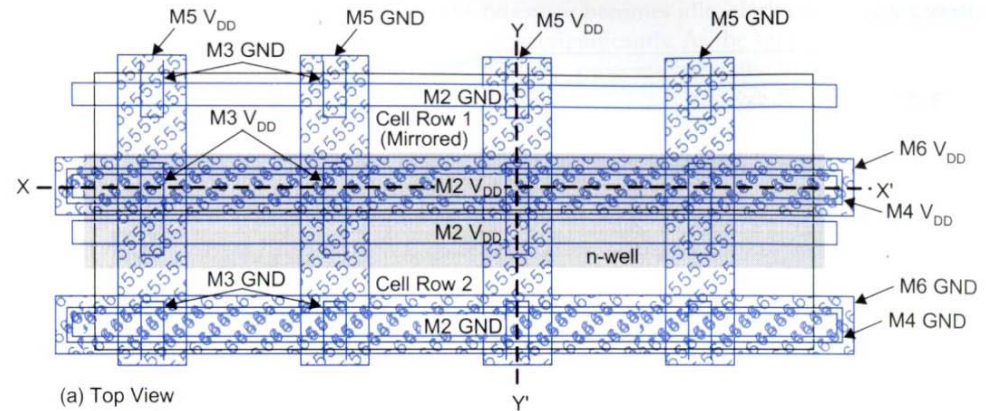
Power Distribution Network

- Network for standard-cell design



Power Distribution Network

- Network for high-power IC
 - Use grid of top-level metal to reduce resistance.
 - Plenty of vias to carry large current.





IR Drop and Ldi/dt

- IR Drop

- When a large current flow through non-zero-resistance power/ground lines, there will be voltage drop due to Ohm's law.

- Ldi/dt noise

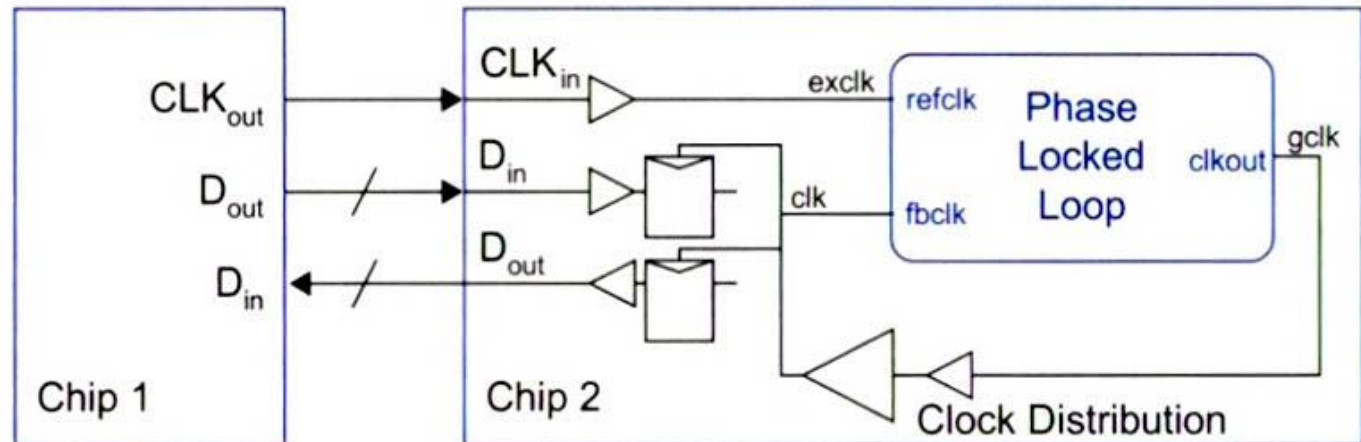
- Wires (especially bonding wires) have inherent inductance and with change of current magnitude along the wires, there will be Ldi/dt voltage drop across the wires.

- Remedy

- On-chip bypass capacitance can reduce the need to go through long wires for local current needs and thus reduces IR drop and Ldi/dt effects.

Clock Generation

- Receive an external clock signal and generate a global clock to be distributed to all sequencing elements and memory.
- Simplest design will be a big buffer.
- Nowadays, many different version/phase/frequency of clock signals are needed in a complicated IC.
- Use PLL to generate clock signals with different phase and frequency.



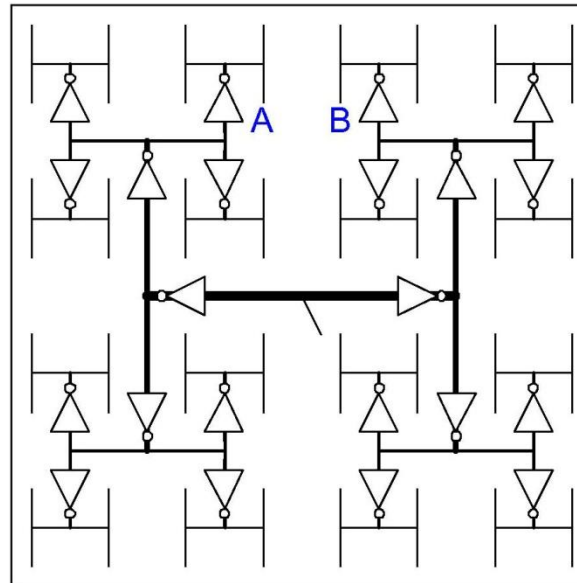


Clock Distribution -- Grid

- Use grid on two or more levels to carry clock (similar to power grid)
- Make wires wide to reduce RC delay
- Ensures low skew between nearby points
- But possibly large skew across die

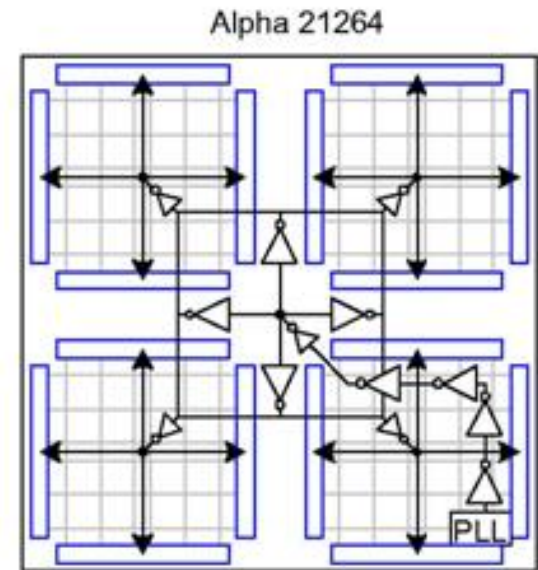
Clock Distribution – H-Tree

- Fractal structure
 - Gets clock arbitrarily close to any point
 - Matched delay along all paths
- Delay variations cause skew
- A and B might see big skew though they are very close. This is due to non-uniform clock loading.



Clock Distribution – Hybrid

- Use H-tree to distribute clock to many points
- Tie these points together with a grid
- Ex: IBM Power4, PowerPC, Alpha
 - H-tree drives 16-64 sector buffers
 - Buffers drive total of 1024 points
 - All points shorted together with grid





Summary on Clock Signal

- Clock is a very sensitive signal. It must be delivered to all registers without distortion in waveform or too much delay skew.
- Clock drivers are needed for driving large load. Actually, drivers are needed to drive all signals with large load, e.g. RESET signal.
- Gated clock is often used to reduce circuit activity and thus power consumption. Make sure that proper gated clock waveform is provided.
- Never use outputs of some complex combinational circuits as clock for some registers (hazard of glitches and spurious switching)



Chip Inputs/Outputs

- Input/Output System functions
 - Communicate between chip and external world
 - Drive large capacitance off chip
 - Operate at compatible voltage levels
 - Provide adequate bandwidth
 - Limit slew rates to control di/dt noise
 - Protect chip against electrostatic discharge
 - Use small number of pins (low cost)



I/O Pad Design

- Pad types
 - V_{DD} / GND
 - Output
 - Input
 - Bidirectional
 - Analog

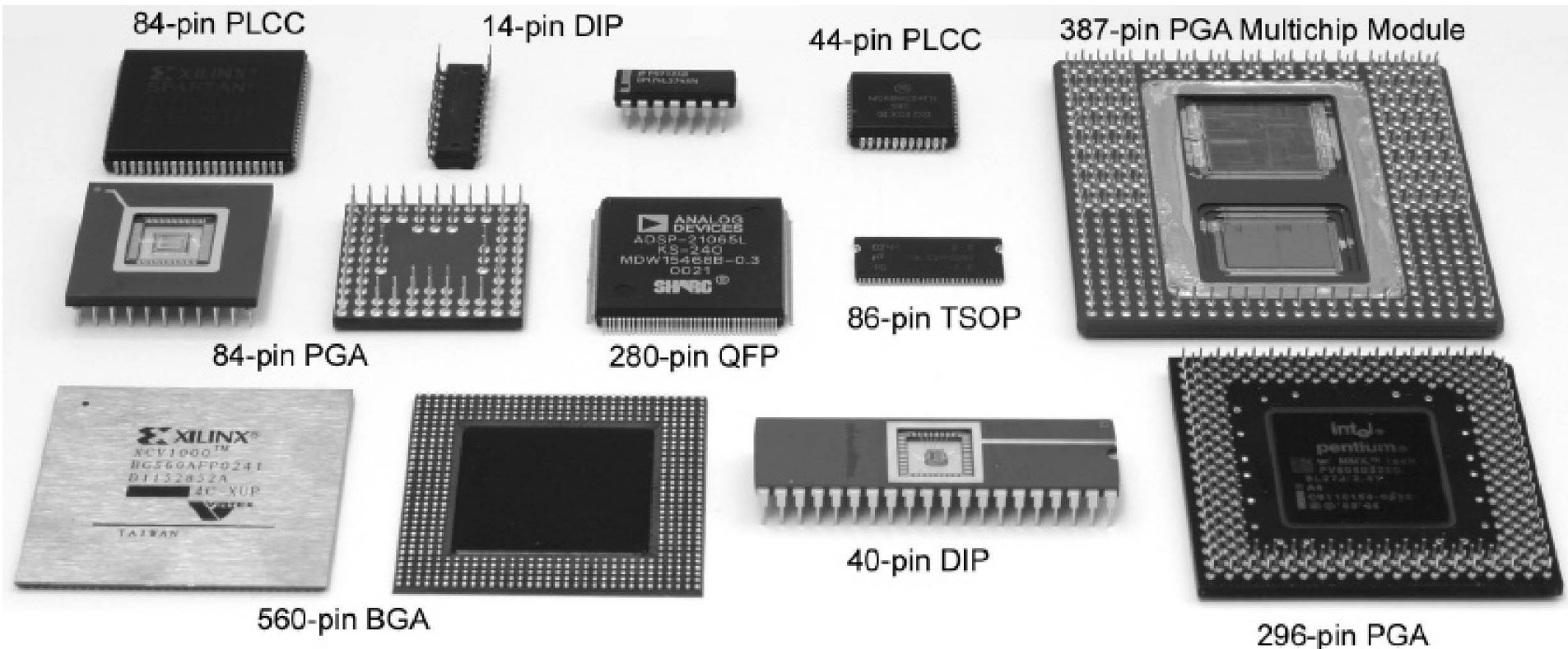


Packages

- Package functions
 - Electrical connection of signals and power from chip to board
 - Little delay or distortion
 - Mechanical connection of chip to board
 - Removes heat produced on chip
 - Protects chip from mechanical damage
 - Compatible with thermal expansion
 - Inexpensive to manufacture and test

Package Types

- Through-hole vs. surface mount



Multi-chip Modules (MCM)

- a. k. a. System in Package (SiP)
- CPU MCM
 - Fast connection of CPU to cache
 - Expensive, requires known good dice

