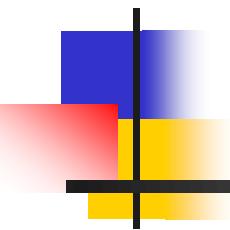


Chapter 0

IC 科技：



始終為了人類

台大電機系

闕志達

2019. Sep.

IC時代以前

- 汽車電話



- 野戰電話



IC時代以前

■ 按鍵式電話

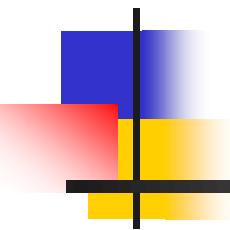


2006 3 16

後IC時代

■ iPhone 11

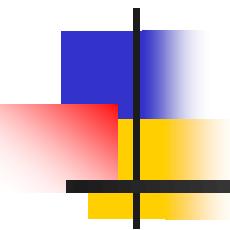




不只是手機

電視





甚至是最酷的玩意兒

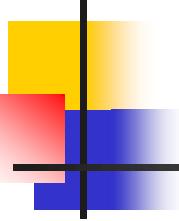
空拍機

■ 幻影3 (phantom 3)



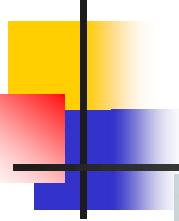
擊敗棋王的AlphaGO





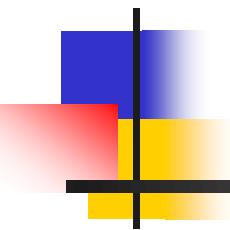
3D印表機





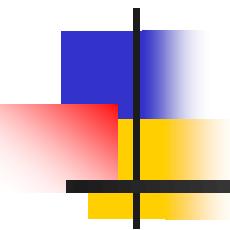
自駕車





都拜IC之賜！

讓我們來看看這些
東東裡面長什麼樣？



拆解 iPhone X

電路板

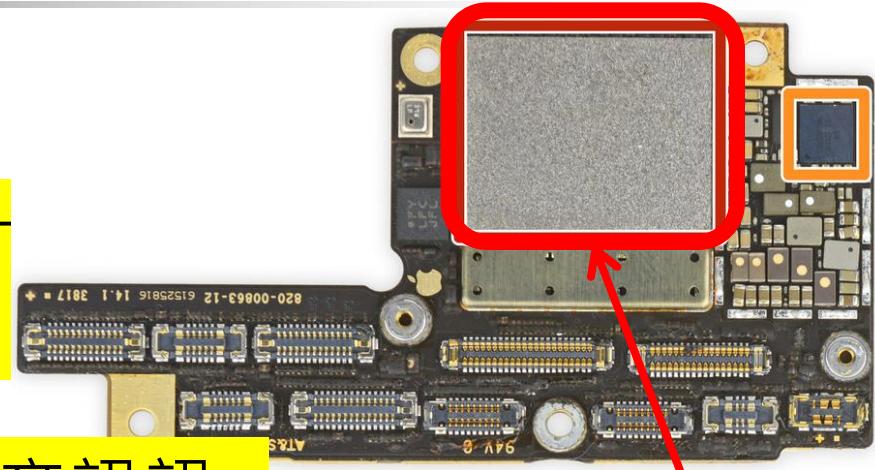
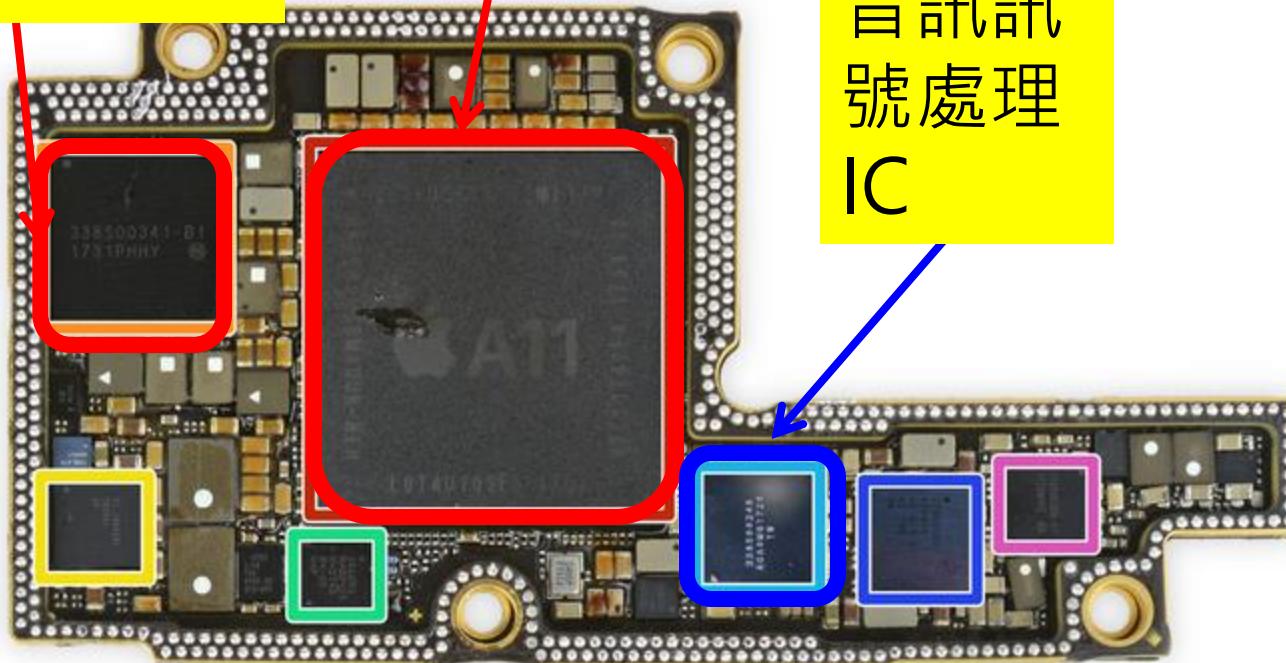


iPhone X
拆解圖

iPhone X 電路板正面

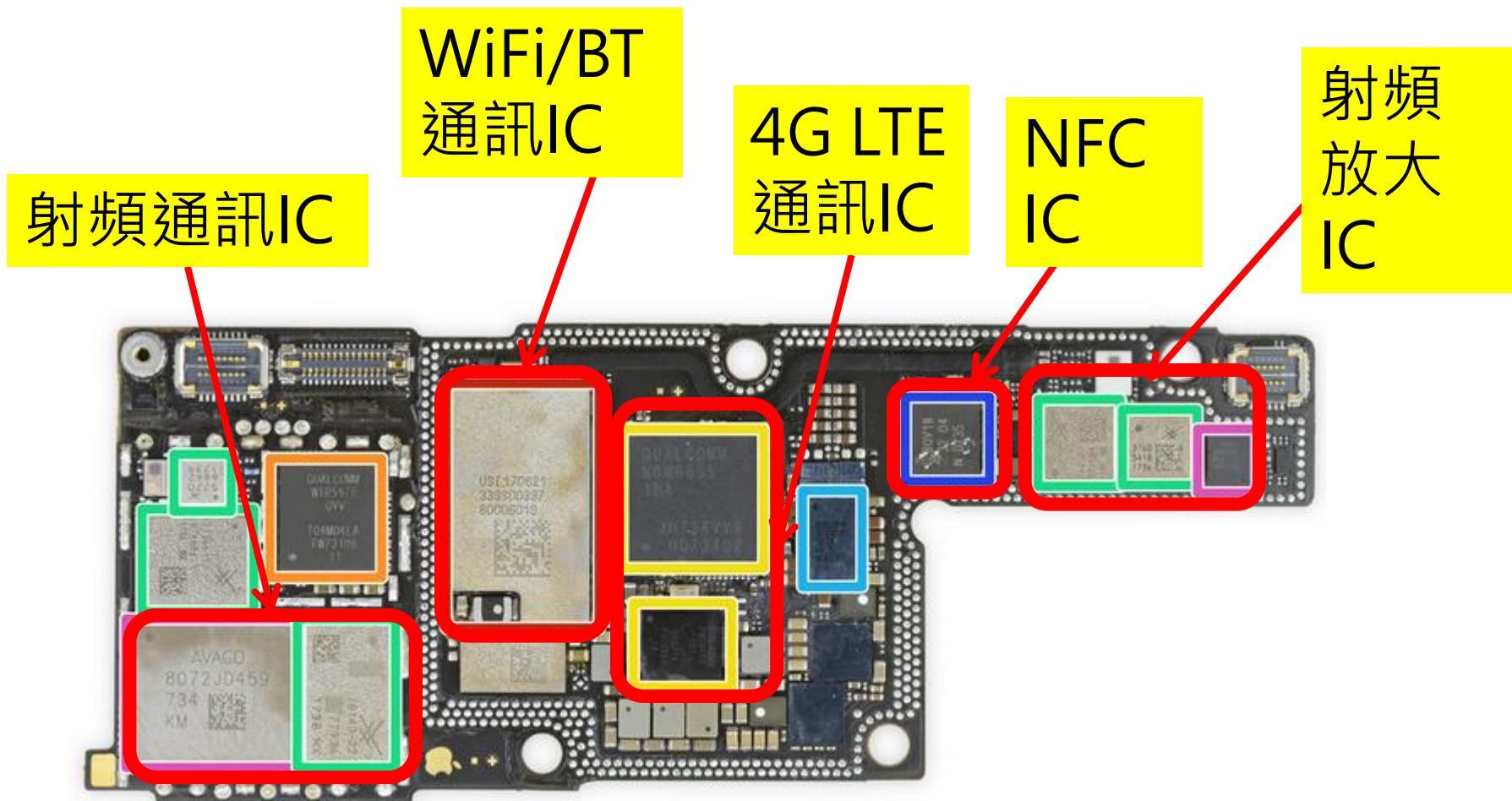
電源管理
晶片

Apple 自行設計
發之CPU, A11



64GB
NAND
Flash

iPhone X 電路板反面



拆解 無人機 AR.Drone 2

電路板

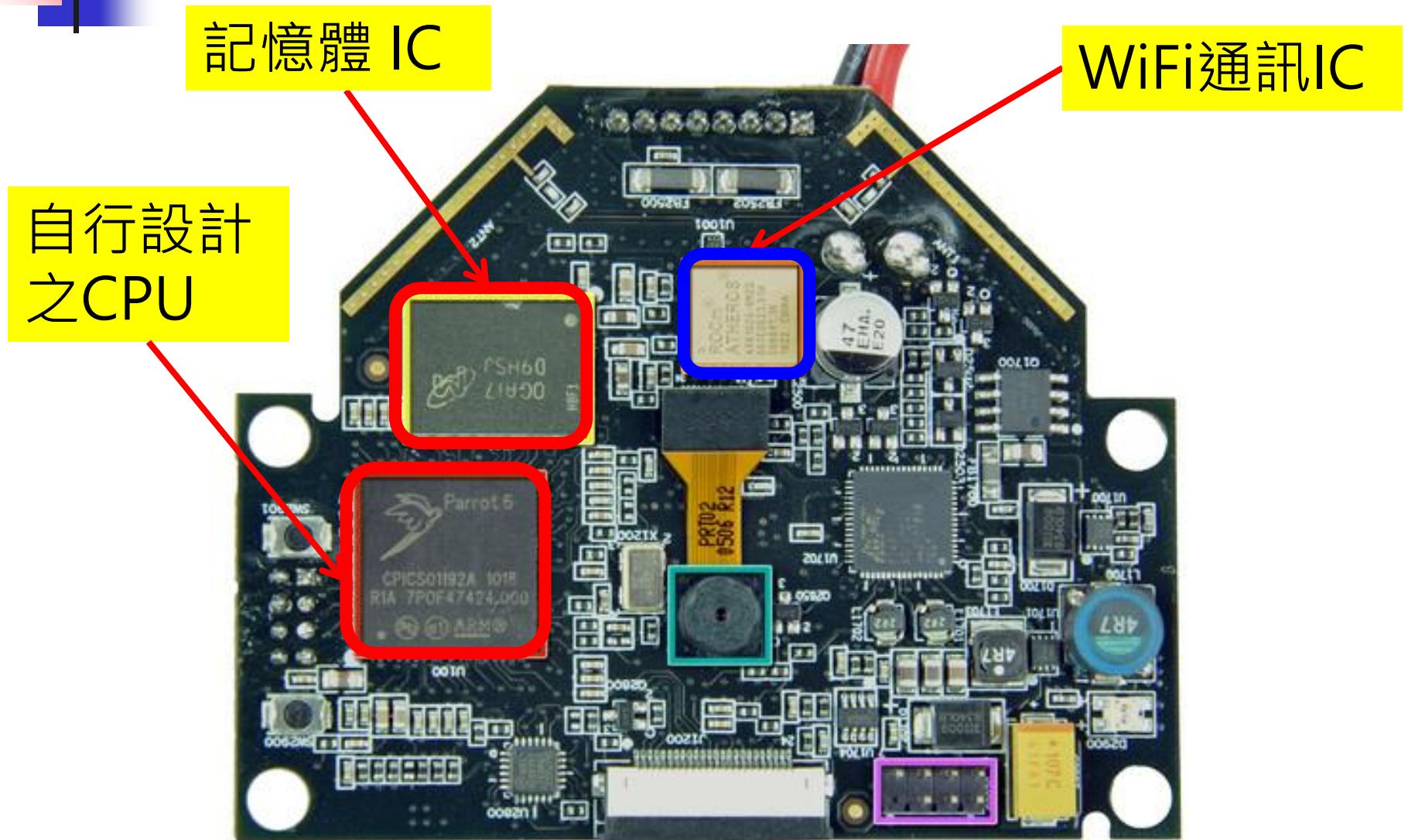


拆解 無人機 AR.Drone 2

控制電路板



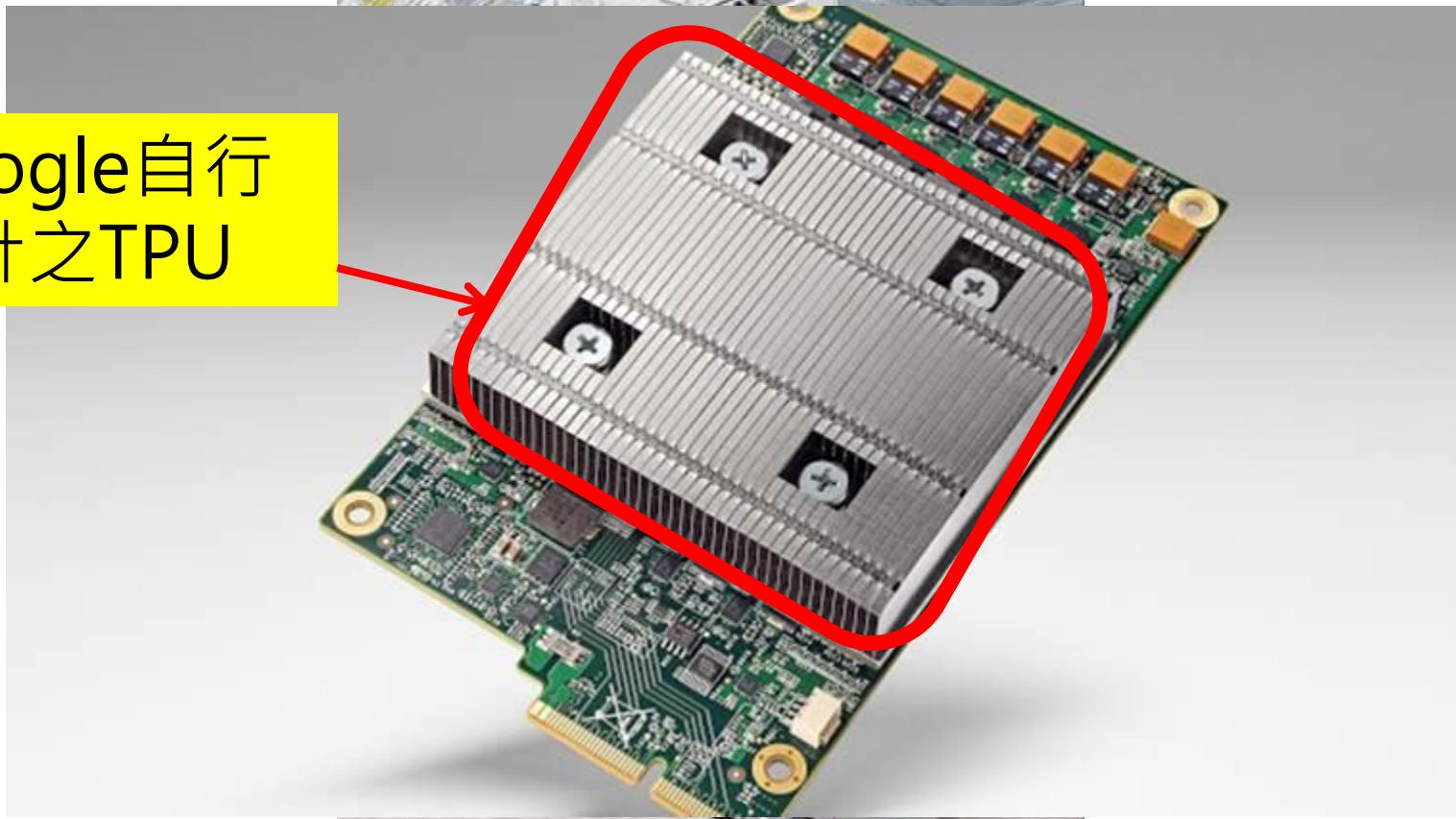
主控電路板正面

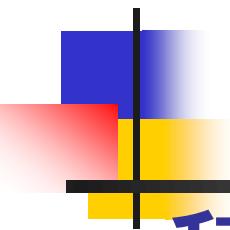


AlphaGO 所使用的人工智慧電腦



Google自行
設計之TPU





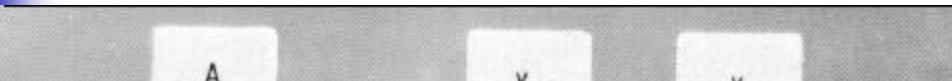
積體電路(Integrated Circuits)直
接促成過去數十年電子產品爆
炸性成長

電晶體的發明



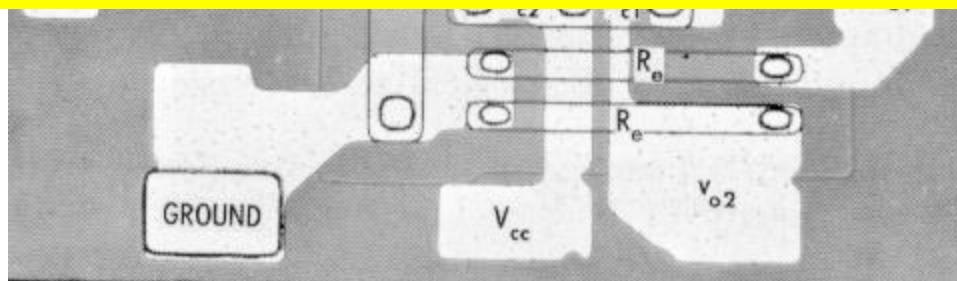
1956諾貝爾物理獎 · Shockley,
Bardeen, Brattain
"for their researches on
semiconductors and their
discovery of the transistor effect"

第一個積體電路(IC)



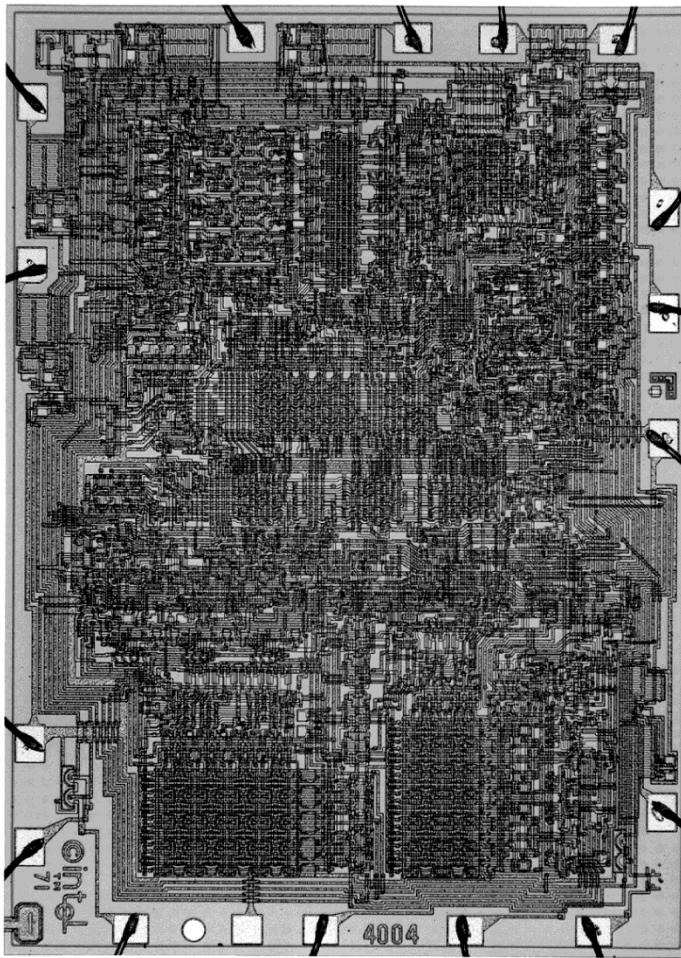
諾貝爾物理獎 2000 Jack Kilby

"for his part in the invention of the
integrated circuit"



ECL 3-input Gate
Motorola 1966

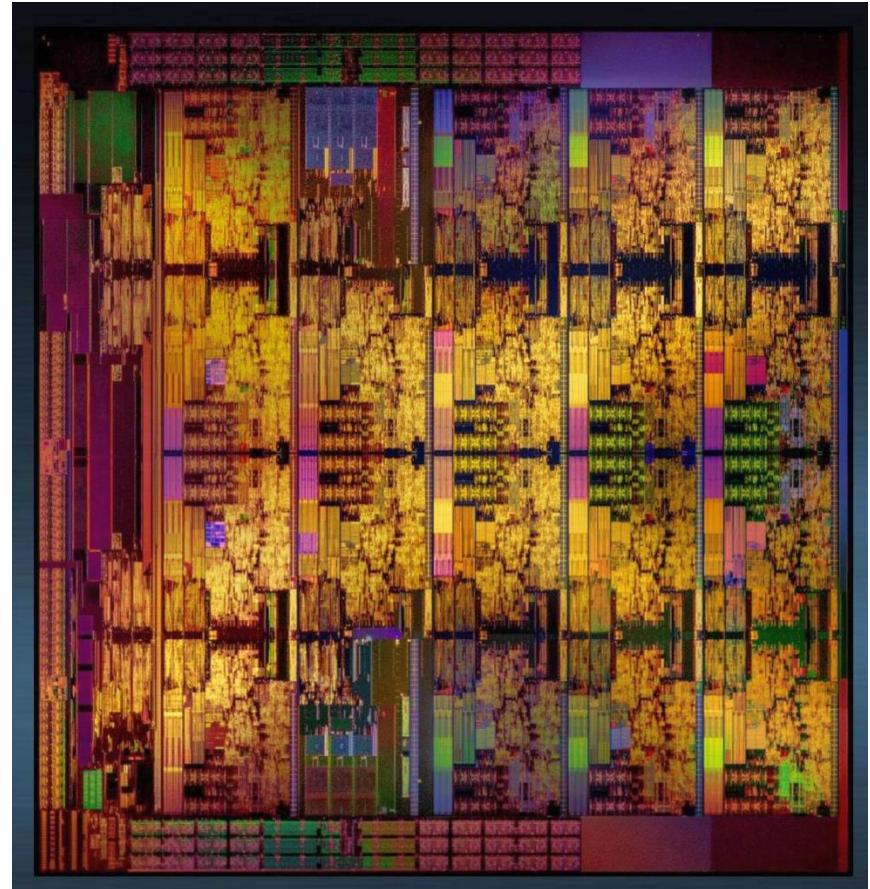
Intel 4004 微處理器 (1971)



1000 電晶體
1 MHz 操作速度

Intel 十八核微處理器 (2017)

- 2017, Xeon W-2195 Skylake
- >50億電晶體, 14奈米製程, 晶片面積 484 mm^2 , 時脈速度 2.3GHz , 43MB 記憶體.
- 十八核心



不只是電腦內的微處理器

1536M
2017

全球歷年手機銷售量

Worldwide Cellular Market
(Phones Shipped)

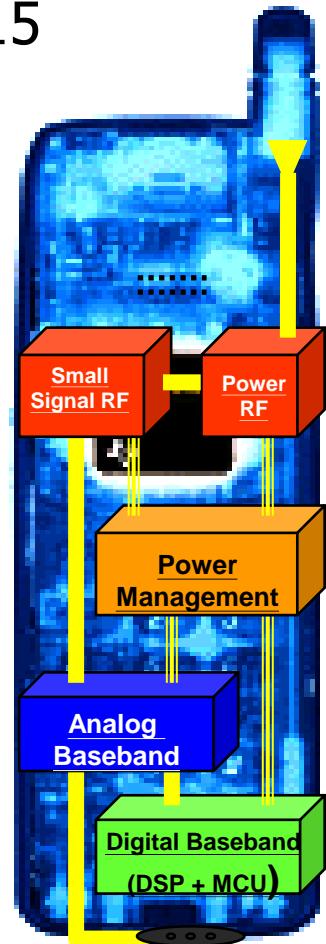


Source: IDC Worldwide Mobile Phone Tracker, Jan. 27, 2014.

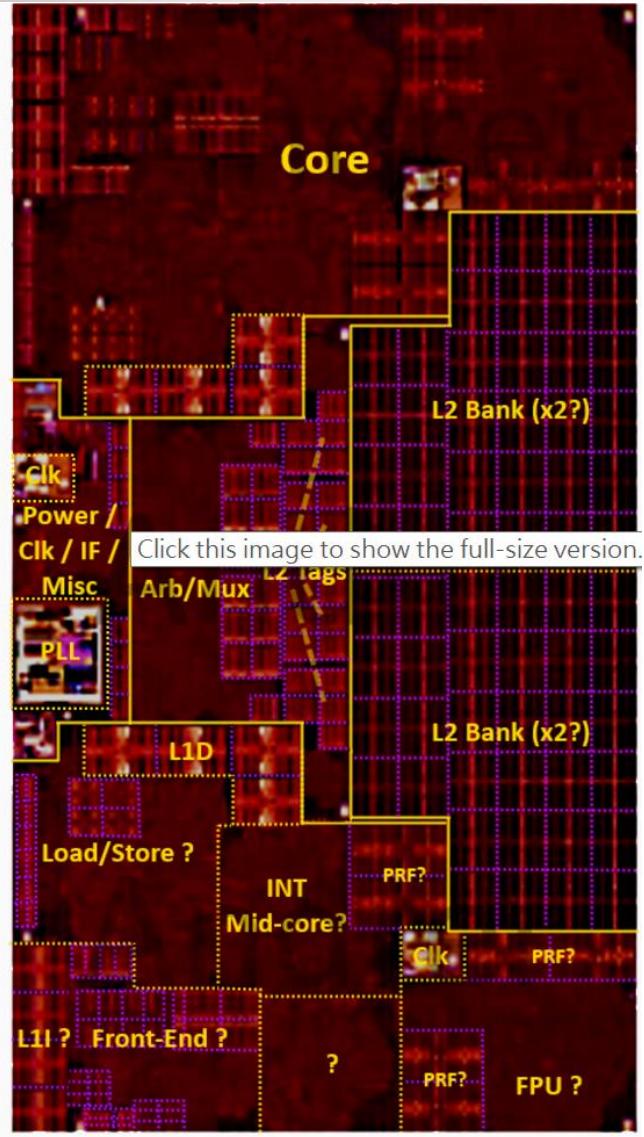
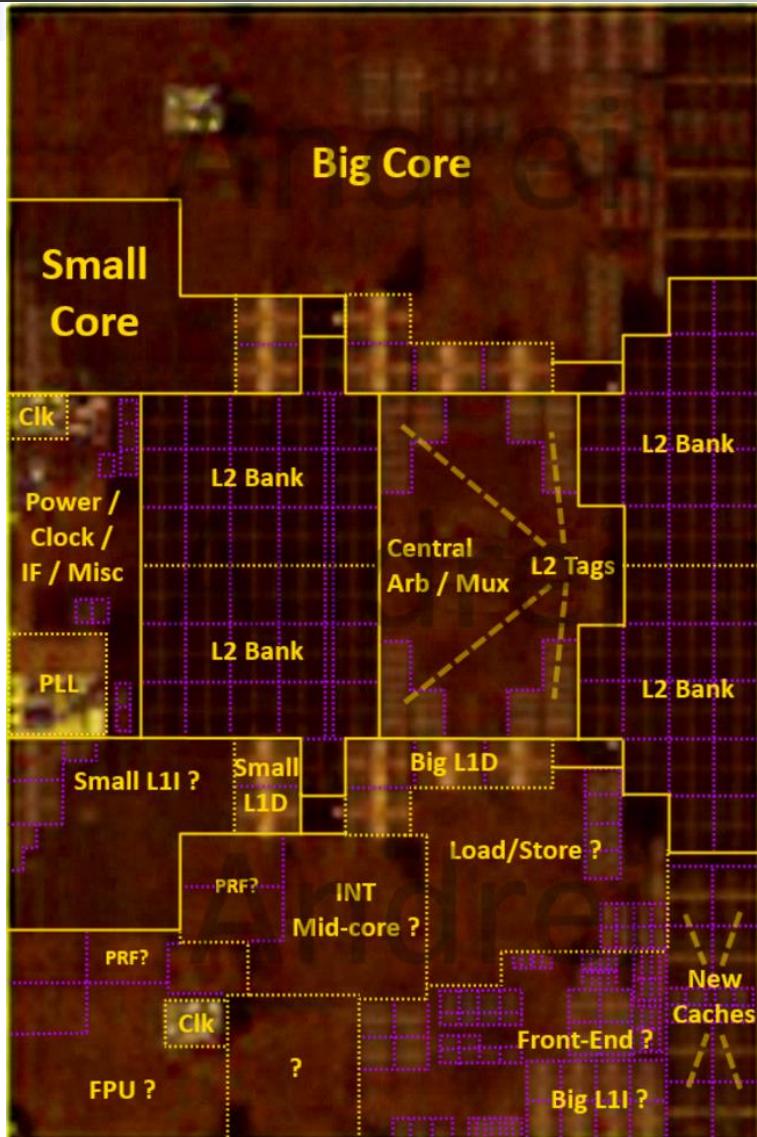
1423M
2015

1244M
2014

1004M
smartphones

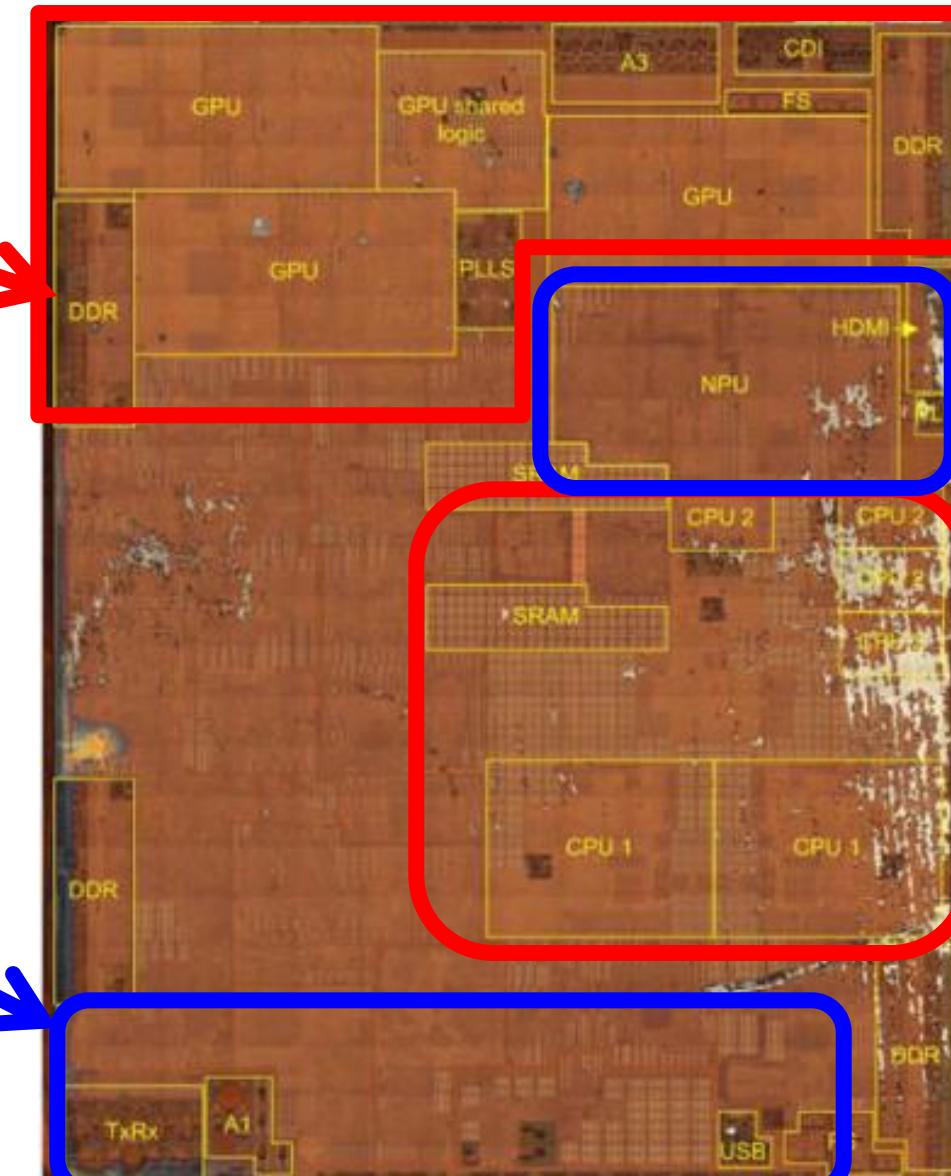


Apple A10/A9 Processors (16nm)



Apple A11 Processor (TSMC 10nm)

圖形運算
處理器
(GPU)

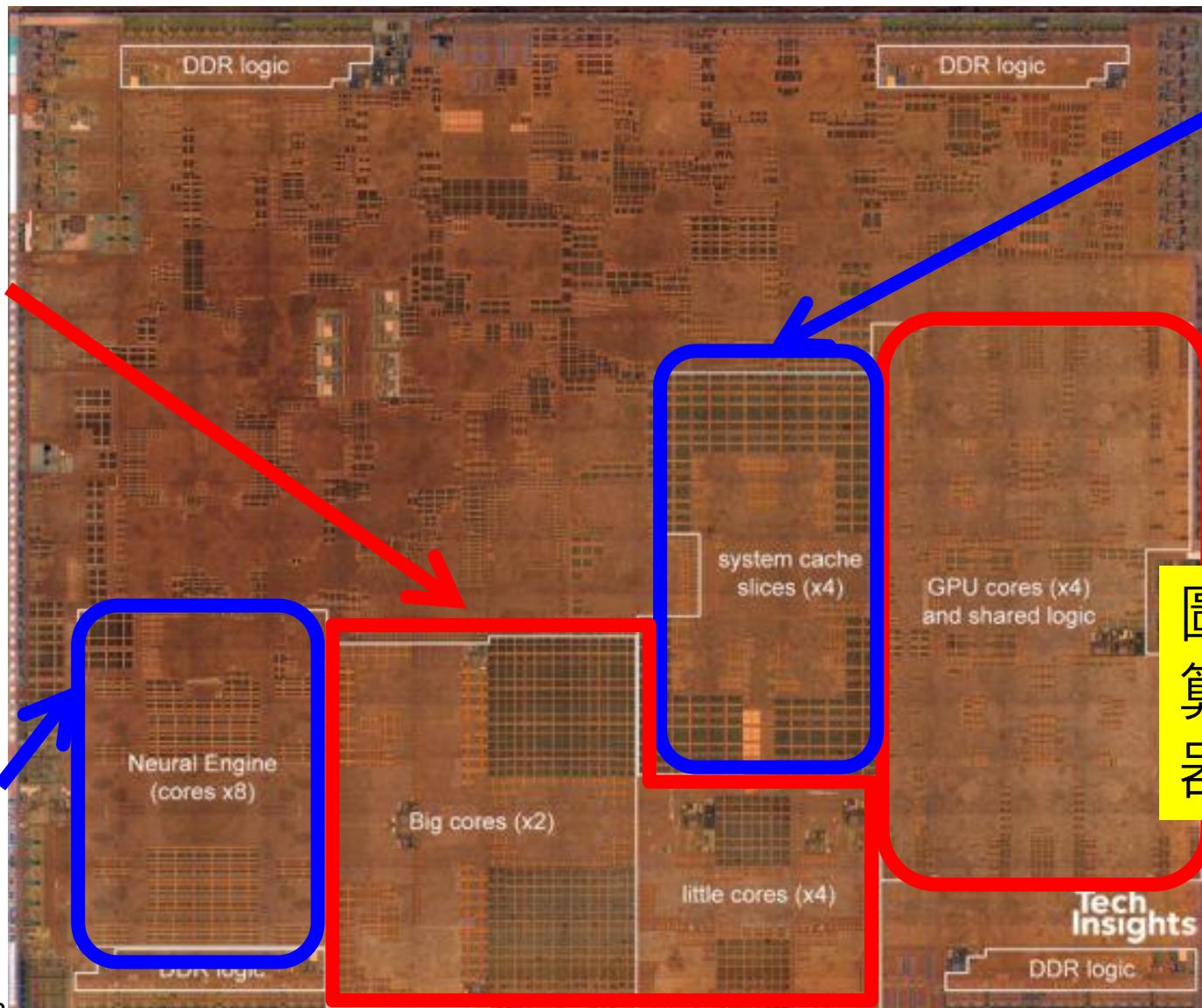


神經網
路AI處
理器]

六核處理
器(CPU)

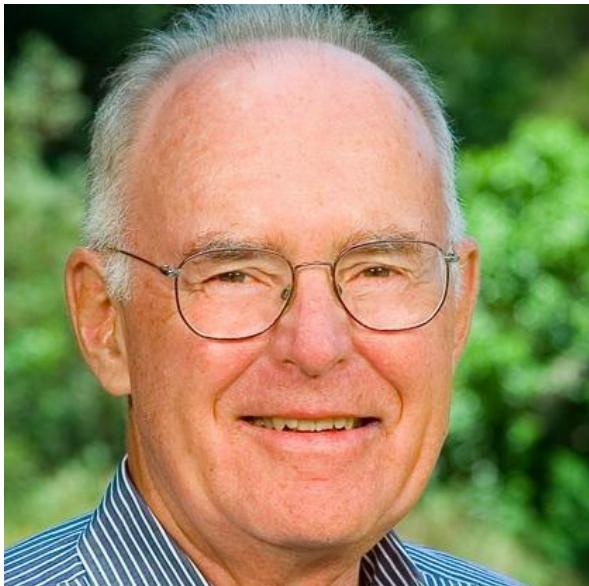
其他通
訊與多
媒體處
理電路

Apple A12 Processor (TSMC 7nm)

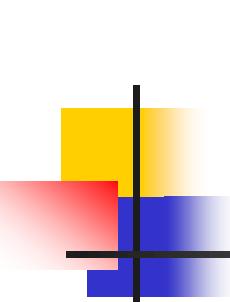


摩爾定律

Moore' s Law



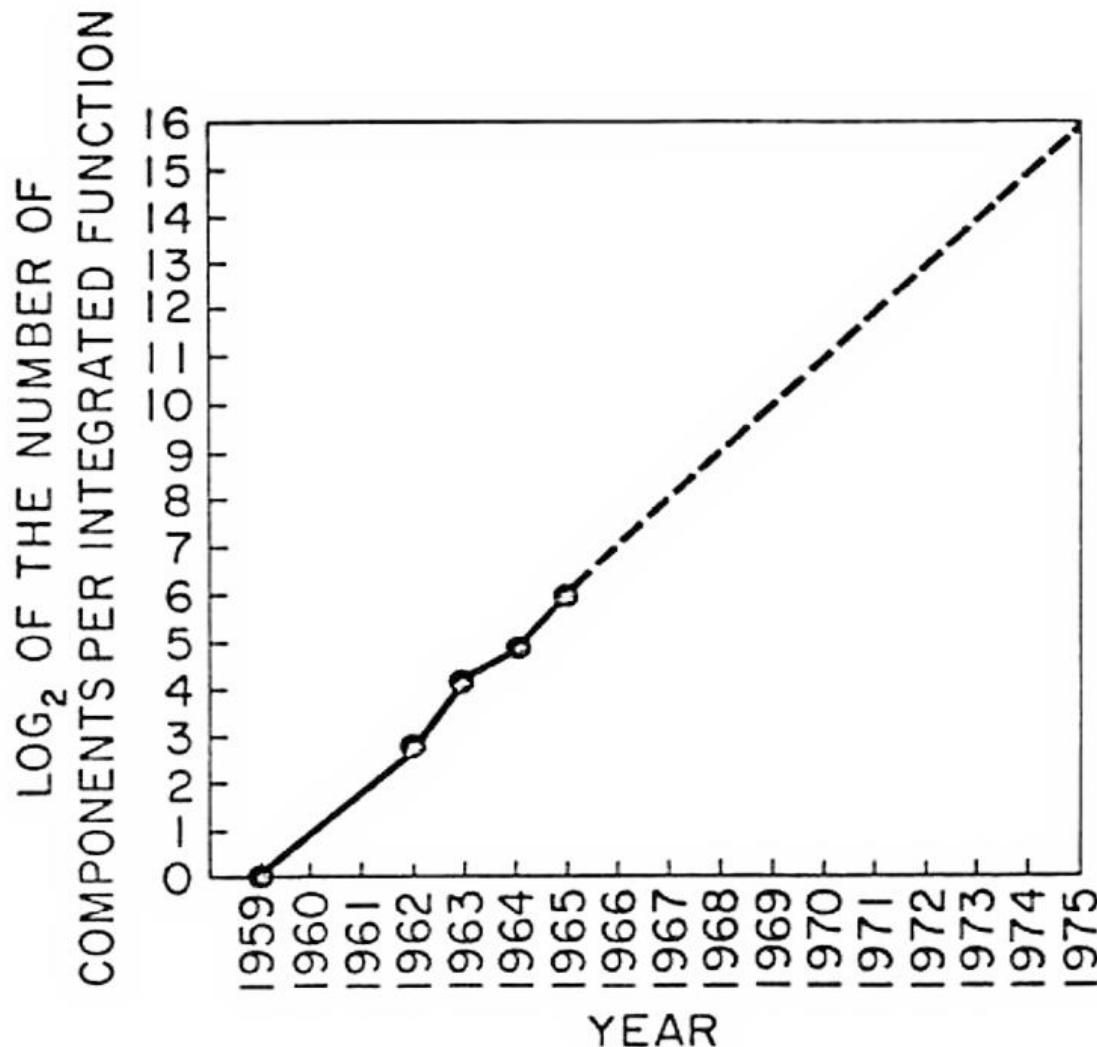
- 生於 1929年
- Intel 創辦人
- PhD, Caltech, 1954年
- 身價67億美金



摩爾定律

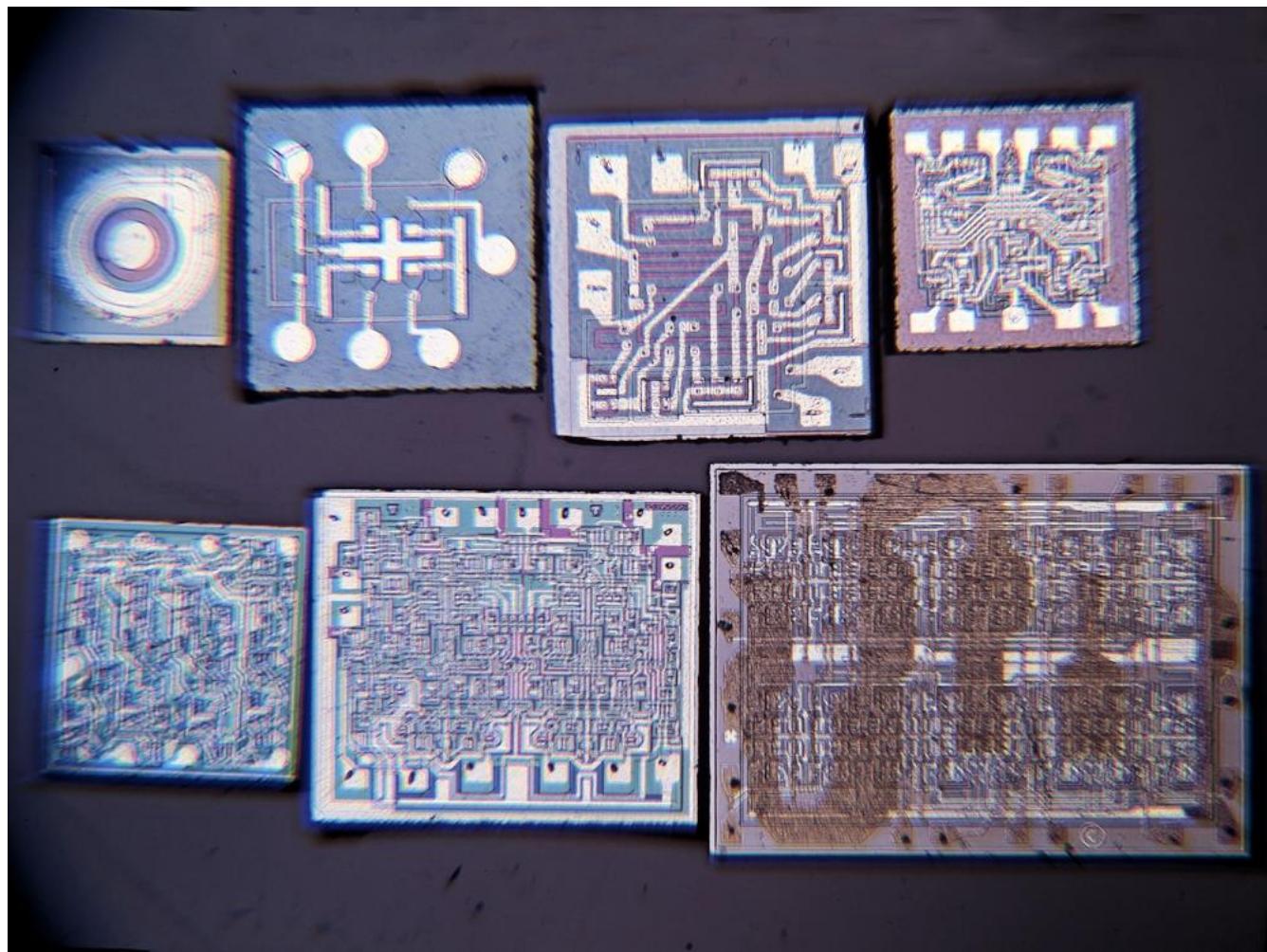
- 在1965年，Moore 發現一個IC(晶片)中的電晶體總數每18到24個月會加倍。
- 於是他提出一個預測說IC製程技術會以這個速率持續的進步，也就是說最尖端的IC效能會每18個月翻一倍。

摩爾定律圖解



Electronics, April 19, 1965.

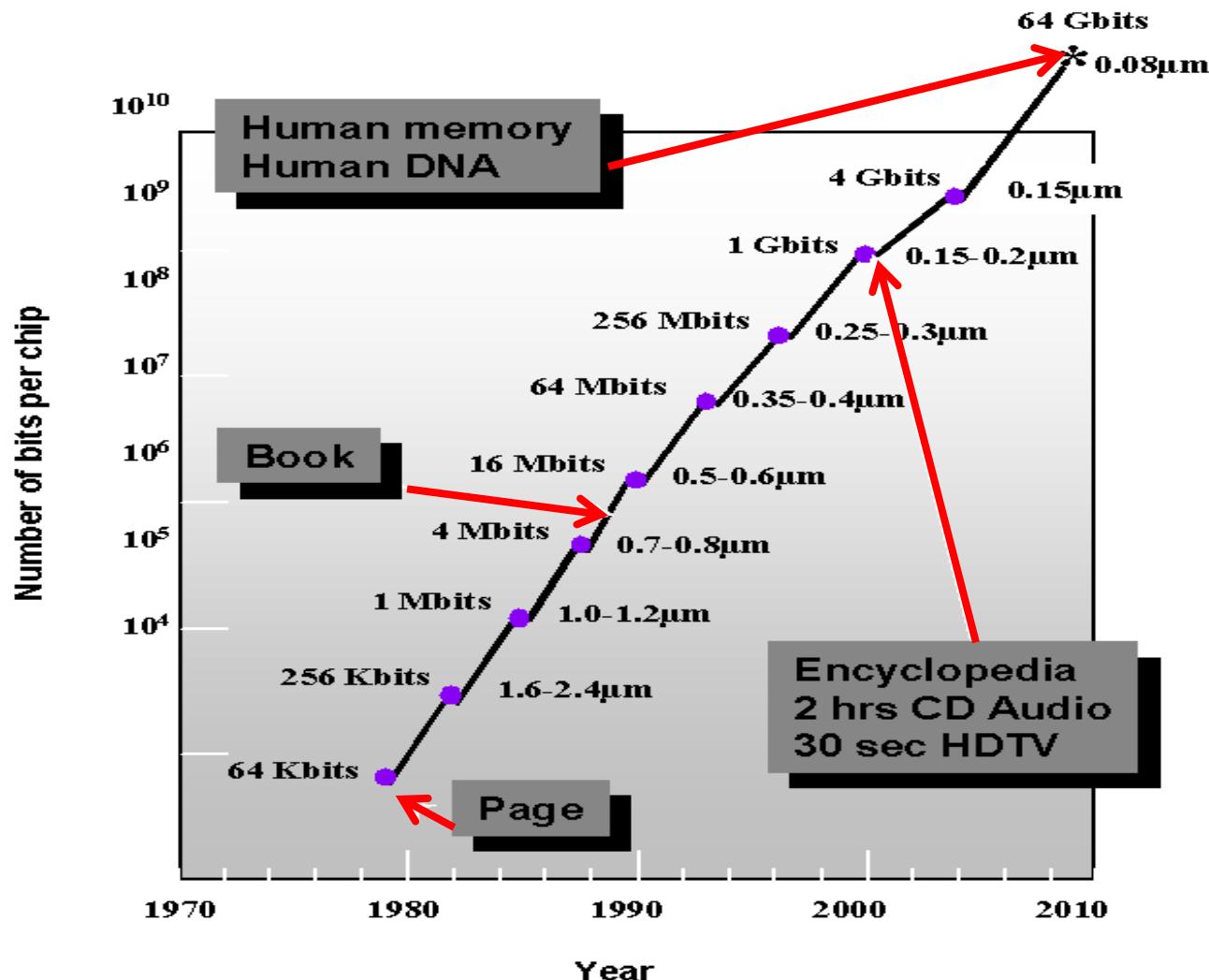
摩爾定律圖中使用的IC

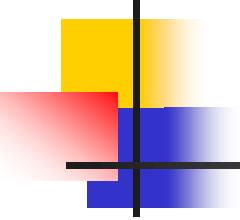


EE Journal, Feb. 7, 2019.

<https://www.eejournal.com/article/moores-law-and-the-seven-devices/>

記憶晶片(ROM)容量的演進



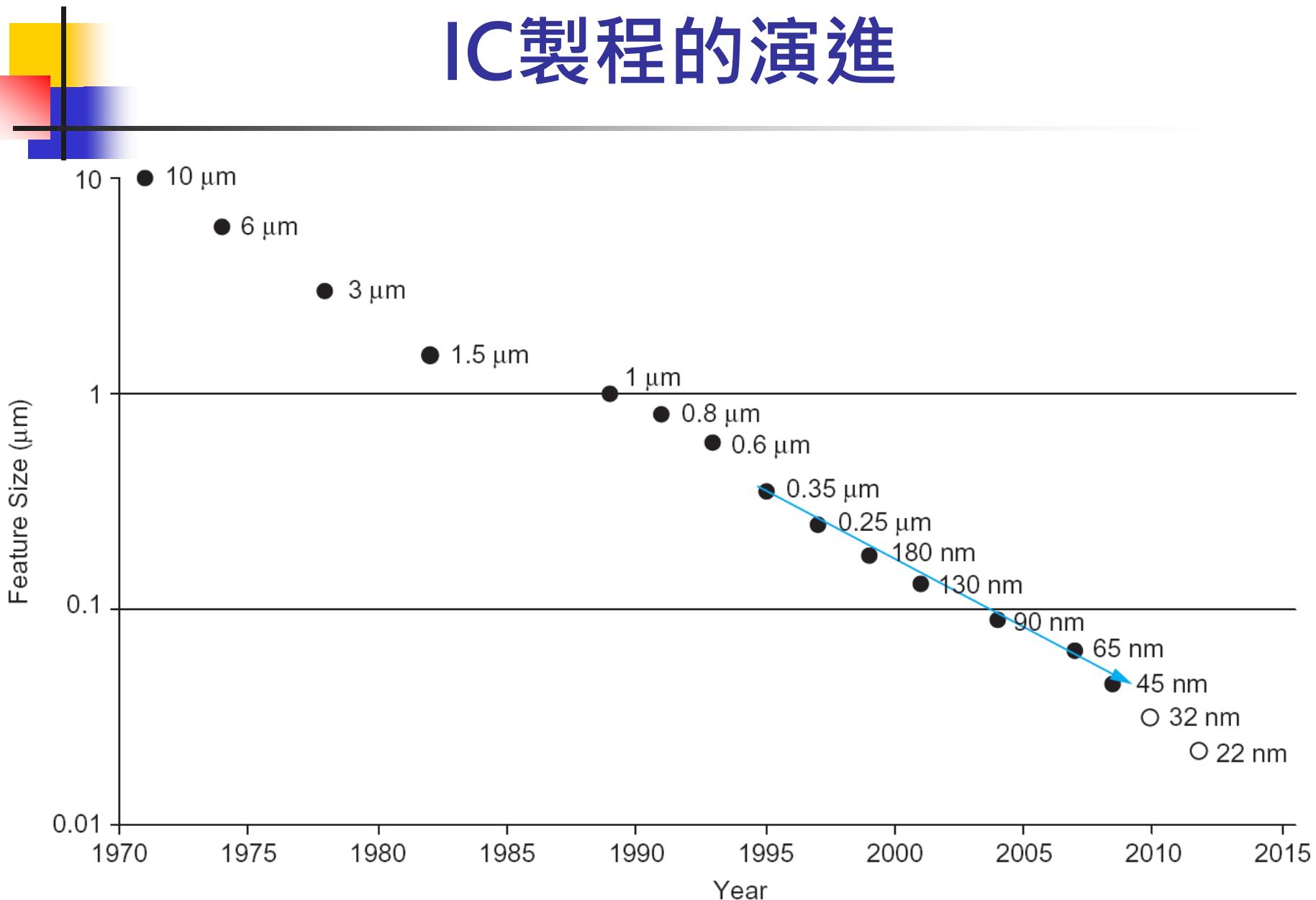


IC製程的發展

- 製程的命名是以該製程中所能製作元件的精度為基礎，目前主要是以製程中最細的元件的寬度為主，又稱feature size (特徵尺度)
- 過去數十年來已經從5微米(um, micron)逐漸進步
- 0.13 um -> 90nm -> 65nm -> 45nm (40nm)
- 現在20nm/14nm/10nm 是最尖端製程。
- 7nm製程也已經推出了。

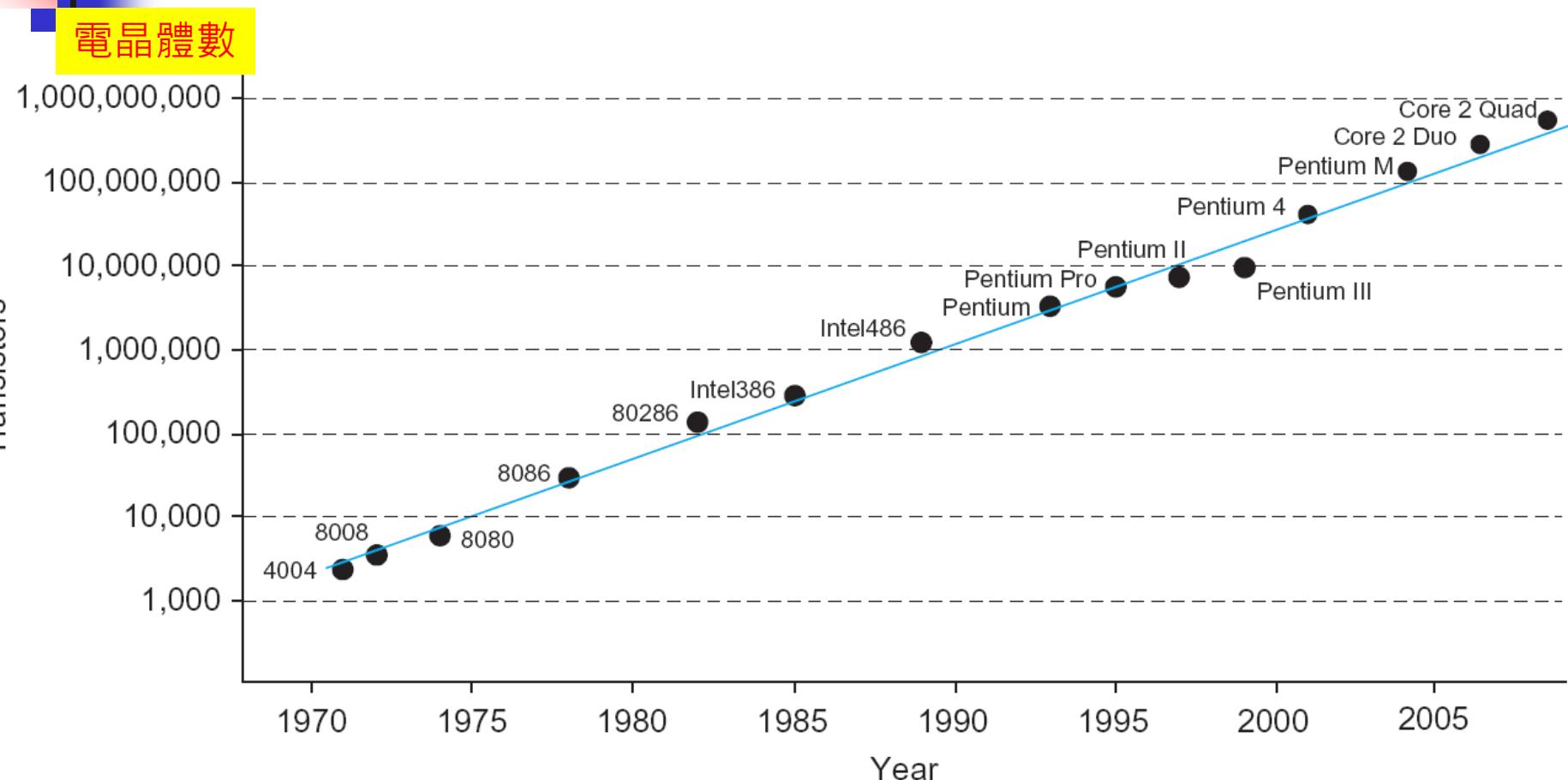
nm 是nanometer，是1公尺的十億分之一($1/1,000,000,000$)

IC製程的演進



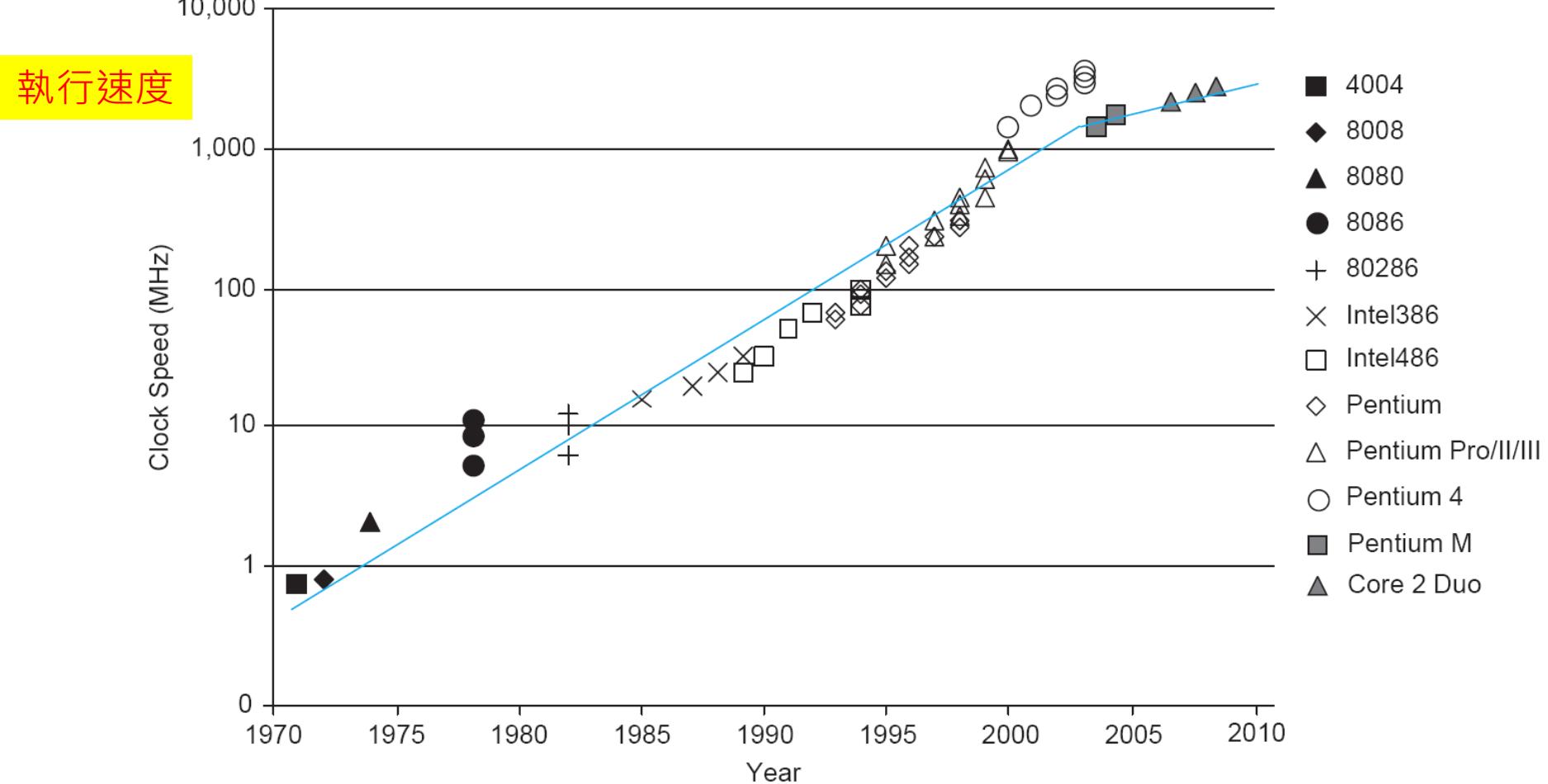
Source: SIA 2007

微處理器 (CPU) 的摩爾定律



最先進的微處理器中的電晶體數每兩年倍增

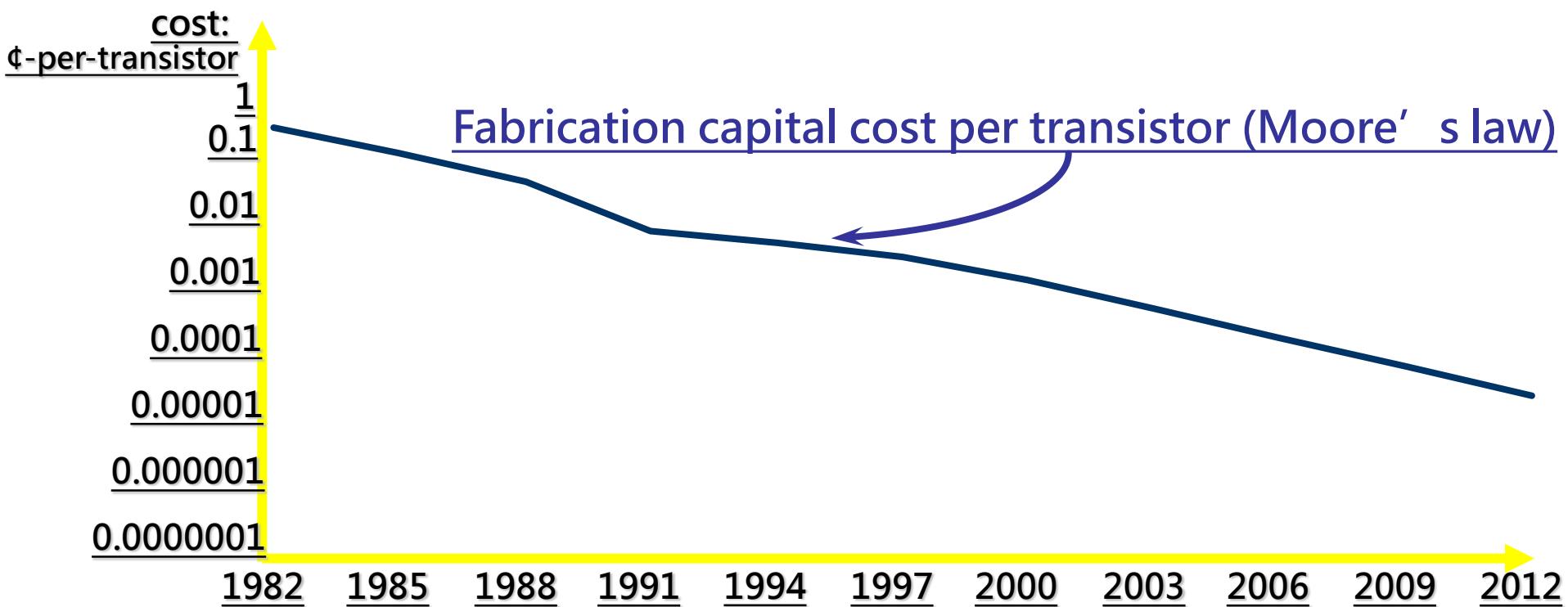
晶片速度的摩爾定律

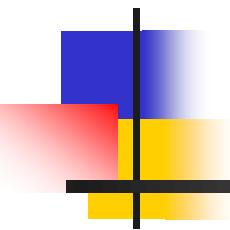


最先進的微處理器速度每兩年倍增

電晶體的單位製造成本

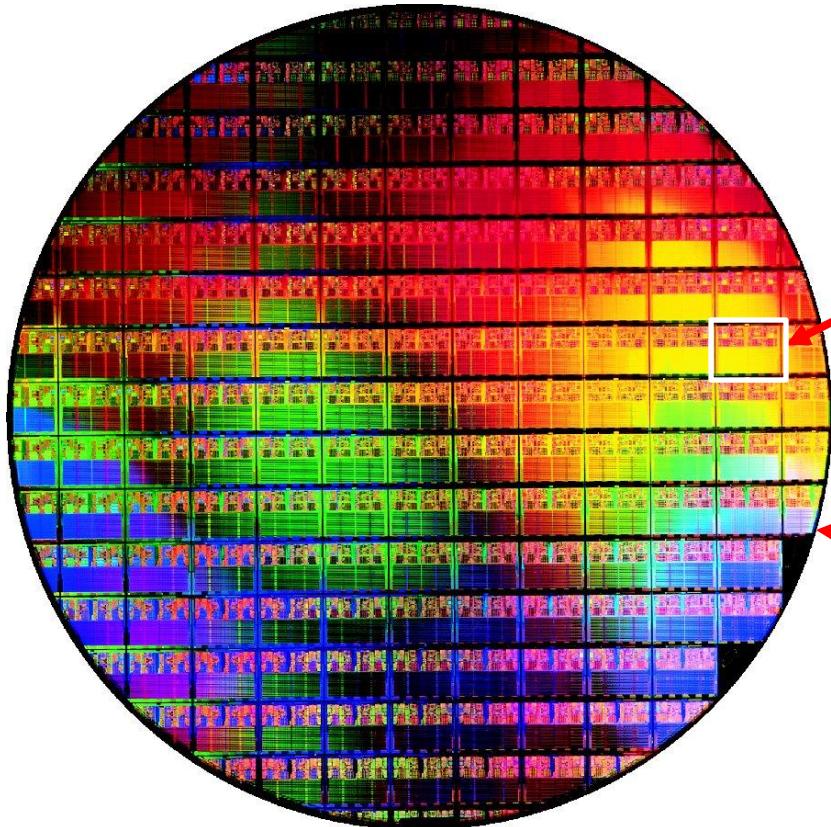
製造成本





IC 製程

Silicon Wafer

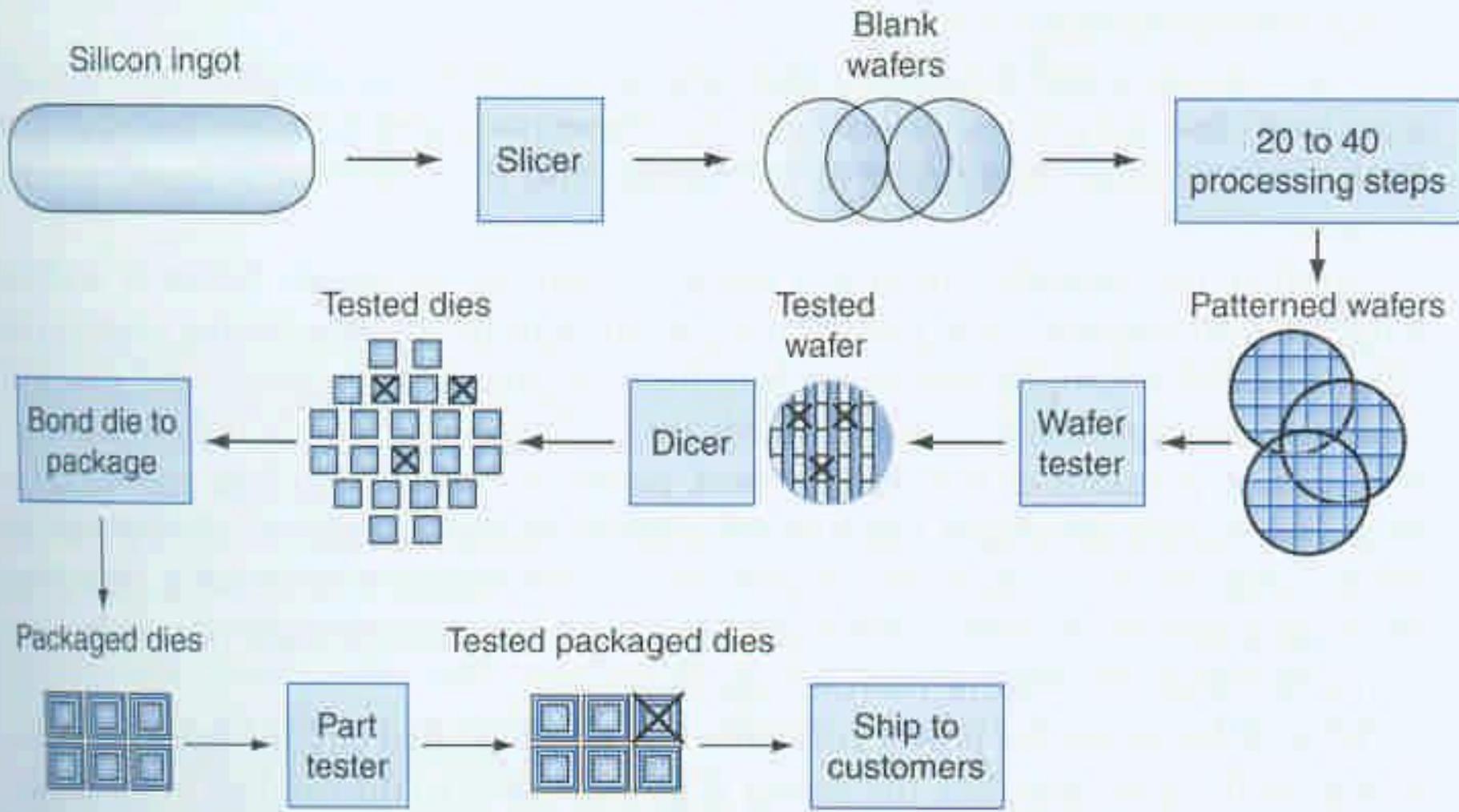


未封裝前晶片

晶圓

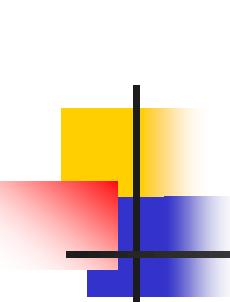
最大可達直徑12" (30cm)

IC 製造程序 (製程)



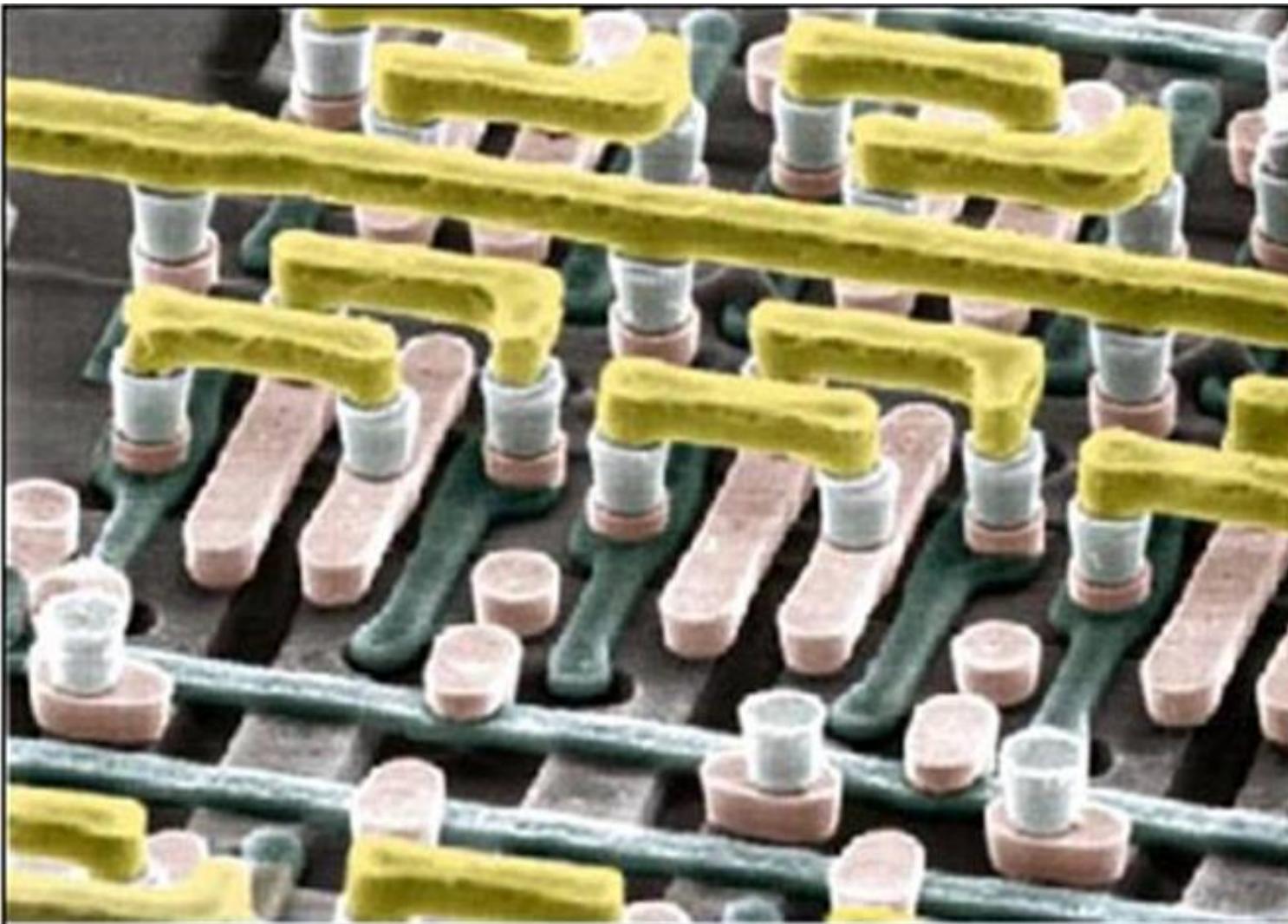
製造IC有點像在做Pizza



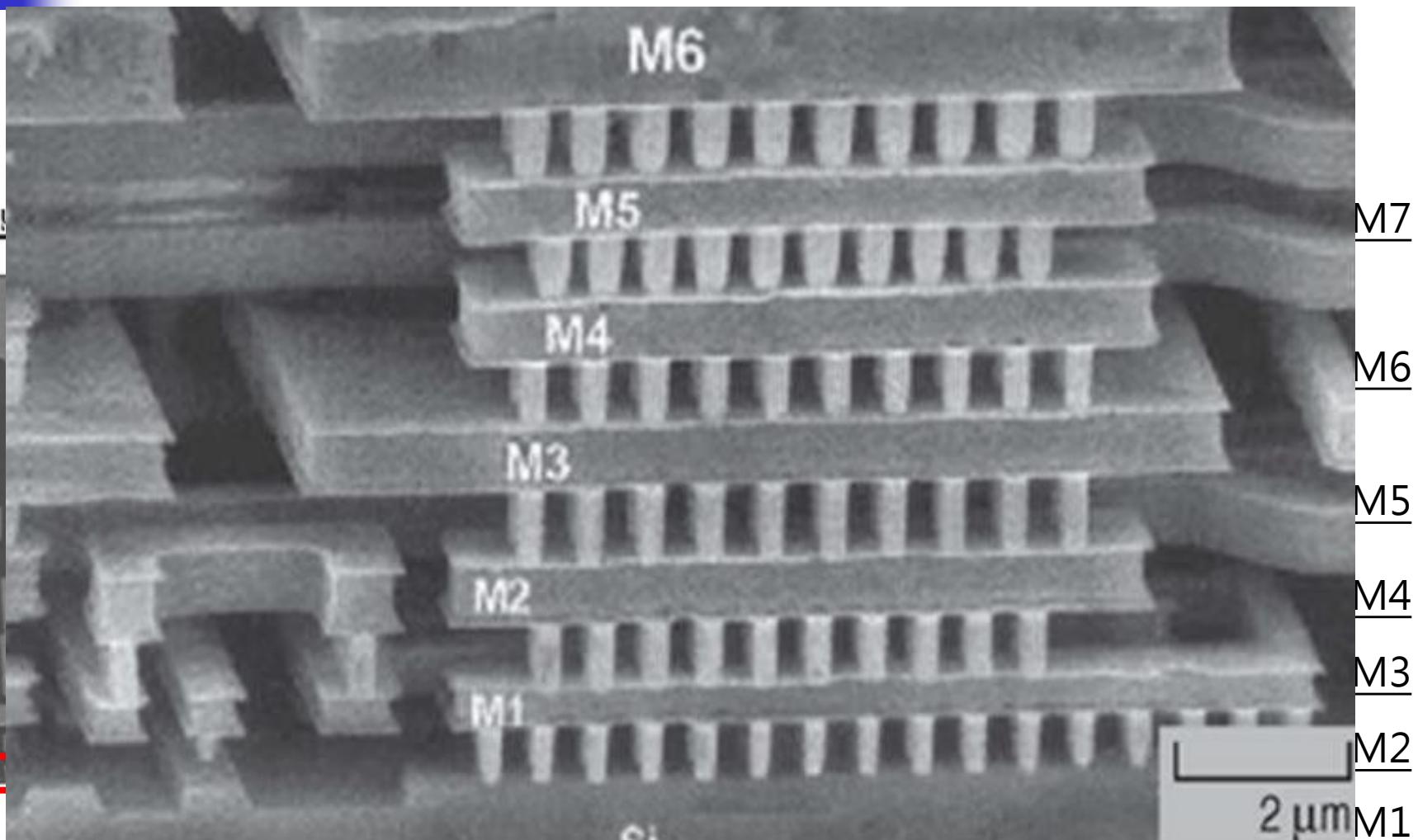


IC製作過程影片

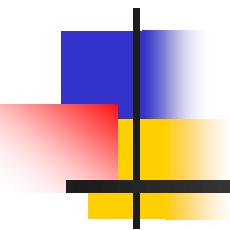
IC局部放大相片



IC 側視放大照片

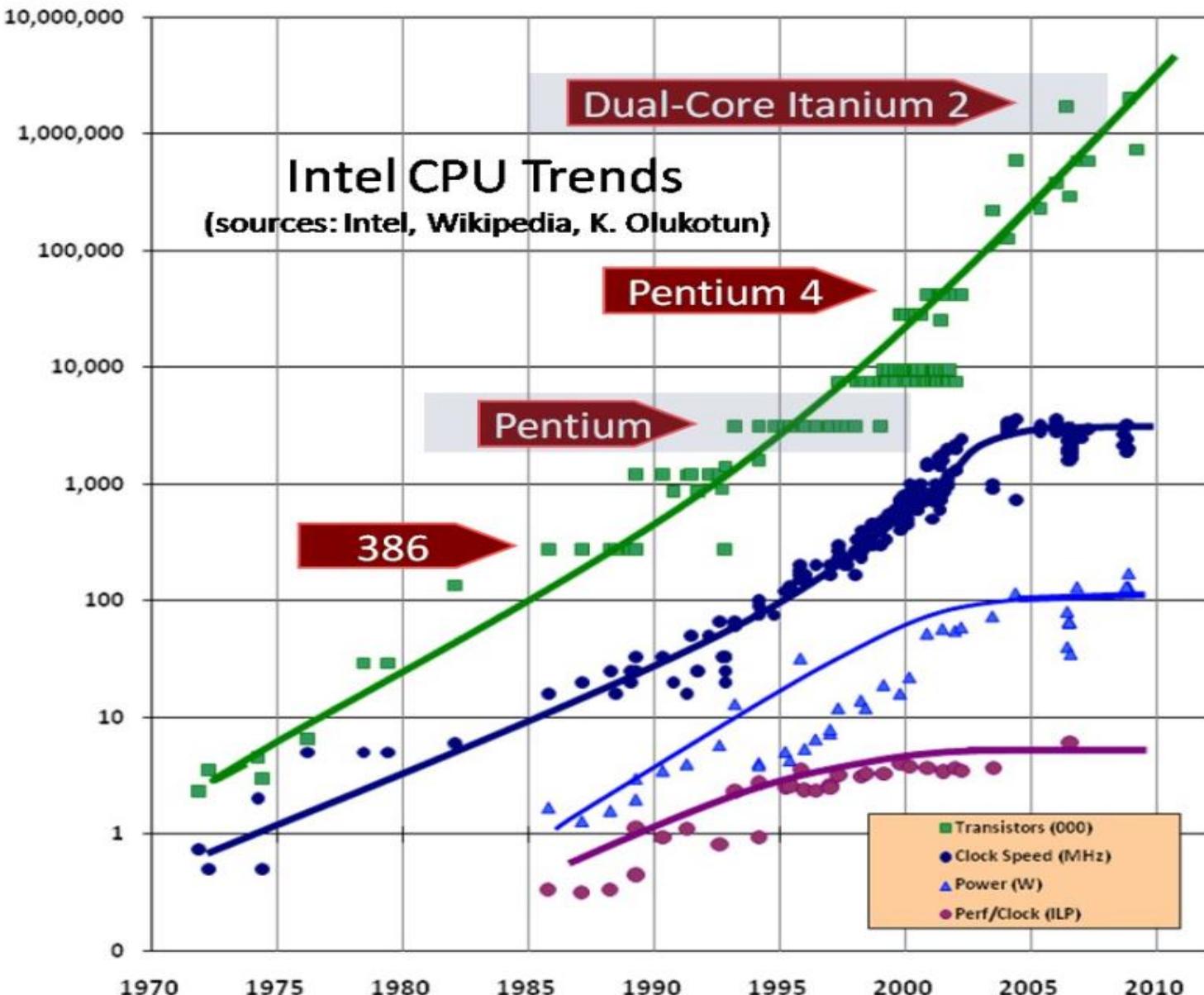


電晶體

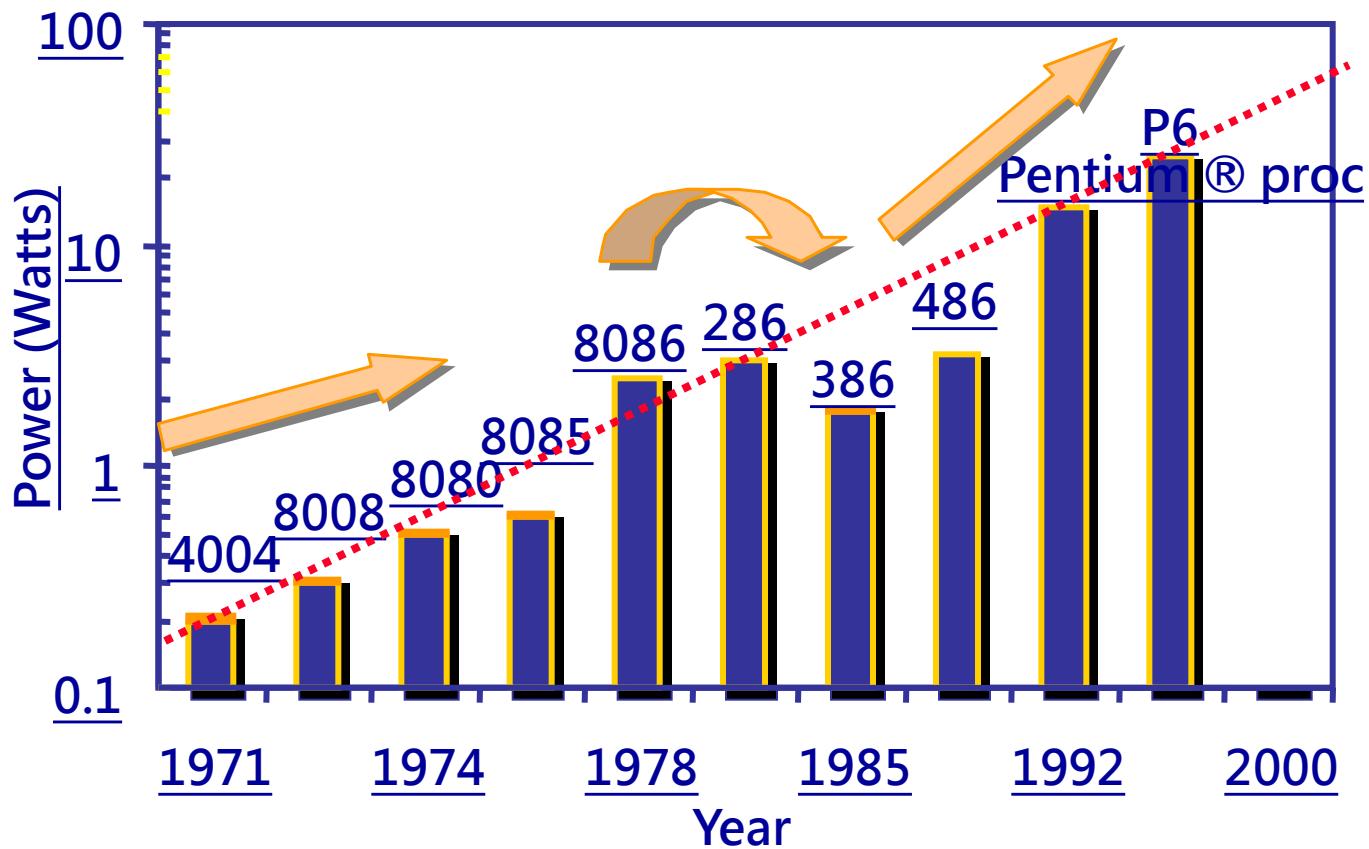


IC 進步有限制嗎？

Intel CPU 的趨勢

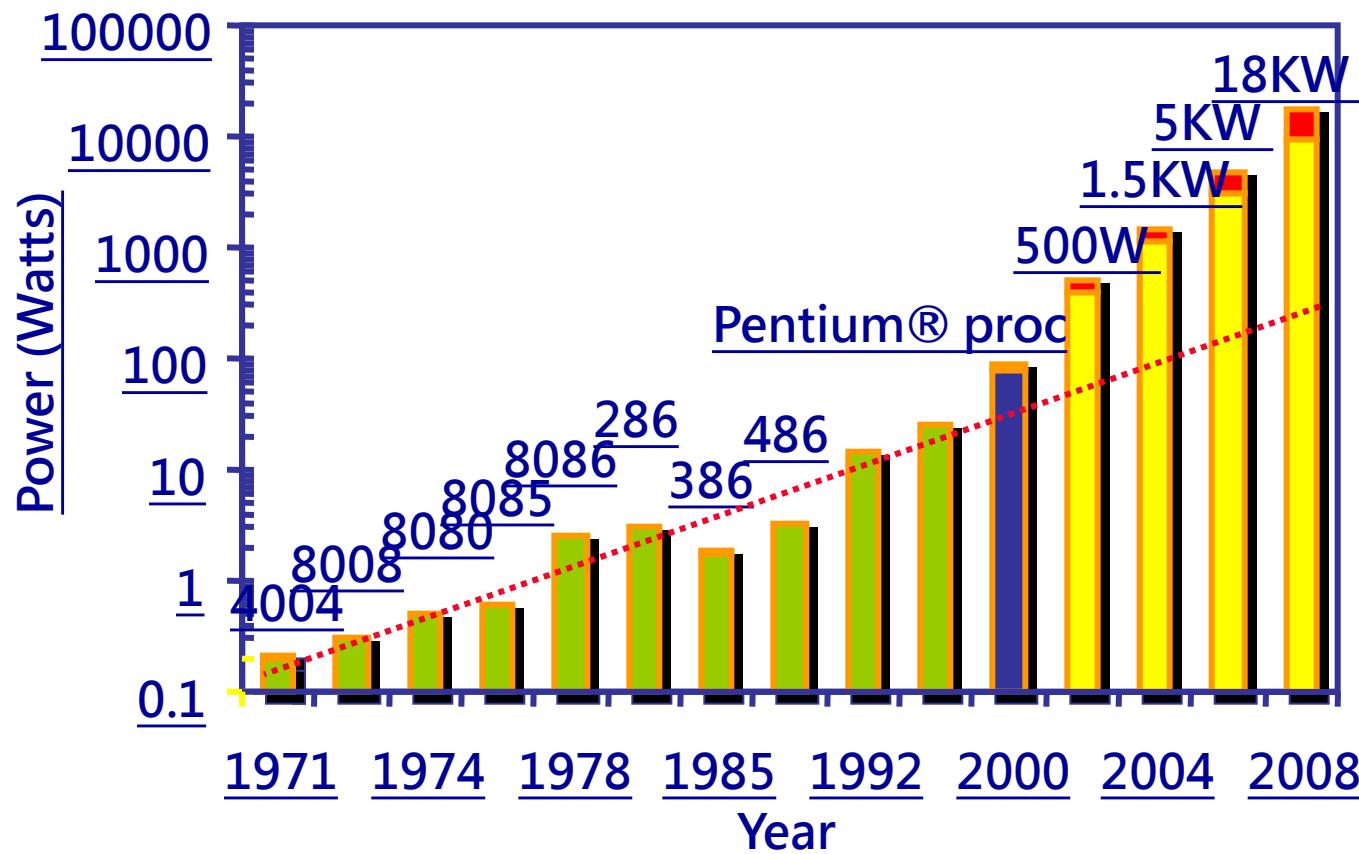


微處理器消耗的功率



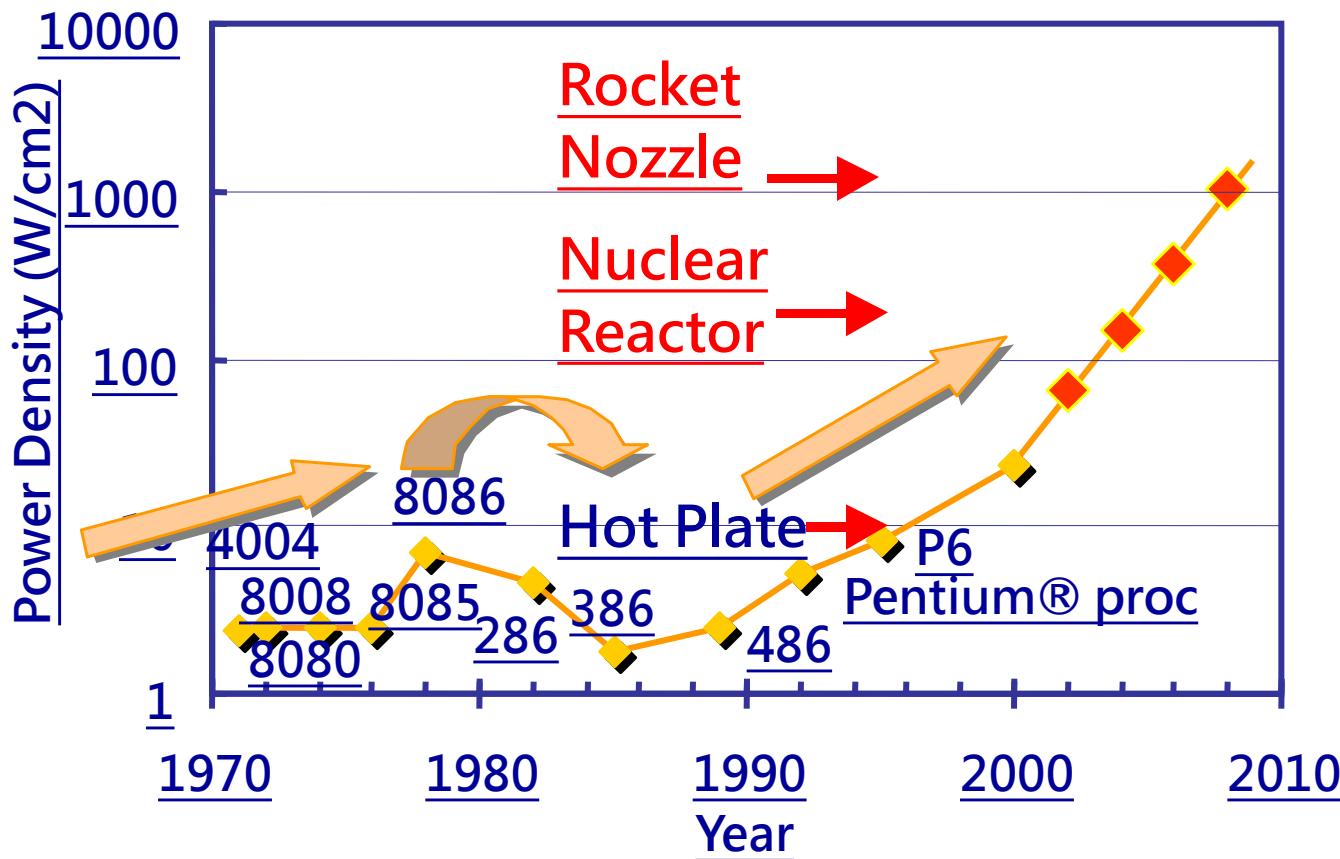
微處理器功率一直增加

IC消耗功率太高是一大問題

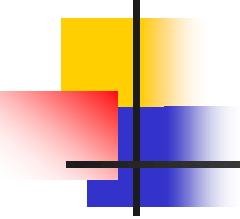


Source: Intel

功率密度

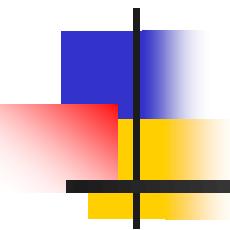


Source: Intel



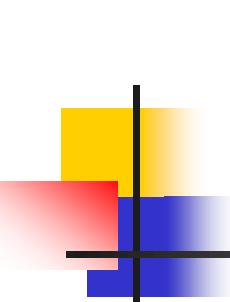
走向多核

- 在一個晶片上製作多個處理器
- 每一個處理器用較慢的速度來執行，耗能較低
- 16核心，64核心，甚至上千核心。



超過五十歲的摩爾 定律玩完了嗎？

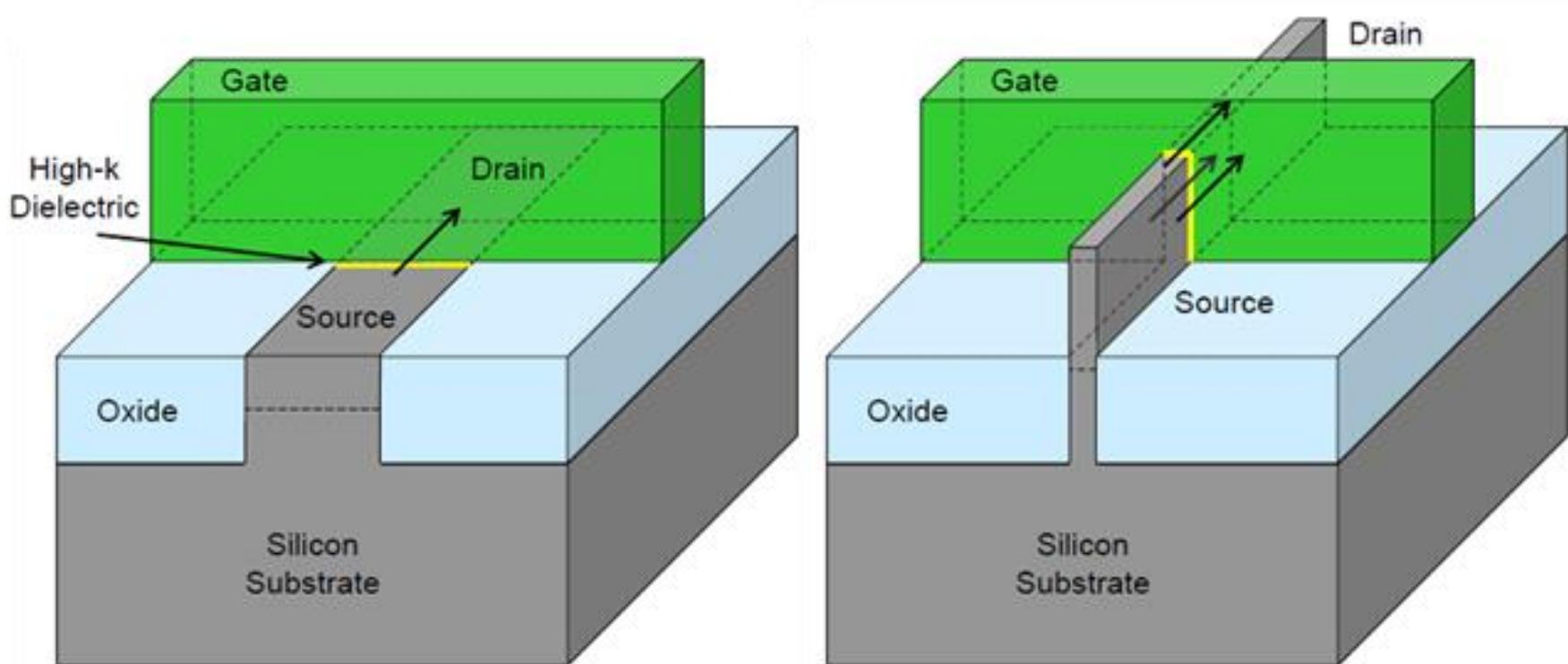
1965 – ????

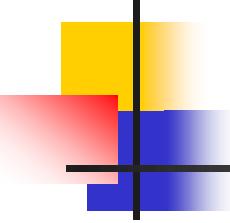


摩爾定律的未來

- 持續微縮至5nm, 3nm，甚至以下。
- 到達原子尺寸極限以前，會走向立體化。
- 立體化(3D)有幾種方法，可以只採用一種或採用多種
 - 3D電晶體 (鳍式電晶體，FinFET)
 - 堆疊晶片 (3D IC)
 - 堆疊電晶體層 (Monolithic 3D IC)

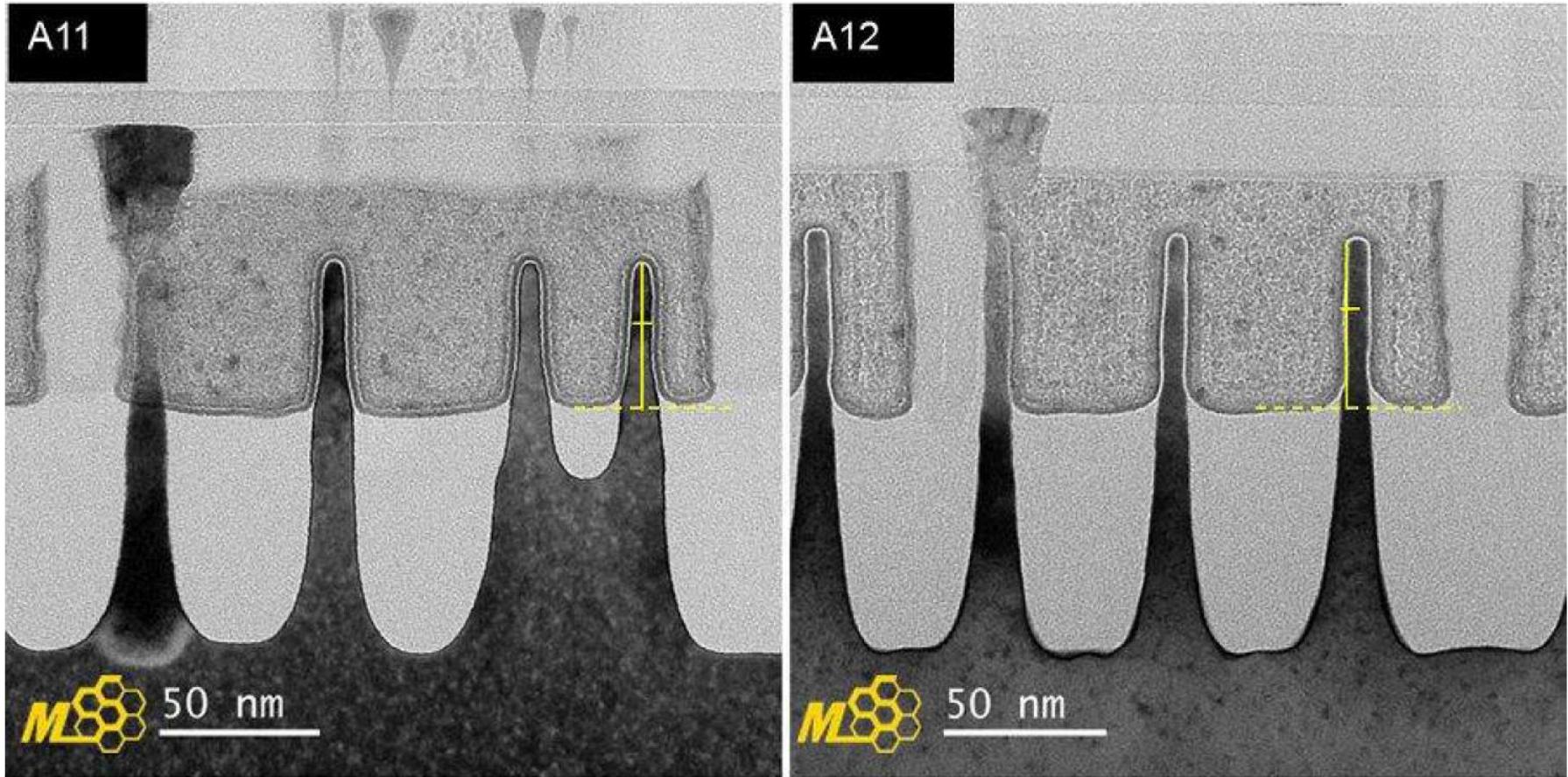
3D電晶體 (FinFET)



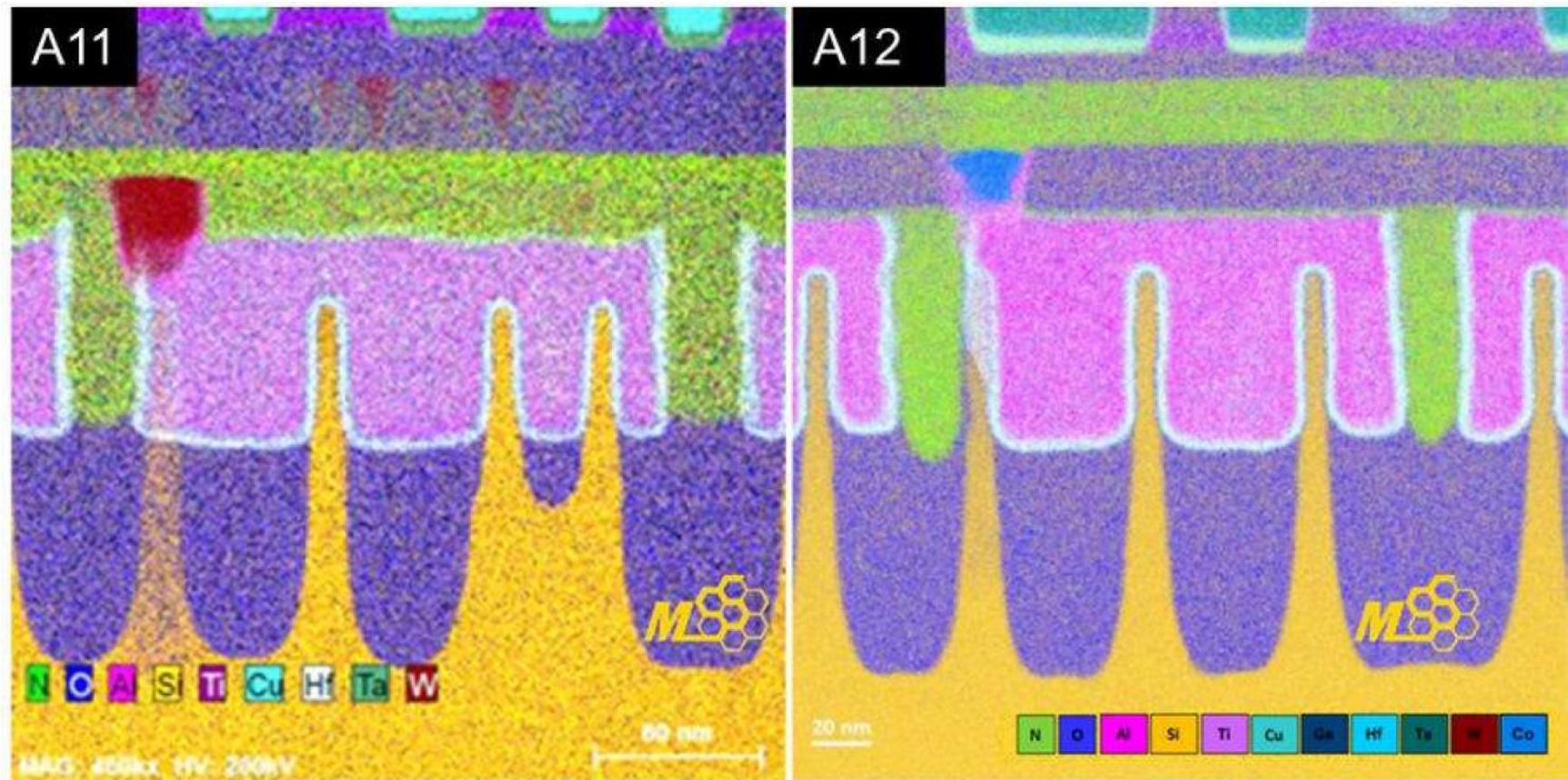


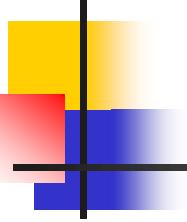
3D電晶體 (FinFET) 影片

3D電晶體 (FinFET) 比較



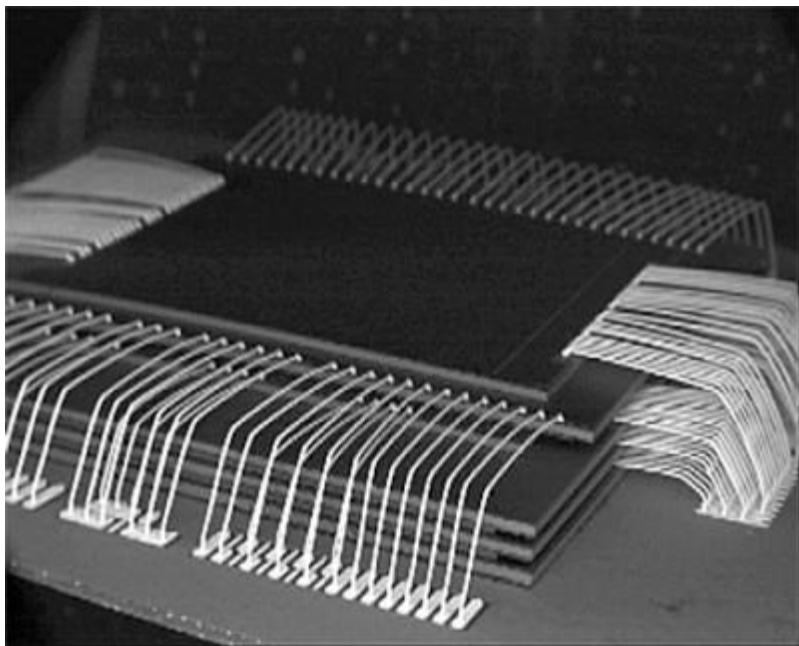
3D電晶體 (FinFET) 比較





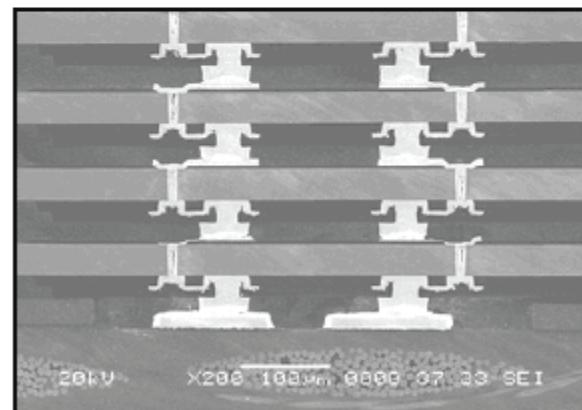
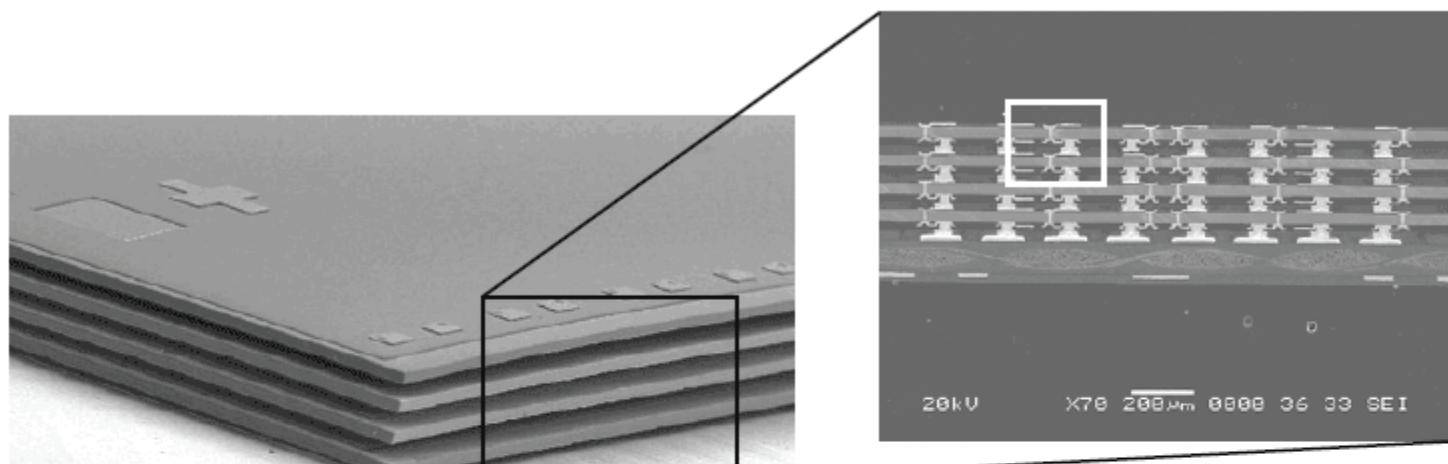
3D IC --- 晶片堆疊

- 垂直方向堆疊多個晶片 (16, 32甚至100層)
- 利用金屬線來連結晶片之間的訊號



3D IC --- 穿矽連結 (TSV)

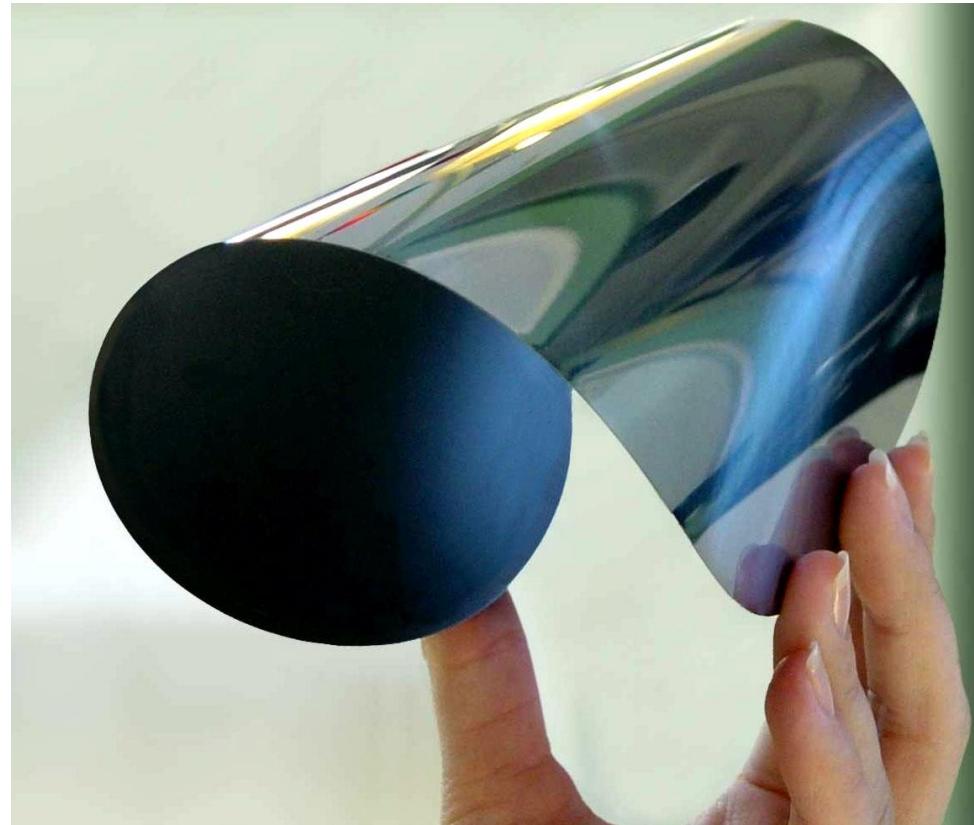
■ Through-silicon Via (TSV) 技術



2. Amkor Technologies is working on a four-die memory stack with 50- μm die thickness and 10- μm diameter TSVs. (courtesy of Amkor Technologies)

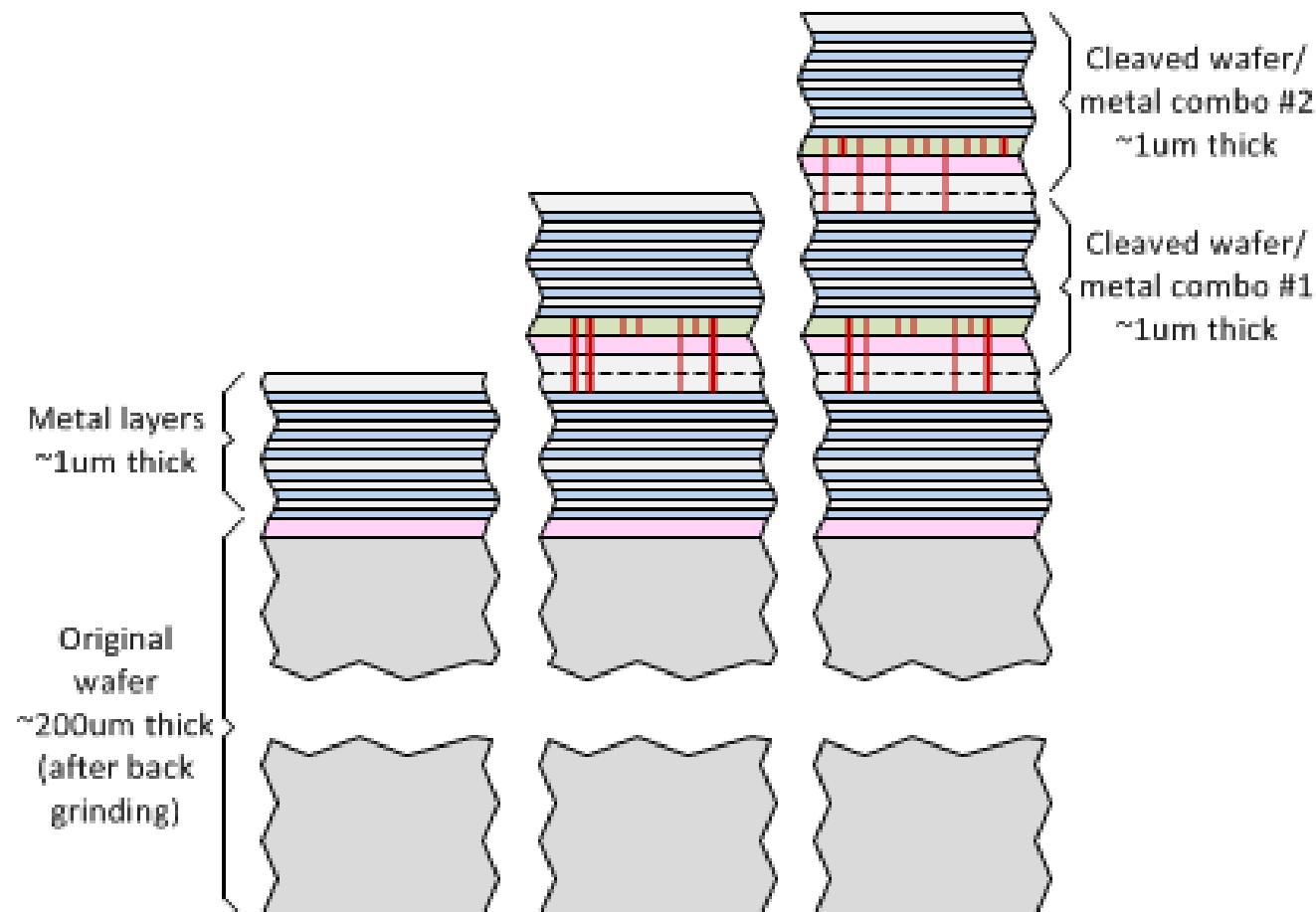
晶圓磨薄

- 晶圓堆疊之前要先磨薄
- 從 $300\mu m$ 磨成 $30\mu m$.



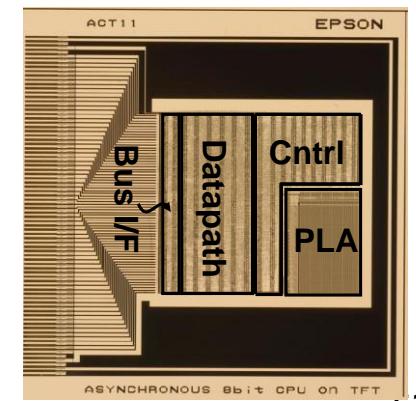
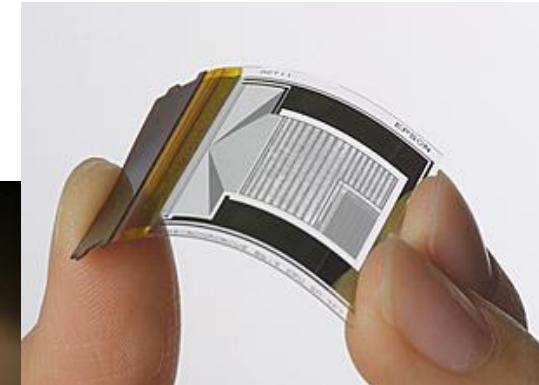
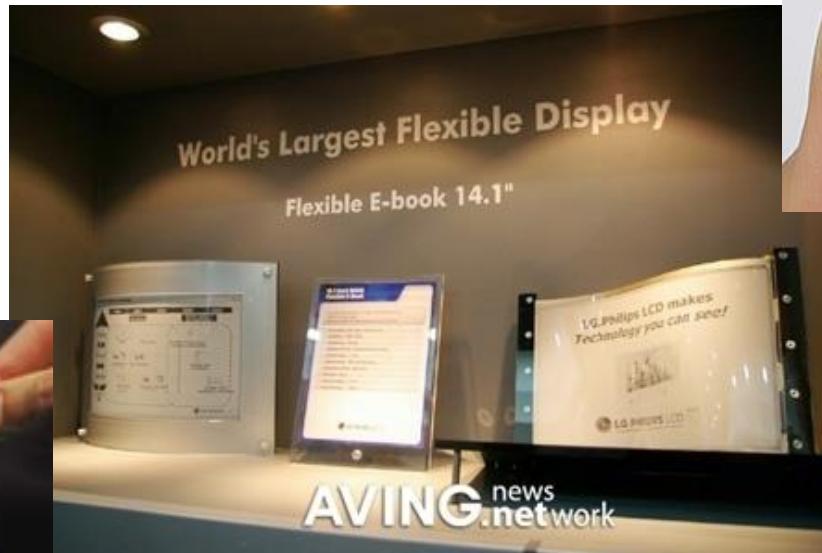
Monolithic (單晶) 3D IC

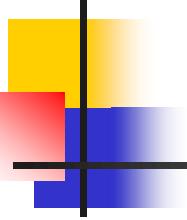
- 一層一層的電晶體與連結直接堆疊



Flexible Electronics

- Thin-film transistors that are on LCD can be fabricated on flexible substrates as display
- Flexible e-book
- Flexible digital processor realized.



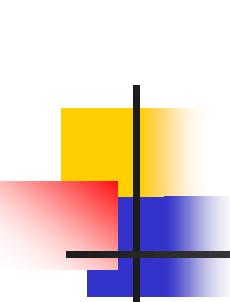


折疊式螢幕

- Samsung Galaxy Fold

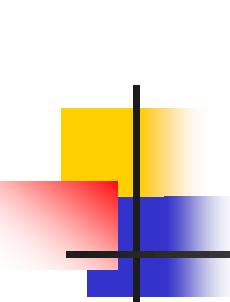


<https://www.youtube.com/watch?v=rkBSau4Yu-I>
<https://www.youtube.com/watch?v=Cno-NRGnERM>



總結

- IC設計與製造技術在過去半個世紀來促成了電子科技爆炸性的成長。
- 影響了所有人類的各個生活層面：通訊，能源，醫療，科學，農業，工業，運輸，娛樂等等。
- 展望未來，摩爾定律還會持續。
- 工程師們也會持續do this good job，為人類的福祉與更好的生活品質創造出更多的創新產品與技術。



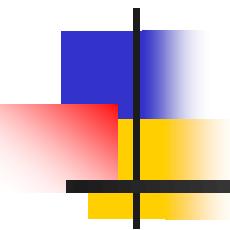
IC60周年影片

Chapter 1

Introduction to CMOS Circuits



闕志達
台灣大學電機系



邏輯IC設計： 從電晶體到功能電路

MOS Switches

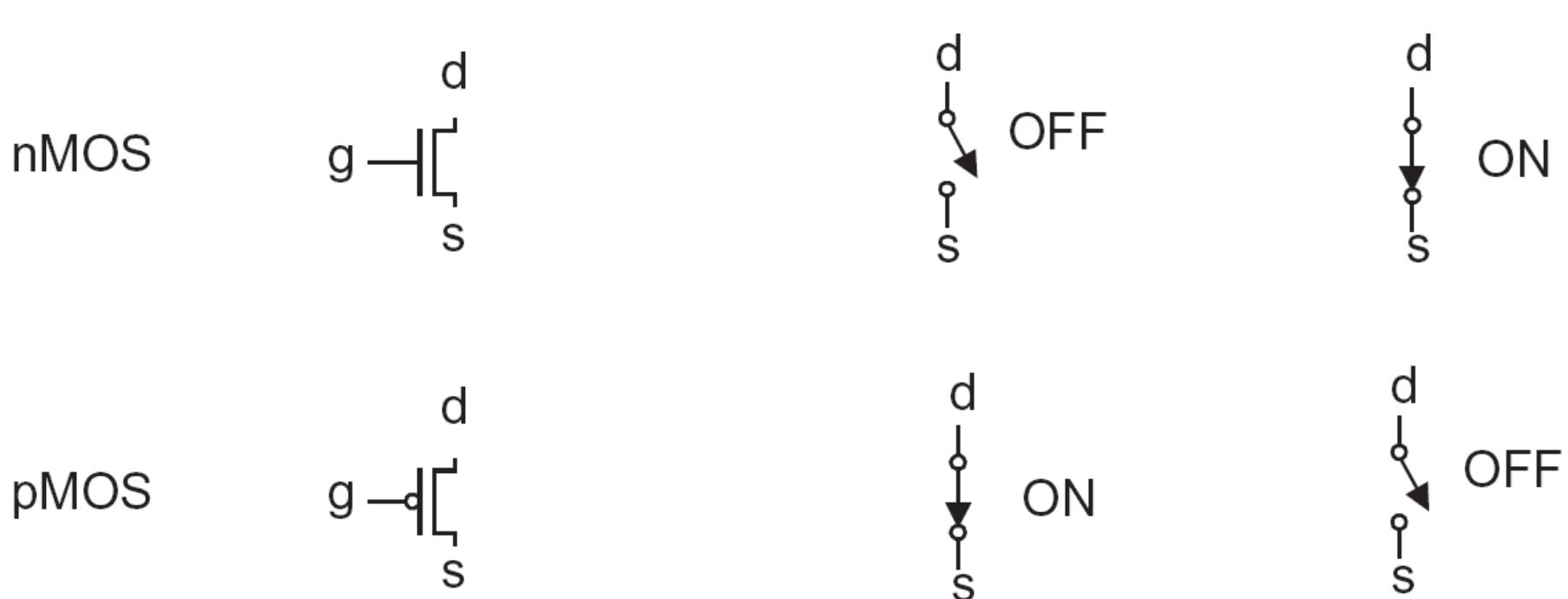


FIGURE 1.10 Transistor symbols and switch-level models

CMOS Static Logic

- Restored logic

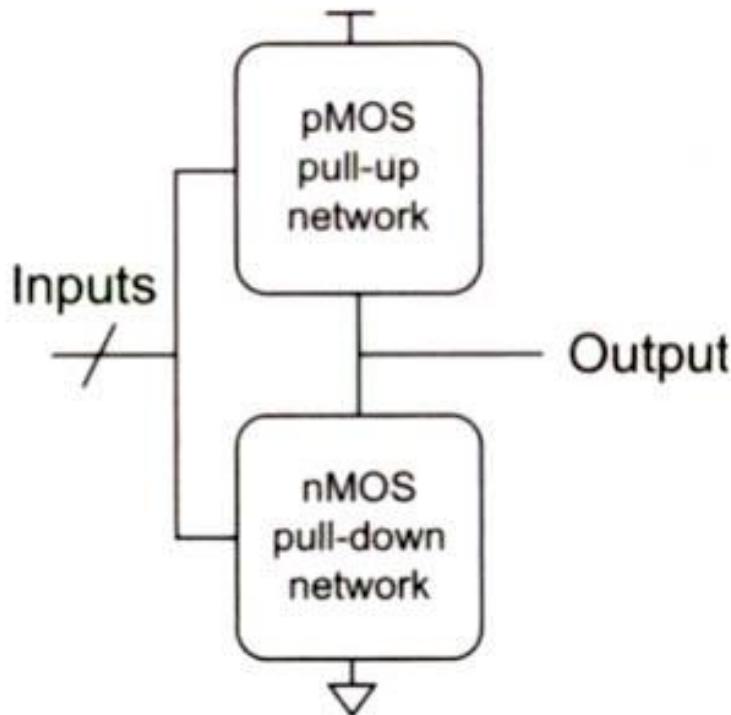
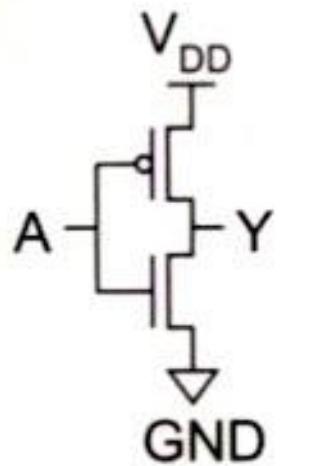


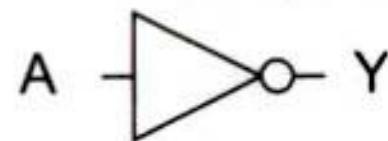
Table 1.3 Output states of CMOS logic gate

	pull-up OFF	pull-up ON
pull-down OFF	Z	1
pull-down ON	0	crowbarred (X)

CMOS Inverter



(a)



(b)

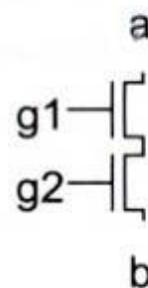
FIGURE 1.11

Inverter schematic

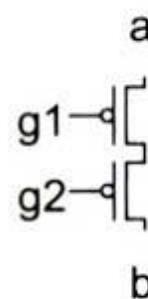
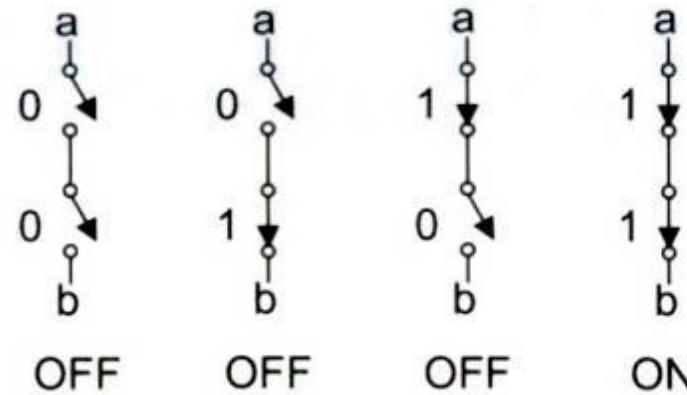
(a) and symbol

(b) $Y = \overline{A}$

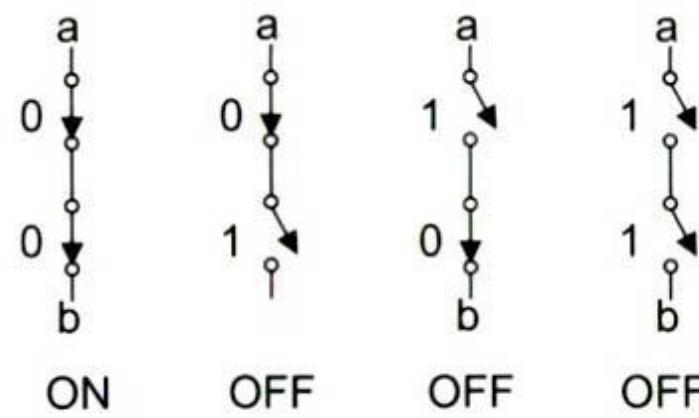
Series Connection of Switches



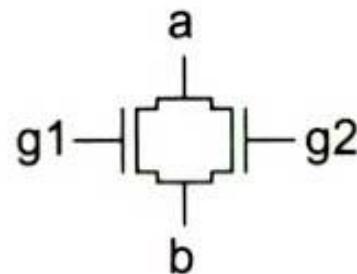
(a)



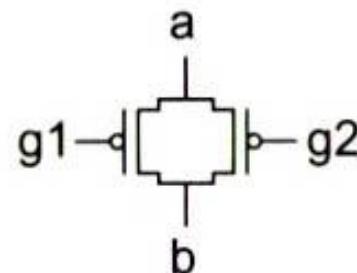
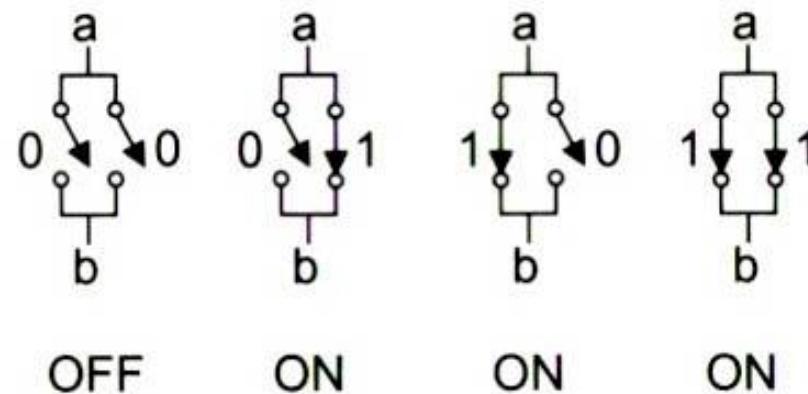
(b)



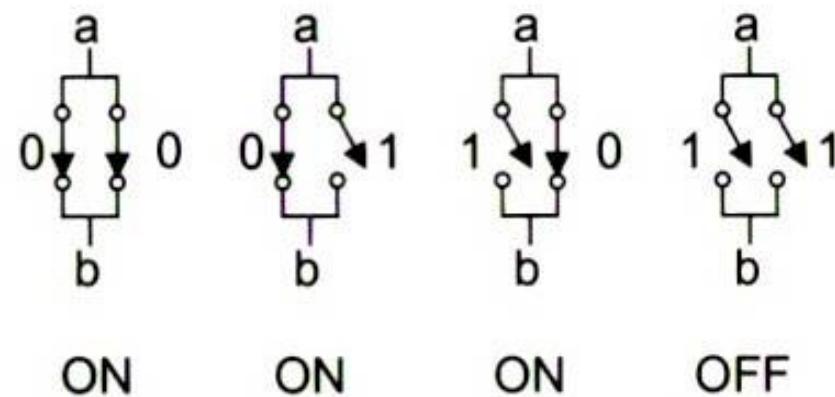
Parallel Connection of Switches



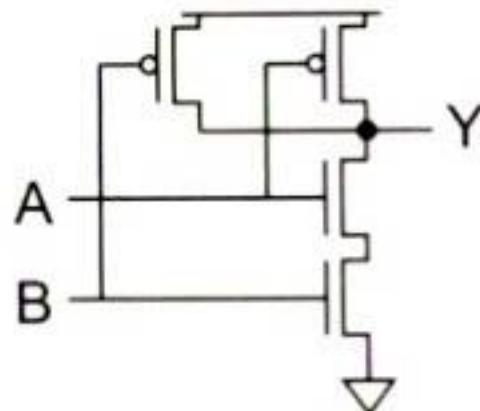
(c)



(d)



NAND Gate



(a)



(b)

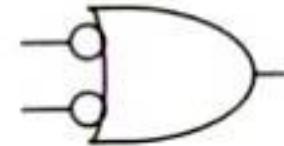


FIGURE 1.12 2-input NAND
gate schematic (a) and symbol
(b) $Y = \overline{A \cdot B}$

NOR Gate

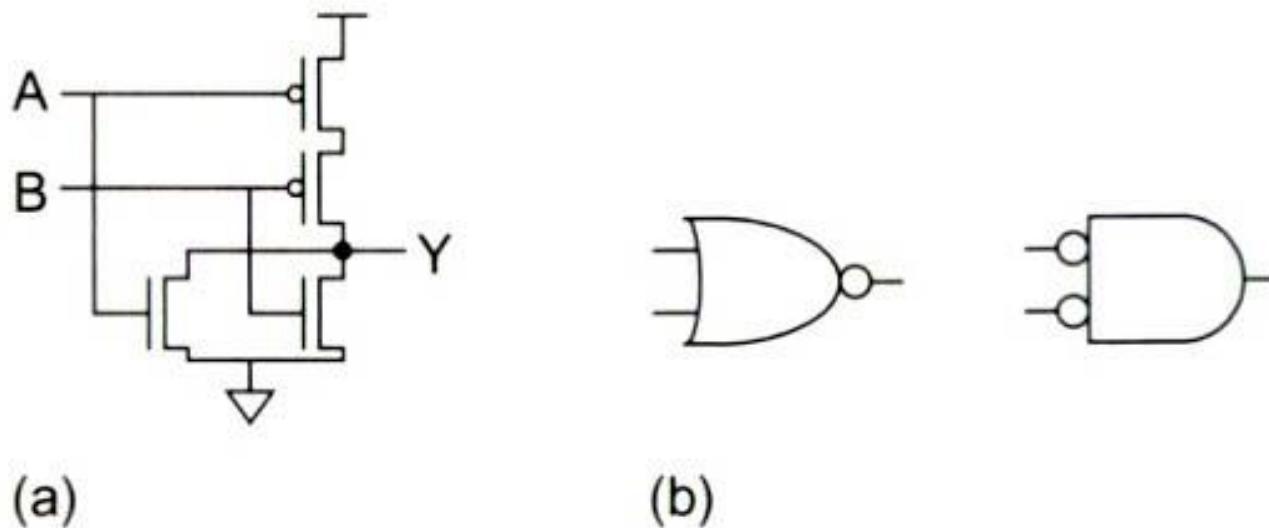


FIGURE 1.16 2-input NOR
gate schematic (a) and symbol
(b) $Y = \overline{A + B}$

Compound Gates

- NMOS first, AND => serial connection, OR => parallel connection
- PMOS is the dual of NMOS.
- Note that the gate has an inverting output.

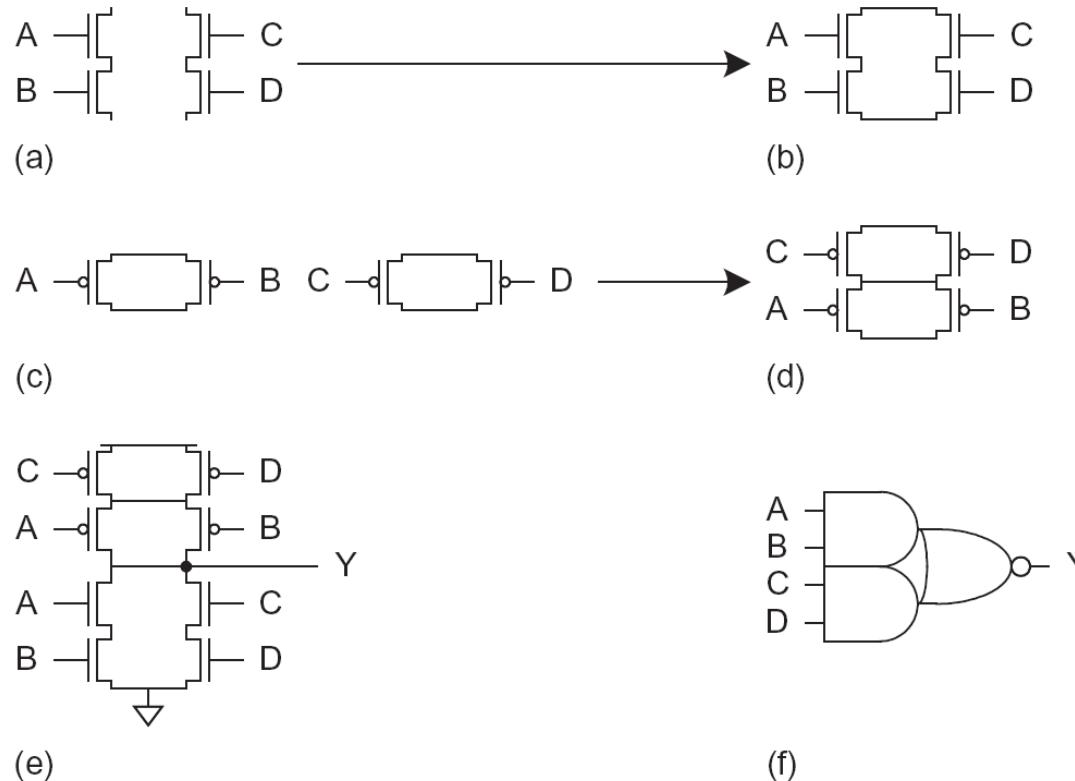


FIGURE 1.18 CMOS compound gate for function $Y = \overline{(A \cdot B)} + \overline{(C \cdot D)}$

Another Example

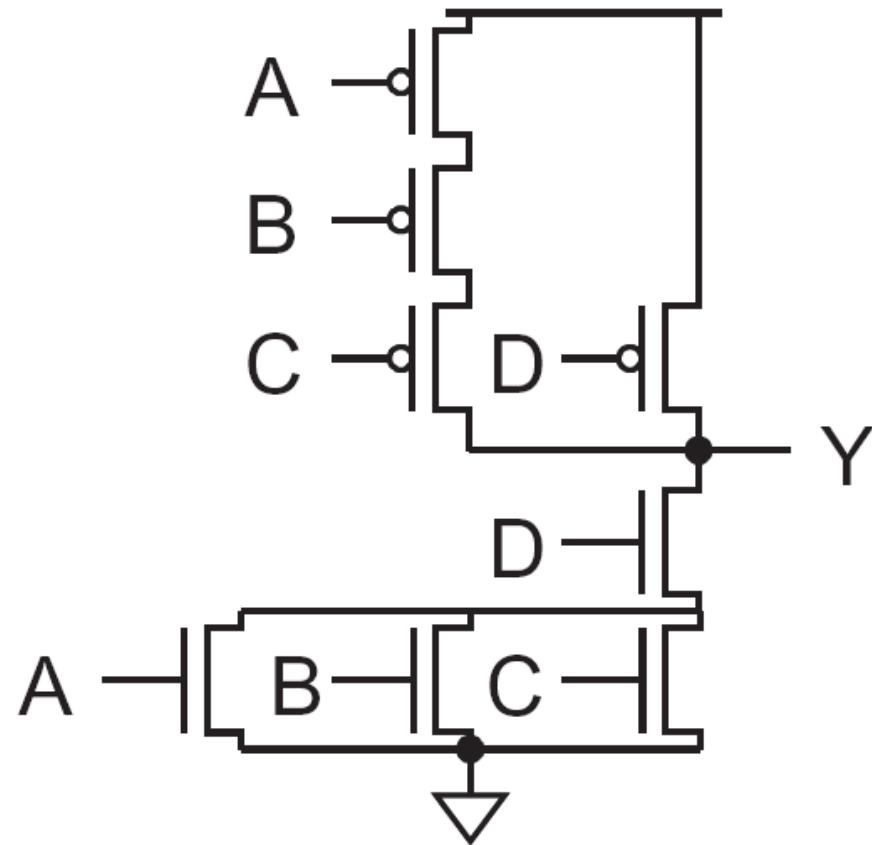


FIGURE 1.19

CMOS compound gate
for function
$$Y = \overline{(A + B + C)} \cdot D$$

Pass Transistors

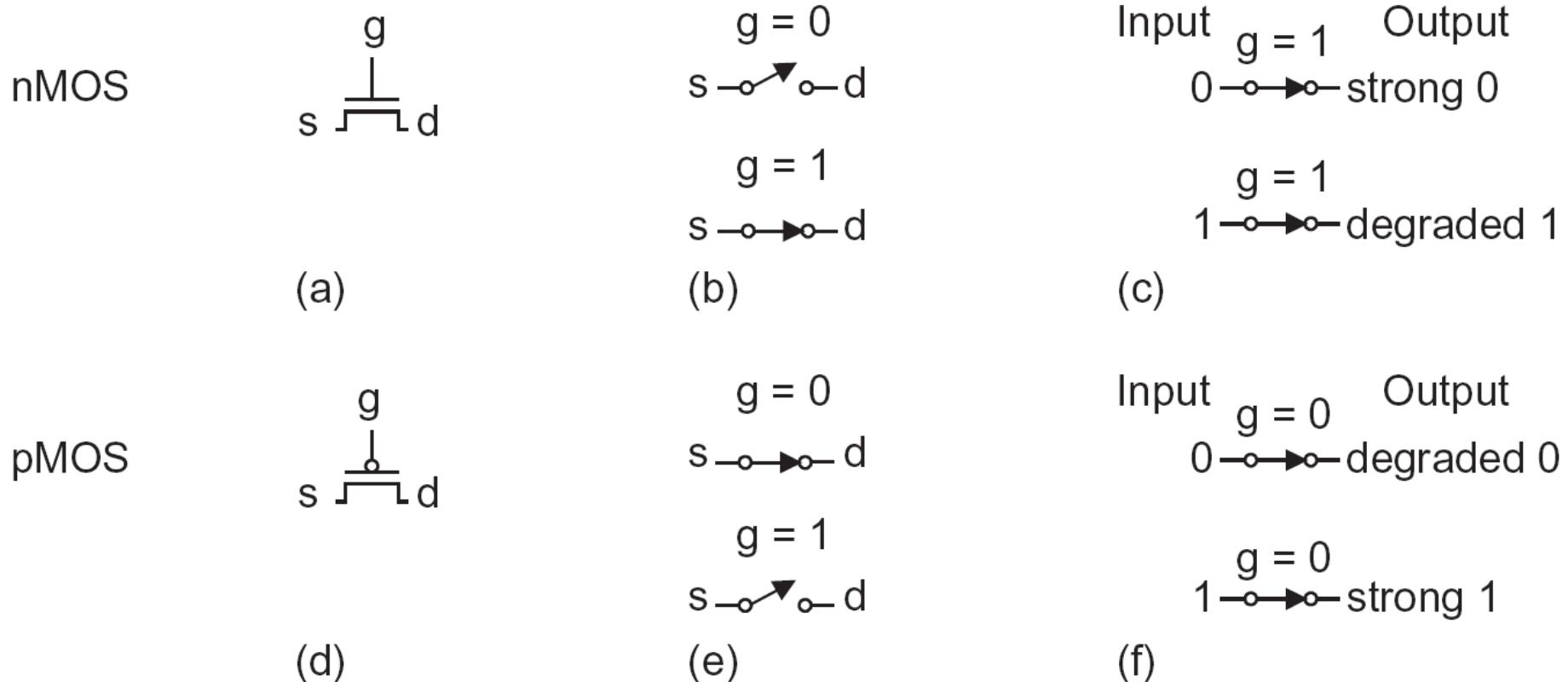
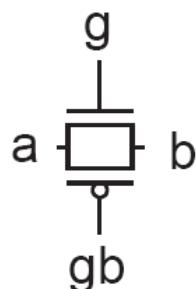


FIGURE 1.20 Pass transistor strong and degraded outputs

CMOS Switch

- Transmission Gate



(a)

$g = 0, gb = 1$
 $a \xrightarrow{\circ} \circ b$

$g = 1, gb = 0$
 $a \xrightarrow{\bullet} \circ b$

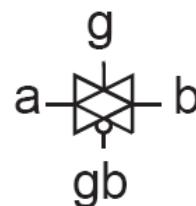
(b)

Input Output

$g = 1, gb = 0$
 $0 \xrightarrow{\circ} \bullet$ strong 0

$g = 1, gb = 0$
 $1 \xrightarrow{\bullet} \circ$ strong 1

(c)



(d)

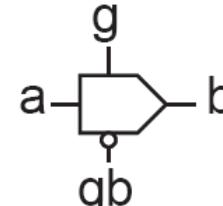
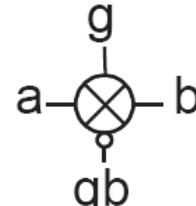
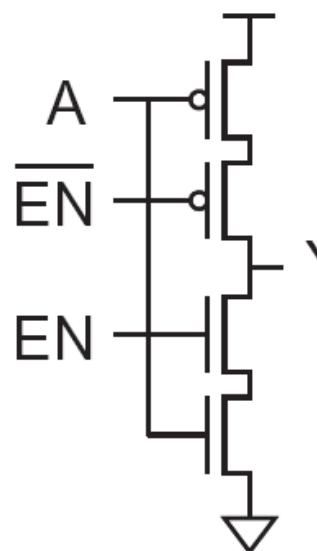


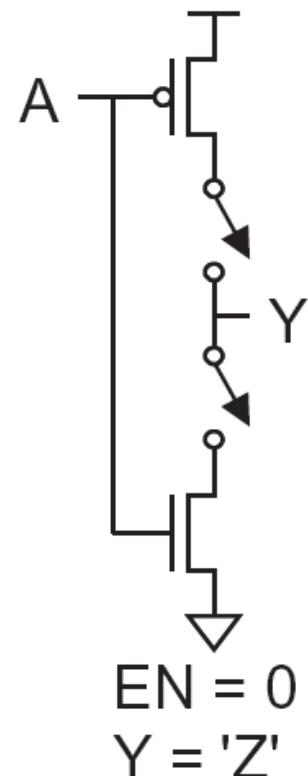
FIGURE 1.21 Transmission gate

Tri-state Inverter

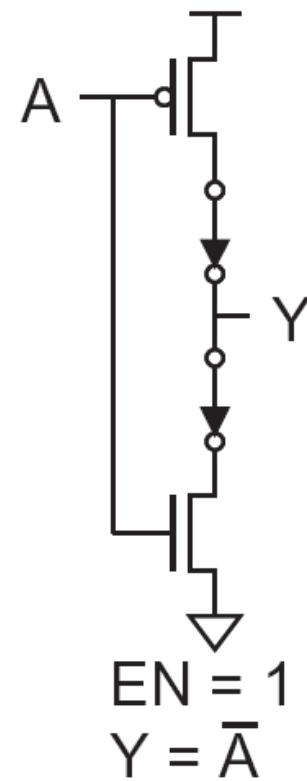
- Bus driver



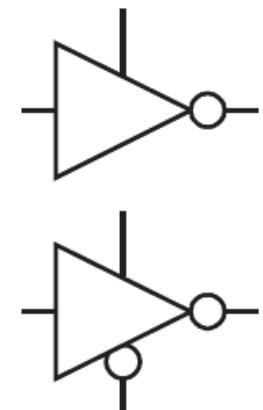
(a)



(b)



(c)

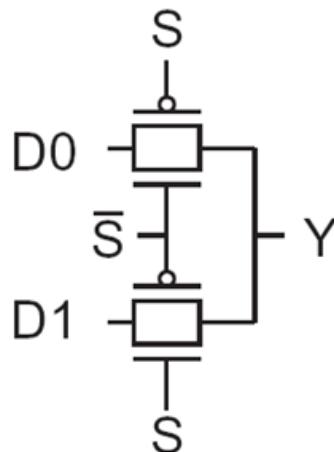


(d)

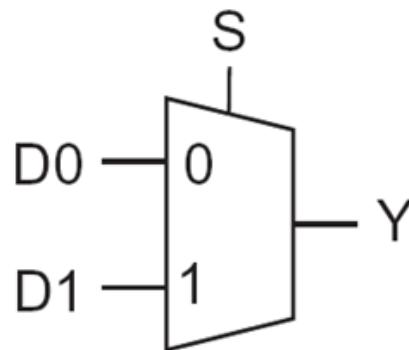
FIGURE 1.27 Tristate Inverter

Multiplexer

- Use transmission gates to build a 2-to-1 multiplexer.
- Note that transmission gates are "bilateral" devices, hence this multiplexer can also be looked upon as a 1-to-2 demultiplexer depending on which end is the driving (more forceful) end.



(a)



(b)

FIGURE 1.28 Transmission gate multiplexer

Static Inverting Multiplexer

- $Y = \overline{(D0 \bullet S' + D1 \bullet S)}$

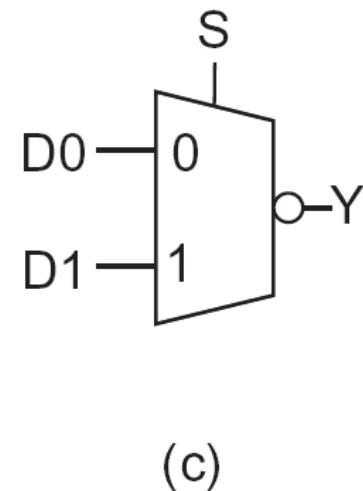
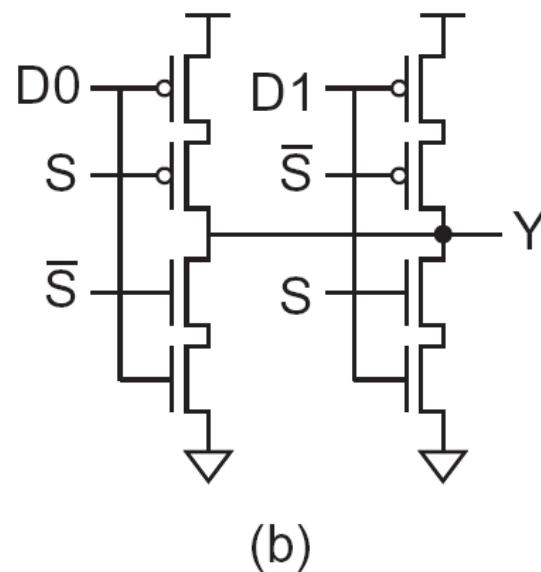
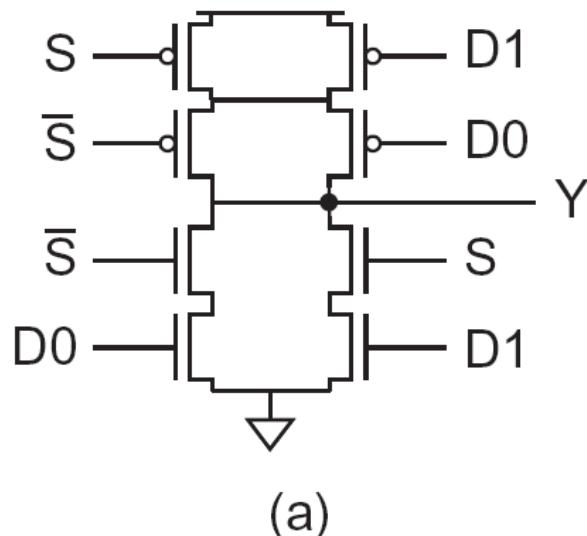


FIGURE 1.29 Inverting multiplexer