IC Design

Homework #1

Due on 10/18/2019, 1:20PM in class,
10% penalty for each day of delay

1. (20%) Please answer the following questions. Your answer should contain pictures and texts for better explanation. A single page of A4 is recommended.

   (a) As the fin width in a FINFET approaches 5nm, channel width variations could cause undesirable variability and mobility loss. One promising and futuristic transistor candidate–gate-all-around(GAA) FET–could circumvent the problem. Explain briefly, what is GAAFET, how does it work, as well as the main features and benefits of it. (學號尾數為單數者回答此題)

   (b) Resistive random access memory (RRAM) is regarded as one of the most promising emerging memory technologies for next-generation. Explain briefly, what is RRAM, how does it work, as well as the main features and benefits of it. (學號尾數為雙數者回答此題)

2. (15%) Sketch transistor-level schematics for the following logic functions using **static logic**. You may assume you have both true and complementary versions of the inputs available.

   (a) (5%) A 2:4 decoder defined by

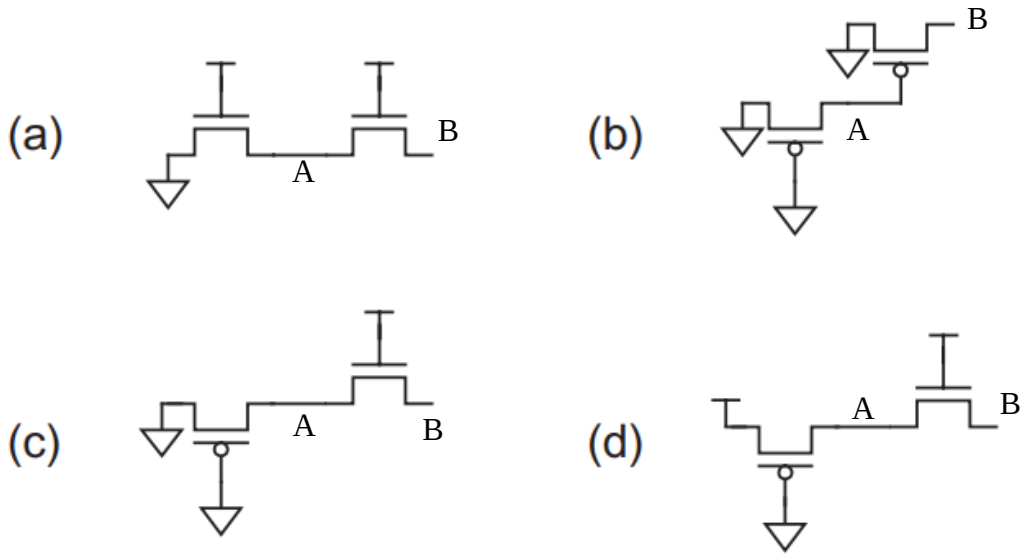
   $Y0 = \overline{A0} \cdot \overline{A1}$
   $Y1 = A0 \cdot \overline{A1}$
   $Y2 = \overline{A0} \cdot A1$
   $Y3 = A0 \cdot A1$

   (b) (5%) A 3:2 priority encoder defined by

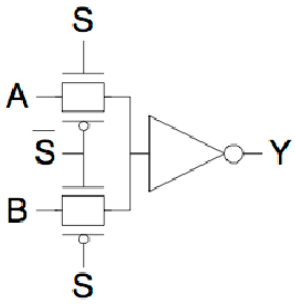
   $Y0 = \overline{A0} \cdot (A1 + \overline{A2})$
   $Y1 = \overline{A0} \cdot \overline{A1}$

   (c) (5%) $Y = \overline{((A+B)C+DEF)(GH+I)}$

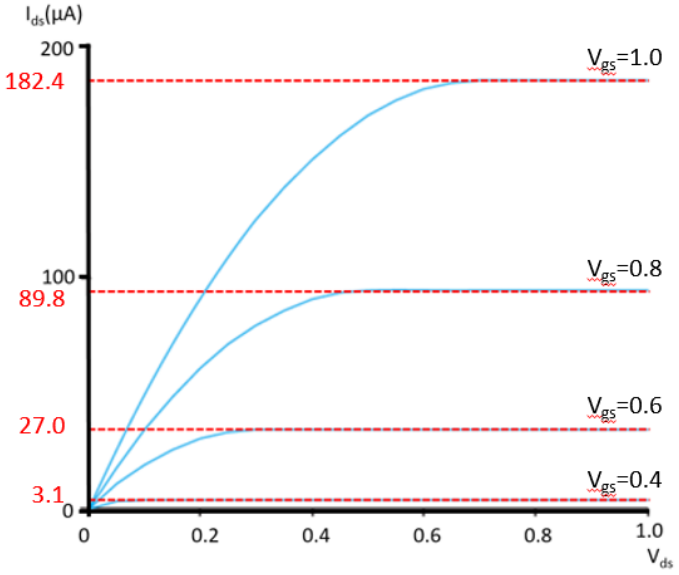
3. (20%) Give an expression for **all the node voltages** in the pass transistor networks shown below (neglect the body effect).
(You can use **V_{DD}, GND, $|V_{tp}|$, V_{tn}** to express your answer.)
(Assume that every NMOS has the same threshold voltage, and so does the PMOS.)



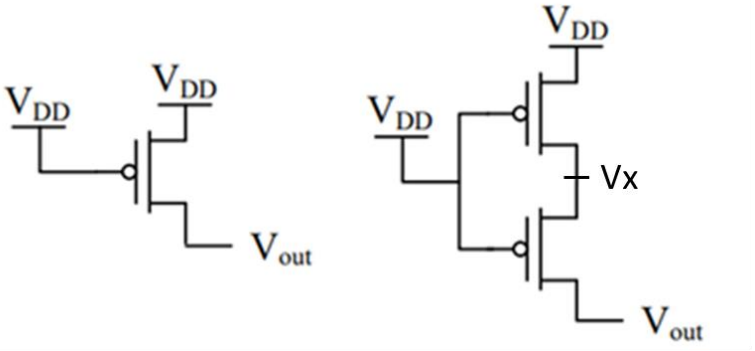
4. (15%) For the following transmission-gate circuit
(a) If you want to compute Y= $\overline{EF}$, how do you set A, B, and S? **Explain why.**
(b) If you want to compute Y= $\bar{E} \oplus \bar{F}$, how do you set A, B, and S? **Explain why.**



5. (10%) For the following I-V curves of an NMOS transistor, given the Isat of all four curves. Estimate a precise value of V_t (小數點以下兩位). Explain how you find this value from four I_{sat}.



6. (20%) Stacking transistors is a circuit technique to reduce leakage current. Assume V_{out} = 0.9V, V_{DD} = 1V. $|V_{tp}|$ = 0.3V. Please estimate $I_{non\text{-}stack}$/ I_{stack}., where I_{stack} denotes the leakage current in (b), $I_{non\text{-}stack}$ denotes the leakage current in (a).



(a) (b)

Hint: (1) sub-threshold current for PMOS:

$$I_{sub} = I_0 \times e^{\frac{V_{SG}}{n \cdot v_t}} \times \left(1 - e^{\frac{-V_{SD}}{v_t}}\right), n = 1, v_t = 26mV$$

(2) compute Vx first when solving I_{stack}

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HW1 Office hours: 10/15 19:00-21:00 @ 博理 114 室
Office hours: 10/17 19:00-21:00 @ 博理 114 室

If you have no time during the office hours, you can email TA to discuss another time for appointment.