Chapter 5

Wires (Interconnect)

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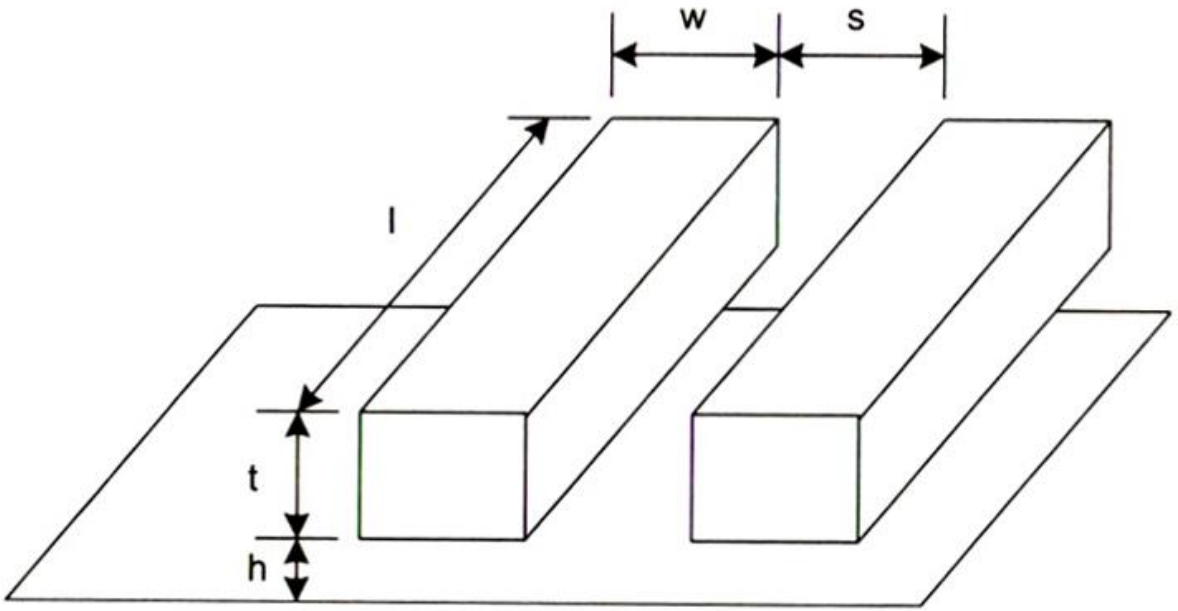
Interconnect

- Pitch = w + s
- Aspect ratio = t/w, about 2 in modern processes.



Metal Layers

- More than 6 layers in modern processes (e.g. 0.13um)
- M1 is thin, narrow, used for high-density cell routing
- M2-M4, thicker, longer range routing.
- M5-M6, thickest, for GND, VDD, CLK.

Layer	t (nm)	w(nm)	s(nm)	AR
6	1720	860	860	2.0
	1000			
5	1600	800	800	2.0
	1000			
4	1080	540	540	2.0
	700			
3	700	320	320	2.2
	700			
2	700	320	320	2.2
	700			
1	480	250	250	1.9
	800			

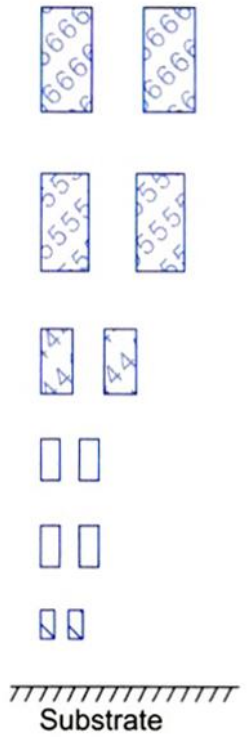
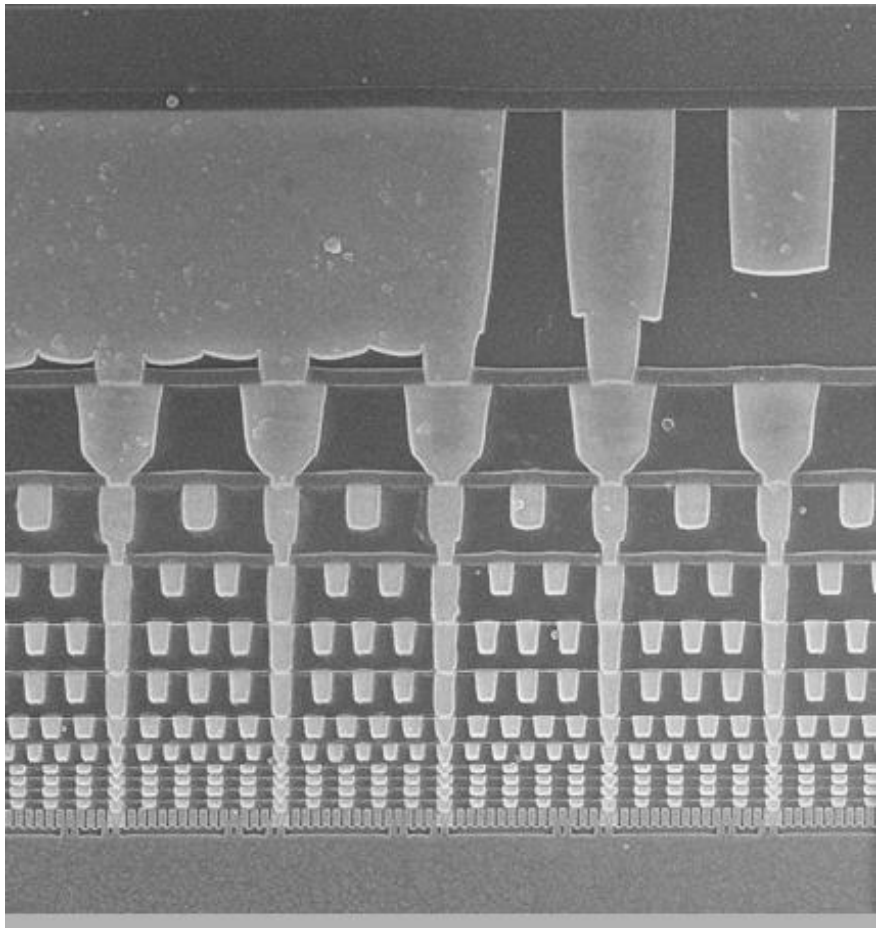


Photo of Metal Stack

- Intel 14nm FinFET process has 13 layers of metal.

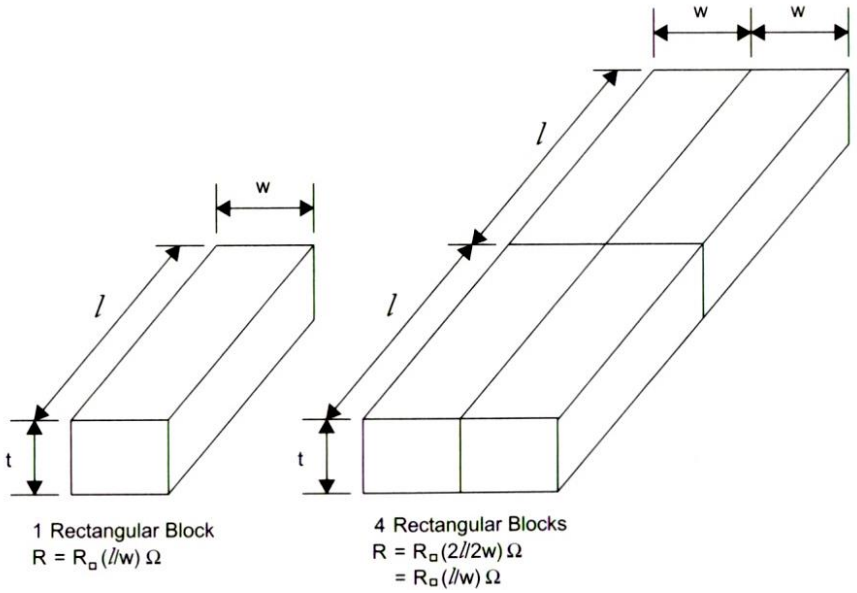


Resistance Estimation

- The resistance of a uniform slab of conducting material is given by

$$R = \frac{\rho}{t} \cdot \frac{l}{w} = R_S \cdot \frac{l}{w}$$

where ρ is the resistivity, t, l, and w are the thickness, length, and width of the conductor respectively. R_S is the sheet resistance having units of ohm/square.



More Resistance

- Until 0.18um, mos
- Modern processes
  - Copper diffuses int
- Diffusion and poly: resistivity.
- All resistances incr

British Dictionary definitions for silicide

silicide

/ˈsɪlɪˌsaɪd/

noun

1. any one of a class of binary compounds formed between silicon and certain metals

Table 4.6 Bulk resistivity of pure metals at 22° C

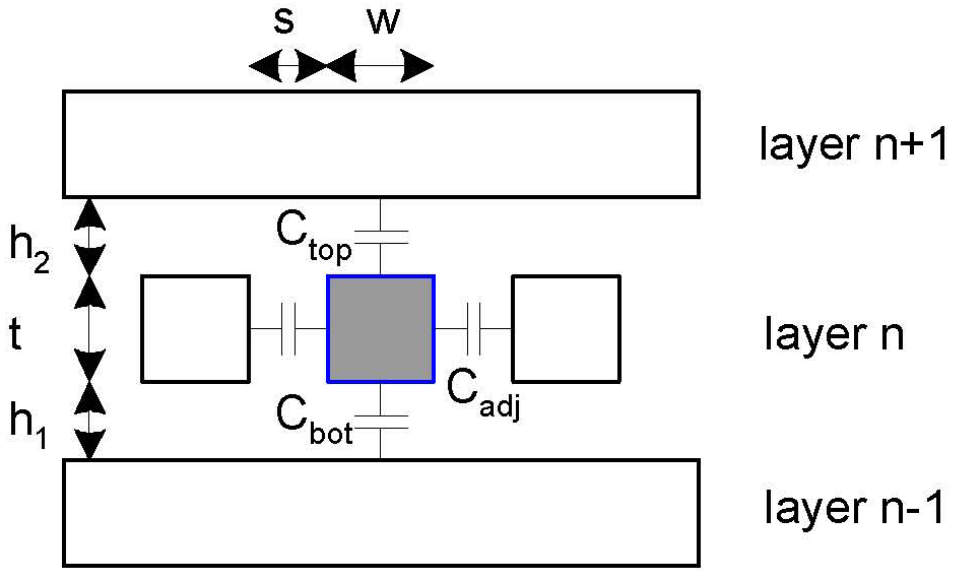
Metal	Resistivity (μΩ • cm)
Silver (Ag)	1.6
Copper (Cu)	1.7
Gold (Au)	2.2
Aluminum (Al)	2.8
Tungsten (W)	5.3
Molybdenum (Mo)	5.3
Titanium (Ti)	43.0

Table 4.7 Sheet resistances

Layer	Sheet Resistance (Ω /□)
Diffusion (silicided)	3-10
Diffusion (unsilicided)	50-200
Polysilicon (silicided)	3-10
Polysilicon (unsilicided)	50-400
Metal1	0.08
Metal2	0.05
Metal3	0.05
Metal4	0.03
Metal5	0.02
Metal6	0.02

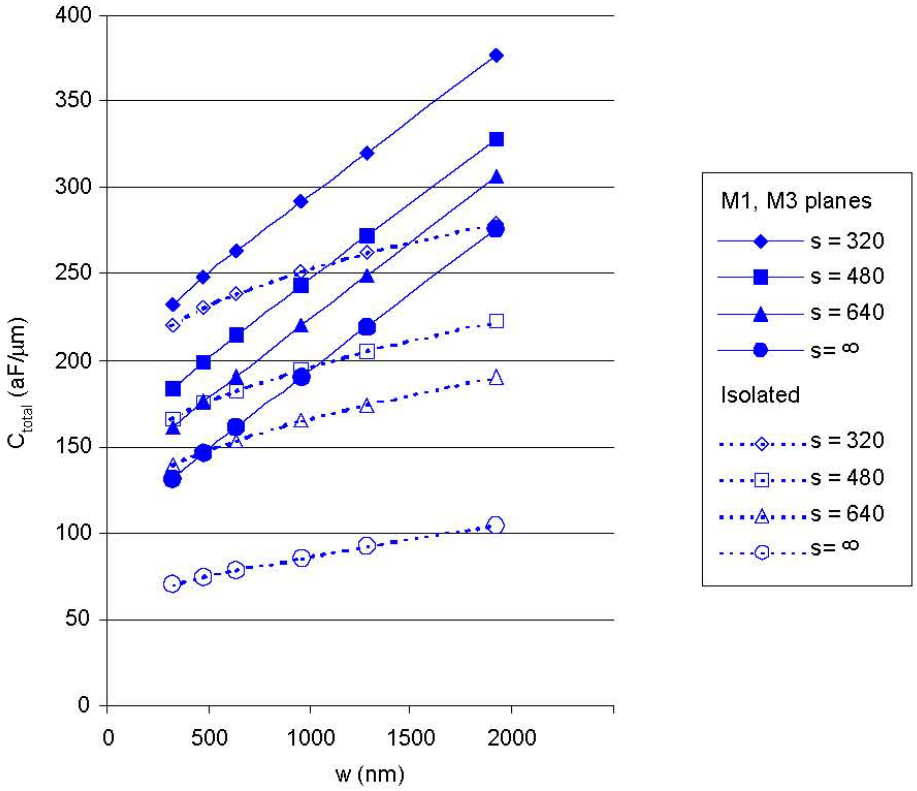
Interconnect Capacitance

- Wire has capacitance per unit length
  - To neighbors
  - To layers above and below
- $C_{total} = C_{top} + C_{bot} + 2C_{adj}$



Typical Metal Wire Capacitance

- Typical wires have ~ 0.2 fF/μm
  - Isolated wire capacitance is lower and more sensitive to spacing, while sandwiched wire capacitance is more sensitive to width.
  - Compare to 2 fF/μm for gate capacitance

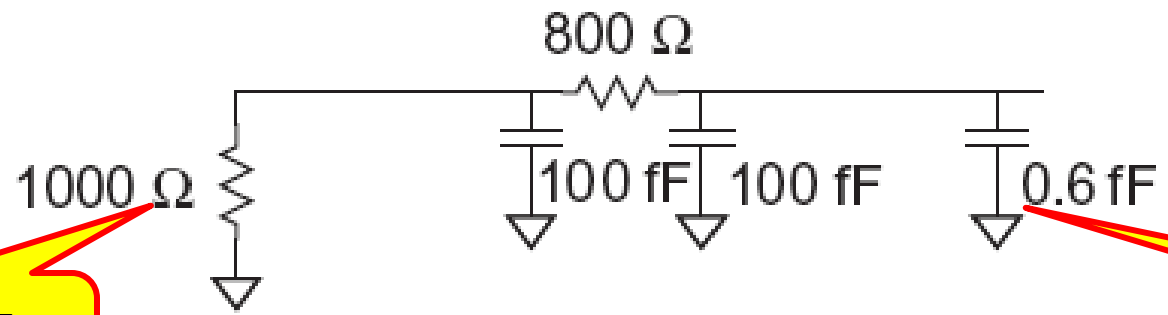


Diffusion & Polysilicon

- Diffusion capacitance is very high (1-2 fF/μm)
  - Comparable to gate capacitance
  - Diffusion also has high resistance
  - Avoid using diffusion *runners* for wires!
- Polysilicon has lower C but high R
  - Use for transistor gates
  - Occasionally for very short wires between gates

Wire RC Delay

- Estimate the delay of a 10x inverter driving a 2x inverter at the end of the 1 mm wire. Assume wire capacitance is 0.2 fF/μm and that a unit-sized nMOS has R = 10 KΩ and C = 0.1 fF. The wire resistance is 800 ohm.
  - Use π model for long wire
  - t_{pd} = (1000 Ω)(100 fF) + (1000 + 800 Ω)(100 + 0.6 fF) = 281 ps



10K /10X = 1K

W=2 NMOS + 4 PMOS

Crosstalk

- A wire has high capacitance to its neighbor.
  - When the neighbor switches from 1 -> 0 or 0 ->1, the wire tends to switch too.
  - Called capacitive coupling or crosstalk.
- Crosstalk effects
  - Noise on nonswitching wires
  - Increased delay on switching wires
- Large load and short wire will not have significant crosstalk while long wires in parallel (e.g. bus lines) tend to have serious crosstalk.

Effective Capacitance

- Assume layers above and below on average are quiet
  - Second terminal of capacitor can be ignored
  - Model as Cgnd = Ctop + Cbot
- Effective Cadj depends on behavior of neighbors
  - Miller effect – Miller Coupling Factor (MCF)

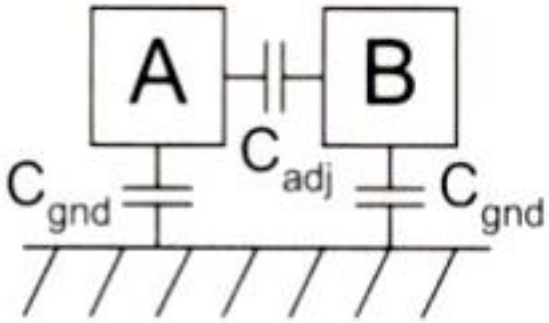


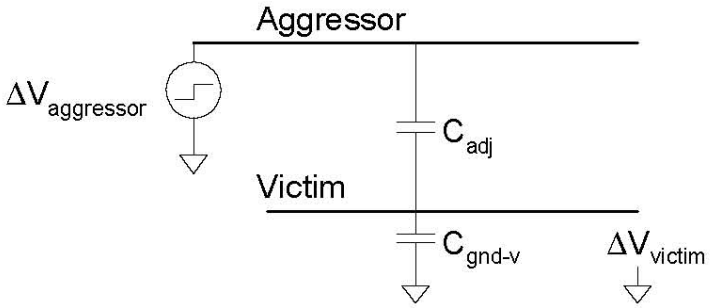
Table 4.10 Dependence of effective capacitance on switching direction

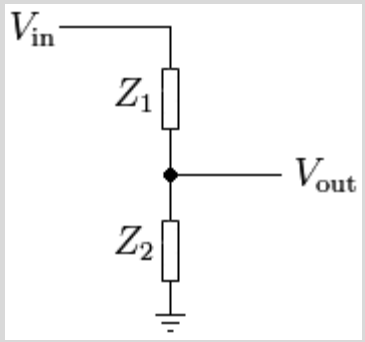
B	ΔV	$C_{eff(A)}$	MCF
constant	V_{DD}	$C_{gnd} + C_{adj}$	1
switching same direction as A	0	C_{gnd}	0
switching opposite to A	$2V_{DD}$	$C_{gnd} + 2C_{adj}$	2

Crosstalk Noise

- Crosstalk causes noise on nonswitching wires
- If victim is floating:
  - model as capacitive voltage divider

$$\Delta V_{victim} = \frac{C_{adj}}{C_{gnd-v} + C_{adj}} \Delta V_{aggressor}$$





Capacitive dividers do not pass DC input. For an AC input a simple capacitive equation is:

$$V_{out} = V_{in} \cdot \frac{C_1}{C_1 + C_2}$$

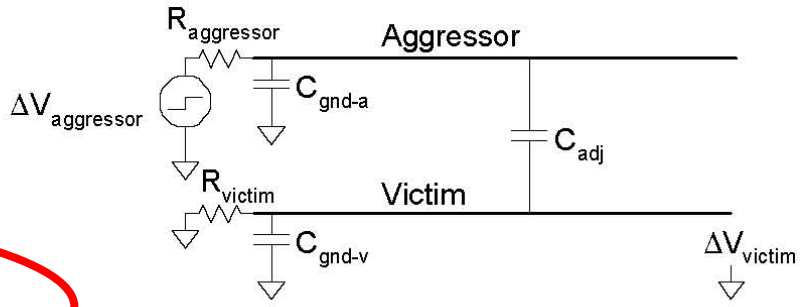
http://en.wikipedia.org/wiki/Voltage_divider

Driven Victims

- Usually victim is driven by a gate that fights noise
  - Noise depends on relative driving strengths
  - k > 0, k gets larger as the victim is driven more.

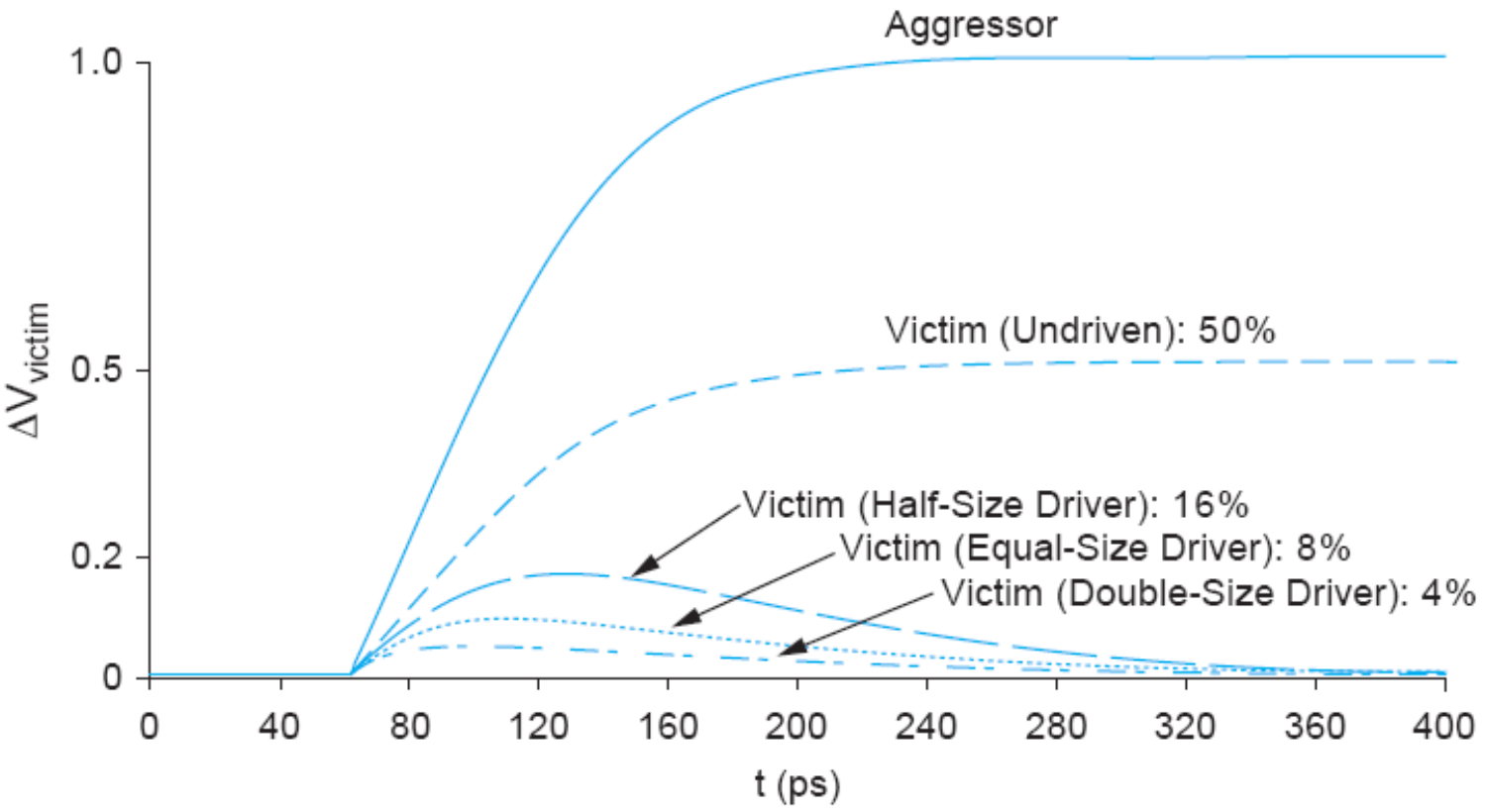
$$\Delta V_{victim} = \frac{C_{adj}}{C_{gnd-v} + C_{adj}} \frac{1}{1+k} \Delta V_{aggressor}$$

$$k = \frac{\tau_{aggressor}}{\tau_{victim}} = \frac{R_{aggressor}\left(C_{gnd-a} + C_{adj}\right)}{R_{victim}\left(C_{gnd-v} + C_{adj}\right)}$$



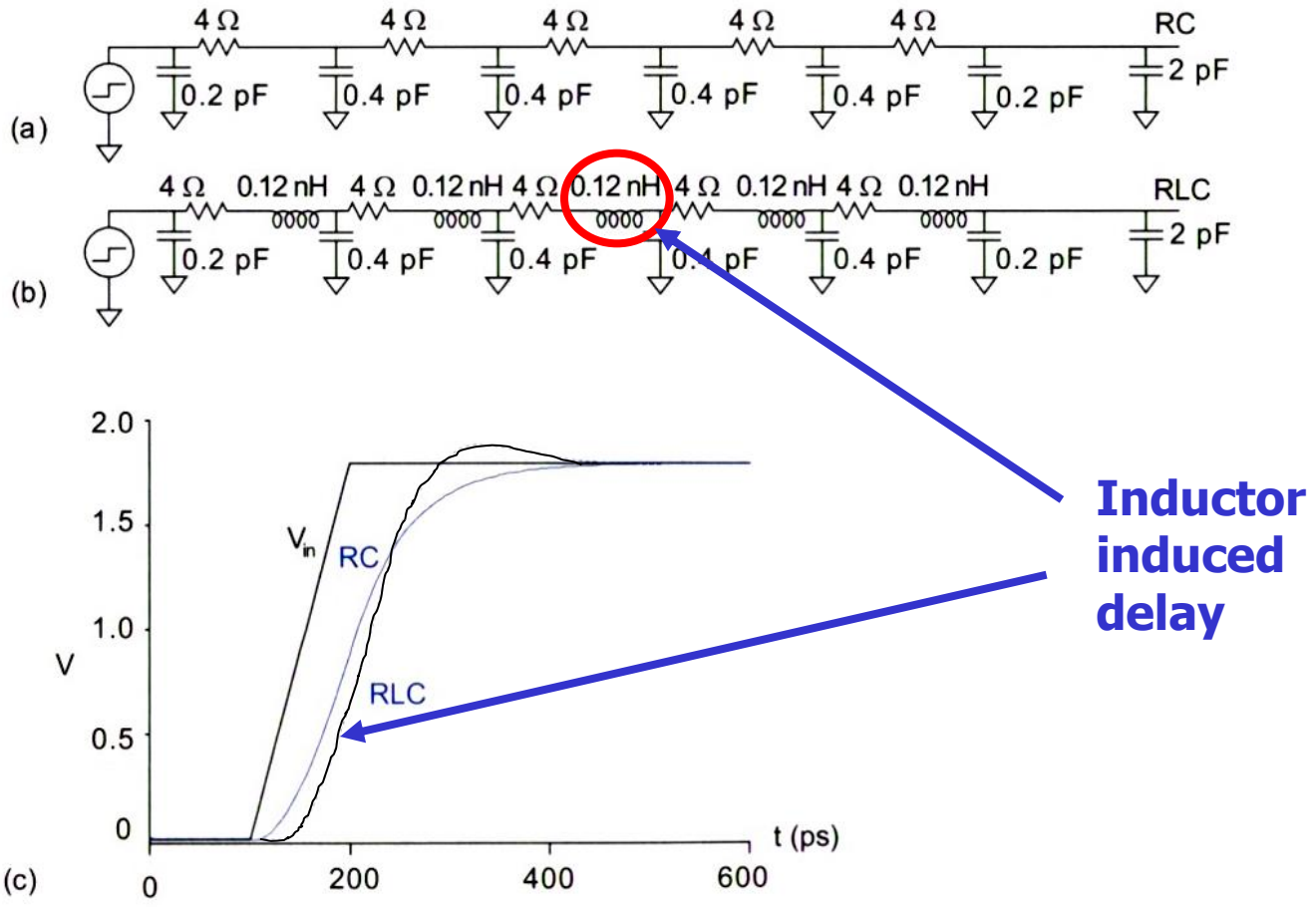
Coupling Waveforms

- Simulated coupling for $C_{adj} = C_{gnd}$



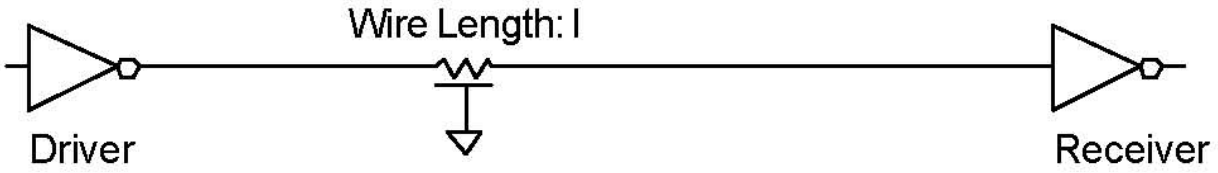
Wire Inductance

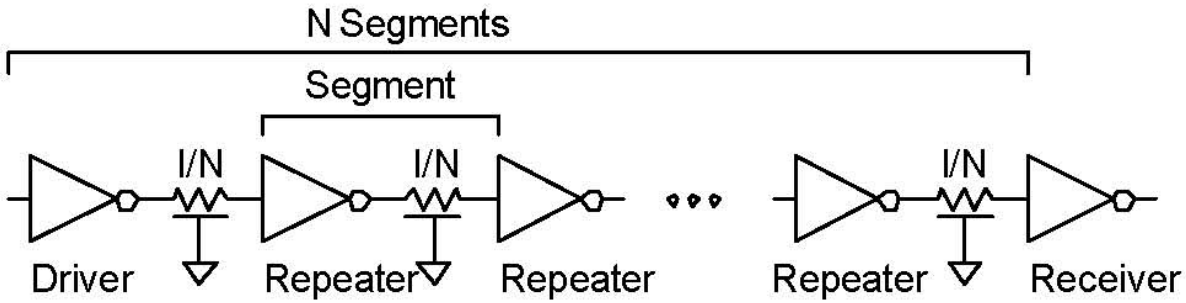
- Fast-switching wires can have significant inductor-induced delay.

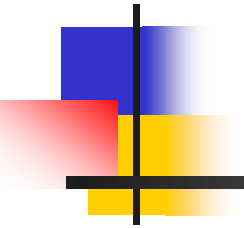


Repeaters

- R and C are proportional to l
- RC delay is proportional to l^2
  - Unacceptably great for long wires
- Break long wires into N shorter segments
  - Drive each one with an inverter or buffer







補充教材

Wire Engineering

- Width/Spacing – wider wires not only decrease R but also increase C. But they can be necessary to decrease IR drop.
- Layer selection
- Shielding topology

Table 4.11 Sample metal layer usage in 6-level process

Layer	Purpose
Metal 1	Interconnect within cells
Metal 2/3	Interconnect between cells within units
Metal 4/5	Interconnect between units, critical signals
Metal 6	I/O pads, clock, power, ground