Lecture 12

Date: March 1st, 2011

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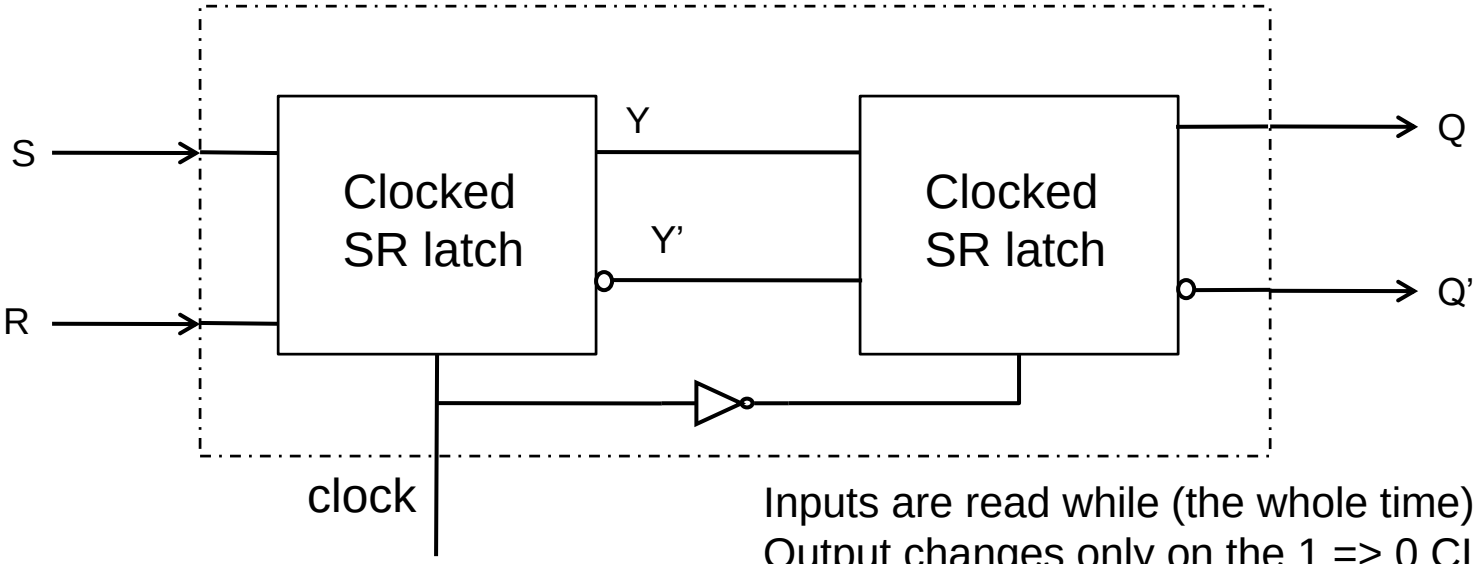
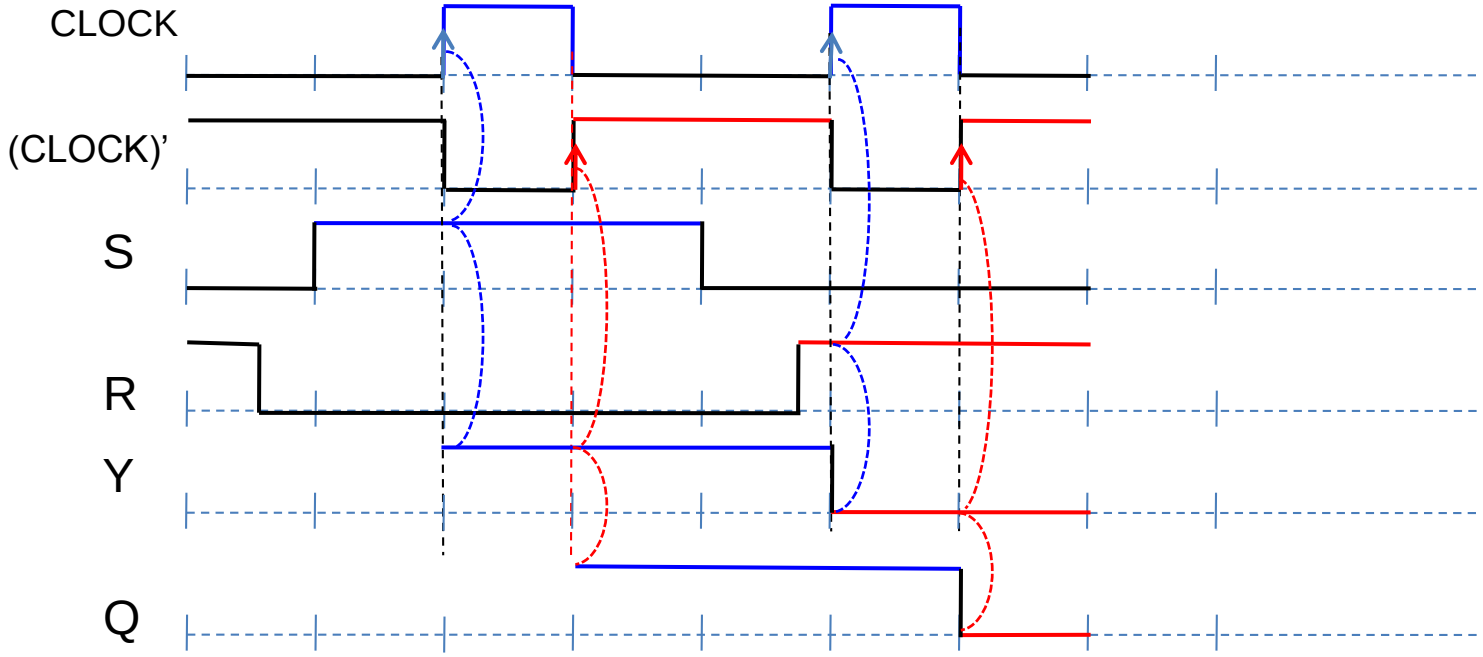
Today

- SR latch
- Develop SR master–slave flip-flop
- Clock
- Type of flip-flop clocking:
  - positive-edge, negative-edge, master-slave
- Reading sequential circuits

Review: a Clocking Solution: Master-Slave



Inputs are read while (the whole time) CLK = 1
Output changes only on the 1 => 0 CLK transition



Types of Flip-Flops

D Flip-Flop

Next-State Table

D	Q^+
0	0
1	1

Excitation Table

Q Q^+	D
0 0	0
0 1	1
1 0	0
1 1	1

T Flip-Flop

Next-State Table

T	Q^+
0	Q
1	Q'

Excitation Table

Q Q^+	T
0 0	0
0 1	1
1 0	1
1 1	0

SR Flip-Flop

Next-State Table

S R	Q^+
0 0	Q
0 1	0
1 0	1
1 1	?

Excitation Table

Q Q^+	S	R
0 0	0	x
0 1	1	0
1 0	0	1
1 1	x	0

JK Flip-Flop

Next-State Table

J K	Q^+
0 0	Q
0 1	0
1 0	1
1 1	Q'

Excitation Table

Q Q^+	J	K
0 0	0	x
0 1	1	x
1 0	x	1
1 1	x	0

Combinational vs. Sequential Circuits

Combinational:

1. No memory
2. Output a function only of current inputs
3. Build using only combinational components (AND, OR, NOT gates, etc.)

Sequential:

1. Has memory
2. Output a function of current inputs & previous inputs
3. Build using only combinational components & storage elements (latches, FF's)

State of a Sequential Circuit

The state is the binary information stored at any given time.

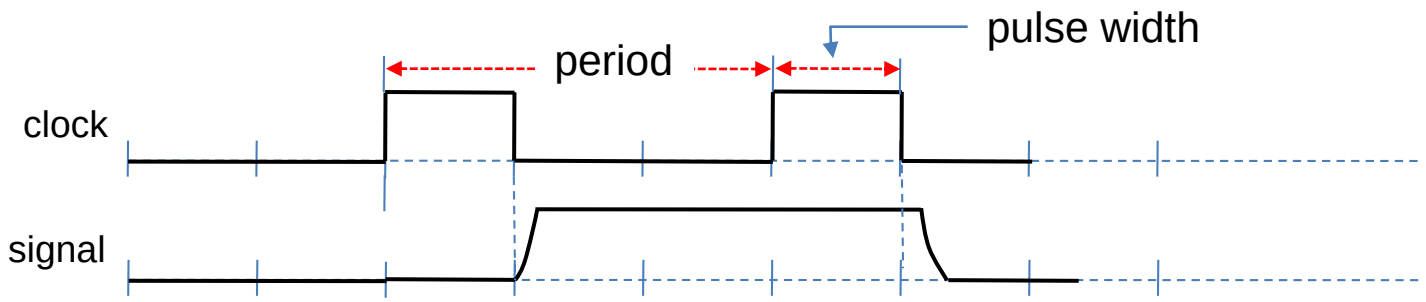
Synchronous Circuits

All storage elements are clocked: their states change simultaneously at fixed intervals, specified by a period input called clock.

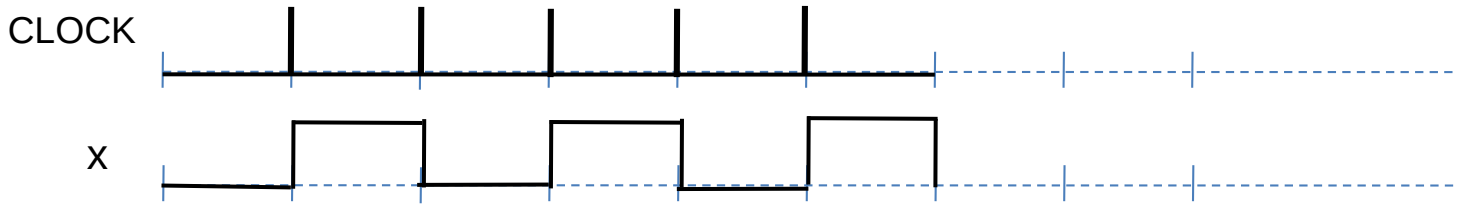
Clocking Requirements

- Clock period must be long enough for network to stabilize
- Clock pulse must be long enough to provide sufficient switching energy to the flip-flops

Actual case master-slave flip-flop

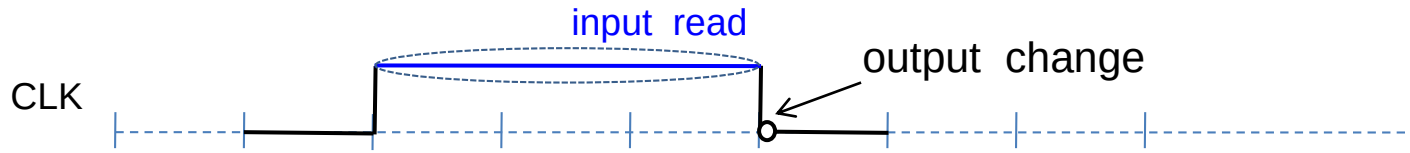


Ideal model (ideal clock)

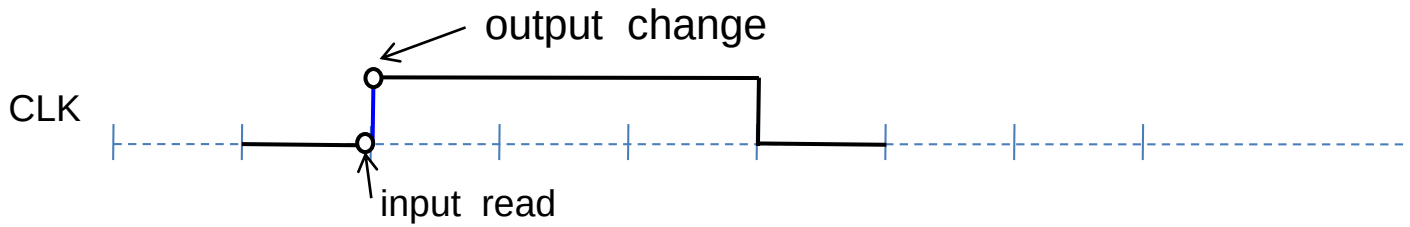


Flip-Flop Clocking (1)

A ***master-slave flip-flop*** changes state on the falling CLK edge, based on the S and R values while CLK = 1 and immediately prior to 1 => 0 CLK transition

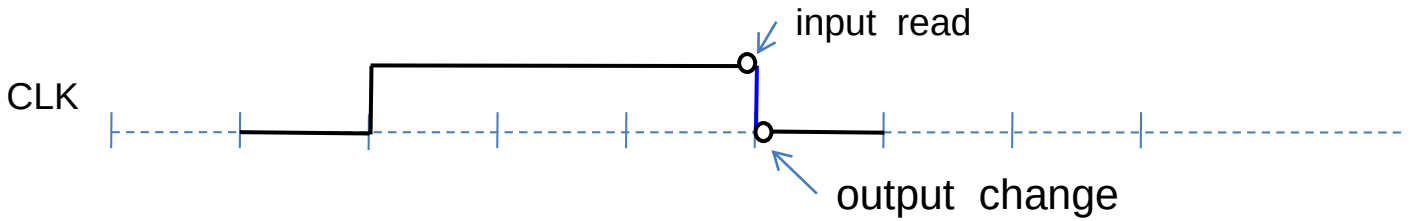


A ***positive-edge-triggered flip-flop*** changes state on the rising CLK edge, based on the S and R values immediately prior to 0 => 1 CLK transition



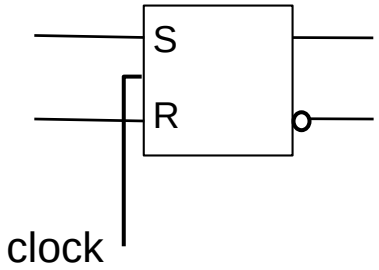
Flip-Flop Clocking (2)

A *negative-edge-triggered flip-flop* changes state on the falling CLK edge, based on the S and R values immediately prior to 1 => 0 CLK transition

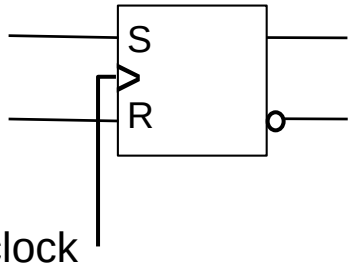


Types of flip-flops

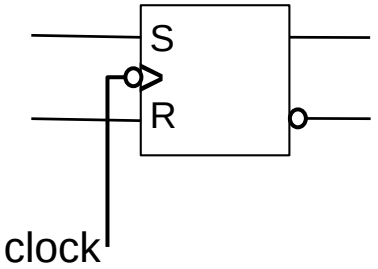
master-slave



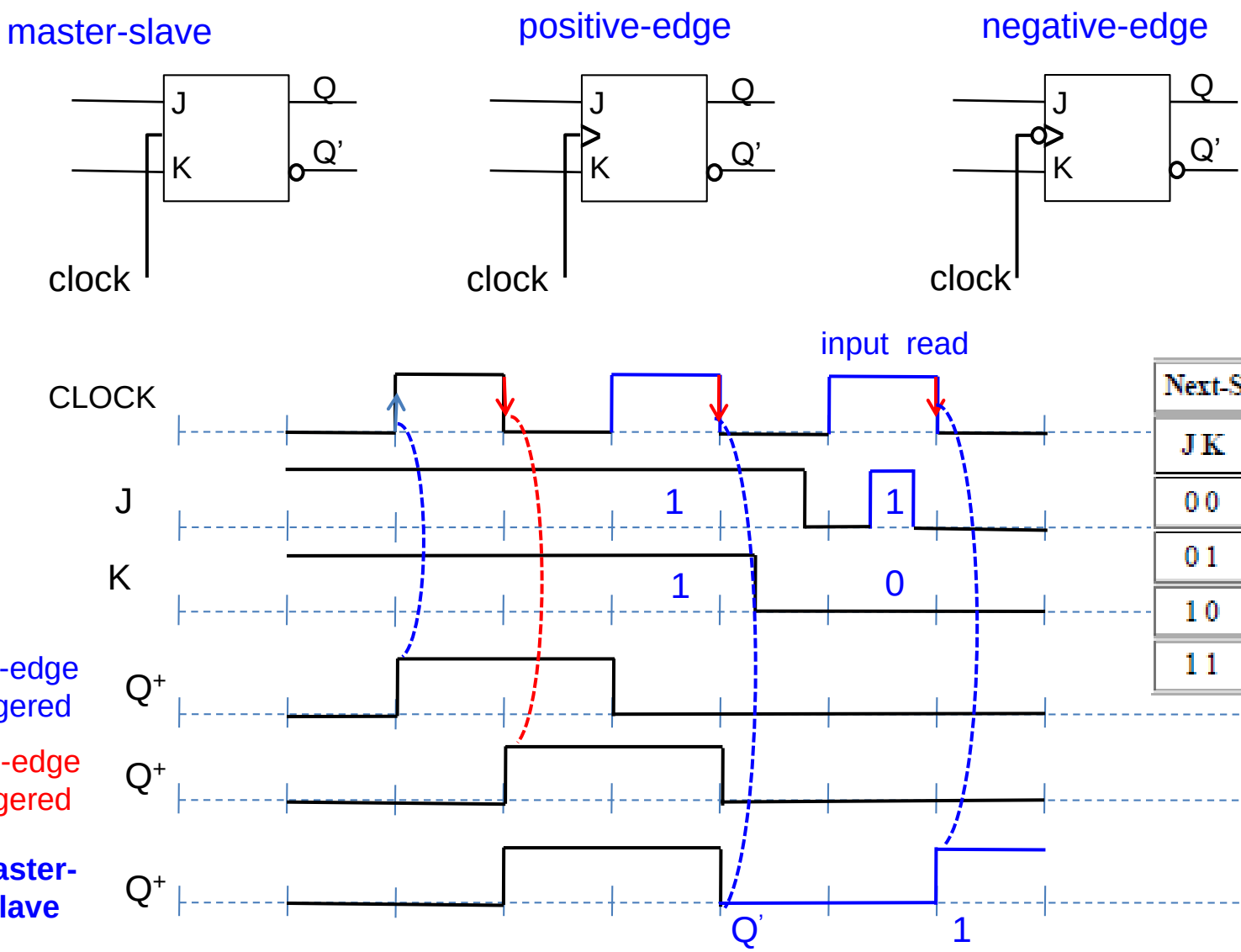
positive-edge



negative-edge

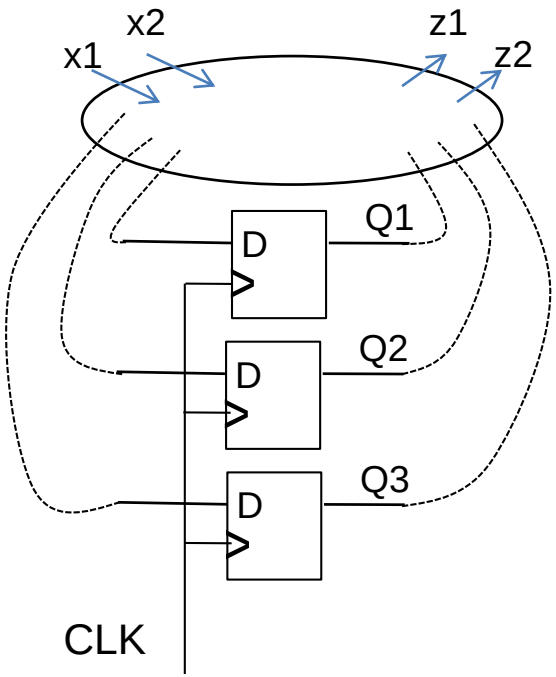


Types of Flip-flop Clocking



Assume initially Q = 0

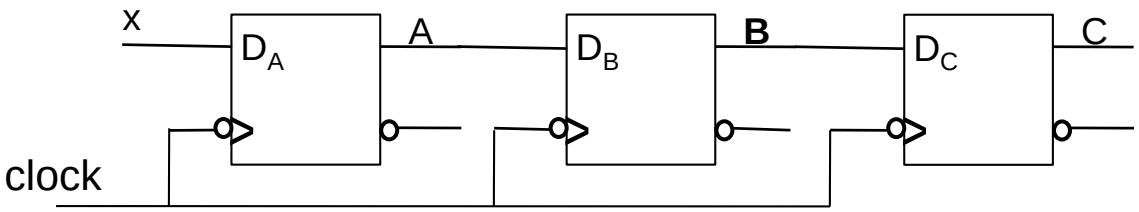
State Variables vs. States



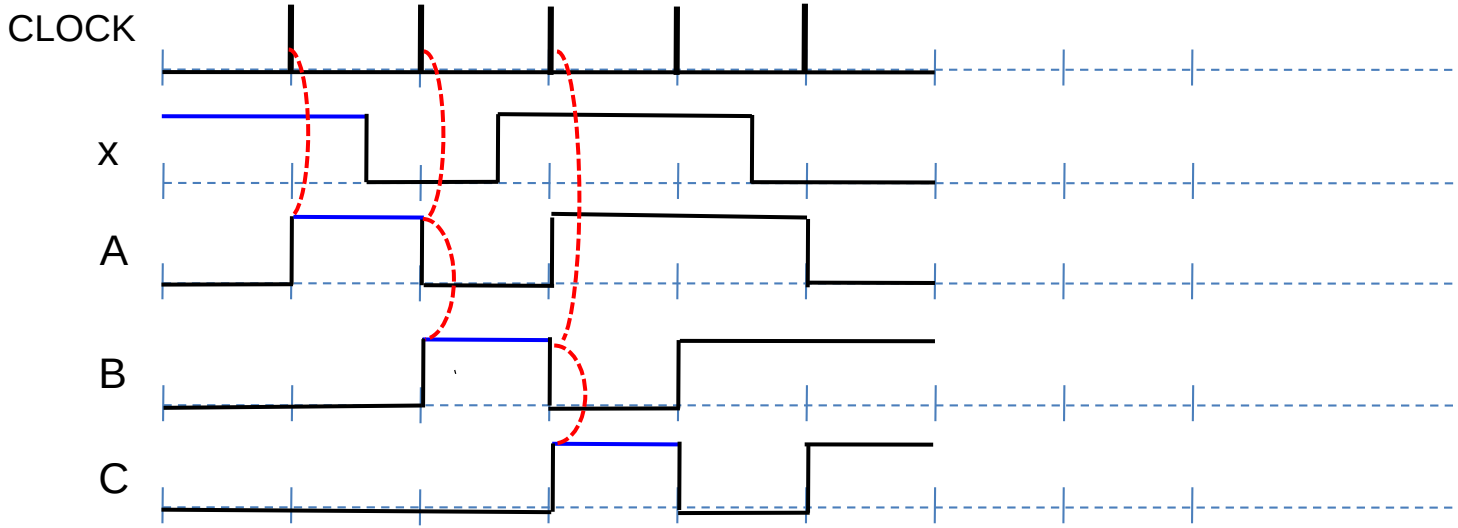
- State in a sequential circuit is the binary information stored at any given time.
- When state changes occur?
  - only at the clock pulse
- When can output change?
  - when the state changes

    or
  - when the inputs change
- How many states are there?
  - 1 FF => 1 state var, 2 states: 0, 1
  - 2 FFs => 2 state var's, 4 states: 00, 01, 10, 11
  - 3 FFs => 3 state var's, 8 states: 000, 001, …., 111

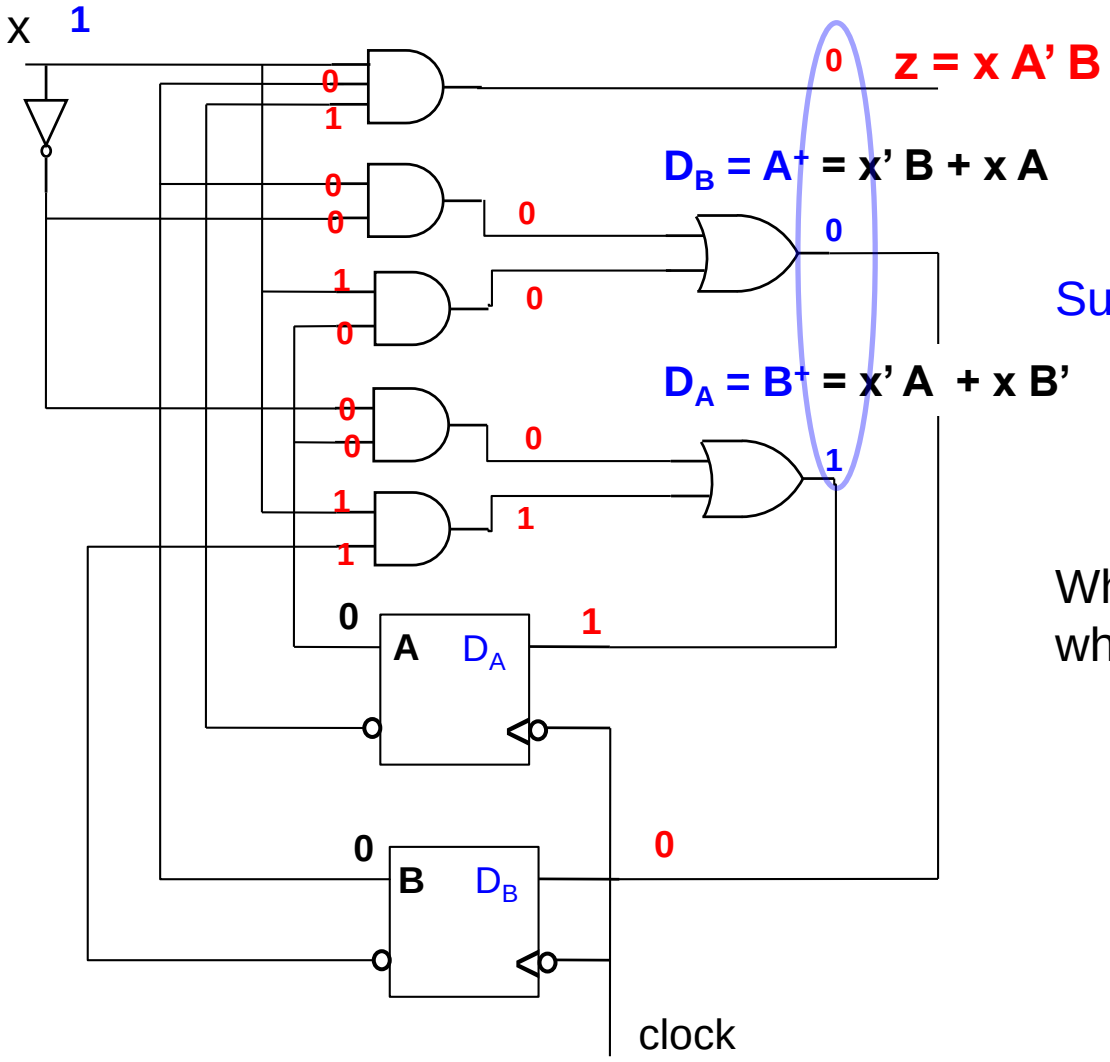
Simple Sequential Circuit Timing Diagram
D Flip-Flops



Assume:
A = B = C = 0



Sequential Network Analysis Example
D Flip-Flops



Suppose we are in **state 00 and x=1**

A	B	x
0	0	1

What is our **current output** and what will be the **next state**?

A^+	B^+	z
1	0	0

Sequential Network Analysis Example
D Flip Flops (cont.)

Flip-flop inputs:

$D_A = x' A + x B'$

$D_B = x' B + x A$

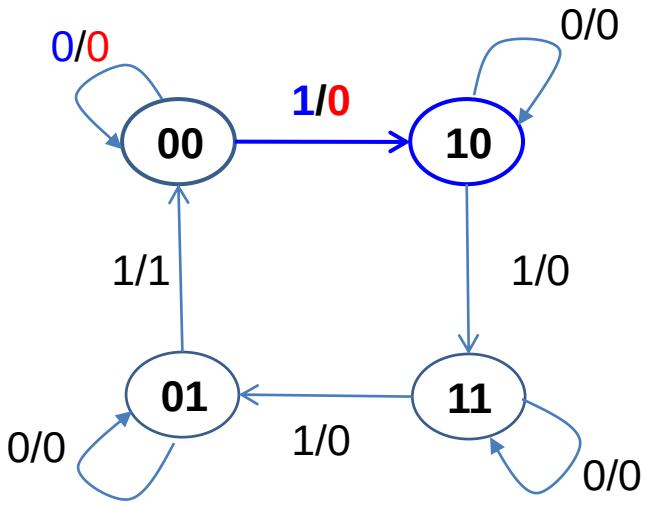
Flip-flop outputs:

$z = x B A'$

Next state table:

Current state		input	FF inputs		Next state		output
A	**B**	**x**	**D_A**	**D_B**	**A^+**	**B^+**	**z**
0	0	0	0	0	0	0	**0**
0	**0**	**1**	1	0	**1**	**0**	**0**
0	1	0	0	1	0	1	**0**
0	1	1	0	0	0	0	**1**
1	0	0	1	0	1	0	**0**
1	0	1	1	1	1	1	**0**
1	1	0	1	1	1	1	**0**
1	1	1	0	1	0	1	**0**

State diagram:



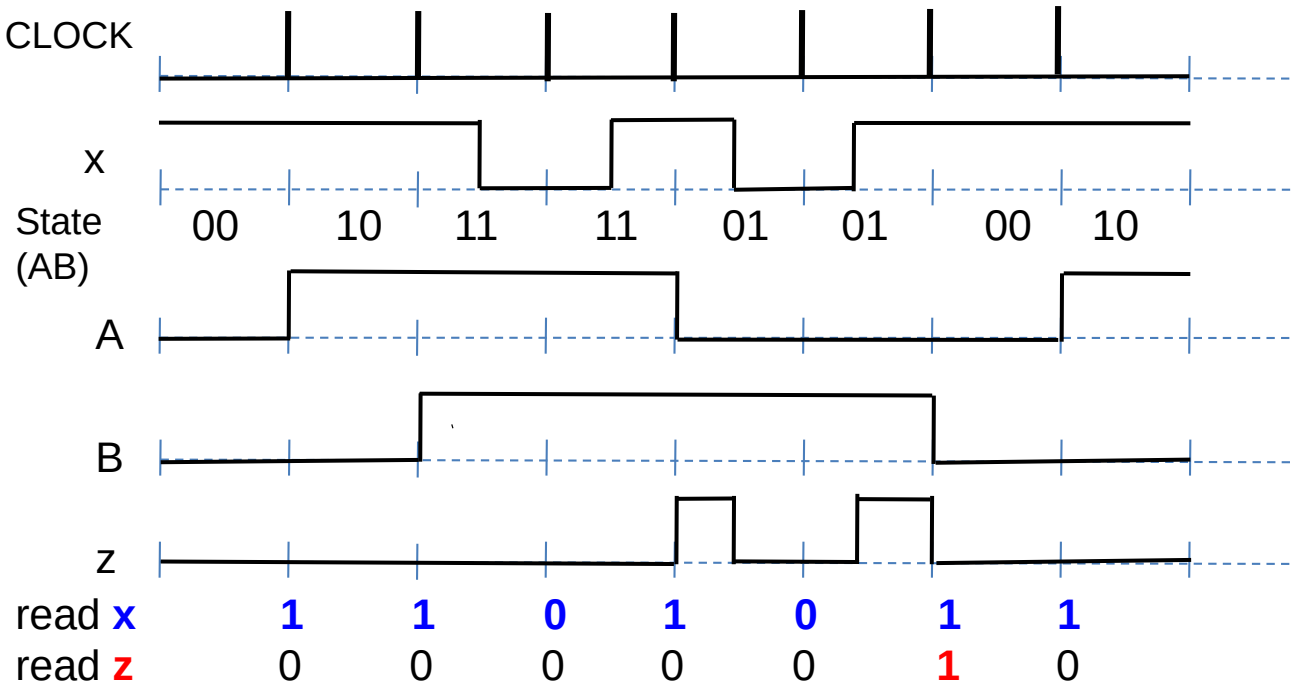
States: AB or A^+B^+

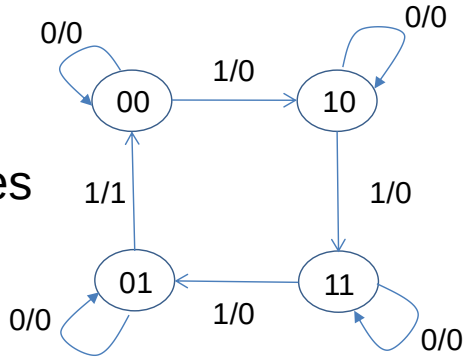
Label: x/z (input/output)

Sequential Network Analysis Example (cont.)

What does this circuit do?

Examine a timing diagram
Given input x, determine output z and the sequence of states
Assume initial state is 00





Meaning of states:

00 start, read 4 1's, 8 1's …

01 read 111, 7 1's, 11 1's …

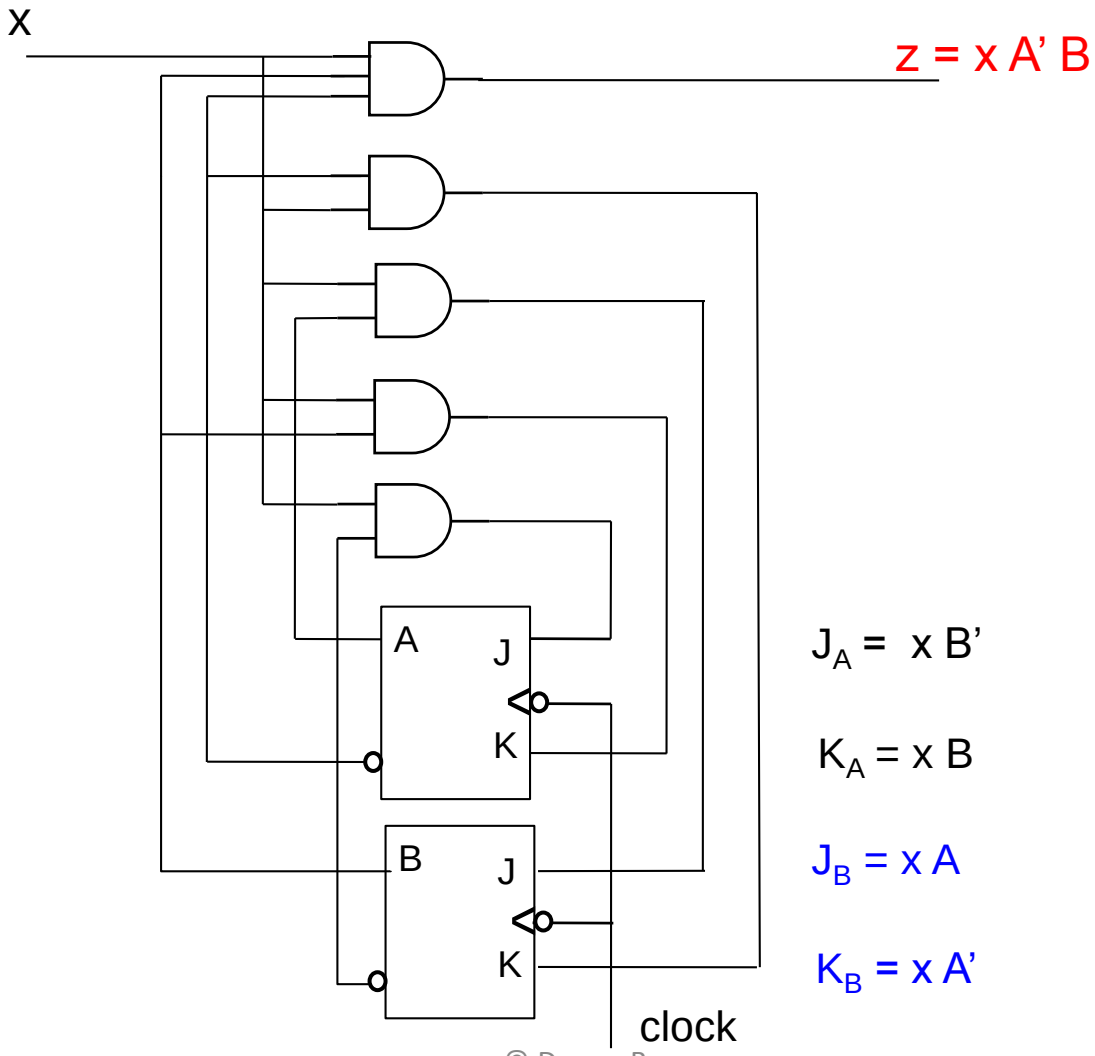
11 read 11, 6 1's, 10 1's, …

10 read 1, 5 1's, 9 1's, …

z = 1 when the number of 1's read thus far is *0 mod 4* (and >= 4)

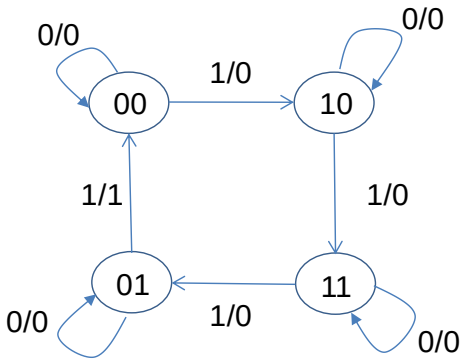
Sequential Network Analysis Example

JK Flip-Flops



Sequential Network Analysis Example

JK Flip Flops (cont.)



Flip-flop inputs:

$J_A = x B'$ $J_B = x A$

$K_A = x B$ $K_B = x A'$

Flip-flop outputs:

$z = x A' B$

Next state table:

Current state		input	FF inputs				Next state		output
A	B	x	J_A	K_A	J_B	K_B	A^+	B^+	z
0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	1	1	0	0
0	1	0	0	0	0	0	0	1	0
0	1	1	0	1	0	1	0	0	1
1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	1	0	1	1	0
1	1	0	0	0	0	0	1	1	0
1	1	1	0	1	1	0	0	1	0

Does the same thing as our previous example:

The state diagram would be identical !