

計算機結構 (Computer Architecture) EE4039 (901 43200) Spring 2019																																																													
陳少傑 csj@ntu.edu.tw Tel: 3366-3647																																																													
<p>This course gives a thorough presentation on the design of modern digital computer systems and their hardware and software interfaces. Topics covered in this course are as follows:</p> <ol style="list-style-type: none">1. Computer Abstractions, Technology, and Performance2. Instructions: Language of the Computer3. Arithmetic for Computers4. The Processor and its Enhancement with Pipelining5. Large and Fast: Exploiting Memory Hierarchy6. Parallel Processors from Client to Cloud <p>Senior Under-graduate students are all welcomed to this course.</p> <p>Grading Rules: Midterm 30%, Exercises 30%, Final 40%.</p>	<table><tr><td>Lec. 1:</td><td>Intr. to Computer Architecture</td><td>(Ch.1-1)</td></tr><tr><td>Lec. 2:</td><td>Cost and Performance</td><td>(Ch.1-2)</td></tr><tr><td>Lec. 3:</td><td>Instruction Set Architecture</td><td>(Ch.2-1)</td></tr><tr><td>Lec. 4:</td><td>MIPS Instruction Set Architecture</td><td>(Ch.2-2)</td></tr><tr><td>Lec. 5:</td><td>ALU Design, Add, Subtract</td><td>(Ch.3-1, 3-2)</td></tr><tr><td>Lec. 6:</td><td>ALU Design, Multiply</td><td>(Ch.3-3)</td></tr><tr><td>Lec. 7:</td><td>ALU Design, Divide, Floating-Point</td><td>(Ch.3-4)</td></tr><tr><td>Lec. 8:</td><td>Single Cycle Processor</td><td>(Ch.4-1)</td></tr><tr><td>Lec. 9:</td><td>Single Cycle Controller</td><td>(Ch.4-2)</td></tr><tr><td>Lec. 10:</td><td>Multiple Cycle Processor/Controller</td><td>(Ch.4-3)</td></tr><tr><td>Lec. 11:</td><td>Pipelined Processor</td><td>(Ch.4-4)</td></tr><tr><td>Lec. 12:</td><td>Microprogramming and Exceptions</td><td>(Ch.4-5)</td></tr><tr><td>Lec. 13:</td><td>Hardware Description Language</td><td>(Ch.4-6)</td></tr><tr><td>Lec. 14:</td><td>Memory System Design</td><td>(Ch.5-1)</td></tr><tr><td>Lec. 15:</td><td>Cache System Design</td><td>(Ch.5-2)</td></tr><tr><td>Lec. 16:</td><td>Virtual Memory</td><td>(Ch.5-3)</td></tr><tr><td>Lec. 17:</td><td>I/O Systems</td><td>(Ch.5-4)</td></tr><tr><td>Lec. 18:</td><td>Parallel Processors</td><td>(Ch.6-1)</td></tr><tr><td>Lec. 19:</td><td>Network-on-Chips</td><td>(Ch.6-2)</td></tr><tr><td>Lec. 20:</td><td>Final Review</td><td></td></tr></table>	Lec. 1:	Intr. to Computer Architecture	(Ch.1-1)	Lec. 2:	Cost and Performance	(Ch.1-2)	Lec. 3:	Instruction Set Architecture	(Ch.2-1)	Lec. 4:	MIPS Instruction Set Architecture	(Ch.2-2)	Lec. 5:	ALU Design, Add, Subtract	(Ch.3-1, 3-2)	Lec. 6:	ALU Design, Multiply	(Ch.3-3)	Lec. 7:	ALU Design, Divide, Floating-Point	(Ch.3-4)	Lec. 8:	Single Cycle Processor	(Ch.4-1)	Lec. 9:	Single Cycle Controller	(Ch.4-2)	Lec. 10:	Multiple Cycle Processor/Controller	(Ch.4-3)	Lec. 11:	Pipelined Processor	(Ch.4-4)	Lec. 12:	Microprogramming and Exceptions	(Ch.4-5)	Lec. 13:	Hardware Description Language	(Ch.4-6)	Lec. 14:	Memory System Design	(Ch.5-1)	Lec. 15:	Cache System Design	(Ch.5-2)	Lec. 16:	Virtual Memory	(Ch.5-3)	Lec. 17:	I/O Systems	(Ch.5-4)	Lec. 18:	Parallel Processors	(Ch.6-1)	Lec. 19:	Network-on-Chips	(Ch.6-2)	Lec. 20:	Final Review	
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主要參考書：J. L. Hennessy and D. A. Patterson, <i>Computer Architecture: A Quantitative Approach</i> , 5 th Edition, ©2012 Elsevier Inc.																																																													
上課時間/教室：(四)2, 3, 4/電二 225 學生面談時間：(四)14:00-16:00/電二 417	Browse https://ceiba.ntu.edu.tw/1072EE4039_ for class notes TA: 鄧傑方 d06943020@ntu.edu.tw																																																												

SCHEDULE of COMPUTER ARCHITECTURE (Spring 2019)

I. 2/21 Lec. 1 / 2	X. 4/25 Lec. 12
II. 2/28 和平紀念日	XI. 5/2 Lec. 13 HDL (TA)
III. 3/7 Lec. 3 / 4	XII. 5/9 Lec. 14 / 15
IV. 3/14 Lec. 5 / 6	XIII. 5/16 Lec. 16
V. 3/21 Lec. 7 / 8	XIV. 5/23 Lec. 17
VI. 3/28 Lec. 9 / 10	XV. 5/30 Lec. 18
VII. 4/4 兒童節	XVI. 6/6 Lec. 19
VIII. 4/11 Lec. 11	XVII. 6/13 Lec. 20 (Review)
IX. 4/18 <i>Midterm Exam.</i>	XVIII. 6/20 <i>Final Exam.</i>

上課時間/教室：(四)2, 3, 4/電二 225 學生面談時間：(四)14:00-16:00/電二 417