- The tool used is HDLparse which is used to implement an automated testbench from an existing verilog module
- It uses python to implement the functions needed to make the testbench from the module.
- It reads all the variables such as inputs and outputs automatically from the target module
- To use the tool you open the ubuntu terminal and go to the directory of the folder containing the code and run the module.
- A test bench will appear containing all the needed lines of code in optimal order.
- Dependencies needed were the installation of python itself if not available.and the hdl parse library has to be imported into the file.
- It also needs the module itself to be written in the code to generate it's testbench.

  Code structure

  The code begins by defining all inputs found in the module and all the outputs. After that it loops over all of them and writes the needed uut for the testbench and proceeds to initiate a clock generator that runs forever. Then it begins by making sure all ports are monitored and proceeds to initialise all inputs with 0 initialises a dumpfile and names it after the module name then ends the module.