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A Design Methodology for a CLLLC Bidirectional Resonant Converter with an Integrated Planar Transformer

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Abstract

The efficiency and power density of a bidirectional CLLLC resonant converter can be improved by integrating its magnetic components into a single transformer (known as integrated transformer). However, integrated transformers, especially integrated planar transformers, usually suffer from high parasitic capacitance. In the conventional design process of the CLLLC converter, the parasitic capacitance of the transformer is neglected while a high parasitic capacitance can affect the performance of the converter noticeably. Therefore, this paper presents a new design methodology for a bidirectional CLLLC resonant converter, which studies the effect of parasitic capacitance and guarantees ZVS conditions for the switches even when integrated planar transformers with high stray capacitance are used. Simulation results are presented to verify the theoretical analysis.

1 Introduction

Energy storage systems (ESSs) are systems that enable energy to be stored and then released when customers need power most or when an uninterruptible power supply is needed [1-6].

There is usually a bidirectional AC-DC converter followed by a bidirectional DC-DC converter in ESSs. The bidirectional DC-DC converter transfers the power from the DC bus to the batteries and vice versa. It is preferred that the bidirectional DC-DC converter has a low cost and high efficiency and power density [7, 8].

The pulse-width-modulated (PWM) DC-DC converters such as flyback converter suffer from high switching losses due to hard-switching and cannot be switched at high switching frequencies, leading to a low power density [9, 10]. On the other hand, the resonant converters benefit from soft-switching capability inherently and can be switched at high switching frequencies for a higher power density [11-13]. Therefore, the resonant converters have been developed to be used in many applications such as ESSs, arc-striking for creating plasma [14-16] and renewable energy systems [17].

Amongst different bidirectional resonant converters, the CLLLC topology has gained popularity for ESSs in recent years since it benefits from soft-switching capability and can be used under wide input and output voltage ranges which is needed for energy storage systems [18]. The topology of the CLLLC resonant converter is shown in Fig. 1(a) and its important waveforms are shown in Fig. 1. As shown, this converter needs four magnetic components which makes the converter expensive and giant. To increase the power density and efficiency and to cut the cost of the converter, the magnetic components can be integrated into a single transformer as presented in Fig. 1(b) [19].

There are many methods for magnetic integration in LLC-type resonant converters [20, 21]. Amongst different methods, inserted-shunt integrated planar transformers have gained popularity in recent years [22-24]. The inserted-shunt integrated planar transformer benefits from precise estimation of leakage inductance during design, capability for achieving high leakage inductance, the ability to use cores readily available in the market and simple manufacturing. In addition, this method uses planar cores which have many other advantages, *viz* high power density, improved

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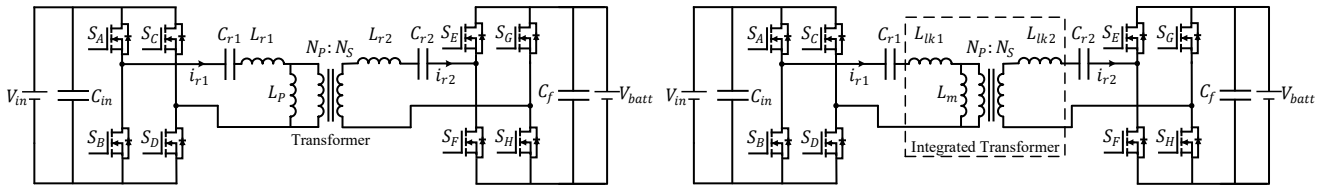

Fig. 1 Topology of bidirectional CLLLC resonant converter. (a) without magnetic integration. (b) with magnetic integration

cooling capability, modularity and manufacturing simplicity [25].

Integrated transformers usually have a higher parasitic capacitance, especially when they use planar transformers [26]. The parasitic capacitance of the transformer is neglected in the conventional design process of the CLLLC resonant converter while the operation of the converter can be affected noticeably by a high parasitic capacitance. In Fig. 3, the topology of the CLLLC converter considering the parasitic capacitance of the integrated transformer is presented.

In this paper, the effect of the parasitic capacitance of integrated transformers on the CLLLC resonant converter is investigated, and it is shown that the converter may lose its soft-switching capability when the transformer has a high parasitic capacitance. To keep the soft-switching capability even with high parasitic capacitance, a new design methodology for the CLLLC resonant converter is proposed which considers the effect of the parasitic capacitance of the transformer. An exemplar CLLLC resonant converter is designed based on the proposed and conventional methodology. The simulation results are presented to verify the theoretical analysis and to investigate the designed CLLLC converters.

The paper is organised as follows: the CLLLC resonant converter is fully investigated in Section II. In Section III, a new design methodology for the CLLLC converter is presented that guarantee ZVS even when an inserted-shunt integrated planar transformer with a high parasitic capacitance is used. The simulation results and conclusion are presented in Sections IV and V, respectively.

2 Fundamental analysis of CLLLC resonant converter

The operation of the CLLLC resonant converter is fully investigated in [18] and is again presented shortly in this section. The topology of the CLLLC resonant converter is shown in Fig. 1. As shown,

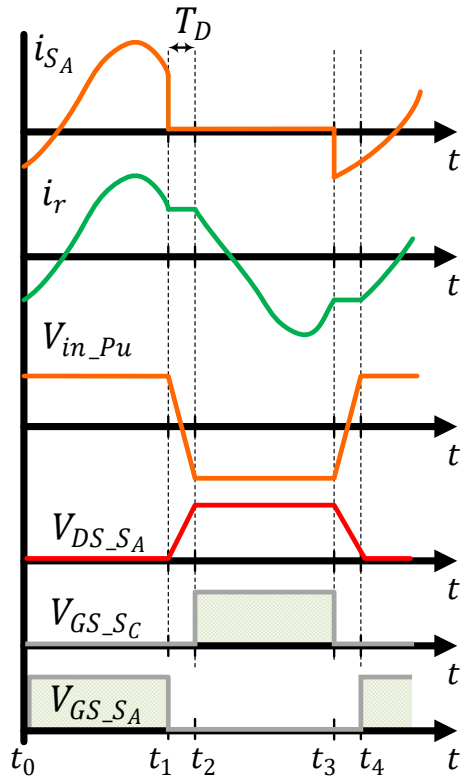

Fig. 2 Important waveforms of the CLLLC resonant converter for BCM.

this converter is similar to the LLC resonant converter with an extra inductor and an extra capacitor on the secondary side. However, in contrast with the LLC topology, the CLLLC topology is capable of transferring power in both directions. The important waveform of the converter in battery charging mode (BCM) including drain-to-source (DS) and gate-to-source (GS) voltages, resonant current (i_{r}), switch current (i_{S}) and input pulse voltage ($V_{\mathrm{in-Pu}}$) for operating frequency near resonance frequency (defined in (4)) are presented in Fig. 2.

A small dead time, T_{D}, is usually introduced to avoid short-circuit between consecutive transitions. In BCM, the primary switches (S_A, S_B, S_C and S_D),

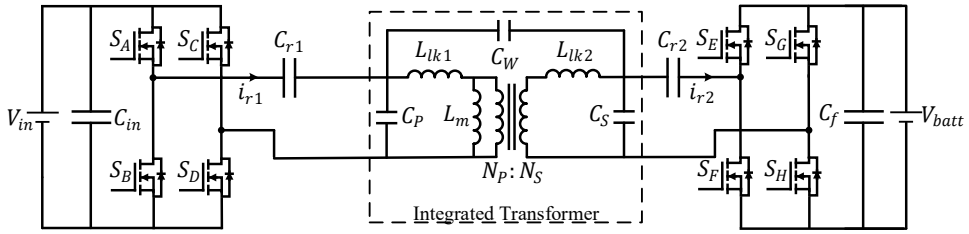

Fig. 3 Circuit topology for bidirectional CLLLC resonant converter considering parasitic capacitors of the transformer.

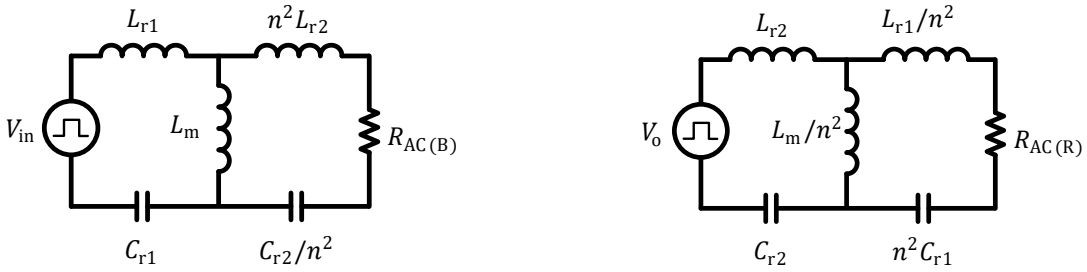

Fig. 4 AC circuit of CLLLC resonant converter. (a) BCM. (b) RM

which are switched at zero voltage (ZVS) conditions, convert the input DC voltage to a square wave voltage, $V_{\mathrm{in-Pu}}$. The square wave then enters the CLLLC resonant tank, which eliminates the square wave's harmonics and outputs a sinusoidal current at the switching frequency. The sine wave is finally rectified to a purely DC voltage by antiparallel diodes of the secondary switches (S_E, S_F, S_G and S_H).

In reverse mode (RM), in which the battery is discharging, the converter follows the same procedure as BCM except the secondary switches convert the battery voltage to a square wave and the primary switches' antiparallel diodes rectifier the square wave to a purely DC voltage.

2.1 Gain analysis of CLLLC converter

In this section, AC gain of the CLLLC resonant converter for both power directions (BCM and RM) is presented. It is assumed that the main harmonic of the circulating current in the resonant network is at or close to the series resonance frequency ((4) for BCM and (11) for RM) and other harmonics are heavily attenuated. Analysis making this assumption is called the fundamental harmonic approximation (FHA) method [27].

2.1.1 Equivalent circuit for BCM

The AC equivalent circuit of the CLLLC converter in BCM is shown in Fig. 4(a), in which all the components are referred to the primary side according to the transformer's turns ratio. Using FHA, equivalent load resistance for BCM, $R_{\mathrm{AC(B)}}$, can be expressed as (1) [27].

$$R_{\mathrm{AC(B)}} = \frac{8n^2}{\pi^2} R_{\mathrm{o(B)}} \tag{1}$$

where n is transformer's trans ratio and $R_{\mathrm{o(B)}}$ is the output load resistance in BCM.

The normalised frequency, $f_{\mathrm{N(B)}}$, quality factor, Q_{B}, and resonance frequency, $f_{\mathrm{r(B)}}$, in BCM are defined as follows:—

$$f_{\mathrm{N(B)}} = \frac{f_{\mathrm{s}}}{f_{\mathrm{r(B)}}} \tag{2}$$

$$Q_{\mathrm{B}} = \frac{\sqrt{\frac{L_{\mathrm{r1}}}{C_{\mathrm{r1}}}}}{R_{\mathrm{AC(B)}}} \tag{3}$$

$$f_{\mathrm{r(B)}} = \frac{1}{2\pi\sqrt{L_{r1}C_{r1}}} \tag{4}$$

$$\omega_{\mathrm{r(B)}} = 2\pi f_{\mathrm{r(B)}} \tag{5}$$

$$\omega_{\mathrm{s}} = 2\pi f_{\mathrm{s}} \tag{6}$$

$$\omega_{\mathrm{N(B)}} = \frac{\omega_{\mathrm{s}}}{\omega_{\mathrm{r(B)}}} \tag{7}$$

where f_{s} is the operating (switching) frequency.

2.1.2 Equivalent circuit for RM

The AC circuit of the CLLLC converter in RM is shown in Fig. 4(b), in which all the components are referred to the secondary side according to the transformer's turns ratio. Using FHA, equivalent load resistance for RM, $R_{\mathrm{AC(R)}}$, can be expressed as (8) [27].

$$R_{\mathrm{AC(R)}} = \frac{8n^2}{\pi^2} R_{\mathrm{o(R)}} \tag{8}$$

where $R_{\mathrm{o(R)}}$ is the output load resistance in RM.

The normalised frequency, $f_{\mathrm{N(R)}}$, quality factor, Q_{R}, and resonance frequency, $f_{\mathrm{r(R)}}$, in RM are defined as follows:—

$$f_{\mathrm{N(R)}} = \frac{f_{\mathrm{s}}}{f_{\mathrm{r(R)}}} \tag{9}$$

$$Q_{\mathrm{R}} = \frac{\sqrt{\frac{L_{\mathrm{r2}}}{C_{\mathrm{r2}}}}}{R_{\mathrm{AC(R)}}} \tag{10}$$

$$f_{\mathrm{r(R)}} = \frac{1}{2\pi\sqrt{L_{r2}C_{r2}}} \tag{11}$$

$$\omega_{\mathrm{r(R)}} = 2\pi f_{\mathrm{r(R)}} \tag{12}$$

$$\omega_{\mathrm{N(R)}} = \frac{\omega_{\mathrm{s}}}{\omega_{\mathrm{r(R)}}} \tag{13}$$

2.1.3 Gain for BCM and RM

The AC gain of the CLLLC topology for BCM and RM can be derived from Figs. 4(a) and (b). The AC gain of CLLLC converter in BCM may be calculated as (14), where h_{B} is defined as (15), m_{B} is defined as (16) and g_{B} is defined as (17) [3].

$$h_{\mathrm{B}} = \frac{L_{\mathrm{m}}}{L_{\mathrm{r1}}} \tag{15}$$

$$m_{\mathrm{B}} = \frac{n^2 L_{\mathrm{r2}}}{L_{\mathrm{r1}}} \tag{16}$$

$$g_{\mathrm{B}} = \frac{C_{\mathrm{r2}}}{n^2 C_{\mathrm{r1}}} \tag{17}$$

Similarly, the AC gain of the CLLLC converter in RM may be calculated as (18), where h_{R} is defined as (19), m_{R} is defined as (20) and g_{R} is defined as (21) [3].

$$h_{\mathrm{R}} = \frac{L_{\mathrm{m}}}{n^2 L_{\mathrm{r2}}} \tag{19}$$

$$m_{\mathrm{R}} = \frac{L_{\mathrm{r1}}}{n^2 L_{\mathrm{r2}}} \tag{20}$$

$$M_{\mathrm{AC(B)}} = \frac{nV_{\mathrm{o}}}{V_{\mathrm{in}}} = \frac{1}{\sqrt{\left(\frac{1}{h_{\mathrm{B}}} - \frac{1}{h_{\mathrm{B}}\omega_{\mathrm{N(B)}}^2} + 1\right)^2 + \left(\frac{1}{\omega_{\mathrm{N(B)}}}\left(\frac{m_{\mathrm{B}}}{h_{\mathrm{B}}} + \frac{1}{h_{\mathrm{B}}g_{\mathrm{B}}} + \frac{1}{g_{\mathrm{B}}} + 1\right)Q_{\mathrm{B}} - \omega_{\mathrm{N(B)}}\left(\frac{m_{\mathrm{B}}}{h_{\mathrm{B}}} + m_{\mathrm{B}} + 1\right)Q_{\mathrm{B}} - \frac{Q_{\mathrm{B}}}{h_{\mathrm{B}}g_{\mathrm{B}}\omega_{\mathrm{N(B)}}^3}\right)^2}} \tag{14}$$

$$M_{\mathrm{AC(R)}} = \frac{V_{\mathrm{in}}}{nV_{\mathrm{o}}} = \frac{1}{\sqrt{\left(\frac{1}{h_{\mathrm{R}}} - \frac{1}{h_{\mathrm{R}}\omega_{\mathrm{N(R)}}^2} + 1\right)^2 + \left(\frac{1}{\omega_{\mathrm{N(R)}}}\left(\frac{m_{\mathrm{R}}}{h_{\mathrm{R}}} + \frac{1}{h_{\mathrm{R}}g_{\mathrm{R}}} + \frac{1}{g_{\mathrm{R}}} + 1\right)Q_{\mathrm{R}} - \omega_{\mathrm{N(R)}}\left(\frac{m_{\mathrm{R}}}{h_{\mathrm{R}}} + m_{\mathrm{R}} + 1\right)Q_{\mathrm{R}} - \frac{Q_{\mathrm{R}}}{h_{\mathrm{R}}g_{\mathrm{R}}\omega_{\mathrm{N(R)}}^3}\right)^2}} \tag{18}$$

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$$g_{\mathrm{R}} = \frac{n^2 C_{\mathrm{r1}}}{C_{\mathrm{r2}}} \tag{21}$$

2.1.4 Design methodology

Design of the CLLLC converter includes determining the transformer's turns ratio, n, and the resonant tank's components consisting of primary and secondary resonant inductances (L_{r1} and L_{r2}), primary and secondary capacitances (C_{r1} and C_{r2}), magnetising inductance (L_{m}) and the operating frequency range. The switching frequency needs to be considered high enough to achieve a high-power density for the converter and the resonant tank's components determination are presented as follows:—

a) Considering the converter operates at or close to the resonance frequency to achieve the maximum efficiency, the transformer's turns ratio, n, can be calculated from (22).

$$n = \frac{V_{\mathrm{in}}}{V_{\mathrm{o}}} \tag{22}$$

b) The output capacitor of the primary switches needs to be charged and discharged by the primary current during the dead time. The operation of the CLLLC converter during the dead time is similar to the operation of the full-bridge LLC resonant converter during the dead time. Therefore, the magnetising inductance can be calculated using the same expression as the full-bridge LLC resonant converter [28, 29].

$$L_{\mathrm{m}} \leq \frac{T_D}{8 f_{\mathrm{s(max)}} (C_{\mathrm{oss(P)}} + \frac{C_{\mathrm{oss(S)}}}{n^2})} \tag{22}$$

where $f_{\mathrm{s(max)}}$ is the maximum operating frequency, $C_{\mathrm{oss(P)}}$ and $C_{\mathrm{oss(S)}}$ are primary and secondary switches' output capacitance, respectively. A small magnetising inductance guarantees the ZVS of the switches, but it increases the conduction losses.

Resonant components are selected so that they guarantee the proper performance of the converter for every possible operating condition such as load, frequency, circulating energy, and input/output voltage variations. In [18], a design example considering these conditions is presented.

3 Considering stray capacitance for ZVS

The conventional design procedure is presented for the CLLLC resonant converter with a negligible transformer's parasitic capacitance (see Fig. 1).

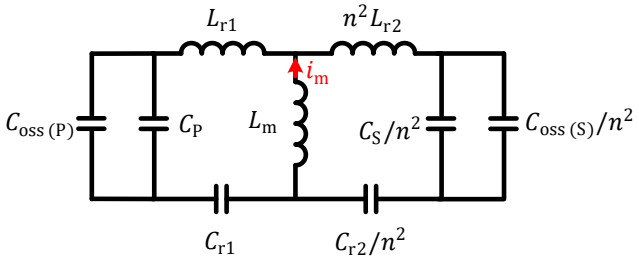


Fig. 5 Equivalent circuit of CLLLC converter during dead time

However, using inserted-shunt integrated planar transformer for higher power density comes with the penalty of a high parasitic capacitance for the transformer (see Fig. 3). The performance of resonant converters is very sensitive to resonant components (inductors and capacitors) and, therefore, the parasitic capacitors need to be modelled in the analysis of CLLLC resonant converter when it benefits from inserted-shunt integrated planar transformers.

In inserted-shunt integrated planar transformers, the primary (C_{P}) and secondary (C_{S}) windings have a high self-parasitic (stray) capacitance because of the large overlapping area and a small distance between the turns. However, the parasitic capacitance between the primary and secondary windings (C_{W}) is negligible since the primary and secondary windings are separated from each other and placed far from each other. Therefore, in this paper, the effect of C_{W} is neglected.

A large stray capacitance affects the ZVS behavior of the MOSFET switches and the Inequality (22) does not guarantee ZVS anymore. The reason is that the magnetising current needs to discharge both the output capacitor of the MOSFET switches and stray capacitor of the integrated planar transformer during dead time as presented in Fig. 5.

To guarantee achievement of the ZVS condition for the switches in the CLLLC converter with integrated planar transformer, (22) is revised as (23).

$$L_{\mathrm{m}} \leq \frac{T_D}{8 f_{\mathrm{s(max)}} C_{\mathrm{total}}} \tag{23}$$

where C_{total} is summation of the output capacitance of the primary switch, $C_{\mathrm{oss(P)}}$, output capacitance of the secondary switch, $C_{\mathrm{oss(S)}}$, referred to the primary side, primary stray capacitance, C_{P},

Symbol	Parameter	Conventional	Proposed
$N_{\mathrm{P}}: N_{\mathrm{S}}$	Primary and secondary turns numbers	20:4	20:4
L_{m}	Magnetising inductance	200 μH	100 μH
L_{r1}	Primary resonant inductance	50 μH	50 μH
L_{r2}	Secondary resonant inductance	1.2 μH	1.2 μH
C_{r1}	Primary resonant capacitance	39 nF	39 nF
C_{r2}	Secondary resonant capacitance	1 μF	1 μF
V_{in}	Input voltage	125 V	125 V
V_{out}	Output voltage	20-26 V	20-26 V
P_{out}	Output power	200 W	200 W
f_{s}	Switching frequency	60-130 kHz	60-130 kHz
C_{P}	Primary parasitic capacitance	4 nF	4 nF
C_{S}	Secondary parasitic capacitance	3 nF	3 nF
$C_{\mathrm{oss(P)}}$	Primary switches' output capacitance	160 pF	160 pF
$C_{\mathrm{oss(S)}}$	Secondary switches' output capacitance	300 pF	300 pF

Table 1 The bidirectional CLLLC resonant converter's specification

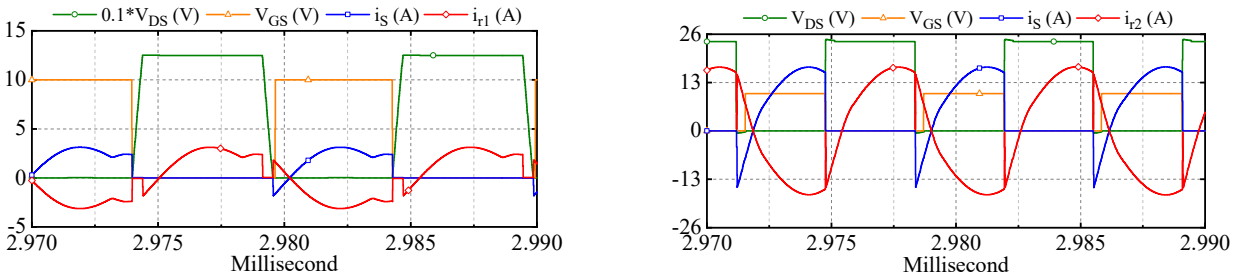
and secondary stray capacitance, C_{S}, referred to the primary side as presented in (24).

$$C_{\mathrm{total}} = C_{\mathrm{oss(P)}} + \frac{C_{\mathrm{oss(S)}}}{n^2} + C_{\mathrm{P}} + \frac{C_{\mathrm{S}}}{n^2} \qquad (24)$$

4 Simulation study

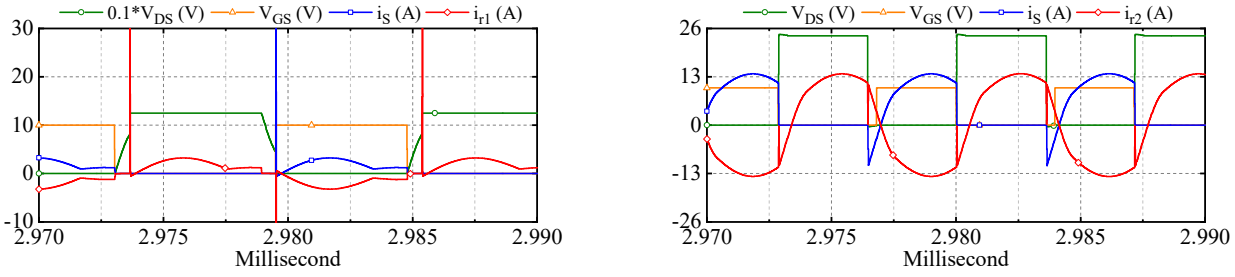
An exemplar bidirectional CLLLC resonant converter is designed based on the design procedure outlined in Section III, and its specification is presented in Table 1. In addition, another bidirectional CLLLC resonant converter with identical operating power, voltage and frequency is designed based on the conventional method presented in [18], which its specification is presented in Table 1. Both the designed converters are simulated in MATLAB/Simulink and the results are presented and compared in this Section. It should be mentioned that both converters use the same integrated transformer.

The operating waveforms of the CLLLC converter designed based on the proposed methodology are presented for BCM and RM in Figs. 6(a) and (b), respectively. The operating waveforms of the CLLLC converter designed based on the conventional methodology are presented for BCM and RM in Figs. 7(a) and (b), respectively. As shown, the proposed methodology can still guarantee the soft-switching of the switches for both BCM and RM while the converter designed based on the



(a) (b)

Fig. 6 Waveforms of the proposed CLLLC resonant converter. (a) For BCM, primary resonant current (i_{r1}) drain-to-source (V_{DS}) and gate-to-source (V_{GS}) voltages and current (i_{S}) of switch S_{D}. (b) For RM, secondary resonant current (i_{r2}), V_{GS}, V_{DS}, and i_{S} of switch S_{F}



(a) (b)

Fig. 7 Waveforms of the conventional CLLLC resonant converter. (a) For BCM, primary resonant current (i_{r1}) drain-to-source (V_{DS}) and gate-to-source (V_{GS}) voltages and current (i_{S}) of switch S_{D}. (a) For RM, secondary resonant current (i_{r2}), V_{GS}, V_{DS}, and i_{S} of switch S_{F}

conventional method cannot be switched at soft-switching condition for BCM (V_{GS} rises before V_{DS} drops to zero in Fig. 7(a)).

5 Conclusion

The effects of the planar transformer's stray capacitance on the performance of the bidirectional CLLLC resonant converter are discussed. In addition, a new design methodology for bidirectional CLLLC resonant converter is presented that still guarantees ZVS for the switches even when there is high stray capacitance in the integrated planar transformer. An exemplar converter based on the new methodology is designed and to show the advantages of the proposed design methodology, another bidirectional CLLLC resonant converter with identical operating power, voltage and frequency is designed based on the conventional methodology. Both designed converters are simulated and compared. It is shown that the proposed method can guarantee the soft-switching capability of the converter even when the integrated transformer has a high parasitic capacitance while the converter designed based on the conventional method suffers from hard-switching.

6 Acknowledgment

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