Design Methodology for Symmetric CLLC Resonant DC Transformer Considering Voltage Conversion Ratio, System Stability and Efficiency

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***Abstract*—With the popularity of DC microgrid, the symmetric CLLC resonant dual active bridge (DAB) converter usually works as a DC transformer (DCT) when it is applied in DC microgrid. It has received increasing attention for that it provides galvanic isolation and also enjoys high power density. In such application, the open-loop control with 50% duty ratio is commonly adopted for the CLLC resonant DCT (CLLC-DCT) for simple control scheme and high efficiency. However, this will bring about difficulties for the design of CLLC-DCT: firstly, the fluctuating values of the practical inductors or capacitors because of temperature or power variation may lead to deviated voltage conversion ratio (VCR) of CLLC-DCT; secondly, chances are that system instability will happen when CLLC-DCT and a constant power load connect in a cascaded structure because of impedance interactions, which will also be affected when parameters fluctuate; and thirdly, high efficiency of the DCT is also expected even when the inductance or capacitance fluctuate. With all the above concerns, the five-stage design methodology for the CLLC-DCT converter is put forward to meet design objectives regarding VCR, system stability and power efficiency simultaneously. And the effects of fluctuating inductance and capacitance have been fully taken into account by the assistance of particle swarm optimization (PSO). Besides, a 1 kW hardware prototype has experimentally validated that the proposed design methodology is feasible.**

***Index Terms*—DC transformer, CLLC, voltage conversion ratio, system stability, power efficiency, PSO algorithm.**

I. Introduction

Due to the popularity of renewable generations, the DC microgrid has attracted increasing attention. Because of the integration of various clean-energy sources and DC power loads, different voltage levels are required in multi-DC-bus in DC microgrid [1]–[3]. The traditional way to realize voltage transfer is to apply a low frequency AC transformer (ACT). However, ACT suffers from low power transfer efficiency and low power density. Thus, the traditional ACT has been substituted by the high-frequency DC transformer (DCT). One of the most frequently used topologies for DCT is the dual active bridge (DAB) topology, which contains two full bridges and one high frequency transformer. It enjoys outstanding benefits including galvanic isolation and high power density [4]–[6].

Resonant tanks have been adopted by many research works to realize wider soft-switching range of the DAB topology. The typically adopted resonant tanks include: LC, LLC [7], asymmetric CLLC [8] and symmetric CLLC [9]. Among them, the soft switching range of the LC-type resonant DAB is not as wide as those of others. And only the symmetric CLLC-type resonant DAB converter is able to realize exactly same power conversion operation and efficiency when power flows in the two directions [10]. The leakage inductance of the transformer is viewed as the resonant inductance so that the power density can be increased. Two resonant capacitors are put on both primary and secondary sides to ensure same operation principles and same soft-switching performance in the forward and backward power conversion modes [11], [12]. Thus, the symmetric CLLC-DCT is adopted in this research work and it is called as the CLLC-DCT for convenience. Fig. 1 describes a structure of CLLC-DCT based DC microgrid, where the DC bus can belong to high voltage (HV), medium voltage (MV) or low voltage (LV).

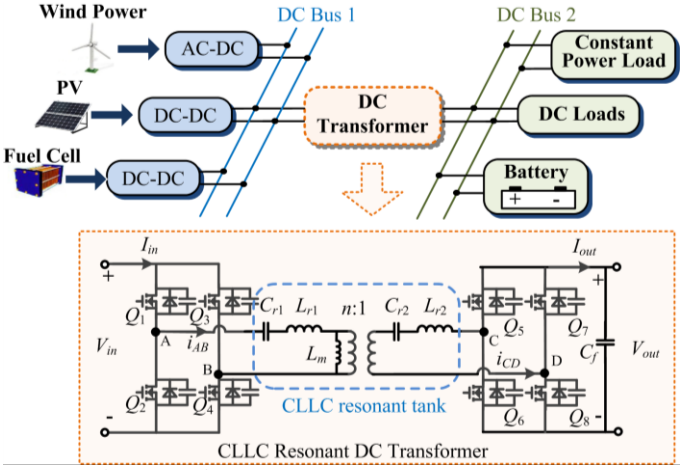

Fig. 1. Configuration of a CLLC-DCT based DC microgrid.

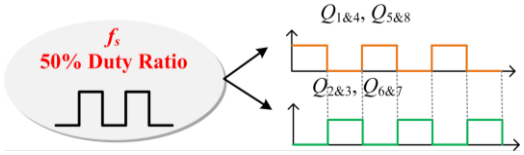

Fig. 2. Description of the open-loop control with 50% duty ratio for the CLLC-DCT in DC microgrid.

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It is worth noticing that the CLLC-DCT is usually controlled by open-loop control with 50% duty ratio, as shown in Fig. 2, in which the switching frequency and the resonant frequency of the CLLC resonant tank share the same value [13]. The resonant tank has realized a load-independent operating point when the switching frequency is close to the resonant frequency, making the CLLC-DCT work as an ideal transformer [14]. Thus, for the DCT applied in DC microgrid where the voltage of DC bus is regulated by the energy management system (EMS), the open-loop control with 50% duty ratio is suitable [15]. Also, this control strategy is easy to implement and enables good efficiency performance [11].

However, even though this control strategy is simple, it fails to maintain good performance of CLLC-DCT when parameter fluctuations happen. While it is normal for parameters to deviate from their rated values due to temperature and operating power variations, whose fluctuation ranges can reach up to 10% [16]–[18]. Hence, there exist some challenges when designing CLLC-DCT.

The first challenge is to maintain robust voltage conversion ratio (VCR) when parameter fluctuations happen. If there are differences between the real values of parameters and the rated ones, as a result, VCR of the CLLC-DCT will go beyond the required range. Admittedly, there has been preliminary research work which managed to maintain robust VCR against parameter fluctuations [19]. However, the case analysis is complex and relatively hard to implement.

Apart from that, considerations only in individual-operating performance are far from enough for the sake of stable system-level operation.

The second challenge is to maintain system stability when the CLLC-DCT and a constant power load (CPL) connect in a cascaded structure when parameter fluctuations happen. CPL can be found in many applications in the DC microgrid, such as information and communication technology facilities and voltage regulators [20]. Whereas, CPL increases the instability risk for the cascaded system because it is intrinsically a negative impedance [21]. An example of the cascaded system in which buck converter plays the role of CPL is given in Fig. 3. Instability phenomenon may happen due to impedance interactions even though two individual subsystems can operate stably. According to the study by Middlebrook in 1976 [22], it is necessary to keep the amplitude of Z_{out_DCT}, the output impedance of CLLC-DCT, smaller than that of Z_{in_CPL}, the input impedance of CPL, for the sake of system stability. Since the circuit parameters will directly affect Z_{out_DAB}, system stability objective must be considered in parameter design. Additionally, the unpredictable fluctuations of circuit parameters bring about difficulties to parameter design.

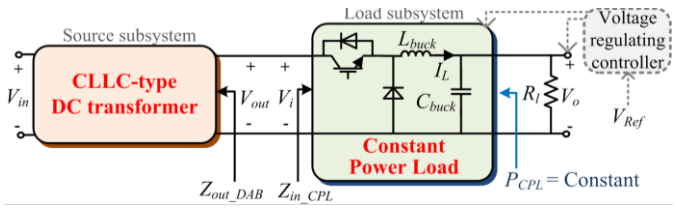


Fig. 3. A system in which a CLLC-DCT and a CPL cascade with each other.

The third challenge is to guarantee that the CLLC-DCT has satisfactory power conversion efficiency. The CLLC-DCT under the open-loop control with 50% duty ratio in the DC microgrid plays a role as an ideal transformer to realize voltage transfer between two DC bus [11]. In such case, the power conversion efficiency is expected to be as high as possible [23]. Since the design of circuit parameters will affect power loss, power conversion efficiency is also an important concern when CLLC-DCT is designed. Admittedly, there exists some research work on the optimization of power loss in the CLLC-DCT [4], [15] but only the power conversion efficiency design objective is focused on. It should be noted that without robust VCR and system stability, deviated output voltage and the instability phenomenon will negatively affect power supplies and even destroy power devices [24]. Hence, considerations only on power conversion efficiency design requirement are not enough for a good comprehensive performance.

As discussed above, when CLLC-DCT is under 50% duty-ratio open-loop control, circuit parameter fluctuations will undermine the operating performance in VCR, system stability and power efficiency. Since the possible fluctuations of inductance and capacitance cannot be predicted, infinite parameter combinations can be resulted in, contributing to heavy computational burden and high computational complexity. Thus, the proposed design methodology adopts the state-of-the-art metaheuristic optimization algorithm to thoroughly consider the fluctuations of circuit parameters. Bee colony optimization (BCO) [25], [26], particle swarm optimization (PSO) [27] and genetic algorithm (GA) [28] have been frequently adopted in power electronic areas. Especially, the PSO algorithm is famous for its fast convergence speed and easy implementation. PSO algorithm mimics the behavior pattern of bird flocks. It fully utilizes the memory of the swarm to find the global optima accurately and quickly and is appropriate for continuous optimization problems. However, the premature convergence problem exists in the conventional PSO algorithm and some popular variants including PSO-LDIW [29] and HPSO-TVAC [30]. To deal with this problem, one of the latest PSO algorithms, the randomly occurring distributed delayed PSO (RODD-PSO) [31] is specially offered. It utilizes the historical information for updating particles' velocities distributedly, which can improve results accuracy by avoiding the local optima. Thus, for more accurate solutions, RODD-PSO is utilized in the proposed methodology for the CLLC-DCT to take the fluctuations of circuit parameters into considerations.

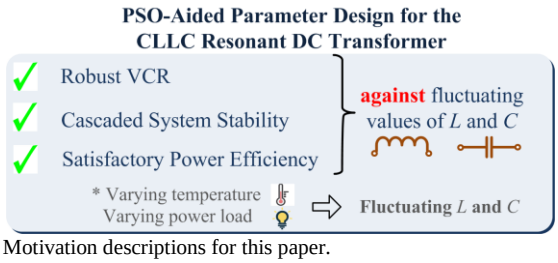


Fig. 4. Motivation descriptions for this paper.

Briefly, in this paper, the five-stage design methodology has been proposed to realize three design objectives at the same time: robust VCR, system stability and satisfactory power conversion

efficiency, which is also described with Fig. 4. Also, the adopted RODD-PSO enables full considerations of the effects of parameter fluctuations. Thus, not only does the designed CLLC-DCT enjoy good performance individually (VCR & efficiency), it can also operate stably in a cascaded system. In the first to the third stages, how to determine the proportion of magnetizing inductance to leakage inductance is focused on from the perspective of every design objective. And in the fourth stage, VCR, stability and efficiency will be considered simultaneously. In the last stage, the designed values of circuit parameters are computed.

The structure of this paper is given as the followings: the effects of CLLC parameters to VCR, system stability and power conversion efficiency are analyzed in the second section; challenges in designing CLLC-DCT brought by parameter fluctuations are discussed in the third section; the fourth section presents the proposed five-stage design methodology together with a design example; in the fifth section, experimental validation is provided and final conclusion is summarized in the sixth section.

II. Effects of Parameters on Performance of CLLC-DCT

In the following part, from the perspectives of VCR, system stability and power conversion efficiency, the influences of CLLC parameters on the performance of CLLC-DCT are analyzed.

A. Basic Design of CLLC-DCT

For CLLC-DCT, the circuit parameters, incorporating magnetizing inductance (L_m), resonant inductance (L_{r1}, L_{r2}), and resonant capacitance (C_{r1}, C_{r2}), need to be designed.

In the beginning, based on (1), the high frequency transformer between two full bridges will be given a turn ratio according to the voltages on DC bus (V_{in} and V_{out}).

$$n = V_{out} / V_{in} \tag{1}$$

According to [19], in the open-loop control with 50% duty ratio, the resonant angular frequency ω_r and the switching angular frequency ω_s share the same rated value, as expressed in (2). And this setting can guarantee zero current switching (ZCS) to reduce power loss.

$$\omega_r = \frac{1}{\sqrt{L_{r1}C_{r1}}} = \frac{1}{\sqrt{L_{r2}C_{r2}}} = \omega_s \tag{2}$$

To achieve zero voltage switching (ZVS), L_m is required to meet (3) [9], where C_{oss}, T_{dead} and f_s are output capacitor of switches, dead time and switching frequency, respectively.

$$L_m \le \frac{T_{dead}}{16 f_s C_{oss}} \tag{3}$$

For higher power efficiency and ZVS at the same time, L_m is selected with (4) [15], [32].

$$L_m = \frac{T_{dead}}{16 f_s C_{oss}} \tag{4}$$

An intermediate parameter k is defined as (5). With k, it is easy to express other circuit parameters as shown in (6) and (7).

$$k = L_m / L_{r1} = L_m / n^2 L_{r2} \tag{5}$$

$$L_{r1}(k) = n^2 L_{r2}(k) = \frac{L_m}{k} \tag{6}$$

$$C_{r1}(k) = C_{r2}(k) / n^2 = \frac{k}{4\pi^2 f_s^2 L_m} \tag{7}$$

Thus, deciding the value of k can be summarized as the key point for parameter deign of the CLLC-DCT.

B. Effects of Parameters on VCR Performance

In the DC microgrid, CLLC-DCT is expected to function as an ideal transformer, which should be able to maintain a robust VCR no matter how parameters of CLLC-DCT fluctuate in practice. For convenience, VCR performance is evaluated with an indicator M, which is defined with (8):

$$VCR \triangleq M = \frac{V_{out}}{n V_{in}} \tag{8}$$

If the acceptable varying percentage of V_{out} and V_{in} are set as α% and β% in (9) and (10), the range of them can be shown with (11), in which V_{outR} and V_{inR} stand for the corresponding rated values.

$$V_{in} \in \left[(1-\alpha\%)V_{inR}, (1+\alpha\%)V_{inR}\right] \tag{9}$$

$$V_{out} \in \left[(1-\beta\%)V_{outR}, (1+\beta\%)V_{outR}\right] \tag{10}$$

$$M \in \left[M_{lower}, M_{upper}\right] \tag{11a}$$

$$M_{lower} = \frac{(1-\alpha\%)V_{outR}}{n(1+\beta\%)V_{inR}} \tag{11b}$$

$$M_{upper} = \frac{(1+\alpha\%)V_{outR}}{n(1-\beta\%)V_{inR}} \tag{11c}$$

Based on the analysis regarding VCR of CLLC-DCT in [19], M has been found to be determined by k, Q, and ω_*. The relevant expressions are given in (12) in which P_L is the load power.

$$M(k, Q, \omega_*) = \frac{V_{out}}{n V_{in}} = \frac{k}{\sqrt{\lambda_3 k^2 + \lambda_2 k + \lambda_1}} \tag{12a}$$

$$\lambda_1 = \left(\omega_*^2 - 1\right)^2 \left[Q^2\left(\omega_*^2 - 1\right)^2 + \omega_*^2\right] / \omega_*^6 \tag{12b}$$

$$\lambda_2 = 2\left(\omega_*^2 - 1\right)\left[2Q^2\left(\omega_*^2 - 1\right)^2 + \omega_*^2\right] / \omega_*^4 \tag{12c}$$

$$\lambda_3 = 4Q^2\left(\omega_*^2 - 1\right)^2 / \omega_*^2 + 1 \tag{12d}$$

$$\omega_* = \omega_s / \omega_r = 2\pi f_s \sqrt{L_{r1}C_{r1}} = 2\pi f_s \sqrt{L_{r2}C_{r2}} \tag{12e}$$

$$Q = \frac{n^2 \sqrt{L_{r1} / C_{r1}}}{8 V_{out}^2 / \pi^2 P_L} \tag{12f}$$

As can been seen from (12), CLLC parameters and P_L will directly affect VCR performance. In Fig. 5 (a), the visual representation of the relationships between M and increasing P_L and the relationships between M and increasing k are provided.

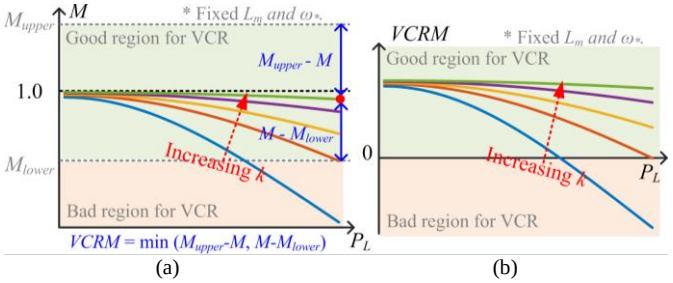


Fig. 5. VCR performance when k and P_L both increase: (a) M performance; (b) $VCRM$ performance.

To evaluate the performance of VCR, the margin of voltage conversion ratio is referred to as $VCRM$. The smaller safety margin of M from M_{lower} and M_{upper} determines the value of

VCRM as given in (13). It can be understood that larger value of *VCRM* represents strong robustness of *VCR*. The relationships between *VCRM* and *k* are provided in Fig. 5 (b). To meet VCR design objective, requirement in (14) should be satisfied.

$$VCRM(k,Q,\omega_*) = \min(M_{upper} - M, M - M_{lowcr}) \tag{13}$$

$$VCRM \geq 0 \tag{14}$$

Therefore, it can be summarized that a larger *k* selection is beneficial for robust VCR.

C. Effects of Parameters on System Stability Performance

(a) Output impedance deduction for CLLC-DCT

Generalized state space averaging (GSSA) modeling method is a common method for impedance deduction. In this method, DC and AC components in state variables are expressed with Fourier series [33]–[35]. But only the zeroth-order and first-order terms in the Fourier series are included in this case to achieve a balance between simplicity and model accuracy. The state variable $x(\tau)$ in which τ lies within $[t - T, t]$ is expressed with Fourier series. The switching function of two full bridges in the circuit which are under the open-loop control with 50% duty ratio can be described with (15).

$$s_1(\tau) = \begin{cases} 1, & 0 \le \tau \le \frac{T}{2} \\ -1, & \frac{T}{2} \le \tau \le T \end{cases}, \quad s_2(\tau) = \begin{cases} -1, & 0 \le \tau \le \frac{T}{2} \\ 1, & \frac{T}{2} \le \tau \le T \end{cases} \tag{15}$$

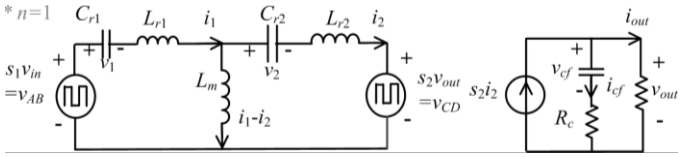


Fig. 6. Equivalent circuit to deduce the output impedance Z_{out_DCT}.

The equivalent circuit model for the deduction of Z_{out_DCT} is given in Fig. 6 [32] in which the turn ratio is taken to be 1 as an example. State variables incorporate i_1, i_2, v_1, v_2 and v_{cf}. The input and output voltage v_{in}, v_{out} are input variables. And the output current i_{out} is the output variable. Then Fourier series is applied to these variables [33]. To form a small-signal model for Z_{out_DCT}, perturbations are injected into the operating point of the steady states, and the results are given in (16)-(17) where the superscript *R* and *I* mean the real part of a complex number and the imaginary part of a complex number, respectively.

$$\frac{d}{dt}\hat{x} = A\hat{x} + B\hat{u} \tag{16a}$$

$$A = \begin{bmatrix} 0 & \omega_s & 0 & 0 & \frac{1}{C_1} & 0 & 0 & 0 & 0 \\ -\omega_s & 0 & 0 & 0 & 0 & \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & \omega_s & 0 & 0 & \frac{1}{C_2} & 0 & 0 \\ 0 & 0 & -\omega_s & 0 & 0 & 0 & 0 & \frac{1}{C_2} & 0 \\ -\frac{L_2+L_m}{a} & 0 & -\frac{L_m}{a} & 0 & 0 & \omega_s & 0 & 0 & 0 \\ 0 & -\frac{L_2+L_m}{a} & 0 & -\frac{L_m}{a} & -\omega_s & 0 & 0 & 0 & 0 \\ -\frac{L_m}{a} & 0 & -\frac{L_2+L_m}{a} & 0 & 0 & 0 & 0 & \omega_s & 0 \\ 0 & -\frac{L_m}{a} & 0 & -\frac{L_2+L_m}{a} & 0 & 0 & -\omega_s & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{R_c C_f} \end{bmatrix} \tag{16b}$$

$$B = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{2L_m}{a\pi} & 0 & \frac{2(L_1+L_m)}{a\pi} & 0 & \frac{1}{R_c C_f} \\ 0 & 0 & 0 & 0 & 0 & -\frac{2(L_2+L_m)}{a\pi} & 0 & -\frac{2L_m}{a\pi} & 0 \end{bmatrix}^T \tag{16c}$$

$$a = L_1 L_2 + (L_1 + L_2) L_m \tag{16d}$$

$$\hat{x} = \begin{bmatrix} \langle \hat{v}_1 \rangle_1^R & \langle \hat{v}_1 \rangle_1^I & \langle \hat{v}_2 \rangle_1^R & \langle \hat{v}_2 \rangle_1^I & \langle \hat{i}_1 \rangle_1^R & \langle \hat{i}_1 \rangle_1^I & \langle \hat{i}_2 \rangle_1^R & \langle \hat{i}_2 \rangle_1^I & \langle \hat{v}_{cf} \rangle_0 \end{bmatrix}^T \tag{16e}$$

$$\hat{u} = \begin{bmatrix} \hat{v}_{out} & \hat{v}_{in} \end{bmatrix}^T \tag{16f}$$

$$\langle \hat{i}_o \rangle_0 = C\hat{x} + D\hat{u} \tag{17a}$$

$$C = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & -\frac{4}{\pi} & 0 & \frac{1}{R_c} \end{bmatrix} \tag{17b}$$

$$D = \begin{bmatrix} -\frac{1}{R_c} & 0 \end{bmatrix} \tag{17c}$$

The transfer function in (18) can be obtained with the above small signal model. And Z_{out_DCT} can be obtained as (19) where $G_{vout}(s)$ is the transfer function of v_{out} to i_{out}.

$$G(s) = C(sI - A)^{-1} B + D = \begin{bmatrix} G_{vout}(s) & G_{vin}(s) \end{bmatrix} \tag{18}$$

$$Z_{out\_DCT} = v_{out} / i_{out} = 1 / G_{vout}(s) \tag{19}$$

(b) Effects of parameters on system stability performance

For stability analysis, Z_{out_DCT} and Z_{in_CPL} are both needed. Equation (19) has provided the expression of Z_{out_DCT}. As for the input impedance of the CPL, it is intrinsically a negative resistance when the frequency is smaller than the cut-off frequency [36]. Z_{in_CPL} can be calculated with (20) in which V_{BUS} is equal to V_{out} in the cascaded system shown in Fig. 3.

$$Z_{in\_CPL} = -V_{BUS}^2 / P_{CPL} = -V_{out}^2 / P_{CPL} \tag{20}$$

Based on Middlebrook stability criterion, the amplitude of Z_{out_DCT} has to be lower than the Z_{in_CPL} within the entire range of ω. In other words, the global peak amplitude of Z_{out_DCT} (Z_{o_p}) is required to be lower than Z_{in_CPL} as shown in (21).

$$Z_{o\_p} = \max(Z_{out\_DCT}(\omega)) \tag{21a}$$

$$Z_{out\_DCT} < Z_{in\_CPL} \Rightarrow Z_{o\_p} < Z_{in\_CPL} \tag{21b}$$

To assess system stability performance, gain margin (*GM*), which is the amplitude gap between Z_{o_p} and Z_{in_CPL}, is defined in (22). For lower possibility of system instability, the value of *GM* needs to be big enough to reduce the risk of impedance intersection.

$$GM = Z_{in\_CPL} - Z_{o\_p} \tag{22}$$

Considering the cascaded power converter system incorporating CLLC-DCT and a CPL, the Bode plot of Z_{out_DCT} when *k* increases is shown in Fig. 7 (a). The Nyquist plot of this cascaded system with a rising *k* is presented in Fig. 7 (b). The relationships between *GM* and P_L are described in Fig. 7 (c) when *k* increases. From all the above information, larger *k* selectin has been found to contribute to smaller Z_{o_p} and can

make Nyquist plot away from (-1, *j*0). Thus, a larger *k* is recommended from the perspective of system stability.

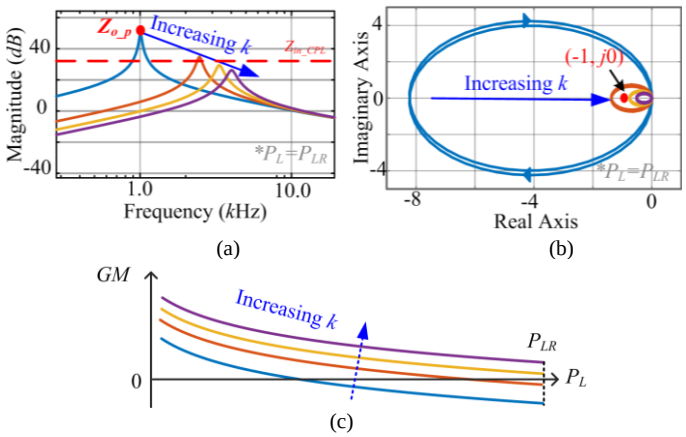


Fig. 7. Effects of *k* on system stability performance: (a) Bode plot of Z_{out_DCT} when *k* increases; (b) Nyquist plot of Z_{out_DCT} when *k* increases; (c) *GM* performance when *k* and P_L both increases.

To directly present the possible instability phenomenon, under the design conditions given in Table I, *k* is selected at 32 based on the design approach in Ref. [19]. The experimental waveforms are presented in Fig. 8 and 9.

TABLE I. DESIGN SPECIFICATIONS

DCT	V_{in}	n	f_s	P_L	L_m	C_f	R_c
	200V	1	100*k*Hz	1kW	2*m*H	10μF	0.3Ω
CPL	V_i	V_o	f_{buck}	P_{CPL}	L_{buck}	C_{buck}	
	200V	150V	100*k*Hz	1kW	47μH	10μF	

Fig. 8 presents the waveforms of the CLLC-DCT and the CPL when they both operate alone. Under this circumstance, both subsystems enjoy stability.

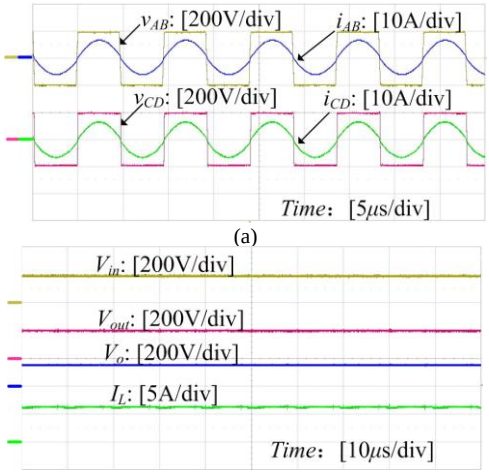


Fig. 8. Hardware experiments of individually operating case (*k* = 32): (a) waveforms of the CLLC-DCT when it operates alone; (b) input and output voltage of the CLLC-DCT, output voltage and inductor current of the CPL when they both operate alone.

However, as shown in Fig. 9, when the two subsystems work in a cascaded structure, the system suffers from serious oscillation. The large oscillation amplitude of i_{AB} in the CLLC-DCT and I_L in the buck converter will inevitably destroy power devices.

Therefore, for the sake of system instability, a large *k* is recommended to avoid system instability, which will seriously do great damage to the whole cascaded system.

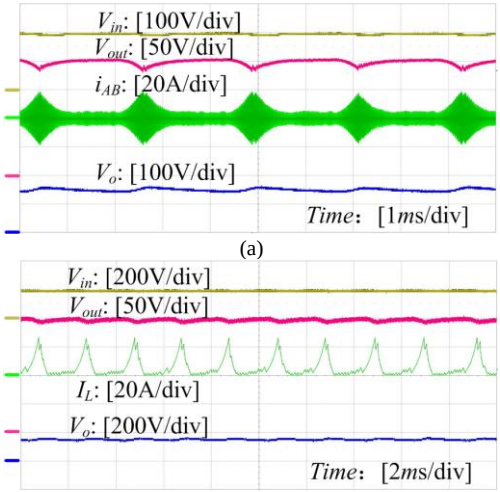


Fig. 9. Hardware experiments of the system in which the CLLC-DCT and the CPL cascade with each other (*k* = 32): (a) unstable waveforms of the CLLC-DCT in the cascaded system; (b) unstable waveforms of the CPL in the cascaded system.

D. Effects of Parameters on Efficiency Performance

Based on the power efficiency analysis in [15], there mainly exist 6 parts of power loss in the CLLC-DCT: core loss P_{T_Fe}, copper loss P_{T_Cu}, driving loss $P_{S(R)\_dr}$, conduction loss $P_{S(R)\_on}$, turn-off loss $P_{S(R)\_off}$ and resonant capacitance loss P_{RC}. Each of them is analyzed as follows.

$$P_{total} = P_{T\_Fe} + P_{T\_Cu} + P_{S(R)\_dr} + P_{S(R)\_on} + P_{S(R)\_off} + P_{RC} \tag{23}$$

a) Core loss P_{T_Fe}

Steinmetz equation can be adopted for the analysis of P_{T_Fe}. The expression is given in equation (24) where V_e, A_e and n_p are the volume of the core, the cross-sectional area of the core and the turn number of primary winding, respectively. I_{m_pk} is the peak magnetizing current. a_0, b_0 and k_c are the Steinmetz coefficients of the adopted magnetic core, which can be found in the datasheet.

$$P_{T\_Fe}(L_m) = k_c f_s^{a_0} \left[L_m I_{m\_pk} / \left(n_p A_e \right) \right]^{b_0} V_e \tag{24}$$

b) Copper loss P_{T_Cu}

As shown in (25), P_{T_Cu} can be calculated with the RMS current flowing through the primary side (I_{p_rms}) and the equivalent ac resistance of the transformer (R_{T_ac}).

$$P_{T\_Cu}(C_{r1}, C_{r2}, L_{r1}, L_{r2}, L_m) = I_{p\_rms}^2 R_{T\_ac} \tag{25}$$

c) Driving loss $P_{S(R)\_dr}$

$P_{S(R)\_dr}$ can be calculated with the gate charge ($Q_{S(R)g}$) and the driving voltage ($V_{S(R)g}$) as expressed in (26).

$$P_{S(R)\_dr} = 4 Q_{S(R)g} V_{S(R)g} f_s \tag{26}$$

d) Conduction loss $P_{S(R)\_on}$

$P_{S(R)\_on}$ can be calculated with the RMS current flowing through primary side I_{p_rms} and the RMS current flowing through secondary side I_{s_rms} as well as the on-resistor of the main switches or rectifiers ($R_{S(R)\_on}$), which is given in (27).

$$P_{S(R)\_on}(C_{r1}, C_{r2}, L_{r1}, L_{r2}, L_m) = 2 I_{p(s)\_rms}^2 R_{S(R)\_on} \tag{27}$$

e) Turn-off loss $P_{S(R)\_off}$

$P_{S(R)\_off}$ can be derived with the dead time (T_{dead}) and the drain-source parasitic capacitance of the MOSFET (C_{oss}), which is given in (28).

$$P_{S\_off}(L_m) = \left(I_{m\_pk}^2 T_{dead}^2 f_s\right) \Big/ 12C_{oss} \tag{28a}$$

$$P_{R\_off}(L_m) = \left(I_{m\_pk}^2 T_{dead}^2 f_s\right) \Big/ 12n^2 C_{oss} \tag{28b}$$

f) Loss of resonant capacitance P_{RC}

The expression of P_{RC} is given in (29) where δ is dielectric loss angle.

$$P_{RC}(C_{r1}, C_{r2}, L_{r1}, L_{r2}, L_m) = \left(I_{p(s)\_rms}^2 \tan\delta\right) \Big/ \left(2\pi f_s C_{r1(2)}\right) \tag{29}$$

More detailed elaboration of efficiency analysis has been presented in [15] and thus only brief analysis is provided above. It should be noticed that the skin and proximity effects are neglected when the switching frequency is below 200 *k*Hz [37]. With the analysis on every part of power loss, overall efficiency of the CLLC-DCT is obtained with (30) in which P_L is the load power of the CLLC-DCT. According to (23)-(30), the curve of η regarding P_L and k can be plotted in Fig. 10 where P_{LR} is the rated values of P_L. An increasing k is found to be beneficial for higher efficiency.

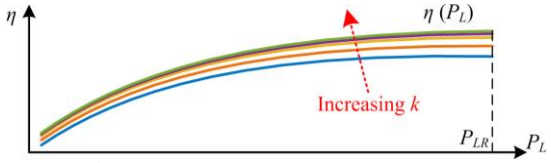


Fig. 10. Change of η regarding k and P_L.

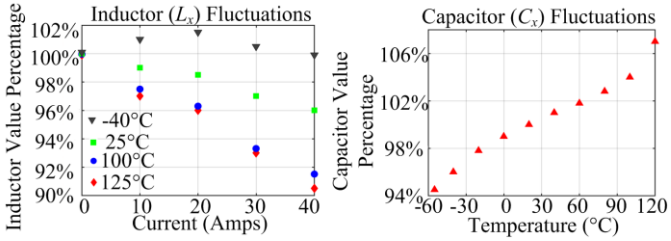
$$\eta = \frac{P_L}{P_L + P_{total}} \tag{30}$$

To conclude, a large k selection can benefit the power efficiency performance of the CLLC-DCT.

III. Challenges in Designing CLLC-DCT Brought by Parameter Fluctuations

In this section, challenges because of fluctuations of circuit parameters in designing CLLC-DCT are discussed.

A. Fluctuations of Inductor and Capacitor Values



(a) (b)

Fig. 11. An example of parameter fluctuations (a) fluctuation range of inductance; (b) fluctuation range of capacitance.

The values of inductance and capacitance are very sensitive to temperature and power changes. An example of their fluctuations has been given in Fig. 11 according to datasheets [17] and [18]. The fluctuation range can be up to 10%. The following two expressions describe the possible parameter fluctuations mathematically, where L_x represents the inductors and C_x represents the capacitors. The fluctuation ranges for inductance and capacitance are estimated as τ% and ξ%. L_{xR} represents the rated value of inductance and C_{xR} represents the rated value of capacitance.

$$L_x \in \left[\left(1-\tau\%\right)L_{xR}, \left(1+\tau\%\right)L_{xR}\right] \tag{31}$$

$$C_x \in \left[\left(1-\xi\%\right)C_{xR}, \left(1+\xi\%\right)C_{xR}\right] \tag{32}$$

As analyzed above, circuit parameters will directly affect VCR, system stability and power efficiency performance. Thus, it is of great significance to take the effects of parameter fluctuations into considerations.

B. Challenges in Designing CLLC-DCT for Robust VCR

From Fig. 5, it can be found that VCR performance will be directly affected by changing P_L and k. Besides that, when parameter fluctuations in (31) to (32) happen, M will also be impacted because they affect ω_* in (12e) and Q in (12f). It is assumed that the variation of ω_* and Q has the following ranges:

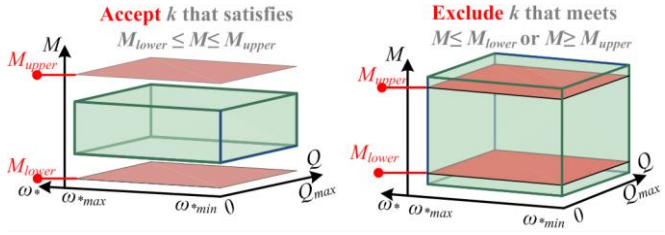
$$\omega_* \in \left[\omega_{*\min}, \omega_{*\max}\right] when \begin{cases} L_x \in \left[\left(1-\tau\%\right)L_{xR}, \left(1+\tau\%\right)L_{xR}\right] \\ C_x \in \left[\left(1-\xi\%\right)C_{xR}, \left(1+\xi\%\right)C_{xR}\right] \end{cases} \tag{33a}$$

$$\omega_{*\min} = 2\pi f_s \sqrt{L_{r1R}(1-\tau\%)C_{r1R}(1-\xi\%)} \tag{33b}$$

$$\omega_{*\max} = 2\pi f_s \sqrt{L_{r1R}(1+\tau\%)C_{r1R}(1+\xi\%)} \tag{33c}$$

$$Q \in \left[0, Q_{\max}\right] when \begin{cases} L_x \in \left[\left(1-\tau\%\right)L_{xR}, \left(1+\tau\%\right)L_{xR}\right] \\ C_x \in \left[\left(1-\xi\%\right)C_{xR}, \left(1+\xi\%\right)C_{xR}\right] \\ P_L \in \left[0, P_{LR}\right] \end{cases} \tag{34a}$$

$$Q_{\max} = \frac{n^2\sqrt{L_{r1R}(1+\tau\%)/C_{r1R}(1-\xi\%)}}{8V_{outR}^2(1-\alpha\%)/\pi^2 P_L}. \tag{34b}$$



(a) (b)

Fig. 12. The challenge due to parameter fluctuations in designing CLLC-DCT from the VCR point of view: (a) acceptable case of VCR; (b) unacceptable case of VCR.

With considerations of varying values of ω_* and Q, as a result, M will also change, whose changing range is described with the green box in Fig. 12. Hence, to guarantee robust VCR when parameter fluctuations happen, the task is to search for a k which realizes the situation in Fig. 12 (a) and eliminate the k selection which will cause the situation in Fig. 12 (b).

To evaluate the performance of VCR, $VCRM_{min\_k}$ is defined in (35). It represents the smallest $VCRM$ for one k when ω_* and Q change as (33) and (34). This $VCRM_{min\_k}$ can stand for the worst performance for the corresponding k from the perspective of VCR.

$$VCRM_{min\_k} = \min\left(VCRM(k, \omega_*, Q)\right) when \begin{cases} \omega_* \in \left[\omega_{*\min}, \omega_{*\max}\right] \\ Q \in \left[0, Q_{\max}\right] \end{cases} \tag{35}$$

According to (14) and (35), to ensure the robust VCR when the circuit parameters fluctuate, it is necessary to select k which satisfies (36).

$$VCRM_{min\_k} \geq 0 \tag{36}$$

Therefore, the challenge in designing CLLC-DCT from VCR point of view can be simplified as to search for $VCRM_{min\_k}$ under one k when parameter fluctuates and load power changes and then choose a k that realizes robust VCR.

C. Challenges in Designing CLLC-DCT for System Stability and Satisfactory Efficiency

Because of changing temperature and operating power, even if the rated values of parameters have been decided, the practical values may deviate from the rated ones. In Fig. 13, one ball on each side stands for one possible practical value and the green bar represents the rated value. Due to the fact that parameters fluctuate unpredictably, there exist infinite possibilities for the values after fluctuations, so the total number of parameter combinations could also be infinite.

(a) Challenges in designing CLLC-DCT from system stability point of view

Take all possible values of circuit parameters after fluctuations into considerations. As shown in Fig. 13, there is one Z_{o_p} for every parameter combination. For one k, all Z_{o_p} make up set Ω_{Z_k} as defined in (37). Among Ω_{Z_k}, the largest Z_{o_p} is named as Z_{max_k} in (38), which causes the worst stability performance under this k selection.

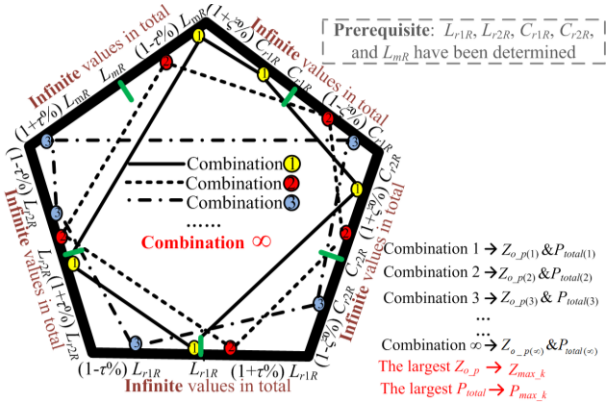


Fig. 13. Fluctuation of C_{r1}, C_{r2}, L_{r1}, L_{r2} and L_m and their influences.

$$\Omega_{Z\_k}=\left\{Z_{o\_p(1)},Z_{o\_p(2)},Z_{o\_p(3)},\cdots,Z_{o\_p(\infty)}\right\} \tag{37}$$

$$Z_{max\_k}=\max\left(\Omega_{Z\_k}\right) \tag{38}$$

As a result, to guarantee the system-level stable operation, k should meet (39) in which GM_{limit} is a predetermined lower boundary for GM to ensure better system stability.

$$Z_{max\_k}\le Z_{in\_CPL}-GM_{\text{limit}} \tag{39}$$

Thus, the challenge in designing CLLC-DCT from the perspective of system stability is simplified as to search for Z_{max_k} under one k when parameter fluctuations are considered and then select a k that can realize system stability.

(b) Challenges in designing CLLC-DCT from power efficiency point of view

Take all possible values of circuit parameters after fluctuations into considerations. Every combination of circuit parameters has one P_{total}. Under one k selection, all P_{total} make up set Ω_{P_k} as defined in (40). Among Ω_{P_k}, the largest P_{total} is named as P_{max_k} in (41), which causes the worst efficiency performance under this k selection.

$$\Omega_{P\_k}=\left\{P_{total(1)},P_{total(2)},P_{total(3)},\cdots,P_{total(\infty)}\right\} \tag{40}$$

$$P_{max\_k}=\max\left(\Omega_{P\_k}\right) \tag{41}$$

Therefore, to meet power efficiency design objective, k should meet (42) in which η_{limit} is a required lower boundary of efficiency.

$$P_{max\_k}\le P_{\text{limit}}=P_L(1-\eta_{\text{limit}})/\eta_{\text{limit}} \tag{42}$$

Thus, the challenge in designing CLLC-DCT from power efficiency point of view is simplified as to search for P_{max_k} under one k when parameter fluctuations are considered and then select a k that can realize efficiency design objective.

IV. The Proposed Five-Stage Design Methodology for CLLC-DCT

In the following parts, the proposed five-stage design methodology for the CLLC-DCT will be detailly introduced. Also, in Section IV-B, RODD-PSO which is used in the first to the third stage is introduced, including its principal and the ways of applying it to the design approach. At the final part of this section, a design example is given to show how to adopt the proposed design methodology.

A. The Proposed Five-Stage Design Methodology for CLLC-DCT

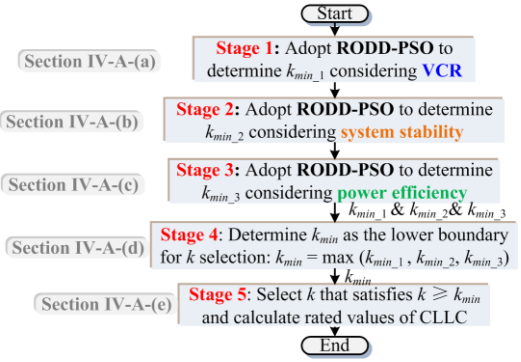


Fig. 14. Flow diagram of the design methodology for CLLC-DCT.

There are totally five stages in the proposed design process which are displayed in Fig. 14.

In Stage 1, k_{min_1}, the lower boundary for k selection will be decided from the perspective of VCR. In the next two stages, the lower boundary for k will be considered from system stability and power efficiency point of view to decide k_{min_2} and k_{min_3}, respectively. And in the fourth stage, three design objectives will be considered at the same time to decide final k_{min}. In the end, rated values of circuit parameters will be calculated.

(a) Stage 1: *determine* k_{min_1} *considering VCR*

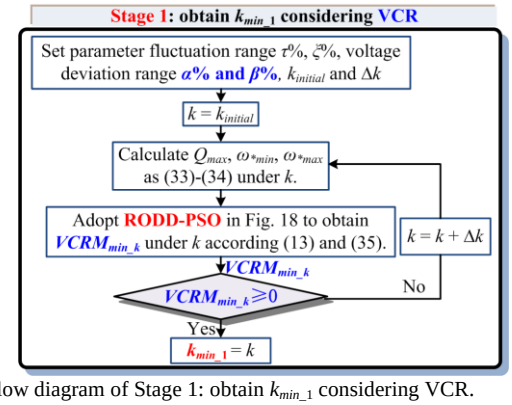


Fig. 15. Flow diagram of Stage 1: obtain k_{min_1} considering VCR.

From the perspective of VCR, the first stage of the proposed design methodology will determine k_{min_1}, of which the flow diagram is given in Fig. 15.

At the beginning of Stage 1, the estimated ranges of parameter fluctuations and the acceptable maximum variation ranges of DC bus voltages should be given. Also, the initial value of k ($k_{initial}$) can be set according to the practical requirement of specific application, which is usually larger than 1 and is expected to be as low as possible to avoid big volume of CLLC-DCT. Additionally, the interval of k selection (Δk) can be decided according to the design accuracy since small Δk leads to more accurate design but results in high complexity.

After all these settings, every k from k_{min} is assessed by RODD-PSO regarding its $VCRM_{min\_k}$ in (35). Only when the condition in (36) is met, the searching process will cease. Otherwise, k will be replaced by $k + \Delta k$ and assessed by RODD-PSO. The value of k at which Stage 1 ends will be k_{min_1}.

The k selection which is no smaller than k_{min_1} is able to guarantee robust VCR performance of the CLLC-DCT even if parameters fluctuations happen.

(b) Stage 2: *obtain k_{min_2} considering system stability*

From the perspective of system stability, the second stage of the proposed design methodology will determine k_{min_2}, of which the flow diagram is given in Fig. 16.

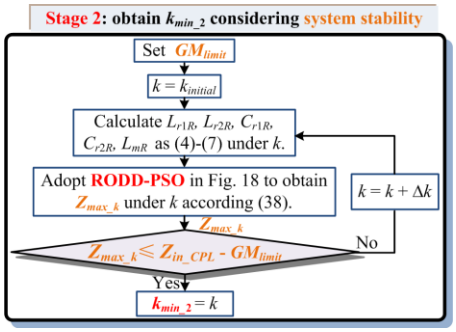


Fig. 16. Flow diagram of Stage 2: obtain k_{min_2} considering system stability.

At the beginning of the second stage, the required GM limit (GM_{limit}) is defined. Then, every k from k_{min} is assessed by RODD-PSO regarding its Z_{max_k} in (38). Only when the condition in (39) is met, the searching process will cease. Otherwise, k will be replaced by $k + \Delta k$ and assessed by RODD-PSO. The value of k at which Stage 2 ends will be k_{min_2}.

The k selection which is no smaller than k_{min_2} will be acceptable from system stability point of view even when parameter fluctuations happen.

(c) Stage 3: *obtain k_{min_3} considering power efficiency*

From the perspective of power efficiency, the third stage of the proposed design methodology will determine k_{min_3}, of which the flow diagram is given in Fig. 17.

At the beginning of the third stage, the required minimal efficiency (η_{limit}) is defined. After that, every k from k_{min} is assessed by RODD-PSO regarding its P_{max_k} in (41). Only when the condition in (42) is met, the searching process will cease. Otherwise, k will be replaced by $k + \Delta k$ and assessed by RODD-PSO. The value of k at which Stage 3 ends will be k_{min_3}.

The k selection which is no smaller than k_{min_3} will be acceptable from power efficiency point of view even when parameter fluctuations happen.

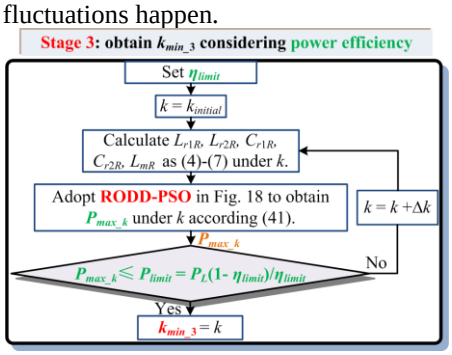


Fig. 17. Flow diagram of Stage 3: obtain k_{min_3} considering power efficiency.

(d) Stage 4: *determine k_{min} as the lower boundary for k selection*

With k_{min_1} obtained in Stage 1, k_{min_2} obtained in Stage 2 and k_{min_3} obtained in Stage 3, k_{min} is determined with (43) in Stage 4.

$$k_{\min} = \max\left(k_{\min\_1}, k_{\min\_2}, k_{\min\_3}\right) \tag{43}$$

The k selection which is no smaller than k_{min} will be acceptable considering all three design objectives even when parameter fluctuations happen.

(e) Stage 5: *choose k and calculate rated parameters*

In the fifth stage, one value of k will be chosen from the range $k \geq k_{min}$. Smaller k should be given priority for the purpose of a compact design since the larger k results in the bigger volume of CLLC-DCT [19]. Afterwards, rated CLLC parameters can be obtained by following (4) to (7). With these parameters, the designed CLLC-DCT can meet robust VCR, stability and satisfactory efficiency even when parameter fluctuations happen.

B. RODD-PSO [31] *Used in the Proposed Design Methodology for CLLC-DCT*

In the proposed design methodology for the circuit parameters of CLLC-DCT, the possible fluctuations of inductance and capacitance values are taken into accounts with the utilization of RODD-PSO [31]. It is one of the cutting-edge PSO algorithms and it can reliably achieve high accuracy in optimization results. Thus, Stage 1 to Stage 3 will all adopt RODD-PSO to find the worst performance under every k selection regarding each design objective: $VCRM_{min\_k}$, Z_{max_k} and P_{max_k} in the first to the third stage, respectively.

RODD-PSO utilizes randomly occurred time-delays to reveal the past personal best result and global best result in the searching history, and thus it can avoid local optima and realize higher accuracy compared with other PSO algorithms. The velocity update equation with historical information in RODD-PSO is given in (44), where v_i and x_i are the velocity and position of the i^{th} particle, respectively. z represents the current iteration time. ω is the inertia weight which linearly decreases with the increasing iteration number z. $pbest_i$ represents the i^{th} particle's personal best result, and $gbest$ represents the global best result among the whole swarm. N is the length of the distributed time-delays considered. $\alpha_{(\phi)}$ is an indicator which has N dimensions whose elements are randomly sampled between 0 and 1, the random sampling of which enables the historical time-delays to randomly occur. c_1, c_2, c_3 and c_4 are the time-varying acceleration

coefficients, and r_1, r_2, r_3 and r_4 are the corresponding random numbers whose values are uniformly distributed in [0,1]. m_l and m_g are the intensity parameters governing the historical time-delays, which are adaptively tuned according to the evolutionary state of the swarm. After the update of velocity, the positions are updated with (45).

$$\begin{aligned} v_i(z+1) &= \omega v_i(z) + c_1 r_1 (pbest_i(z) - x_i(z)) \\ &+ c_2 r_2 (gbest(z) - x_i(z)) + m_l c_3 r_3 \sum_{\phi=1}^{N} \alpha_{(\phi)} (pbest_i(z-\phi) - x_i(z)) \\ &+ m_g c_4 r_4 \sum_{\phi=1}^{N} \alpha_{(\phi)} (gbest(z-\phi) - x_i(z)) \end{aligned} \quad (44)$$

$$x_i(z+1) = x_i(z) + v_i(z+1). \quad (45)$$

The flow diagram of applying RODD-PSO in the proposed design methodology is described in Fig. 18, where the blue, orange and green information are specially for the first, second and third stage, respectively. Overall, after the initialization of RODD-PSO, the objective values (*VCRM*, Z_{o_p} or P_{total}) of all particles in the swarm are evaluated. After that, the personal best and global best results are updated and further stored as historical information. Afterwards, inertia weight and acceleration coefficients are tuned. And then, equations in (44) and (45) will be used to renew the velocity of particles and the position of particles. The procedure repeats until it meets the stopping criterion, and the globally optimal result will be searched as the required $VCRM_{min\_k}$, Z_{max_k} or P_{max_k}.

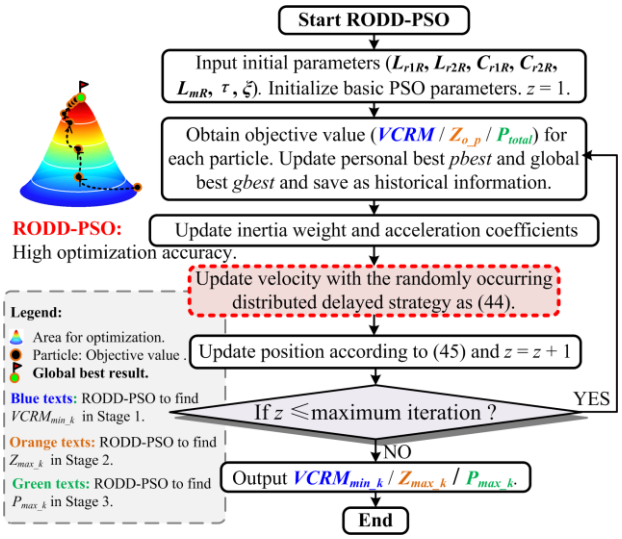


Fig. 18. Flow diagram of applying RODD-PSO in the proposed design methodology.

By applying RODD-PSO to Stage 1, 2 and 3, the design process of CLLC-DCT can take the possible fluctuations of inductor and capacitor into thorough considerations when guaranteeing the three design objectives.

C. Design Example of CLLC-DCT with the Proposed Design Methodology

To introduce how to utilize this proposed design methodology, a design example is provided here. The design conditions are given in Table I. For this design example, the predetermined limits are set as below:

TABLE II. PREDETERMINED LIMITS IN THE DESIGN EXAMPLE

Symbols	τ%	ξ%	α%	β%	GM_{limit}
Values	10%	10%	10%	10%	3 dB
Symbols	η_{limit}	P_{limit}	$k_{initial}$	Δk	
Values	96.5%	36.27W	1	1	

The design process follows the proposed design methodology which has been introduced in detail in Section IV-A and B. The design results in every stage can be summarized below:

- 1st Stage: Based on the process in Fig. 15, k_{min_1} equals to 32;
- 2nd Stage: Based on the process in Fig. 16, k_{min_2} equals to 143;
- 3rd Stage: Based on the process in Fig. 17, k_{min_3} equals to 40;
- 4th Stage: Based on (43), k_{min} equals to 143.
- 5th Stage: Choose k = 143 and then the corresponding values of circuit parameters are computed based on (4) to (7), as shown in Table III.

TABLE III. DESIGN RESULTS

Rated parameter values of CLLC when k = 143					
Symbols	L_{mR}	L_{r1R}	L_{r2R}	C_{r1R}	C_{r2R}
Values	2.0 mH	14.0μH	14.0μH	181.1 nF	181.1 nF

To evaluate the performance theoretically, RODD-PSO in Fig. 18 is used to assess k selection at 143: $VCRM_{min\_143}$ = 0.171 ($VCRM_{min\_143} > 0$); P_{max_143}= 32.72W ($P_{max\_143} < P_{limit}$); Z_{max_143}= 29.03dB ($Z_{in\_CPL} - Z_{max\_143} > GM_{limit}$). And the power efficiency at rated conditions is 96.84% and the power loss is 32.58W. Thus, according to (36), (39) and (42), when k is selected at 143, three design objectives (VCR, system stability and power efficiency) can be met.

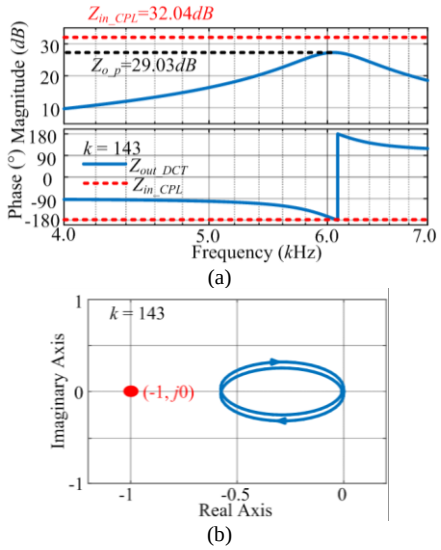


Fig. 19. Performance evaluation from the aspect of system stability for this design example: (a) Bode plot; (b) Nyquist plot.

The performance evaluation for the designed CLLC-DCT from the aspect of system stability is conducted with the Bode plot and Nyquist plot in Fig. 19. From Fig. 19 (a), at least 3 *dB GM* can be found. In additional, (-1, *j*0) is not rung by Nyquist plot in Fig. 19 (b). Both of these two figures theoretically indicate good system stability performance of the designed CLLC-DCT.

In this design example, k selection is dominated by the cascaded system stability objective by following the proposed design methodology. However, it is not always this case. The design objective which will dominate the final k selection depends on the design conditions and settings of α% (β%),

GM_{limit} and η_{limit}.

With the above design results, the instability of the cascaded system in Fig. 9 can be analyzed: the selection of k (k = 32) in the designed CLLC-DCT fails to reach the lower boundary for k (k_{min_2} = 143) from the system stability point of view. Under same design conditions, only k no smaller than 143 is able to guarantee system stability.

TABLE IV. AVERAGE COMPUTATION TIME OF RODD-PSO

Stage	Stage 1 to find $VCRM_{min\_k}$	Stage 2 to find Z_{max_k}	Stage 3 to find P_{max_k}
Average computation time	0.0567s	1.5099s	0.0582s

The average computational time of the RODD-PSO for one k in every stage is given in Table IV. The average computation time of Stage 2 is longer than the other two stages because Z_{out_DCT} derivation from state space matrix to transfer function has high complexity. Even though parameter design is conducted offline, the overall time performance proves the easy and fast implementation of this proposed design approach.

V. EXPERIMENTAL VERIFICATION

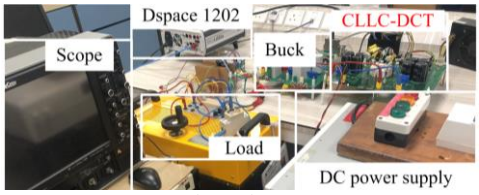


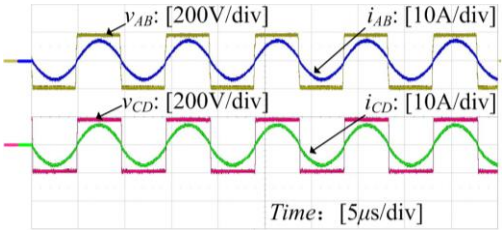
Fig. 20. Experimental hardware platform of the cascaded system (1kW).

TABLE V. SPECIFICATIONS OF THE PROTOTYPE

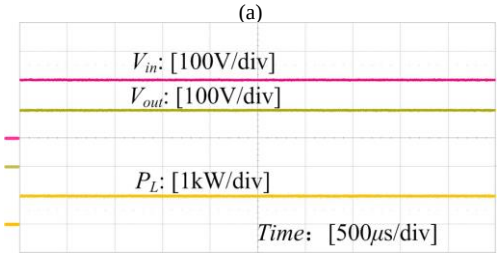
Items	Parameters
MOSFET	C2M0080120D
T_{dead}	250 *ns*

To validate the effectiveness of the proposed design methodology, a prototype for the design example in Section IV-C is built, and the experimental hardware platform is shown in Fig. 20. Some details of this prototype have been listed in Table V. The values of CLLC are selected according to the rated values calculated in Table III.

A. Operating Waveforms of the Designed CLLC-DCT



(a)



(b)

Fig. 21. Waveforms in individual operating condition under rated power: (a) voltage and current of the primary side (v_{AB}, i_{AB}), and voltage and current of secondary side (v_{CD}, i_{CD}); (b) input and output voltage (V_{in}, V_{out}) and load power P_L.

The figures above present the experimental operating waveforms of the designed CLLC-DCT with rated power. v_{AB} and v_{CD} can be found to be in phase with i_{AB} and i_{CD}, respectively. Thus, excellent power and voltage transmission ability can be proved.

B. Hardware Validation of the Designed CLLC-DCT from VCR Point of View

The following experiments have been conducted to verify the performance of the designed CLLC-DCT from VCR point of view.

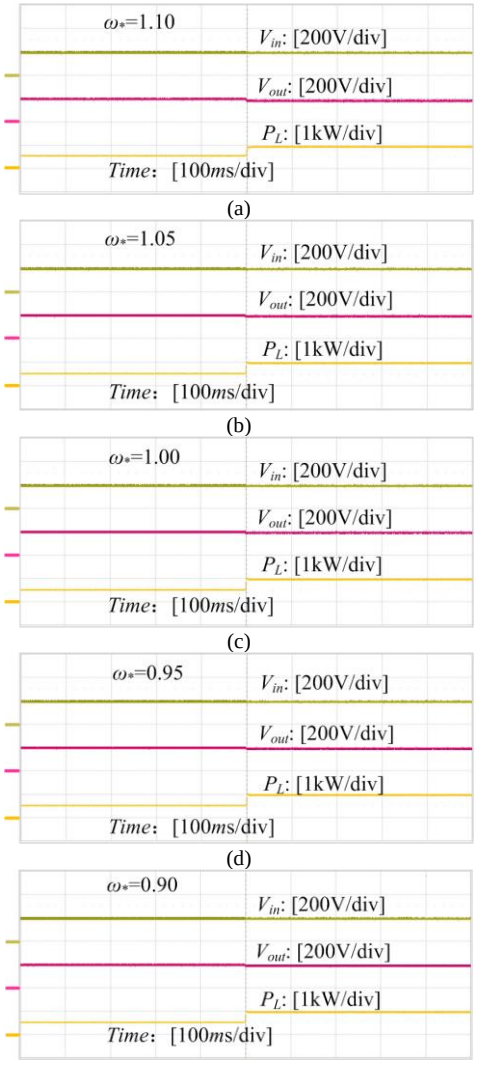


Fig. 22. Waveforms of V_{in} and V_{out} of CLLC-DCT with a load step at different ω_*: (a) when ω_* is equal to 1.10; (b) when ω_* is equal to 1.05; (c) when ω_* is equal to 1.00; (d) when ω_* is equal to 0.95; (e) when ω_* is equal to 0.90.

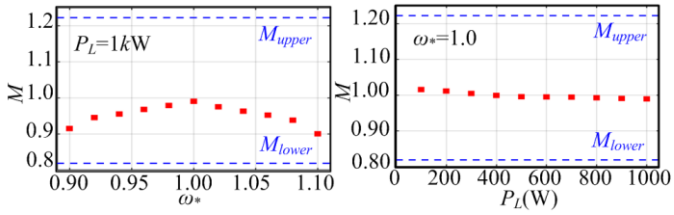


Fig. 23. M in hardware experiments: (a) when ω_* varies from 0.90 to 1.10 under rated power; (b) when P_L varies from 10% load to 100% load and ω_* is equal to 1.

Fig. 22 presents the waveforms of input and output voltage (V_{in}, V_{out}) of CLLC-DCT when a power load step is injected from 50% power to 100% power. The experiments are conducted at different ω_*, which is to mimic the parameter fluctuations. It experimentally validates that this designed CLLC-DCT achieves robust VCR.

Also, the measured M under different ω_* and P_L is plotted in Fig. 23. It shows that the variation of M is within the acceptable range between M_{lower} (0.82) and M_{upper} (1.22).

C. Hardware Validation of the Designed CLLC-DCT from System Stability Point of View

The following experiments have been conducted to verify the performance of the designed CLLC-DCT from the perspective of system stability.

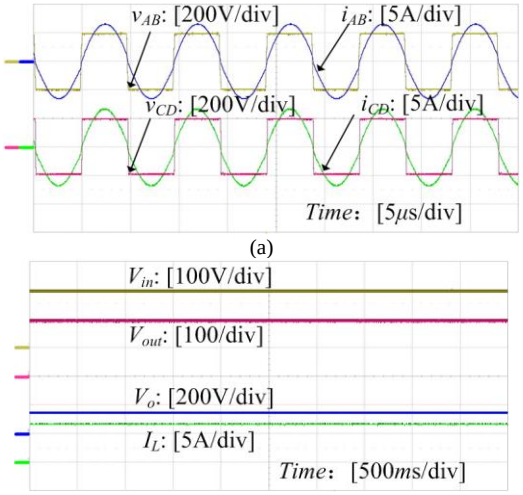


Fig. 24. Hardware experiments of the cascaded system under rated conditions: (a) waveforms of the CLLC-DCT ; (b) waveforms of the Buck converter.

Fig. 24 presents the experimental results when the designed CLLC-DCT and buck converter as the CPL cascades with each other. The waveforms of the designed CLLC-DCT in the cascaded system are given in Fig. 24 (a). The waveforms of the Buck converter are presented in Fig. 24 (b). In a word, this cascaded system enjoys stable operation under rated conditions.

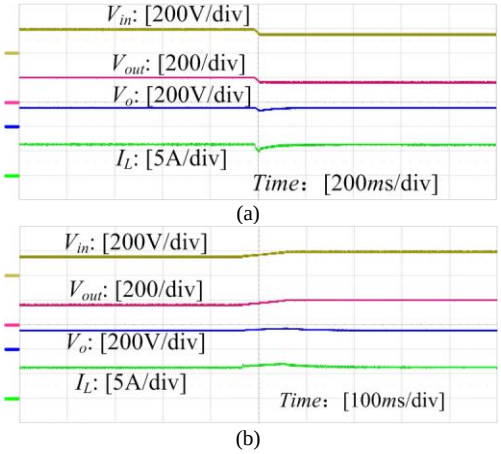


Fig. 25. Hardware experiments of the cascaded system with a step of voltage: (a) V_{in} changes from 200V to 160V; (b) V_{in} changes from 160V to 200V.

Fig. 25 gives the operating waveforms with a voltage step. V_{in}, V_{out}, V_o and I_L are presented when there is a step of V_{in} from 200V to 160V and from 160V to 200V. The experimental results show that this cascaded system of the designed CLLC-DCT and a CPL enjoys quick recovery from a voltage step to stable operation.

Fig. 26 gives the operating waveforms with a load step. V_{in}, V_{out}, V_o and I_L are presented when there is a load step from 1000W to 500W and from 500W to 1000W. This load step experiment is also conducted under different ω_* to mimic the fluctuations of parameters. All the experimental results in Fig. 26 show that this cascaded system incorporating the designed CLLC-DCT and a CPL enjoys quick recovery from a load step to stable operation even when circuit parameters vary.

This designed CLLC-DCT has been experimentally verified to guarantee system stability when it cascades with a CPL.

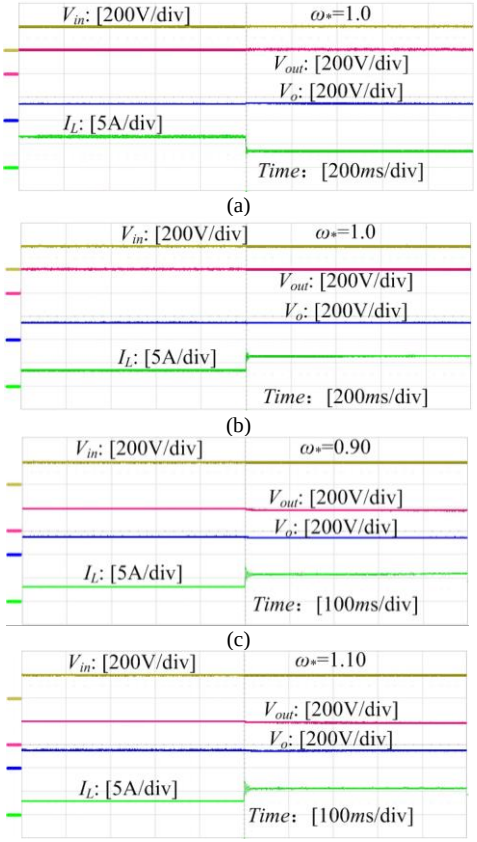
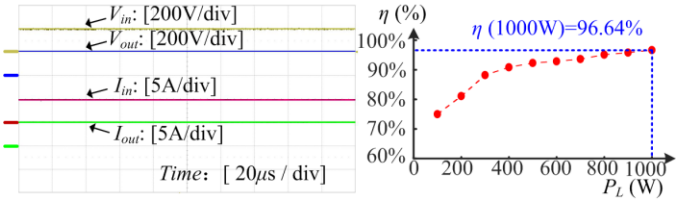


Fig. 26. Hardware experiments of the cascaded system with a load change: (a) when P_L changes from 100% to 50% and ω_* is equal to 1.0; (b) when P_L changes from 50% to 100% and ω_* is equal to 1.0; (c) load change when ω_* is equal to 0.90; (d) load change when ω_* is equal to 1.10.

D. Hardware Validation of the Designed CLLC-DCT from Power Efficiency Point of View

The following experiments have been conducted to verify the performance of the designed CLLC-DCT from power efficiency point of view.

Fig. 27 (a) shows the experimental waveforms of the input voltage (V_{in}), input current (I_{in}), output voltage (V_{out}) and output current (I_{out}) of the designed CLLC-DCT, which are used for efficiency measurement.



(a) (b)

Fig. 27. Efficiency verification: (a) experimental operating waveforms of V_{in}, I_{in}, V_{out}, I_{out}; (b) measured efficiency in experiments.

Fig. 27 (b) shows the efficiency measurement results. The measured efficiency at 100% load is 96.64%, which is very close to the theoretical analysis (96.84%). The measured power loss of hardware prototype is 34.77W, which is also very close to the theoretical analysis (32.58W).

To conclude, all experiments in this section have proved that the proposed design methodology for the CLLC-DCT is valid in ensuring three design objectives (VCR, system stability and power efficiency).

VI. Conclusion

Parameter design for the CLLC-DCT applied in DC microgrid is focused on in this paper. The proposed design methodology is able to guarantee the designed CLLC-DCT can meet three design objectives in VCR, system stability and power efficiency at the same time. In addition, full considerations of parameter fluctuations are realized with RODD-PSO in the design process. Thus, the designed CLLC-DCT can maintain good comprehensive performance in three design objectives against parameter fluctuations.

The key point of the proposed design methodology for the CLLC-DCT lies in determining the proportion of magnetizing inductance to leakage inductance. Three design objectives are considered one by one from Stage 1 to Stage 3 to determine this proportion. The final selection range of this proportion is determined in Stage 4 where all three design objectives are considered simultaneously. In Stage 5, the rated values of parameters for CLLC-DCT are calculated. In the end of this paper, experimental verification has been conducted with 1 kW prototype to prove the validity of the proposed design methodology for CLLC-DCT.

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