Digital Control Method of Synchronous Rectification for Bidirectional CLLLC Converter

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***Abstract*—In order to solve the problems of low efficiency and high temperature of the switches under a wide range of working conditions of the bidirectional CLLLC resonant converter, this paper proposes a digital controller of synchronous rectification for the rectifier on the secondary side of the high frequency transformer. Based on the analysis of operating mode of different frequency, the relationship between driving time of the synchronous switch on the secondary side and the driving time of the active device on the primary side is obtained. In a wide operating frequency range, the delayed turn-on and leading turn-off time of driving signal for the synchronous devices is obtained respectively by calculation and piecewise linear function fitting methods. Compared with other synchronous rectification control, this method is realized by pure digital control, and can be flexibly applied to high-power applications with a wide range of bus voltage variation. Furthermore, this method is suitable for bidirectional converters. The shortcoming that the analog control chip is sensitive to bus voltage variation can be overcomed by using this method. Meanwhile, the proposed control method is simple to be implemented and is very cost-effective. Finally, a simulation platform and experimental prototype were built to verify the proposed method. The results of simulation and experiment show that this strategy can increase the efficiency of the CLLLC system by about 3%, and the temperature of the synchronous switches are greatly decreased.**

Keywords—On Board Charger, Bidirectional CLLLC converter, PFM Control, Digital Controlled Synchronous Rectification, Multiple Linear Fitting.

I. INTRODUCTION

With the continuous development of the renewable energy industry, electric vehicles have become the mainstream direction of the future vehicle industry by the advantages of environmental protection and energy saving. In the applications such as on-board chargers (OBC) and charging station, the isolated bidirectional DC-DC converter with bidirectional power flow characteristics has become the research hotspot[1-4]. The bidirectional isolated DC-DC conversion topologies mainly include bidirectional resonant converter (CLLLC) and bidirectional active full bridge (DAB) converter[5]. Usually, Dual Active Bridge Converter (DAB) only achieves zero voltage switching (ZVS) of the switches on both sides within a narrow power range when the voltage matches. However, the control is complicated [6-7]. Due to the symmetrical structure of its own resonant network and good soft switching characteristics,

CLLLC not only ensure the consistency of bidirectional operation, but also can achieve zero voltage turn-on and zero current turn-off in a wider voltage range and power conversion range[8]. In addition, since the resonant current of CLLLC is sinusoidal, its turn-off losses are smaller than that of DAB [9-10].

When the power of the converter increases, the losses caused by the forward voltage drop of the diode is getting bigger. In order to improve the efficiency of the resonant converter and reduce the temperature of the switches and the losses, the synchronous rectification technology is generally used. Traditional synchronous control is generally realized by using an analog synchronous rectifier chip, which controls the switch by detecting the voltage or current on both sides of the switch device[11-12]. For example, literature [13] and [14] proposed to use the professional chips to achieve synchronous rectification, but it adds peripheral circuits and requires

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additional circuits for bidirectional energy transfer. Also, the structure is more complicated. In a wide range of voltage applications such as the charging application for the vehicle batteries, it is difficult to find a synchronous rectifier chip that can match the withstand voltage, and meanwhile the additional chips and peripheral circuits will reduce the reliability and efficiency of the converter and increase the costs [15] as well. In the bidirectional power flow and wide voltage applications of CLLLC converter, the use of digital control is more flexible and stable than analog control. Literature [15] first proposed digital synchronous control, but it neither conducts specific analysis nor proves the feasibility through experiments. Besides, some scholars proposed digital synchronous rectification control by using differential comparator circuits and high-speed comparators to turn on the synchronous switches. A digital control method by sampling the zero-crossing point of drain-source voltage is proposed[16], but this method will increase hardware cost, complexity and bring additional sampling cost and losses.

This paper proposed a new digital synchronous rectification control strategy. First, considering the characteristics of the synchronous switching device and the conditions of zero voltage turn-on, the turn-on delay time of the synchronous driving signal is obtained through calculation. Secondly, based on the PFM control mode of the CLLLC topology, the relationship of turn-off time of the synchronous switch and the active switch is analyzed and summarized, and the linear function segmentation fitting method is used to obtain the leading turn-off time of the synchronous switch before the active switch for different switching frequency operation. Compared with other synchronous rectification control, this method only use software to realize CLLLC synchronous rectification. The proposed method is suitable for high-power and wide-voltage occasions, and is not limited by the direction of energy flow, and it also can be adopted to full operating frequency. Therefore, the new digital synchronous control method greatly reduces the complexity of hardware design and additional hardware costs. In addition, this method is not sensitive to bus voltage changes, and its applicability is much stronger than the existing analog solutions. Finally, a simulation platform and an experimental prototype were built to verify the proposed method. Combined with the results of experiments, it is verified that this strategy can increase the system efficiency by about 3% in high-power and wide-voltage applications. Meanwhile, it can greatly reduce the temperature of the synchronous switching devices.

II. LOSSES ANALYSIS OF BIDIRECTION CLLLC

A. Basic working principle and losses analysis

Resonant bidirectional DC/DC converter topology has symmetrical structure, as shown in Fig. 1. The working characteristics of CLLLC circuit in forward and reverse operation are similar to LLC. V_{in} and V_{out} are the input and output DC voltages of the circuit respectively, the power switches S_1-S_4 and S_5-S_8 respectively constitute two full-bridge H_1 and H_2 of the converters[17-19]. The bridges of H_1 and H_2 work in inverter and rectifier state respectively. Wherein, L_{r1}, L_{r2} and C_{r1}、C_{r2} are the resonant inductance and resonant capacitor respectively, L_m is the magnetizing inductance of the high frequency transformer. Generally, $L_m \gg L_{r1}$, L_{r2}. During the bidirectional operation of the converter, the resonant network operates in ZVS condition[20], which effectively reduces the transmission losses of the converter.

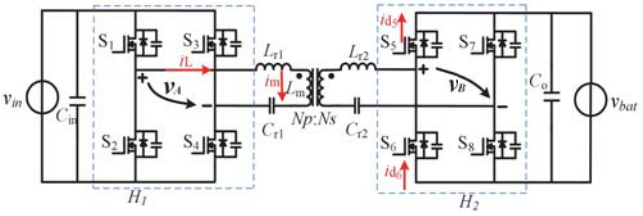


Fig. 1 CLLLC resonant converter

The converter has two resonant frequency points. When the energy is transferred from left to right, as shown in Fig. 1, the inductor L_{r1} and the capacitor C_{r1} resonate together, the resonant frequency is defined as f_{r1}. When L_{r1}, C_{r1} and the magnetizing inductance L_m resonate together, the resonant frequency is defined as f_{r2}. The working frequency of the converter is set to f_s. In order to prevent the CLLLC from being in the capacitive region, the steady-state operating frequency is generally greater than f_{r2}. Under this condition, the working modes of the CLLLC converter are divided into three types: under-resonance $f_s < f_r$, resonant state $f_s = f_r$, over-resonance $f_s > f_r$(f_r=f_{r1}). When the circuit works in steady state, the operating principles of the three states are analyzed respectively below. The operating waveforms of turn-off process of primary switches and turn-on process of secondary switches are concerned.

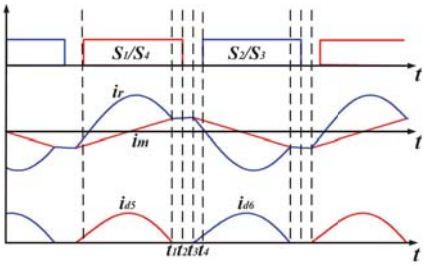
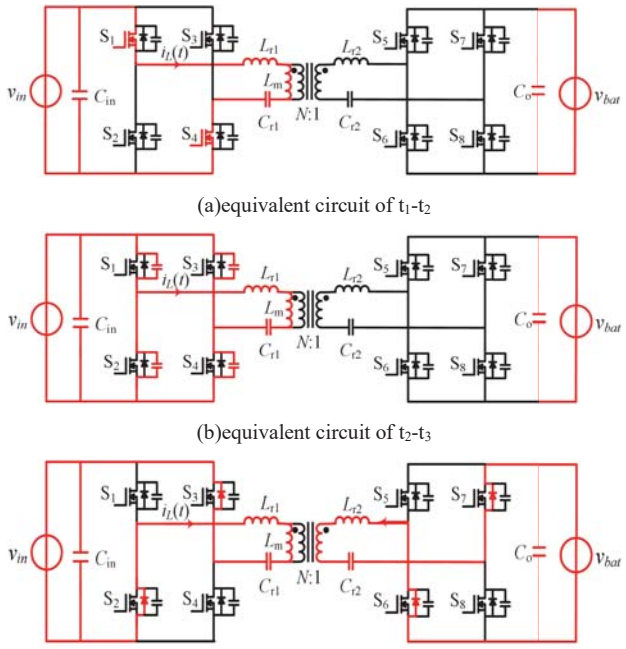


Fig. 2 Key operating waveform of under-resonance.

The operation of under-resonance for CLLLC will be discussed first. As shown in Fig. 2, in the interval t_1-t_2 for under-resonance, the equivalent circuit is shown in Fig. 3(a). S_1 and S_4 are still turned on during this period, the primary resonant current i_r is equal to the excitation current i_m at t_1, the primary side resonant inductance L_{r1}, capacitor C_{r1} and magnetizing inductance L_m resonate together. Because the magnetizing inductance L_m is much larger than L_{r1}, the resonant current can be regarded as a straight line (constant value) during this period, and the current i_{d5} of the secondary side drops to 0, which can achieve Zero Current Switching (ZCS) for the corresponding switches. At t_2, S_1 and S_4 are turned off, the primary side does not transmit energy to the secondary side, there is no current on the secondary side of the transformer.

The equivalent circuit of the dead time interval t_2-t_3 is shown in Fig. 3(b). At t_2, S_1-S_4 are turned off. At t_3, the drain-source voltage of the switches S_1 and S_4 is equal to the input DC voltage Vin and the drain-source voltage of the switches S_2 and S_3 is approximate to zero. It is known that the parasitic capacitance of the switches is much smaller than the resonant capacitance. During this period, there is no current on the secondary side of the transformer.

The equivalent circuit of interval t_3-t_4 is shown in Fig. 3(c), the primary side switches are still off, and the drain-source voltage is zero before the primary side S_2 and S_3 being turned on, therefore the condition of zero voltage switching for S_2 and S_3 is achieved. After fully discharging of the parasitic capacitors S_2 and S_3, the resonant current is freewheeling through the corresponding body diodes, therefore, the voltage of v_p is equal to $-v_{in}$. Then, i_m is linearly changing, whereas C_{r1} resonates with L_{r1}. The secondary side current of the transformer is rectified and carried by the parasitic diodes of S_6 and S_7. In order to realize the zero voltage condition of the secondary side switching devices, the parasitic capacitance of the secondary side switches needs to be charged and discharged. Therefore, the secondary side switches should not be turned on during this period. In order to ensure the complete discharge of the parasitic capacitor, the switching devices in H_2 should be turned on after the turning on of switching devices in H_1. The delayed time of driving signals for the synchronous switches can be derived.



(a)equivalent circuit of t_1-t_2

(b)equivalent circuit of t_2-t_3

Fig. 3 Equivalent circuit of under-resonance mode from t_1-t_4.

Next, the operation of resonant state and over resonance for CLLLC will be discussed. The key waveforms of the primary side driving signal, resonant current, excitation current and secondary current are given respectively in Fig. 4 and Fig. 5. when the converter works at the status of resonance and over-resonance. The detailed operating analysis of these modes have been carried out in previous literatures. Some conclusion will be introduced for further utilization.

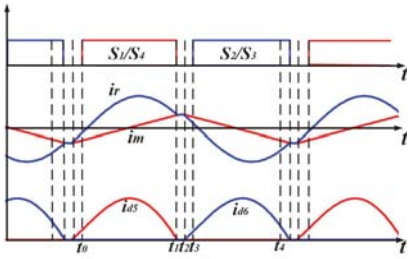


Fig. 4 Key operating waveforms of resonance point mode

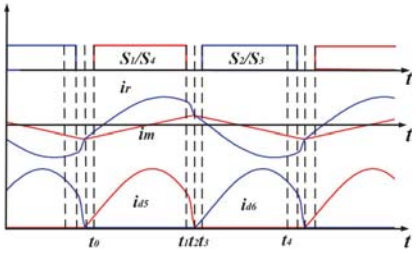
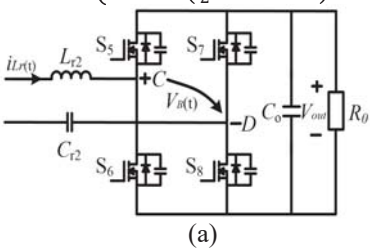


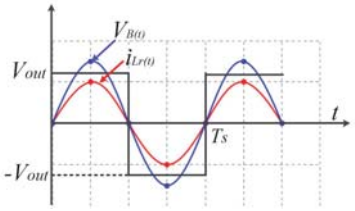
Fig. 5 Key operating waveforms of over-resonance mode

For the SiC switches in H_1 on the primary side of the transformer, the ZVS condition of CLLLC can be realized. And the turn-off loss can be further ignored because the output parasitic capacitor of the switches is much smaller. Therefore, there is almost no switching loss in H_1. Since the body diode conduction losses is much bigger than the active switch channel conduction losses, so it is better to turn on the synchronous switch during the conduction time on the secondary side to reduce the conduction loss. Fig. 6 (a) shows the rectifier network, and Fig. 6 (b) shows the fundamental wave component and input current waveform. Assuming that the driving signals of the switches in one bridge are complementary, and the dead time is ignored. According to the fundamental wave analysis method, the voltage at points C and D of Fig. 6(a) is a square wave that changes between V_{out} and $-V_{out}$[4],

$$V_B(t) = \begin{cases} V_{out} & \left(0 < t < \frac{T_s}{2}\right) \\ -V_{out} & \left(\frac{T_s}{2} < t < T_s\right) \end{cases} \quad (1)$$



(a)



(b)

Fig. 6 (a) Rectification network of secondary side of the transformer, (b)basic operating waveform.

T_s is the working period, $T_s=1/f_s$, f_s is the switching frequency, then we have,

$$V_B(t) = \frac{4V_{out}}{\pi}\sum_{n=1,3,5\ldots}^{\infty} sin(2\pi n f_s t - \theta) \quad (2)$$

t is a time parameter, n is an integer parameter expanded by Fourier series, and θ is the phase difference between v_A and v_B as shown in Fig. 1.

From (2), the corresponding fundamental wave component and the RMS value of the fundamental wave component are:

$$V_B.FHA(t) = \frac{4V_{out}}{\pi} sin(2\pi f_s t - \theta)$$

$$(3) V_B.FHA(RMS) = \frac{2\sqrt{2}}{\pi} V_{out} \quad (4)$$

The impedance of the output is approximately equivalent to the resistance R_o, the voltage and current phases of the output end are the same, and the secondary side resonant current is

$$i_{Lr2}(t) = \sqrt{2} I_{Lr2} \sin(2\pi f_s t - \theta) \quad (5)$$

I_{Lr2} is the RMS value of the secondary side resonant current,

$$i_o = \frac{2}{T_s}\int_0^{\frac{T_s}{2}} |i_{Lr2}(t)| dt = \frac{2\sqrt{2}}{\pi} I_{Lr2} = \frac{V_{out}}{R_o} \quad (6)$$

The RMS value of the resonant current is,

$$I_{Lr2} = \frac{i_o \pi}{2\sqrt{2}} \quad (7)$$

At this time, the secondary side resonant current can be regarded as a sine wave, and the current flowing through the secondary side diodes is the corresponding sine half wave, the RMS value of the diode current i_d is

$$I_d = \frac{I_{Lr2}}{\sqrt{2}} = \frac{i_o \pi}{4} \quad (8)$$

If the on-state voltage drop of the parasitic diode of the SiC switches devices is V_{rev}, the on-state losses generated by the secondary side rectifier circuit in a single cycle is: $P_s = 4V_{rev} \times I_d = V_{rev} i_o \pi$ (9)

If the dead time is ignored, the losses on the secondary side of the CLLLC are related to the output current on the secondary side and the diode conduction voltage drop.

B. Modulation strategy for synchronous control

According to the above analysis, the turn-on and turn-off moment of the synchronous driving signals is related to the operating frequency, so the relation between the driving time and the frequency should be analyzed and derived. Therefore, it is necessary to make a specific analysis of the working conditions of the synchronization strategy.

When CLLLC works in both directions, the circuit needs to achieve the lowest and highest gain within the range of voltage changes. When CLLLC works in the forward direction, the circuit quality factor is obtained according to the equivalent circuit in Fig. 6 (a).

$$Q = \frac{2\pi f_r L_r}{R_{ac}} \quad (10)$$

The Q factor is inversely proportional to the equivalent impedance R_{ac}. When the output voltage is constant, the magnitude of R_{ac} is inversely proportional to the power at the output.

Fig. 2 shows the gain versus the normalized frequency with different Q. Let Q_2 and Q_1 be the corresponding Q value under full load and light load respectively, $Q_2 > Q_1$, and set the corresponding gain range of CLLLC to Gain1~Gain2. As shown in Fig. 7, the gain curve describes the change rule of the converter gain. In order to prevent the topology from working in the capacitive region, the operating frequency is limited with f_{w1}-f_{w2} (f_{w1} and f_{w2} correspond to the normalized frequencies w_1 and w_2).

When the voltage at both ends of the converter is constant, according to the design requirements and gain curve, the circuit topology can achieve the maximum and minimum gains under full load conditions through PFM control. Generally, in practical applications, affected by circuit components, PCB and non-ideal factors in control, minimum gain adjustment under light load conditions cannot be achieved. Since Q is inversely proportional to R_{ac}, the Q value is smaller while the output power is smaller. As shown in Fig. 2, the Q_1 and Q_2 gain curves can achieve the maximum gain at points A and B, but the minimum gain achieved by these two curves in the frequency range is different. If the power is reduced so that the corresponding Q value is less than Q_1, it will be more difficult to achieve low gain output in the frequency range. At this time, PFM modulation is difficult to meet the output demand under light load. In order to realize the accurate control of the full power range of CLLLC, the PWM modulation strategy is adopted for light load to achieve stable output under small current conditions. PFM modulation is still used from medium to full load condition, as shown in Fig. 3.

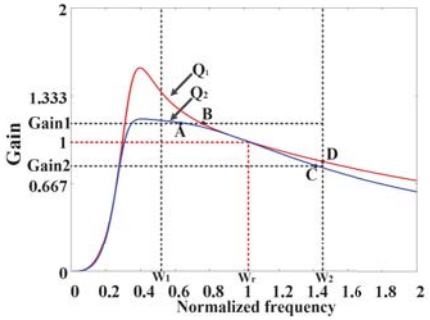


Fig. 7 Gain curve at different Q

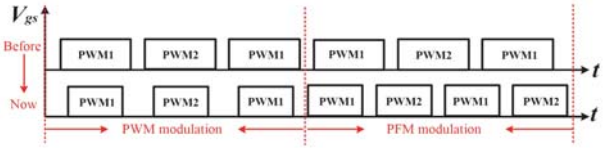


Fig. 8 PWM and PFM control

It should be clarified that when the current is small at light load, the temperature of the devices is not high, and the efficiency improvement brought by synchronous control is

tiny. Therefore, it is necessary to set the threshold of the current and determine the activation of the synchronization strategy according to the current power.

III. SYNCHRONOUS RECTIFICATION CONTROL STRATEGY

According to the above analysis, the synchronous switches need to be turned on at the same time as the active switches are turned on. However, when the synchronous switches are turned on at this moment, and the charge on the junction capacitor will be directly dissipated on the switch, resulting in turn-on losses and quick temperature rising. Therefore, the synchronous switches should be turned on with the delay time of Δt_1, so that the junction capacitor can be fully discharged during this time, and the zero-voltage switching condition of the synchronous switches can be guaranteed. The switching losses caused by synchronous rectification can be reduced.

According to the analysis in previous section, if the current operating frequency $f_s<f_r$, then the synchronous rectifier switches should be turned off before the active switches. However, it is difficult to calculate the theoretical turn-off time in real time according to the current frequency. However, the leading turn-off time can be realized by fitting the function of the operating frequency. If $f_s \geqslant f_r$, the synchronous rectifier switches should be turned off at the same time as the active switches. However, considering the safety of the synchronous switch, a certain leading turn-off time should be added as shown in Fig. 4. The specific leading time Δt_2 can be set by the corresponding fitting function.

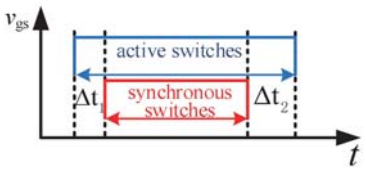


Fig. 9 Turn-off and turn on time of the synchronous driving signals

A. Calculation of the delay time of turn-on for the synchronous switches

The resonant operating point is taken as an example for analysis. Taking the zero-voltage turn-on of the synchronous switch into account, the resonant current needs to provide the energy required for the full charge and discharge of the output capacitor C_{oss} of the synchronous devices. t_A is set to be the time required for the synchronous switching devices to fully charge and discharge, which can be obtained from equation (5),

$$\frac{1}{t_A}\int_0^{t_A}|i_{Lr2}(t)|dt \geq \frac{2V_{out}C_{oss}}{t_A} \tag{11}$$

Then we have

$$\frac{1}{t_A}\int_0^{t_A}\left|\sqrt{2}I_{Lr2}\sin(2\pi f_s t-\theta)\right|dt \geq \frac{2V_{out}C_{oss}}{t_A} \tag{12}$$

The resonant frequency point $\theta = 0°, f_s = f_r$ is the resonant frequency, (12) can be simplified to:

$$1-\frac{8f_sV_{out}C_{oss}}{i_o} \geq cos2\pi f_r t_A \tag{13}$$

From the above analysis, tA can be obtained, which is the minimum time to achieve the condition of ZVS for the secondary synchronous switches. In order to fully charge and discharge the output capacitor, the following equation must be satisfied:

$$t_A \geq \frac{arccos\left(1-\frac{8f_sV_{out}C_{oss}}{i_o}\right)}{2\pi f_r} \tag{14}$$

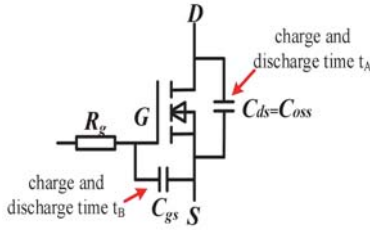


Fig. 10 Parasitic capacitance of SiC device

As shown in Fig. 5, with the same driving resistance R_g, C_{gs} will affect the turn-on and turn-off time. If the dead time of the driving signals for the two switches of the same bridge arm is too short, the upper and lower switches may work in the linear region at the same time, and the switches will be heated up severely and even get damaged. In SiC devices, in order to enhance the filtering effect, 1~2nF capacitors are proposed to connect on both sides of the drive.

The delay time $t_{on\text{-}delay}$ and $t_{off\text{-}delay}$ (both can be found in the switch data sheet) of signal should also be taken into consideration. Therefore, the minimum delayed turn-on time Δt_{1min} of the synchronous switching devices is:

$$\Delta t_{1min} = t_A + t_B + t_{on-delay} + t_{off-delay} \tag{15}$$

The turn-on delay time of Δt_{1min} should satisfy to ensure the ZVS condition for the synchronous switches.

B. Fitting function of leading time of turning-off for the synchronous switches

According to the analysis of previous section, the turn-off lead time of the synchronous switches is related to the working frequency. In this section, the piecewise linear function is used to fit the relation of the lead time versus the operating frequency. According to the subsequent experimental prototype design, the resonant frequency f_{r1} is selected as 160kHz when the CLLLC is working in the power forward flow mode, and the working frequency is set as f_s. Based on the open-loop simulation data, the analysis and fitting curve can be obtained. Furthermore, the open-loop experimental test should be implemented to obtain the fitting curve of the prototype to achieve reliable synchronous rectifier control. According to the parameters of the target prototype, the lead turn-off time versus the operating frequency based on simulation and the open loop test of the prototype are shown in Fig. 6. As a result, in order to get conservative control for the synchronous control, the piecewise linear function of the adopted control strategy can be concluded, as shown in Fig. 6. This piecewise linear fitted curve can meet the requirements of the open-loop switch test and simulation design.

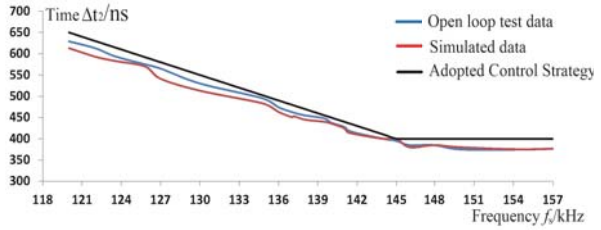


Fig. 11 Open loop experimental curve, simulation curve and adopted fitting curve when the power is positive

According to the calculation in section A and the fitted curve of the control strategy in section B, the lead turn-off time of the forward operation can be obtained as follows:

$$f_s > f_{r1} - 15,\quad \Delta t_2 = 400\text{ns};$$

$$f_s \le f_{r1} - 15,\quad \Delta t_2 = 250\text{ns} + (f_{r1} - f_s) \times 10\text{ns}.$$

For different converter parameters, it is necessary to obtain different piecewise fitting curves for bidirectional transmission through simulation and open-loop testing.

C. *Synchronization of the synchronized rectification of control strategy*

After analyzing the open-loop data in medium load and full load conditions, combined with PFM modulation, the current threshold i_{sr} is established. The output current i_o should be compared with the threshold current of i_{sr}. Then, the control strategy can be obtained as follows,

Synchronous on: $i_o \geqslant i_{sr}$

Synchronous off: $i_o < i_{sr}$

In order to prevent the problem of unstable of the synchronous control switching when i_o switches near the threshold current i_{sr}, another margin value of i_{sr1} is introduced,

$$i_{sr1} = i_{sr} - A(A \ll i_{sr}) \tag{16}$$

During the current switching process, the turn-on and turn-off of the synchronous switches are controlled by comparing sampled current with i_{sr1}. In the vicinity of the threshold current i_{sr}, hysteresis control can be implemented to prevent the synchronous turn-on point from being unstable.

In the implementation, the synchronization control strategy is determined according to different operating frequency, and the corresponding time is recorded in the DSP by calculation and curve fitting. The time is determined according to the simulated data combined with the open-loop experimental test. The specific implementation process is shown in Fig. 8. The process can be described as follows,

1) Judge the current working direction and select the corresponding resonant frequency

2) After calculation and experiment, the appropriate turn-off time and turn-on time of the synchronous switches for different operating frequency are obtained to be recorded.

3) Different frequency range fitting formulas are obtained and recorded in DSP. When the converter is working, DSP needs to select different segmented functions online according to the current operating frequency under normal operating conditions to achieve synchronous rectification control.

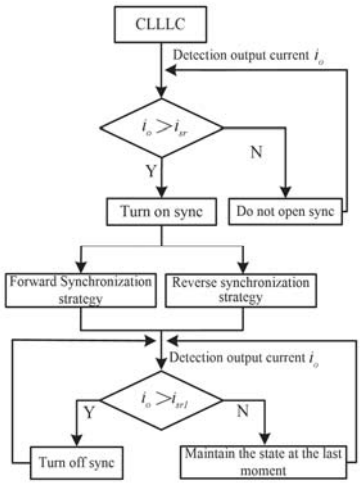


Fig. 12 Synchronization control flow chart Experiment Verification

IV. EXPERIMENT VERIFICATION

In order to verify the feasibility and effectiveness of the digital synchronization scheme, a prototype of bidirectional CLLLC is built, as shown in Fig. 14. Wherein, the input voltage v_{in} is 370V-530V and the output voltage v_{out} is 250V-500V respectively. Assuming that the direction of energy flowing from v_{in} to v_{out} is the forward operating direction, the resonant frequency is 160kHz, and the reverse direction of energy flowing is from V_{out} to V_{in}. The forward operating direction is experimented in this paper.

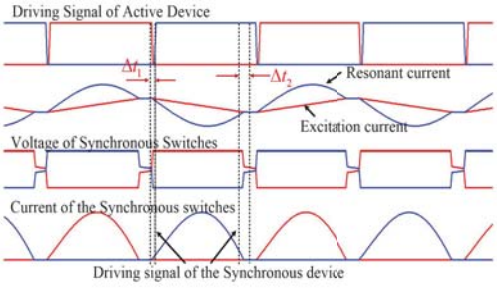
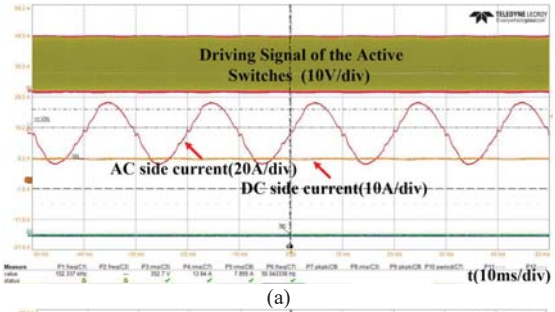


Fig.13 Key simulated waveform

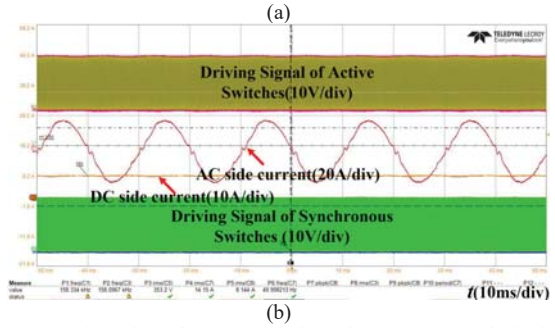
According to the synchronization control flowchart and control requirements, i_o is compared with the threshold current before the digital synchronization is activitated. Considering the application of on board charger(OBC), the threshold current is set to 8A. C_{ds} of the secondary side devices is 76pF, the resonant frequency is 160kHz, and correspondingly t_A=109.74ns is obtained according to equation (13). (The SiC switches are ROHM SCT3040KR)

According to the datasheet and characteristic of the SiC MOSFET switches, the sum of the C_{gs} is about 4nF, the initial driving current is 0.8A, the charging and discharging time is about 90ns, $t_{on\text{-}delay}$ is 6ns, $t_{off\text{-}delay}$ is 29ns, according to (14), Δt_{1min}=228.74ns. when CLLLC works in forward operation. Considering the margin, set the turn-on delay time Δt_1 to 400ns during forward operation.

The experimental results are shown in Fig. 10.



(a)



(b)

Fig. 14 Operation of synchronous switches when CLLLC works in forward operation(a) Output current i_o 7.89A(b) Output current i_o 8.14A

When f_s>f_{r1}-15, the corresponding waveforms of delayed turn-on and lead turn-off for the synchronous switches are shown in Fig. 11. The operating frequency is 156kHz.

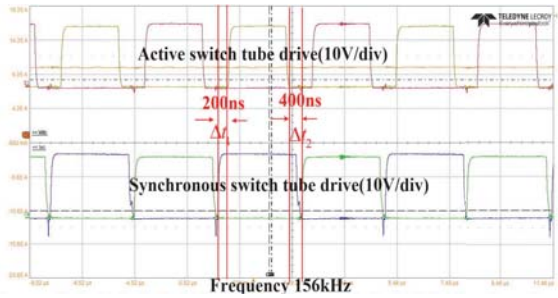


Fig. 15 Operation of synchronous switches for f_s>f_{r1}-15

When $f_s \leqslant f_{r1}$-15, the turn-on delay time is 400ns, and the fitting curve of turn-off lead time is:

$$\Delta t_2 = 250\text{ns} + (f_{r1} - f_s) \times 10\text{ns} \quad (17)$$

The experimental results are shown in Fig. 12. When the operating frequency is 144kHz, the lead time for turn-off is 410ns.

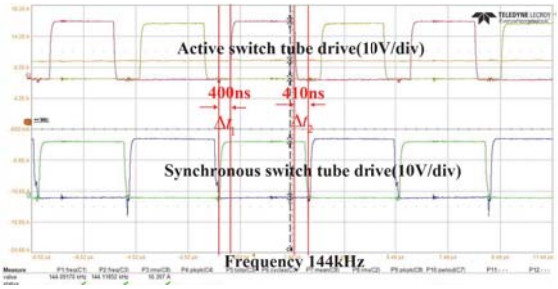


Fig. 16 Operation of synchronous switches for $f_s \leqslant f_{r1}$-15

As shown in Table I, in the two stage OBC bidirectional AC/DC system, the corresponding efficiencies are 93.94% and 91.32% respectively for with or without synchronization control. The power loss of 128W was reduced by using the proposed synchronous control without adding any components.

After the implementation of the digital synchronous control strategy, the efficiency is increased by 2.62%. The voltage drop of the parasitic diode of the SiC devices used in this design is 3.2V. According to formula (9), the theoretical losses value is

$$P_s = V_{rev} i_o \pi = 3.2 \times 12\pi = 120.63 \quad (18)$$

In experiment, due to the coupling of different losses, the calculated value is slightly smaller than the tested value.

Table I Efficiency comparison of synchronous control and non-synchronous control

No synchronization control			
AC input voltage(V)	DC input voltage(V)	Input power(kW)	Output power(kW)
220	350	4.5872	4.189
AC input current(A)	DC input current(A)	Power loss(kW)	Efficiency
20.851	11.971	0.3982	0.9132
Synchronization control			
AC input voltage(V)	DC input voltage(V)	Input power(kW)	Output power(kW)
220	350	4.4513	4.1816
AC input current(A)	DC input current(A)	Power loss(kW)	Efficiency
20.233	11.947	0.2697	0.9394

When the output DC voltage is 350V, the efficiency improvement for different output power is shown in Fig. 13. With different output power in forward operation, both the theoretical and experimental improvement are given. Due to the parasitic parameters for the components, the experimental result is a little bit lower than the theoretical value.

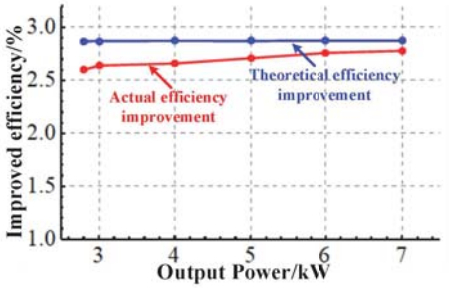
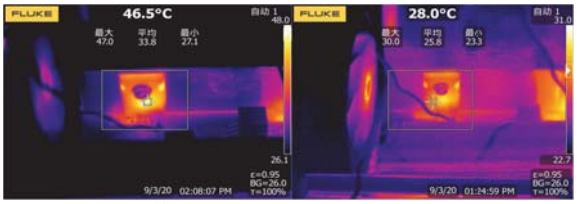


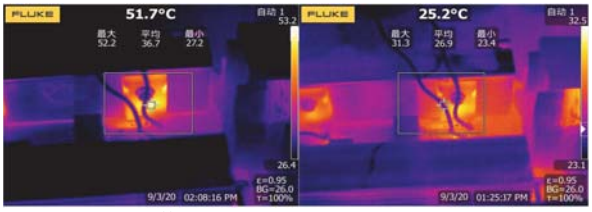
Fig. 17 Efficiency improvement when v_{out} is 350V

From the efficiency improvement curve, it can be seen that in the forward operation, in medium load and heavy load conditions, the efficiency can be effectively improved by the digital synchronous rectification control.

Synchronous control not only can improve the efficiency, but also can effectively solve the thermal problems. When the DC input is 300V and output is 350V, the output current is 12A, the temperature of the synchronous switches for with and without digital synchronization is tested. In Fig. 14, when the prototype is working in the forward operation, the temperature of the synchronous switching devices of the same bridge arm decreases by about 17°C and 20.9°C by activating the proposed control.



Sync off Sync on



Sync off Sync on

Fig. 18 Temperature comparison of switching devices of the same bridge arm

It should be pointed out that the fitting curves used in this paper might not be the optimist one. It takes time to do the simulation and open-loop test to optimize the piecewise linear function to tightly fitting the relation of the lead time of turn-off for the synchronous switches versus the operating frequency.

V. CONCLUSION

This paper proposes a digitized synchronous rectification strategy for CLLLC converters with full operating frequency range. First, the device characteristics and zero-voltage operating conditions are discussed, and the turn-on delay time of the synchronous switch driving signal is obtained by analysis and calculation. Secondly, based on the PFM control mode of the CLLLC topology, the relationship of turn-off time between the synchronous switches and the active switches is summarized. And the synchronous switches need to be turned off in advance by the method of piecewise linear function fitting. Compared with other synchronous rectification control, this method only uses software to realize CLLLC synchronous rectification, it is suitable for high-power and wide-voltage occasions, and it is not restricted by the direction of energy flow. This proposed method can help to achieve full frequency coverage without additional hardware costs, which greatly reduces complexity of the hardware design. The fitting curve margin according to the dispersion and change of the component parameters can be set in the control method, which can be easily realized by the MCU. The proposed method is relatively simple and has stronger applicability than the existing analog solutions.

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