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Gain optimization control method for CLLLC resonant converters under phase shift mode

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Abstract

Bi-directional capacitor-inductor-inductor-inductor-capacitor (CLLLC) resonant converter is widely used in applications such as energy storage systems and portable power stations to efficiently charge/discharge batteries. However, an efficient CLLLC resonant converter has a challenge of covering a wide battery voltage range with various load conditions. Especially at light load, output voltage tends to rise due to parasitic capacitance and could eventually go out of regulation. In this paper, phase shift control is introduced to main output voltage regulation at light load. In addition, a novel synchronous rectifier control method is proposed in this abstract to eliminate the nonlinearity effect caused by parasitic capacitance.

1 CLLLC design consideration

1.1 The basic working principle of the CLLLC converter

Bi-directional CLLLC resonant converter, shown in Fig. 1, is mainly used to charge and discharge batteries in energy storage systems (ESS). The magnetizing inductance of the transformer in the figure is L_m. L_{r1} and L_{r2} are the resonant inductances of the primary and secondary sides, respectively. L_{r1} and L_{r2} are the combined inductances of the transformer leakage inductance with discrete series inductance on each side, respectively. C_{r1} and C_{r2} are the resonant capacitors (and also serve as DC blocking capacitors) of the primary and secondary sides. D_{S1}~D_{S8} are body diodes, and C_{S1}~C_{S8} are junction capacitors of 8 switches.

Compared to conventional LLC resonant converters, bidirectional symmetric CLLLC resonant converters add an additional resonant inductor L_{r2} and a capacitor C_{r2} on the secondary side to make the structure and gain symmetrical. Detailed CLLLC resonant converter operation can be found in [1].

According to the circuit of the CLLLC resonant converter, there are two resonant frequencies in the CLLLC converter. Taking CLLLC forward operation as an example, one is the resonant frequency when L_{r1} and C_{r1}, L_{r2} and C_{r2} are resonant, which is called the first resonant frequency, and the other resonant frequency is the frequency when L_{r1}, C_{r1} and L_m are resonant, which is called the second resonant frequency. The two resonant frequencies are as follows:

$$f_{r1} = 1/(2\pi\sqrt{L_{r1}C_{r1}}) \tag{1}$$

$$f_{r2} = 1/(2\pi\sqrt{(L_{r1}+L_m)C_{r1}}) \tag{2}$$

The traditional control method of CLLLC resonant converters is frequency control, that is, changing the frequency to obtain different gains. The traditional gain analysis method for resonant converters is first harmonic approximation (FHA)[2], Fig.2 is CLLLC resonant converter FHA equivalent circuit diagram without considering parasitic capacitance. As shown in the Fig. 3, the curve of frequency and gain in the ideal state is shown, where Q represents the quality factor and f_n represents the ratio of the switching frequency f_s and the resonant frequency f_{r1},

$$Q = \sqrt{L_{r1}C_{r1}}/R_{eq} \tag{3}$$

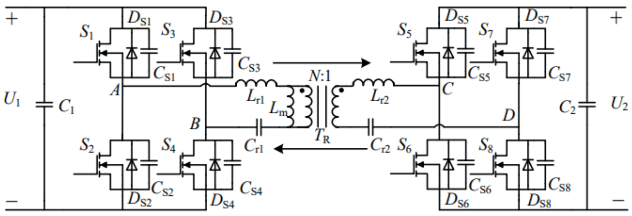

Fig. 1 CLLLC resonant converter topology

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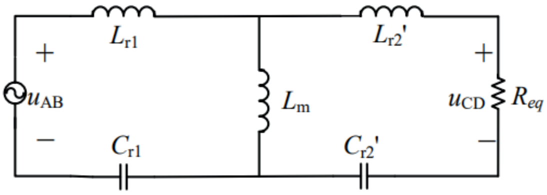

Fig. 2 CLLLC resonant converter FHA equivalent circuit diagram

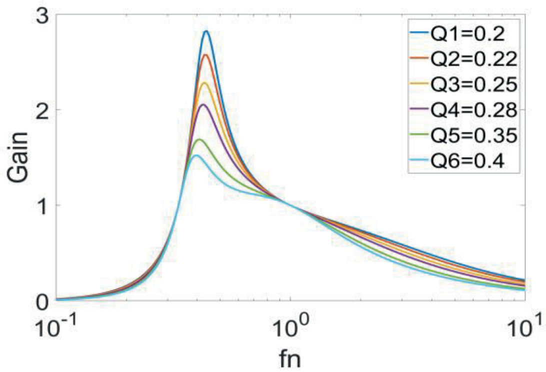

Fig. 3 CLLLC converter gain curve (Ideally)

1.2 Gain regulation problems in light load

Fig. 6 shows parasitic capacitance distribution of CLLLC resonant converter, this chapter will analyze the effect of parasitic capacitance of the transformer on the gain.

The parasitic parameters of a transformer mainly include parasitic capacitance and leakage inductance, and the equivalent circuit containing the parasitic parameters is shown in Fig. 7. In the figure, L_{l1} represents the primary side leakage inductance of the transformer, L_{l2} represents the secondary side leakage inductance, L_m is the magnetizing inductance of the transformer, C_p and C_s represent the inter-turn distributed capacitance of the primary and secondary sides, respectively, and C_{ps} can be expressed as the parasitic capacitance generated by the primary and secondary sides.

Since the bidirectional DCDC converter is used to charge and discharge the battery, and when the battery voltage is low, the battery charger is operating in a pre-charge state with low charging current to prolong battery life. Also, when the battery is nearly full charged, the charging current will become very small. In both conditions the system enters a light load.

Due to the wide input and output voltage range in ESS, we often ensure the switching frequency (f_s) at heavy load is around resonant frequency. Also, the inductance ratio of magnetizing inductor (L_m) and the series inductor (L_s) is generally set to be large for efficiency optimization. However, a large inductance ratio might result in output voltage out of regulation under light load conditions using variable frequency control.

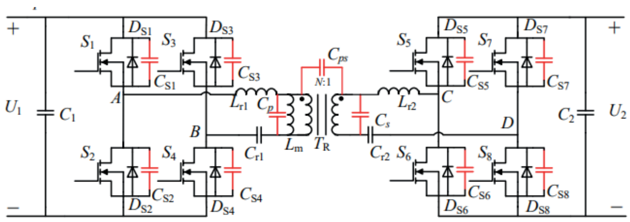

Fig. 6 Parasitic capacitance distribution of CLLLC resonant converter

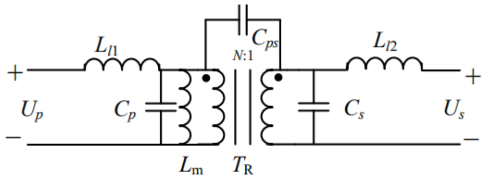

Fig. 7 High frequency transformer equivalent circuit

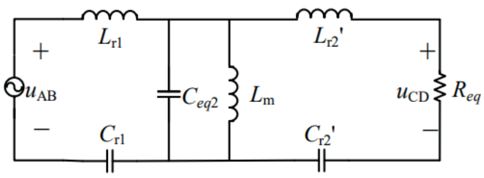

Fig. 8 Consider the distributed capacitance transformer equivalent circuit

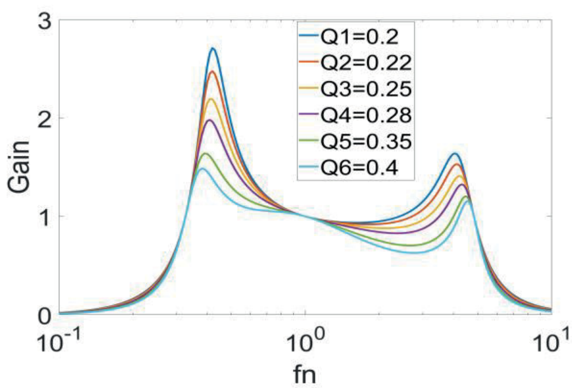

Fig. 9 CLLLC converter gain curve

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Moreover, the parasitic capacitance C_{ps} on the transformer could have a big effect on the gain of converter[3]. Fig. 8 shows the equivalent circuit considering the distributed capacitance on the transformer, where C_{eq2} is the distributed capacitance of the primary and secondary sides of the transformer equivalent to the primary side. After adopting FHA, we can get the curve of frequency and gain considering the parasitic capacitance, as shown in Fig. 9.

From this figure, we can see the parasitic capacitance of the transformer will lead to negative input/output voltage gain slope when $f_s > f_r$ – meaning we are not able to simply reduce gain by increasing f_s. In order to regulate output voltage under light load conditions, phase-shift control is introduced here.

Therefore, for the CLLLC resonant converter, the control scheme proposed in this paper is a phase-shift and varying-frequency hybrid control scheme. And in order to achieve a seamless switch, the control block diagram is shown in the Fig. 10.

The system uses the loop output to select either frequency modulation or phase shift mode, When the load is light and the gain needs to be reduced, the frequency rises and enters phase shift mode when reach the maximum frequency.

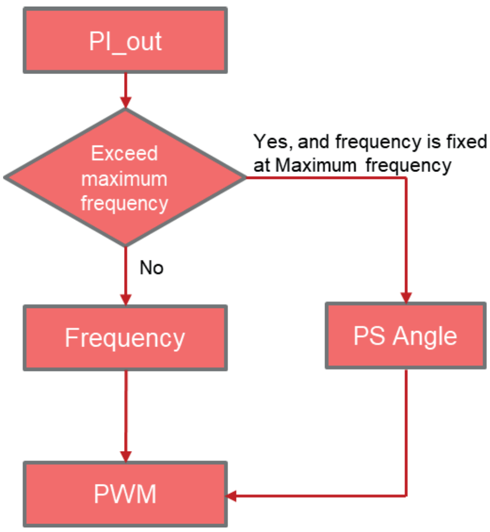

Fig. 10 The control block diagram in phase shift control

2 Phase-shift control in CLLLC converter

2.1 Phase shift basic operation

When a CLLLC converter operates in phase-shift control, f_s is fixed and the output voltage can be regulated by changing the phase shift angle φ between the two bridge legs[4]. The ideal waveform (without considering parasitic capacitance) of a phase-shift controlled CLLLC converter is shown in Fig. 11. By increasing φ, we are able to reduce the effective duty cycle and reduce input/output voltage gain, the relationship between the two is linear, as shown in Fig. 12.

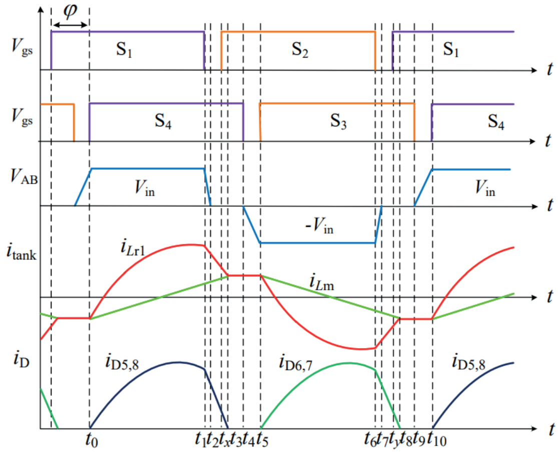

Fig. 11 Ideal waveforms under Phase Shift Mode(f_s>f_r)

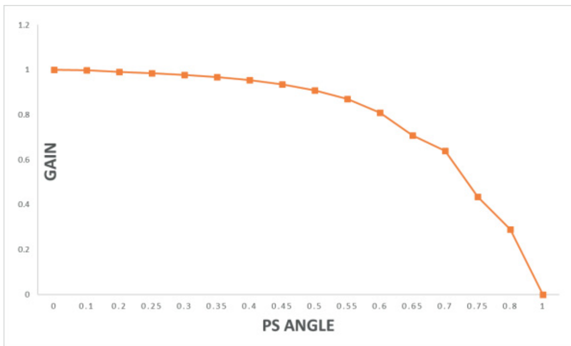

Fig. 12 Gain curve under Phase Shift Mode ideally

2.2 Problems caused by parasitic capacitance

Fig. 11 shows the ideal waveforms under Phase Shift mode, however if we consider parasitic capacitance such as the MOSFETs output capacitance (COSS) shown in Fig. 6, the tank current

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will oscillate with the output capacitors as shown in Fig. 13 compared to Fig. 14, and Fig. 15 is Experimental waveforms with C_{oss} under phase shift mode.

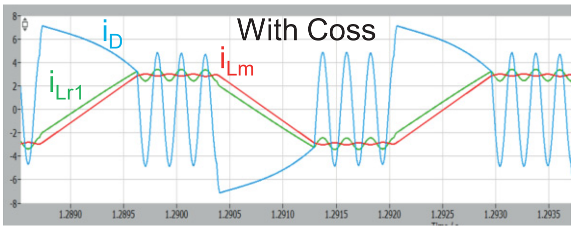

Fig. 13 Simulation waveforms with C_{OSS} under Phase shift mode (and open loop)

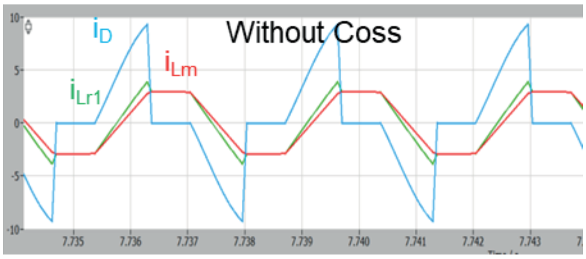

Fig. 14 Simulation waveforms without C_{OSS} under Phase shift mode (and open loop)

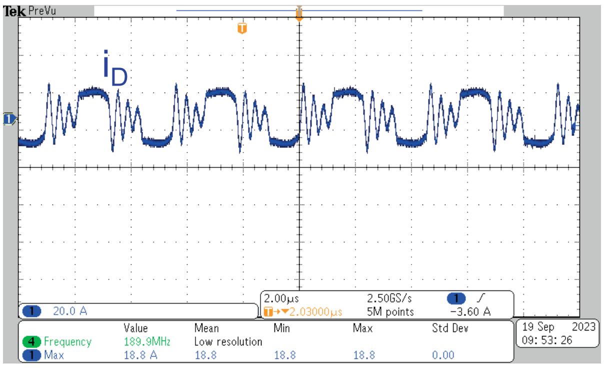

Fig. 15 Experimental waveforms with C_{OSS} under Phase shift mode (and open loop)

As the current initial condition at S1 and S2 turn off transients could be very different due to the oscillation current even with small φ difference. Taking Fig. 16 and Fig. 17 as an example, Ideally, a phase shift angle of 0.4 should transfer less energy than a phase shift of 0.35. But due to the oscillation current, initial current when phase shift angle is 0.4 is higher than it when phase shift angle is 0.35, which means that a phase shift angle of 0.4 will transfer more energy than a phase shift of 0.35.

In this condition, increasing φ is no longer necessary reducing the input/output voltage gain. A gain comparison of a CLLLC converter with and without considering MOSFET C_{OSS} are plotted in Fig. 18. Fluctuation of the gain curve can be observed on the curve by considering MOSFET C_{OSS} in the model. Therefore, φ might be adjusted to a wrong direction under closed loop control and result in large current spikes as shown in Fig. 19.

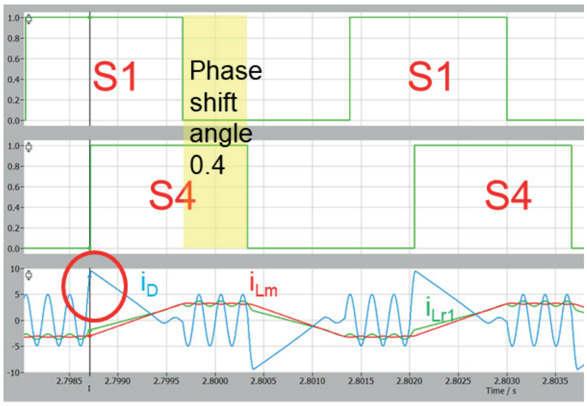

Fig. 16 Simulation waveforms when phase shift angle equals to 0.4

Fig. 17 Simulation waveforms when phase shift angle equals to 0.35

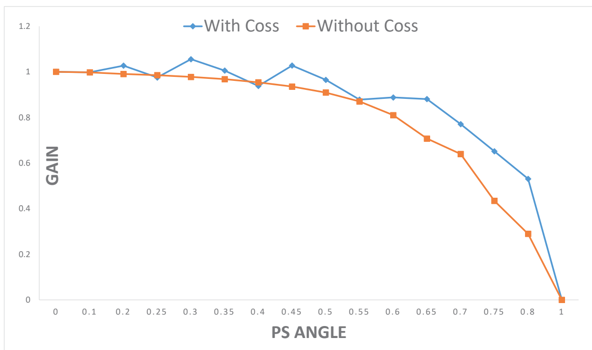

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Fig. 18 Gain curve under Phase Shift Mode with and without C_{OSS}

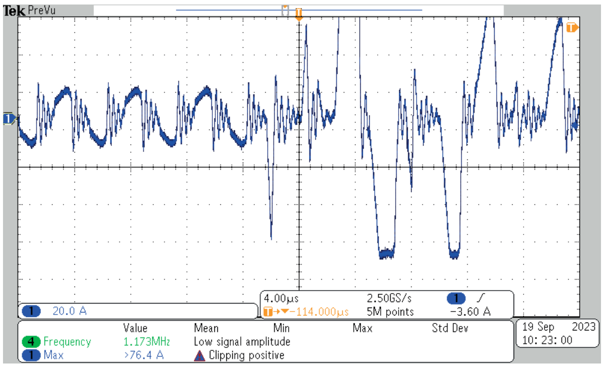

Fig. 19 Current spike under phase shift mode (and closed loop)

3 Solution for gain problems

3.1 SR control scheme

In order to address the current oscillation issue and to ensure a monotonic gain change, a synchronous rectifier (SR) control scheme is shown in Fig. 20. By ensuring either two upper or two lower SR switches to be turned on at the same time during the current oscillation period, the transformer secondary side winding is temporarily shorted and is not able to resonate with SR MOSFET C_{OSS}.

3.2 Test results

After adopting this method, the current waveforms become normal, as shown in Fig. 21. And by doing so, we are able to smooth the input/output voltage gain curve as shown in Fig. 22.

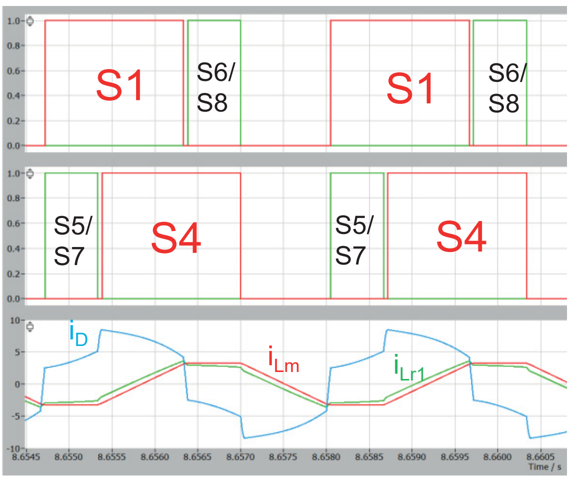

Fig. 20 Waveforms with proposed SR control scheme

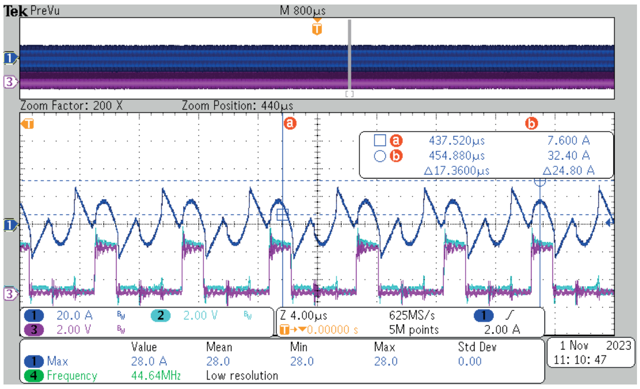

Fig. 21 Experimental waveforms with C_{OSS} under Phase shift mode (and close loop)

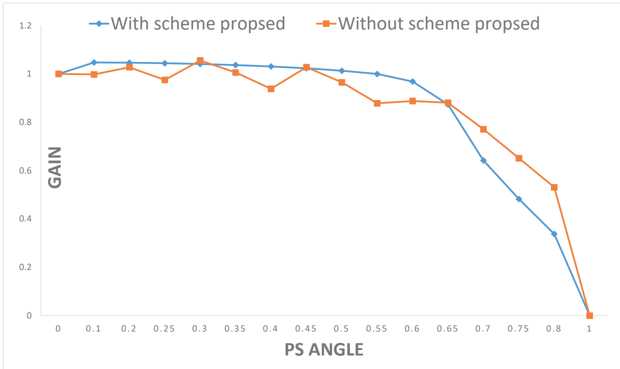

Fig. 22 Gain curve under Phase Shift Mode with and without scheme proposed

4 Summary

CLLLC resonant converter as a popular topology in ESS applications as it can offer soft-switching, high power density, and high efficiency. In order to maintain high converter efficiency and gain regulation ability, we often need to introduce control methods in addition to variable frequency control. A commonly used one is phase-shift control. As depicted in this paper, phase-shift control introduces current oscillation issue which becomes severe in the designs that have large C_{OSS}. A SR control method is proposed in this paper to address the current oscillation issue.

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