

Design Methodology of Bidirectional Resonant CLLC Charger for Wide Voltage Range Based on Parameter Equivalent and Time Domain Model

Lie Zhao^{ID}, Student Member, IEEE, Yunqing Pei^{ID}, Member, IEEE, Laili Wang^D, Senior Member, IEEE, Long Pei^{ID}, Student Member, IEEE, Wei Cao^{ID}, and Yongmei Gan^{ID}, Member, IEEE

Abstract—The bidirectional CLLC resonant converter has distinguished potential in battery chargers and energy storage systems for its advantages in soft switching and bidirectional power flow capability. However, traditional CLLC converters generally adopt symmetrical design to maintain bidirectional symmetrical characteristics, which means the secondary *LC* network is designed to be equal to the primary *LC* network after reflection. The symmetrical design is only suitable for voltage grade matching scenarios where a wide voltage range is not required, such as CLLC-type dc transformers. Whereas in the field of bidirectional chargers, due to the wide voltage range of battery, there are significant differences in the characteristics required between charging and discharging mode, which makes symmetrical design no longer applicable. To cope with this issue, this paper proposes a novel design methodology of CLLC based on parameter equivalent and time domain model. With the parameter equivalent principle, the CLLC resonant tank with arbitrary parameters is investigated to satisfy the requirements of wide voltage range for bidirectional charger application. Compared with the symmetrical design, the proposed method can meet the requirements of bidirectional gain within preset frequency range and guarantee the achievement of zero-voltage switching under required load conditions with the minimum reactive power. In addition, the area product capacity of the magnetic part of the CLLC resonant tank is minimized based on the parameter equivalent principle. Finally, experiments have been performed on a 1 kW prototype to confirm the validity and feasibility of the proposed design methodology.

Index Terms—CLLC resonant converter, parameter equivalent, time domain model, wide voltage range, zero-voltage switching (ZVS).

I. INTRODUCTION

WITH the development of electric vehicles (EV), energy storage systems, and dc microgrid, the demand for

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The authors are with the State Key Laboratory of Electrical Insulation and Power Equipment, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: winter_zl@stu.xjtu.edu.cn; peiyq@mail.xjtu.edu.cn; llwang@mail.xjtu.edu.cn; pl0823@stu.xjtu.edu.cn; caowei@stu.xjtu.edu.cn; ymgan@mail.xjtu.edu.cn).

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bidirectional power flow is becoming increasingly common. The traditional unidirectional battery chargers are gradually becoming obsolete because they cannot address the challenge of feeding energy back to the grid, and the new bidirectional chargers are becoming a research hotspot.

A typical bidirectional EV charger consists of an ac/dc converter for power factor correction and a galvanically isolated bidirectional dc–dc converter for safety in battery applications [1]. Due to the output voltage and current are regulated by dc–dc stage, the characteristic of the bidirectional chargers is mainly dependent on the bidirectional dc–dc converter. Among various bidirectional isolated topologies, CLLC resonant converter is considered to be a promising topology due to its bidirectional energy flow capability, soft switching, and symmetrical structure [2]–[7]. A variable CLLC topology structure is proposed to achieve the asymmetrical power transmission capability for both the charging and discharging modes while the current stress almost doubled [8]. A sensor-less synchronous rectification algorithm combined phase shift modulation for CLLC converter is presented to improve efficiency and expand the voltage regulated range [9]. In order to track the maximum efficiency, the variable dc-link voltage technique is employed to maintain the operating frequency always close to resonant frequency of the CLLC converter [10], [11]. Although the variable dc-link voltage can broaden the output voltage of the converter, the voltage regulation capability of the CLLC converter is still indispensable.

Compared with *LLC*, typical CLLC has an extra *LC* series network on the secondary side to form a five-element resonant tank [12], [13]. In order to maintain symmetrical characteristics during bidirectional operation, the secondary *LC* network is designed to be equal to the primary *LC* network after reflection ($n^2L_s = L_p$, $C_s = n^2C_p$) [13], as shown in Fig. 1. This design implementation is considered as symmetrical CLLC. In fact, since CLLC resonant converters may have arbitrary parameters, depending on whether the primary resonant frequency is the same as the secondary resonant frequency, CLLC can be divided into D-type CLLC ($L_{ap}C_p \neq L_{as}C_s$) with different primary and secondary resonant frequencies and S-type CLLC ($L_pC_p = L_sC_s$) with the same primary and secondary resonant frequencies, as shown in Fig. 2. Obviously, symmetrical CLLC ($n^2L_s = L_p$, $C_s = n^2C_p$) is only a special case of S-type CLLC ($h = 1$ as discussed later).

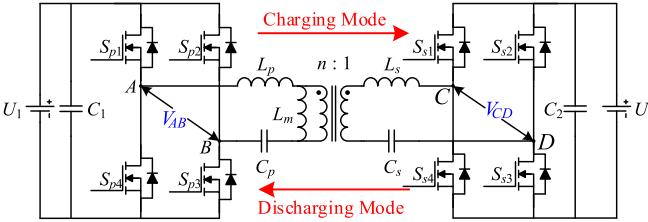


Fig. 1. Topology of CLLC converter.

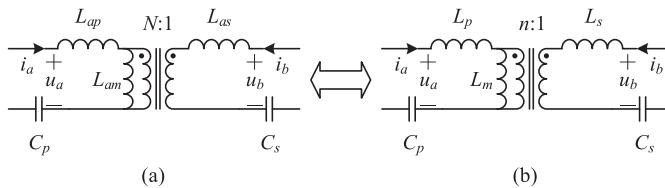


Fig. 2. D-type CLLC and S-type CLLC. (a) D-type CLLC. (b) S-type CLLC.

Recently, the design and optimization of CLLC resonant tanks are attracting more attention. The existing research on the parameter design of CLLC converter can be summarized into first harmonic approximation (FHA) [12], [13], [15]–[23] and time domain model (TDM) [14], [25]–[26]. A common disadvantage of FHA is that its accuracy gets worse as the switching frequency deviates from the resonant frequency for FHA only accounts for the fundamental components of the resonant tank's response while neglecting corresponding high-order components [14]. Many researches adopting FHA focus on symmetrical CLLC for CLLC-type dc transformers application [15]–[20], where narrow voltage regulated range is required. Due to the resonant frequency of the CLLC-type dc transformer is susceptible to parameters variations, a robust design scheme is proposed to handle the parameters deviation issues [15]. Artificial intelligence algorithms can also be adopted to optimize design parameters and system efficiency [16], [17]. Moreover, unlike the dc transformers that only achieve voltage grade matching in [15]–[17], symmetrical CLLC designed for bidirectional chargers in [12], [13], and [21]–[23] are capable of handling the wide-range voltage of battery. Although the proposed design methods achieve bidirectional wide-range voltage gain for battery applications, it cannot guarantee the realization of full-range zero-voltage switching (ZVS) in terms of time-domain accuracy since FHA can only obtain a low-order approximation of the time domain response. In addition, considering that symmetrical CLLC is a special case of the S-type CLLC, together with the more common D-type CLLC, it is unreasonable to focus on only the symmetrical CLLC to handle wide-range voltage gain requirements. The required operating frequency range would be flagrant large if symmetrical CLLC is employed to achieve the bidirectional gain requirements of battery application, which seriously affects the performance of the converter [24]. An asymmetric parameters methodology adopting statistical design of experiments and FHA is proposed for CLLC converters to narrow the switching frequency range for wide-range voltage applications in [24]. However, due to the inaccurate flaw of FHA,

the design methodology still cannot guarantee the achievement of full range ZVS in terms of time domain accuracy.

The largest advantage of TDM over FHA is that precisely time domain response of resonant tank is obtained. Therefore, more accurate voltage gain characteristics is derived and the achievement of full range ZVS in terms of time domain accuracy is guaranteed. The research in [25] proposed a time-domain model of resonant CLLC for fast parameter scanning. However, Sun *et al.* [25] do not presented detailed circuit state expressions and cover the entire circuit operating states. A more detailed analysis adopting time domain solution of operating modes for CLLC is introduced in [26], but it does not provide corresponding parameter optimization design method for wide-range voltage application. In [14], the design criteria are presented through time-domain analysis for symmetrical CLLC under dc transformer application to get an optimized solution. Comprehensive comparison of aforementioned existing research, few literatures based on TDM analyzed CLLC resonant converters with arbitrary parameters (e.g., D-type CLLC and S-type CLLC) for parameters optimization design of wide-range voltage application.

In this article, a novel parameters design methodology for bidirectional CLLC chargers based on parameter equivalent and TDM is presented. Based on proposed parameter equivalent principle, all the design freedom of CLLC resonant tank is utilized to meet the bidirectional gain for on board charger (OBC) applications. Different from conventional design, the proposed method can realize the required bidirectional gain within preset frequency range and guarantee the achievement of ZVS under desired load conditions with the minimum reactive power. Meantime, the AP capacity of the magnetic part of the CLLC resonant tank is minimized based on parameter equivalent principle. The rest of this article is organized as follows. The parameter equivalent principle of CLLC resonant tank is derived in Section II. In Section III, TDM is used to analyze the voltage gain and output characteristics of the CLLC converter with arbitrary parameters in charging and discharging modes under typical OBC applications. And then, a novel design methodology that guarantees the bidirectional voltage gain and ZVS are achieved within preset frequency range under required load conditions is summarized in Section IV. With the parameters equivalent principle, a method that minimizes the AP capacity of the magnetic part of the CLLC resonant tank is introduced in Section V. The design methodology is verified by experiments in Section VI. Finally, Section VII concludes this article.

II. PARAMETER EQUIVALENT

Compared with S-type CLLC, the different primary and secondary resonant frequencies of D-type CLLC brings great inconvenience to subsequent analysis and design. In fact, neither the primary resonance frequency nor the secondary resonance frequency is the genuine resonance frequency of the D-type CLLC resonant tank. By equating D-type CLLC ($L_{ap}C_p \neq L_{as}C_s$) with different primary and secondary resonant frequencies to S-type CLLC ($L_pC_p = L_sC_s$) with the same primary and secondary resonant frequencies, as shown in Fig. 2, the analysis of the D-type CLLC can be simplified to the analysis of

its equivalent S-type *CLLC*. Meantime, the resonant frequency of the equivalent S-type *CLLC* is exactly the genuine resonant frequency of the corresponding D-type *CLLC*.

Equation (1) shows the terminal voltages in term of the loop currents for the magnetic part of the D-type *CLLC* shown in Fig. 2(a). Similarly, the terminal voltages in term of the loop currents for the magnetic part of the equivalent S-type *CLLC* shown in Fig. 2(b) can be derived in (2). To ensure that the equivalent S-type *CLLC* and the given D-type *CLLC* have precisely the same electrical characteristics (e.g., terminal voltages, loop currents, voltage, and current waveforms), (2) should be exactly equal to (1). Due to the reciprocity of passive network, the equivalence of (2) and (1) corresponds to only three equations. Considering that there are four unknowns (L_p , L_s , L_m , n) to be determined in the equivalent S-type *CLLC*, an additional constraint need to be attached. In fact, S-type *CLLC* inherently implies constraint $L_p C_p = L_s C_s$, which is adopted here as $L_s/L_p = C_p/C_s = H_c$ in (3). Where H_c represents the resonant capacitor ratio between primary and secondary sides both for S-type and D-type *CLLC*. N and n are, respectively, the transformer ratio for D-type and S-type *CLLC*

$$\begin{cases} u_a = L_{ap} \frac{di_a}{dt} + L_{am} \frac{d(i_a + \frac{1}{N} i_b)}{dt} = (L_{ap} + L_{am}) \frac{di_a}{dt} \\ \quad + \frac{L_{am}}{N} \frac{di_b}{dt} \\ u_b = \frac{L_{am}}{N} \frac{d(i_a + \frac{1}{N} i_b)}{dt} + L_{as} \frac{di_b}{dt} = \frac{L_{am}}{N} \frac{di_a}{dt} \\ \quad + (L_{as} + \frac{L_{am}}{N^2}) \frac{di_b}{dt} \end{cases} \Rightarrow \begin{bmatrix} u_a \\ u_b \end{bmatrix} = \begin{bmatrix} L_{ap} + L_{am} & \frac{L_{am}}{N} \\ \frac{L_{am}}{N} & L_{as} + \frac{L_{am}}{N^2} \end{bmatrix} \begin{bmatrix} \frac{di_a}{dt} \\ \frac{di_b}{dt} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} u_a \\ u_b \end{bmatrix} = \begin{bmatrix} L_p + L_m & \frac{L_m}{n} \\ \frac{L_m}{n} & L_s + \frac{L_m}{n^2} \end{bmatrix} \begin{bmatrix} \frac{di_a}{dt} \\ \frac{di_b}{dt} \end{bmatrix} \quad (2)$$

$$\begin{cases} L_p + L_m & \frac{L_m}{n} \\ \frac{L_m}{n} & L_s + \frac{L_m}{n^2} \end{cases} = \begin{bmatrix} L_{ap} + L_{am} & \frac{L_{am}}{N} \\ \frac{L_{am}}{N} & L_{as} + \frac{L_{am}}{N^2} \end{bmatrix} \quad (3)$$

$$L_s/L_p = C_p/C_s = H_c.$$

To simplify the subsequent analysis, the relevant normalized parameters of the D-type *CLLC* are introduced in (4), where H_l denotes the resonant inductor ratio between secondary and primary sides for D-type *CLLC*, and K_a indicates the inductor ratio between primary resonant inductor and magnetizing inductor for D-type *CLLC*

$$\begin{cases} H_l = L_{as}/L_{ap} \\ K_a = L_{ap}/L_{am} \end{cases} \quad (4)$$

By solving (3) with $L_s/L_p = C_p/C_s = H_c$, corresponding equivalent S-type *CLLC* parameters are acquired in

$$\begin{cases} L_p = L_{ap} (1 + N^2 (H_c + (H_c + H_l) K_a) - \xi_0) \\ \quad / (2N^2 H_c K_a) \\ L_s = L_{ap} (1 + N^2 (H_c + (H_c + H_l) K_a) - \xi_0) \\ \quad / (2N^2 K_a) \\ L_m = L_{ap} (-1 + N^2 (H_c + (H_c - H_l) K_a) + \xi_0) \\ \quad / (2N^2 H_c K_a) \\ n = (-1 + N^2 (H_c + (H_c - H_l) K_a) + \xi_0) \\ \quad / (2N H_c) \end{cases} \quad (5)$$

where

$$\xi_0 = \sqrt{4N^2 H_c + (1 + N^2 H_l K_a - N^2 H_c (1 + K_a))^2}. \quad (6)$$

Moreover, if C_s tends to infinity in S-type and D-type *CLLC*, which means there is no resonant capacitor on the secondary side. If we solve the constrained (3) again, L_s of equivalent S-type *CLLC* will be 0 as in (7), which means the equivalent S-type *CLLC* is an *LLC* resonant tank now

$$\begin{cases} L_p = L_{ap} + L_{ap} N^2 H_l / (1 + N^2 H_l K_a) \\ L_s = 0 \\ L_m = L_{ap} / (K_a + N^2 H_l K_a^2) \\ n = N / (1 + N^2 H_l K_a). \end{cases} \quad (7)$$

For a S-type *CLLC*, as shown in Fig. 2(b), we have definitions in

$$\begin{cases} k = L_p/L_m \\ h = n^2 L_s/L_p = n^2 C_p/C_s. \end{cases} \quad (8)$$

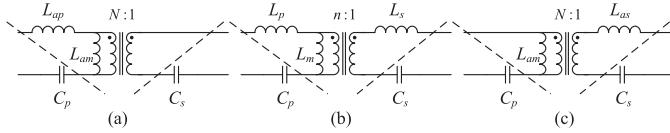
Where k is the inductor ratio between primary resonant inductor and magnetizing inductor, and h is the symmetry coefficient for S-type *CLLC*. For $h = 1$, S-type *CLLC* is exactly the traditional symmetrical *CLLC* resonant tank. If $h = 0$ in (8), then there are no resonant inductor or capacitor on the secondary side. Meantime, the S-type *CLLC* degenerates into an *LLC* resonant tank.

Similarly, for a certain given S-type *CLLC* shown in Fig. 2(b), there are infinite number of D-type *CLLC* shown in Fig. 2(a) with the same electrical characteristics equivalent to it. The corresponding terminal voltages in term of the loop currents for the magnetic part of the equivalent D-type *CLLC* and the given S-type *CLLC* are shown in (1) and (2), respectively. To ensure that the equivalent D-type *CLLC* and the given S-type *CLLC* have precisely the same electrical characteristics (e.g., terminal voltages, loop currents, voltage, and current waveforms), (1) should be exactly equal to (2). Due to the reciprocity of passive network, the equivalence of (1) and (2) corresponds to only three equations. Considering that there are four unknowns (L_{ap} , L_{as} , L_{am} , N) to be determined in the equivalent D-type *CLLC*, an additional constraint need to be attached. By defining the similar symmetry coefficient H for D-type *CLLC* in (9), the given S-type *CLLC* can be equivalent to corresponding D-type *CLLC* with the same electrical characteristic

$$\begin{cases} \left[\begin{array}{cc} L_{ap} + L_{am} & \frac{L_{am}}{N} \\ \frac{L_{am}}{N} & L_{as} + \frac{L_{am}}{N^2} \end{array} \right] = \left[\begin{array}{cc} L_p + L_m & \frac{L_m}{n} \\ \frac{L_m}{n} & L_s + \frac{L_m}{n^2} \end{array} \right] \\ N^2 L_{as}/L_{ap} = H. \end{cases} \quad (9)$$

After solving (9) with $N^2 L_{as}/L_{ap} = H$, corresponding equivalent D-type *CLLC* parameters are acquired in

$$\begin{cases} L_{ap} = L_p (2k(hk + h + 1) + H + 1 - \xi_1) / (2k(hk + 1)) \\ L_{as} = L_p (2hHk^2 + 2(h + 1)Hk + H + 1 - \xi_1) \\ \quad / (2Hk(k + 1)n^2) \\ L_{am} = L_p (\xi_1 - H + 1) / (2k(hk + 1)) \\ N = n(\xi_1 - H + 1) / (2hk + 2) \end{cases} \quad (10)$$

Fig. 3. Three special D-type CLLC. (a) $H = 0$. (b) $H = h$. (c) $H = +\infty$.

where

$$\xi_1 = \sqrt{H(4k(hk + h + 1) + H + 2) + 1} \quad (11)$$

where H can vary from 0~infinity in (10). When $H = 0$, there is no inductor on the secondary side; when $H = h$, the equivalent D-type CLLC returns to the original S-type CLLC; when H approaches infinity, there is no inductor on the primary side, as shown in Fig. 3.

Meantime, when H takes the three special values, (10) can be further simplified to

$$\begin{cases} L_{ap} = L_p(hk + h + 1)/(hk + 1) \\ L_{as} = 0 \\ L_{am} = L_p/(hk + 1) \\ N = n/(hk + 1) \end{cases} \quad \text{with } H = 0 \quad (12)$$

$$\begin{cases} L_{ap} = L_p \\ L_{as} = hL_p/n^2 = L_s \\ L_{am} = L_p/k = L_m \\ N = n \end{cases} \quad \text{with } H = h \quad (13)$$

$$\begin{cases} L_{ap} = 0 \\ L_{as} = L_p(hk + h + 1)/((k + 1)n^2) \\ L_{am} = L_p(1/k + 1) \\ N = (k + 1)n. \end{cases} \quad \text{with } H = +\infty \quad (14)$$

It can be concluded from the parameters equivalent process that the crucial difference between CLLC and LLC is whether there is a resonant capacitor on the secondary side. Both CLLC and LLC can contain resonant inductor on both the primary and secondary sides, or only one side of the primary and secondary sides contain resonant inductor.

III. CHARACTERISTICS OF CLLC CONVERTER

In Section II, the parameter equivalent principle of CLLC resonant tank has been presented. Therefore, we only need to analyze the characteristics of S-type CLLC, which is equivalent to analyzing D-type CLLC with arbitrary parameters.

For typical OBC applications, the input voltage on the primary side of the CLLC converter is generally a fixed value, and the battery voltage on the secondary side fluctuates in a wide range. Therefore, this article mainly analyzes the characteristics of S-type CLLC converter under OBC scenario. Following the definitions in (8), only five parameters (L_p , C_p , k , h , n) are required to describe S-type CLLC completely. The following analysis defines the forward power flow and the reverse power flow as the charging mode and discharging mode, respectively, as shown in Fig. 1.

TABLE I
ABBREVIATIONS AND NORMALIZATIONS

Circuit Variable	Symbol	Normalized Variable
Resonant frequency	$\omega_r = (L_p C_p)^{-1/2} = (L_s C_s)^{-1/2} = 2\pi f_r$	-
Characteristic impedance	$Z_r = (L_p/C_p)^{1/2}$	-
Inductance ratio	$k = L_p/L_m$	-
Symmetry coefficient	$h = n^2 L_s / L_p = n^2 C_p / C_s$	-
Voltage gain	$M = n U_2 / U_1$	-
Time	t	$\theta = \omega_r t$
Secondary resonant frequency	$\omega_1 = ((L_p + L_m) C_p)^{-1/2}$	$\omega_1 = (1+k)^{-1/2} \omega_r$
Switching frequency	$f_s = 1/T_s$	$f_n = f_s/f_r$
Half period	$1/(2f_s)$	$\gamma = \pi/f_n$
Primary resonant capacitor voltage	$u_1(t)$	$u_1(\theta) = u_1(t)/U_1$
Secondary resonant capacitor voltage	$u_2(t)$	$u_2(\theta) = u_2(t)/U_1$
Primary resonant inductor current	$i_1(t)$	$j_1(\theta) = Z_r i_1(t)/U_1$
Secondary resonant inductor current	$i_2(t)$	$j_2(\theta) = Z_r i_2(t)/U_1$
Magnetizing inductor voltage	$u_m(t)$	$m_m(\theta) = u_m(t)/U_1$
Magnetizing inductor current	$i_m(t)$	$j_m(\theta) = Z_r i_m(t)/U_1$
Reflected output voltage	$n U_2$	M

A. Forward Mode

1) *Time Domain Model:* Since switching actions occur on both the primary and secondary sides, the CLLC resonant converter represents a nonlinear time-varying system, which complicates the analysis of its operating principle. The converter may operate in several resonant stages within one switching cycle depending on the specification of the parameters, switching frequency, and load conditions. Considering the CLLC converter adopts variable frequency control to regulate the voltage and the duty cycle is fixed to 50%, the operational states of the resonant tank in both half cycles are symmetrical. The upcoming analysis focuses on the positive half cycle when S_{p1}, S_{p3} turn ON and S_{p2}, S_{p4} turn OFF. During the positive half cycle, according to the conduction states of secondary body diodes, the converter can be simplified into three equivalent circuits as P stage (the body diodes of S_{s1} and S_{s3} turn ON), N stage (the body diodes of S_{s2} and S_{s4} turn ON), and O stage (all body diodes turn OFF). As shown in Fig. 4, where $L_{se} = n^2 L_s$, $C_{se} = C_s/n^2$.

During the P stage, the body diodes of S_{s1} and S_{s3} turn ON, then the output voltage of the resonant tank V_{CD} is clamped to U_2 . According to the circuit in Fig. 4(a), the four-order differential equations are established in

$$\begin{cases} L_m \frac{di_{mP}}{dt} + L_p \frac{di_{1P}}{dt} + u_{1P} = U_1 \\ L_m \frac{di_{mP}}{dt} = L_{se} \frac{di_{2P}}{dt} + u_{2P} + nU_2 \\ i_{1P} = C_p \frac{du_{1P}}{dt}, i_{2P} = C_{se} \frac{du_{2P}}{dt} \\ i_{1P} = i_{2P} + i_{mP}. \end{cases} \quad (15)$$

For the convenience and generality of the analysis, all the following variables are normalized based on the base values in Table I. As can be seen from Table I, there are four main bases for normalization in

$$Z_{\text{base}} = Z_r = \sqrt{L_p/C_p}, U_{\text{base}} = U_1$$

$$I_{\text{base}} = U_{\text{base}}/Z_{\text{base}}, \omega_{\text{base}} = \omega_r = (L_p C_p)^{-1/2} = (L_s C_s)^{-1/2}. \quad (16)$$

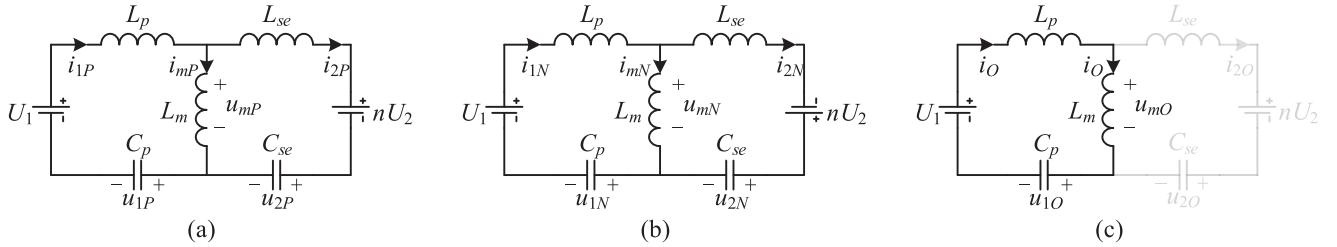


Fig. 4. Equivalent circuit of the CLLC resonant tank in different operating stages. (a) P stage. (b) N stage. (c) O stage.

Through solving (15), the normalized special solution of the P stage is shown in (17).

$$\left\{ \begin{array}{l} m_{1P}(\theta) = \frac{M(\cos(\theta)-\cos(k_1\theta))}{h+1} + 1 \\ \quad + \frac{1}{h+1}((m_{1P0} + m_{2P0} - 1)\cos(\theta) \\ \quad + (j_{1P0} + h j_{2P0})\sin(\theta) + (h m_{1P0} - h - m_{2P0})\cos(k_1\theta) \\ \quad + \frac{h(j_{1P0}-j_{2P0})\sin(k_1\theta)}{k_1}) \\ j_{1P}(\theta) = \frac{M(k_1\sin(k_1\theta)-\sin(\theta))}{h+1} \\ \quad + \frac{1}{h+1}((1 - m_{1P0} - m_{2P0})\sin(\theta) \\ \quad + (j_{1P0} + h j_{2P0})\cos(\theta) + k_1(h + m_{2P0} - h m_{1P0})\sin(k_1\theta) \\ \quad + h(j_{1P0} - j_{2P0})\cos(k_1\theta)) \\ m_{2P}(\theta) = \frac{M(\cos(\theta)h+\cos(k_1\theta))}{h+1} - M \\ \quad + \frac{1}{h+1}(h(m_{1P0} + m_{2P0} - 1)\cos(\theta) \\ \quad + h(j_{1P0} + h j_{2P0})\sin(\theta) + (h + m_{2P0} - h m_{1P0})\cos(k_1\theta) \\ \quad + \frac{h(j_{2P0}-j_{1P0})}{k_1}\sin(k_1\theta)) \\ j_{2P}(\theta) = -\frac{M(h\sin(\theta)+k_1\sin(k_1\theta))}{h(h+1)} \\ \quad + \frac{1}{h+1}((1 - m_{1P0} - m_{2P0})\sin(\theta) \\ \quad + (j_{1P0} + h j_{2P0})\cos(\theta) + \frac{k_1(h m_{1P0} - h - m_{2P0})}{h}\sin(k_1\theta) \\ \quad + (j_{2P0} - j_{1P0})\cos(k_1\theta)) \end{array} \right. \quad (17)$$

Where $k_1 = (hk/(hk + h + 1))^{1/2}$, m_{1P0} , m_{2P0} , j_{1P0} , and j_{2P0} are the normalized initial value of primary resonant capacitor voltage, secondary resonant capacitor voltage, primary resonant inductor current, and secondary resonant inductor current, respectively. $m_{1P}(\theta)$, $m_{2P}(\theta)$, $j_{1P}(\theta)$, and $j_{2P}(\theta)$ are the normalized value of u_{1P} , u_{2P} , i_{1P} , and i_{2P} during P stage, respectively. Moreover, (17) is a precise time domain description of the resonant tank's responses during P stage, and it is not hard to notice that the current or voltage responses contain not only the resonant frequency part (ω_r) but also the other harmonics part ($k_1\omega_r$). Hence, compared with the conventional FHA model, the exact operating behaviors can be obtained based on TDM, which includes not only the fundamental harmonic component (f_s) but also all other higher harmonic components (Kf_s , $K = 2\sim+\infty$). Similar to the P stage, the normalized special solution of the N stage can be derived in (18).

Accordingly, m_{1N0} , m_{2N0} , j_{1N0} , and j_{2N0} are the normalized initial value of primary resonant capacitor voltage, secondary

resonant capacitor voltage, primary resonant inductor current, and secondary resonant inductor current. $m_{1N}(\theta)$, $m_{2N}(\theta)$, $j_{1N}(\theta)$, and $j_{2N}(\theta)$ are, respectively, the normalized value of u_{1N} , u_{2N} , i_{1N} , and i_{2N} during N stage

$$\left\{ \begin{array}{l} m_{1N}(\theta) = \frac{-M(\cos(\theta)-\cos(k_1\theta))}{h+1} + 1 \\ \quad + \frac{1}{h+1}((m_{1N0} + m_{2N0} - 1)\cos(\theta) \\ \quad + (j_{1N0} + h j_{2N0})\sin(\theta) + (h m_{1N0} - h - m_{2N0}) \\ \quad \cos(k_1\theta) + \frac{h(j_{1N0}-j_{2N0})\sin(k_1\theta)}{k_1}) \\ j_{1N}(\theta) = \frac{-M(k_1\sin(k_1\theta)-\sin(\theta))}{h+1} \\ \quad + \frac{1}{h+1}((1 - m_{1N0} - m_{2N0})\sin(\theta) \\ \quad + (j_{1N0} + h j_{2N0})\cos(\theta) + k_1(h + m_{2N0} - h m_{1N0}) \\ \quad \sin(k_1\theta) + h(j_{1N0} - j_{2N0})\cos(k_1\theta)) \\ m_{2N}(\theta) = \frac{-M(\cos(\theta)h+\cos(k_1\theta))}{h+1} + M \\ \quad + \frac{1}{h+1}(h(m_{1N0} + m_{2N0} - 1)\cos(\theta) \\ \quad + h(j_{1N0} + h j_{2N0})\sin(\theta) + (h + m_{2N0} - h m_{1N0}) \\ \quad \cos(k_1\theta) + \frac{h(j_{2N0}-j_{1N0})}{k_1}\sin(k_1\theta)) \\ j_{2N}(\theta) = \frac{M(h\sin(\theta)+k_1\sin(k_1\theta))}{h(h+1)} \\ \quad + \frac{1}{h+1}((1 - m_{1N0} - m_{2N0})\sin(\theta) \\ \quad + (j_{1N0} + h j_{2N0})\cos(\theta) + \frac{k_1(h m_{1N0} - h - m_{2N0})}{h}\sin(k_1\theta) \\ \quad + (j_{2N0} - j_{1N0})\cos(k_1\theta)). \end{array} \right. \quad (18)$$

Different from P or N stage, the resonant tank in O stage degenerates into a typical LC series resonance network, as shown in Fig. 4(c), and the magnetizing current is equal to the resonant current in O stage. Utilizing the same derivation, the normalized special solution of O stage is derived in

$$\left\{ \begin{array}{l} m_{1O}(\theta) = j_{1O0}\sin(k_2\theta)/k_2 \\ \quad + (m_{1O0} - 1)\cos(k_2\theta) + 1 \\ j_{1O}(\theta) = j_{1O0}\cos(k_2\theta) - k_2(m_{1O0} - 1)\sin(k_2\theta) \\ m_{2O}(\theta) = m_{2O0} \\ j_{2O}(\theta) = 0 \end{array} \right. \quad (19)$$

where $k_2 = (k/(k + 1))^{1/2}$, m_{1O0} , m_{2O0} , and j_{1O0} are the normalized initial value of primary resonant capacitor voltage, secondary resonant capacitor voltage, and primary resonant inductor current, respectively. $m_{1O}(\theta)$, $m_{2O}(\theta)$, $j_{1O}(\theta)$, and $j_{2O}(\theta)$ are the normalized value of u_{1O} , u_{2O} , i_O , and i_{2O} during O stage, respectively.

TABLE II
OPERATION CHARACTERISTICS OF CLLC RESONANT CONVERTER

	$k_2 < f_n < 1$						$f_n = 1$			$f_n > 1$				
Mode	PN	PONO	PON	PO	OPO	O	P	OPO	O	NP	NOP	OP	OPO	O
Inverting switches	ZVS/ ZCS	ZVS/ ZCS	ZVS/ ZCS	ZVS/ ZCS	ZVS	ZVS	ZVS	ZVS	ZVS	ZVS	ZVS	ZVS	ZVS	ZVS
Rectifying switches	Hard switching	ZCS	ZCS	ZCS	ZCS	OFF	ZCS	ZCS	OFF	Hard switching	ZCS	ZCS	ZCS	OFF
Voltage gain	$M > 1/M < 1$		$M > 1$		$M = 1$		$M > 1$		$M < 1$		$M > 1/M < 1$		$M > 1/M < 1$	
Output current	Large \rightarrow small						Large \rightarrow small			Large \rightarrow small				

Zero-voltage switching (ZVS), zero-current switching (ZCS).

Note that k_2 is the normalized serial resonant frequency of L_m , L_p , and C_p . In practice, the operation region of CLLC converter is set in the ZVS region and the normalized frequency range is always higher than k_2 .

2) *Analysis of Operation Modes:* According to the analysis and simulation verification, for different parameters specification, switching frequency, and load conditions, ten valuable operation modes are recognized, which are named after the sequence of different stages: PO, PON, PN, PONO, NP, NOP, OP, OPO, P, and O modes. Among them, PO, PON, PN, and PONO can be observed in the below-resonance region ($f_n < 1$) (BRR), NP, NOP, and OP exist in the above-resonance region ($f_n > 1$) (ARR). Besides, P mode only appears at the resonant point ($f_n = 1$), and O mode is the cut-off mode as no power is transferred to the rectifying side. Especially, OPO mode can operate in all three regions abovementioned. All valuable modes and corresponding characteristics are summarized in Table II.

Each operation mode is restricted with several constraints. First, at the joints of adjacent stages, the capacitor voltage and the inductor current should be continuous. Second, by symmetry, once the resonant tank reaches a steady state, the final values of the capacitor voltage, and inductor current should be opposite to their initial values. Third, the resonant current of rectifying side equals 0 at the boundary of every two adjacent stages. Fourth, due to the disconnection between the inverting side and rectifying side in O stage, the energy is transferred to load only in P and N stage, and the secondary resonant current is rectified by a full-bridge, then the normalized output current I_{out_n} can be derived in (20). Where θ_{P0} and θ_P represent the start and end moment of stage P, θ_{N0} , and θ_N represent the start and end moment of stage N

$$\begin{aligned} I_{out_n} &= f_n \int_0^{\pi/f_n} |j_2(\theta)| d\theta / \pi \\ &= f_n \left(\int_{\theta_{P0}}^{\theta_P} j_{2P}(\theta) d\theta - \int_{\theta_{N0}}^{\theta_N} j_{2N}(\theta) d\theta \right) / \pi \\ &= f_n (m_{2P}(\theta_P) - m_{2P}(\theta_{P0}) + m_{2N}(\theta_{N0}) \\ &\quad - m_{2N}(\theta_N)) / (\pi h). \end{aligned} \quad (20)$$

Meantime, it is not hard to derive the normalized output power P_{out_n} in (21). Moreover, there is still an additional constraint for several special operating modes. That is, during a half switching cycle, the voltage of the transformer is continuous when the circuit operates from O stage to P or N stage. To put it in

another way, the absolute value of V_{CD} reaches U_2 precisely when the circuit is commuting from O stage to P or N stage. This additional constraint just applies to PONO, PON, OPO, NOP, and OP modes. PO mode is taken as an example to demonstrate the mode equation set in (22) as follows:

$$\begin{aligned} P_{out_n} &= MI_{out_n} \\ &= Mf_n (m_{2P}(\theta_P) - m_{2P}(\theta_{P0}) + m_{2N}(\theta_{N0}) \\ &\quad - m_{2N}(\theta_N)) / (\pi h) \\ &= 1f_n \int_0^{\pi/f_n} j_1(\theta) d\theta / \pi \\ &= f_n (m_1(\pi/f_n) - m_1(0)) / \pi \\ &= -2f_n m_1(0) / \pi \end{aligned} \quad (21)$$

$$\left\{ \begin{array}{l} j_{1P}(\theta_P) = j_{1O}(\theta_{O0}), j_{2P}(\theta_P) = 0 \\ m_{1P}(\theta_P) = m_{1O}(\theta_{O0}), m_{2P}(\theta_P) = m_{2O}(\theta_{O0}) \\ j_{1P}(\theta_{P0}) + j_{1O}(\theta_O) = 0, j_{2P}(\theta_{P0}) = 0 \\ m_{1P}(\theta_{P0}) + m_{1O}(\theta_O) = 0, m_{2P}(\theta_{P0}) + m_{2O}(\theta_O) = 0 \\ \theta_{P0} = 0, \theta_{O0} = \theta_P, \theta_O = \pi/f_n \\ \int_{\theta_{P0}}^{\theta_P} |j_{2P}(\theta)| d\theta = (m_{2P}(\theta_P) - m_{2P}(\theta_{P0}))/h \\ = \pi I_{out_n}/f_n \end{array} \right. \quad (22)$$

where θ_P or θ_{O0} represents the moment when the circuit is commuting from P stage to O stage, θ_{P0} denotes the start moment of PO mode as 0, and θ_O indicates the end moment of PO mode as π/f_n . I_{out_n} denotes the normalized output current of current PO mode. During a half switching cycle of PO mode, start by P stage maintains for $[0, \theta_P]$, followed by O stage operating for the rest of the half-cycle $[\theta_{O0}, \pi/f_n]$. Similarly, other modes can also list the nonlinear transcendental equations like (22). However, the analytical solutions can only be acquired under P mode and for other modes, only numerical solutions can be obtained with advanced numerical calculation tools like Mathematica/MATLAB. By solving mode equation set like (22), the numerical solutions of voltage and current responses of CLLC resonant tank in each mode are precisely derived. As an illustration, the precise operation waveform of PO mode is shown in Fig. 5.

As for P mode, it is no hard to derive its analytical solutions in (23) and (24). In the positive half cycle of P mode, $j_{2P}(\theta)$ should be nonnegative, combined with the analytical solution of $j_{2P}(\theta)$, the normalized output current I_{out_n} of P mode should

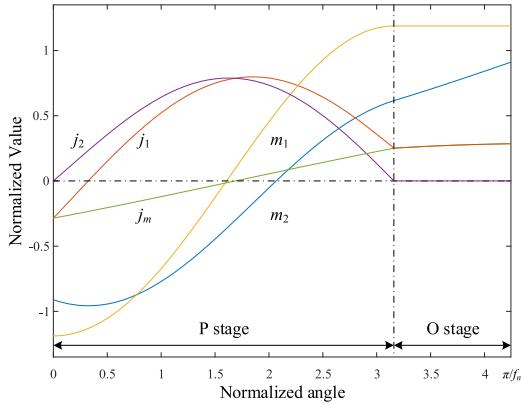


Fig. 5. Operation waveform of PO mode.

be no less than a certain critical value, otherwise, the converter will enter OPO mode. The corresponding critical value I_{b1_n} is derived in (25) as follows:

$$\begin{cases} m_{1P0} = -\pi I_{out_n}/2 \\ m_{2P0} = -\pi I_{out_n}h/2 \\ j_{1P0} = -k_1(h+1)\tan(k_1\pi/2)/h \\ j_{2P0} = 0 \\ M = 1 \end{cases} \quad (23)$$

$$\begin{cases} m_{1P}(\theta) = 1 - \pi I_{out_n} \cos(\theta)/2 - \cos(k_1\theta) \\ \quad - k_1 \sin(\theta) \tan(k_1\pi/2)/h - \tan(k_1\pi/2) \sin(k_1\theta) \\ j_{1P}(\theta) = k_1(h \sin(k_1\theta) - \tan(k_1\pi/2)(h \cos(k_1\theta) \\ \quad + \cos(\theta))/h + \pi I_{out_n} \sin(\theta)/2) \\ m_{2P}(\theta) = -1 - \pi I_{out_n}h \cos(\theta)/2 + \cos(k_1\theta) \\ \quad - k_1 \sin(\theta) \tan(k_1\pi/2) + \tan(k_1\pi/2) \sin(k_1\theta) \\ j_{2P}(\theta) = -k_1(\sin(k_1\theta) + \tan(k_1\pi/2)(\cos(\theta) \\ \quad - \cos(k_1\theta))/h + \pi I_{out_n} \sin(\theta)/2) \end{cases} \quad (24)$$

$$I_{b1_n} = \frac{2k}{(hk+h+1)\pi}. \quad (25)$$

3) *Mode Boundaries and Distribution:* In fact, besides the ten modes mentioned previously, there are still several useless modes exist in the region where f_n is higher than k_2 . Such as PNO, PNPO, PNP, and NPNP modes. Different operations modes of CLLC converter require different load conditions, voltage gain, and frequency range. Therefore, to avoid the complexity of solving all the voltage gain curves, it is crucial to derive the boundaries and distribution of modes. The modes boundary can be seen as a special case of the operation modes. For example, the mode boundary between PO and PON is that V_{CD} reached $-U_2$ exactly at the end of O stage for PO mode. Therefore, the mode boundary can be obtained by solving the PO mode equation set attached with this extra constraint. And it should be noticed that mode boundary only depends on the parameters of the resonant tank, since then, the mode boundary can be solved without load conditions. In addition to normal modes, there are two boundary modes, which are OP mode at the boundary between NOP and OPO modes, and O mode under zero-load condition, all the mode boundary constraints have

TABLE III
BOUNDARY CONSTRAINTS OF OPERATION MODES

Mode boundaries	Solving mode	Constraint
OPO/PO	PO	$m_{mP}(\theta_{P0}) - m_{2P}(\theta_{P0}) = M$
PO/PON	PO	$m_{mO}(\pi/f_n) - m_{2O}(\pi/f_n) = -M$
PON/PN	PN	$m_{mP}(\theta_{N0}) - m_{2P}(\theta_{N0}) = -M$
PON/PONO	PON	$j_{2P}(0) = 0$
PN/others	PN	$j_{2P}(0) = 0$
PONO/others	PNO	$m_{mP}(\theta_{N0}) - m_{2P}(\theta_{N0}) = -M$
NP/NOP	NP	$m_{mN}(\theta_{P0}) - m_{2N}(\theta_{P0}) = M$
NOP/OPO	OP	$m_{mO}(\theta_{P0}) - m_{2O}(\theta_{P0}) = M$

Others: PNO, PNPO, PNP, and NPNP modes.

been listed in Table III. Where θ_{P0} represents the start moment of stage P, θ_{N0} indicates the start moment of stage N. $m_{mP}(\theta)$, $m_{2P}(\theta)$, and $j_{2P}(\theta)$ are the normalized value of u_{mP} , u_{2P} , and i_{2P} during P stage, respectively. $m_{mO}(\theta)$ and $m_{2O}(\theta)$ are the normalized value of u_{mO} and u_{2O} during O stage. $m_{mN}(\theta)$ and $m_{2N}(\theta)$ are the normalized value of u_{mN} and u_{2N} during N stage.

As for O mode under zero-load condition. For this boundary, no power transfers to the rectifying side, and all energy is circulating in the inverting side resonant tank. Output capacitor is cut off from the resonant tank during the whole cycle of O mode. It is no hard to derive the analytical solution of O mode under zero load in (26) and (27). Where $m_{1O}(\theta)$, $m_{mO}(\theta)$, and $j_{1O}(\theta)$ are, respectively, the normalized value of u_{1O} , u_{mO} , and i_O

$$\begin{cases} m_{1O0} = 0 \\ j_{1O0} = -k_2 \tan(k_2\pi/(2f_n)) \end{cases} \quad (26)$$

$$\begin{cases} m_{1O}(\theta) = 1 - \cos(k_2(\pi - 2f_n\theta)/(2f_n)) \sec(k_2\pi/(2f_n)) \\ j_{1O}(\theta) = -k_2 \sec(k_2\pi/(2f_n)) \sin(k_2(\pi - 2f_n\theta)/(2f_n)) \\ m_{mO}(\theta) = \cos(k_2(\pi - 2f_n\theta)/(2f_n)) \sec(k_2\pi/(2f_n))/(1+k). \end{cases} \quad (27)$$

Due to the output capacitor is cut off from the resonant tank during the whole cycle of O mode. The absolute value voltage across magnetizing inductor should no bigger than voltage gain M , as shown in

$$\begin{aligned} M &\geq |m_{mO}(\theta)|_{\max} = |m_{mO}(\pi/(2f_n))| \\ &= \sec(k_2\pi/(2f_n))/(k+1). \end{aligned} \quad (28)$$

Especially, there are three special voltage gain M in (29). Where M_1 denotes the minimum voltage gain that O mode can achieve at $f_n = 1$ when inductor ratio k tends to 0, M_2 represents the maximum voltage gain that OPO mode can achieve at $f_n = 1$ when inductor ratio k close to infinity, and M_3 indicates the minimum voltage gain that O mode can achieve when f_n approaches infinity

$$\begin{cases} M_1 = \lim_{k \rightarrow 0} \sec(k_2\pi/(2f_n))/(k+1) \Big|_{f_n=1} = 1 \\ M_2 = \lim_{k \rightarrow \infty} \sec(k_2\pi/(2f_n))/(k+1) \Big|_{f_n=1} = 4/\pi \\ M_3 = \lim_{f_n \rightarrow \infty} \sec(k_2\pi/(2f_n))/(k+1) = 1/(1+k). \end{cases} \quad (29)$$

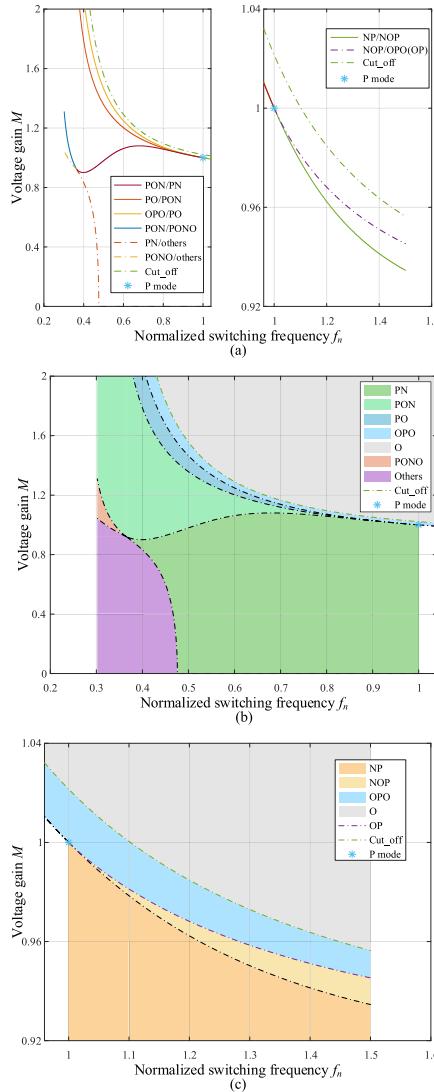


Fig. 6. Typical mode boundaries and distribution of CLLC on f_n - M plane. (a) Mode boundaries. (b) Mode distribution in BRR. (c) Mode distribution in ARR.

Typical mode boundaries and distribution of CLLC on f_n - M plane are determined by parameter k and h , as shown in Fig. 6. After solving all those boundaries equation sets, the characteristics of the CLLC resonant tank can be precisely obtained by solving different mode equations. Different from LLC converter, with different values of h , there are three possibilities for soft switching ON the inverting side. The CLLC resonant converter always has two resistive boundaries in BRR ($k_2 < f_n < 1$). If $0 < h < 1$, these two resistive boundaries divide BRR into two ZVS areas and one zero-current switching (ZCS) area; if $h = 1$, these two resistive boundaries divide BRR into two ZVS areas and two ZCS areas; if $h > 1$, these two resistive boundaries divide BRR into one ZVS area and two ZCS areas, as shown in Fig. 7.

4) Output Characteristics Analysis: In addition to the various situations analyzed previously, there is also a special case of a short circuit on the output side, which means $M = 0$. Under this circumstance, no energy is flowing to the output, and all energy

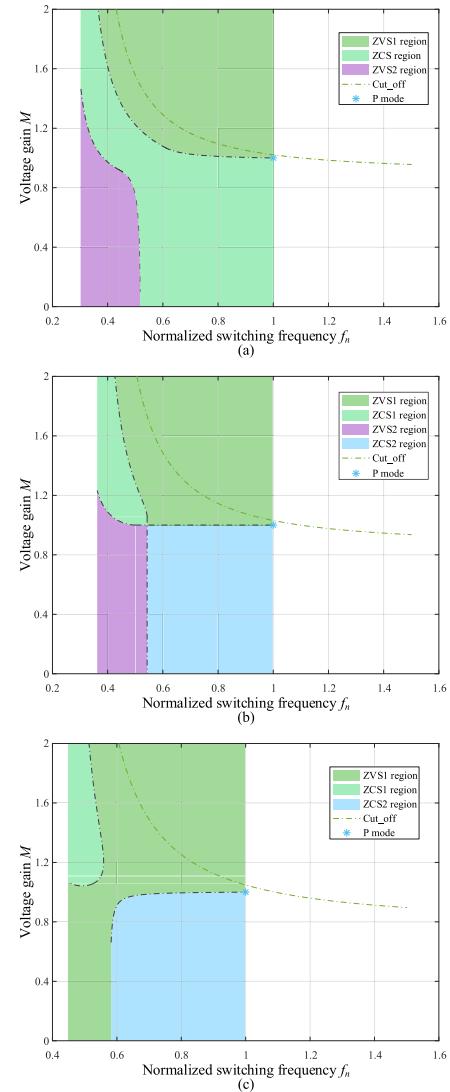


Fig. 7. Three typical resistive boundary of CLLC converter. (a) $0 < h < 1$. (b) $h = 1$. (c) $h > 1$.

is circulating in the resonant tank. Different from O mode, the resonant tank is P or N stages during the whole half cycle. With $M = 0$, the analytical solution of the output short circuit is derived in (30) shown at the bottom of this page.

Due to the CLLC converter with a short circuit on the output side resonates at several frequencies, therefore, these special frequencies in (31) should be excluded

$$f_n \neq \begin{cases} 1/(2q-1) \\ k_1/(2q-1) \end{cases} q = 1, 2, 3, \dots \quad (31)$$

The output current under this circumstance can be derived by combining (20) and (30) as in

$$\begin{aligned} I_{\text{out_n}} = & \frac{f_n}{(h+1)\pi} \int_0^{\pi/f_n} |k_1 \tan(k_1 \pi/(2f_n)) \cos(k_1 \theta) \\ & - \tan(\pi/(2f_n)) \cos(\theta) - k_1 \sin(k_1 \theta) + \sin(\theta)| d\theta. \quad (32) \end{aligned}$$

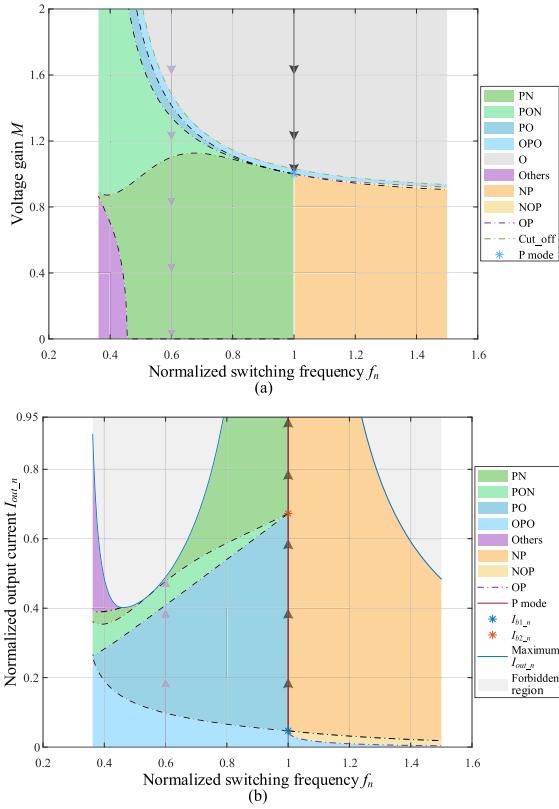


Fig. 8. Modes distribution of CLLC in f_n - M plane and f_n - $I_{out,n}$ plane. (a) f_n - M plane. (b) f_n - $I_{out,n}$ plane.

If CLLC resonant tank operates in PN or NP mode under short circuit circumstance, (32) can be further simplified to

$$I_{out,n} = \begin{cases} \frac{2f_n(\sec(k_1\pi/(2f_n)) - \sec(\pi/(2f_n)))}{\pi(h+1)}, & \text{PN mode} \\ \frac{2f_n(\sec(\pi/(2f_n)) - \sec(k_1\pi/(2f_n)))}{\pi(h+1)}, & \text{NP mode.} \end{cases} \quad (33)$$

As shown in Fig. 8, for a CLLC converter operating at a certain frequency, if the voltage gain M gradually decreases from a large value to 0, the operating mode of the resonant tank starts from O mode, goes through several modes in turn, and finally reaches the state of a short circuit on the output side. During the decreasing process of M , the output current increases monotonically, until the output current reaches the maximum value under the state of short circuit on the output side, which is the output current corresponding to (32). However, for CLLC converter operating at the resonance point $f_n = 1$, when M gradually reduces from a large value to 1, the operating mode of the resonant tank sequentially undergoes O mode, OPO mode, and finally enters P mode. Similarly, the output current increases

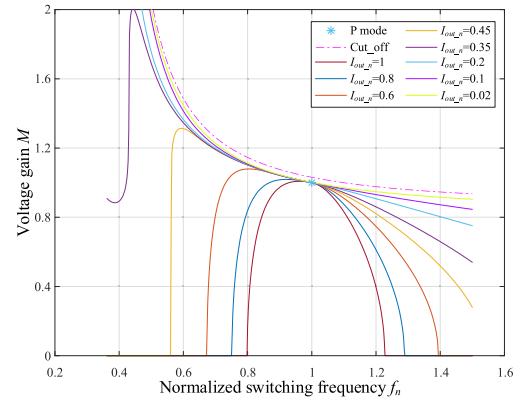


Fig. 9. Gain curves under different output current.

TABLE IV
CONSTRAINTS FOR BOUNDARIES INTERSECTIONS

Intersection	Solving mode	Constraint
OPO/PO, NOP/OPO, NOP/NP	P	$m_{mP}(\theta_{P0}) - m_{2P}(\theta_{P0}) = M = 1$
PO/PON, PON/PN	P	$m_{mP}(\theta_{N0}) - m_{2P}(\theta_{N0}) = -M = -1$

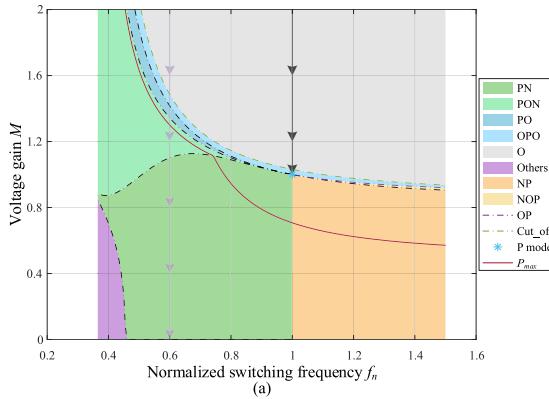
monotonically as M decreases. As analyzed for P mode in (25), as long as $I_{out,n} \geq I_{b1-n}$, the CLLC converter operating at $f_n = 1$ will enter the P mode. In other words, the CLLC resonant converter operating in P mode can output infinite current. When M continues to decrease from 1 of the CLLC converter operating at $f_n = 1$, the response of the resonant tank will oscillate and diverge, which should be avoided in practical applications.

By solving the mode equations, the gain curves of the resonant tank under different $I_{out,n}$ conditions can be accurately obtained, as shown in Fig. 9.

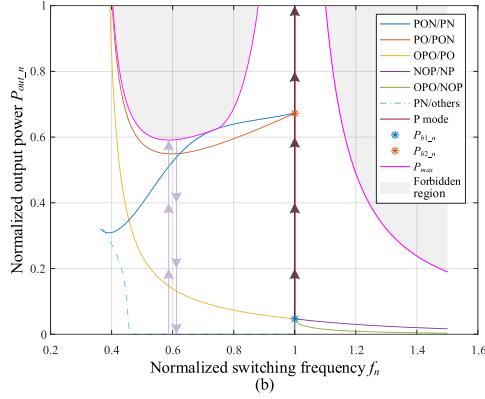
By observing Fig. 8, it is not difficult to notice that the mode boundaries OPO/PO, NOP/OPO, NOP/NP, PO/PON, and PON/PN intersect at the point $(1, 1)$ on f_n - M plane. Similarly, the mode boundaries OPO/PO, NOP/OPO, and NOP/NP intersect at a certain point at $f_n = 1$ on f_n - $I_{out,n}$ plane, and the mode boundaries PO/PON and PON/PN intersect at a certain point at $f_n = 1$ on f_n - $I_{out,n}$ plane, which means that the corresponding operating conditions is a special P mode when the mode boundaries intersect at $f_n = 1$. In other words, the corresponding special P mode can be solved by attaching the relevant mode boundary constraints to P mode. And the mode boundary constraints for intersections are listed in Table IV. Where θ_{P0} represents the start moment of stage P, θ_{N0} indicates the start moment of stage N.

For OPO/PO, NOP/OPO, and NOP/NP boundaries intersection of P mode, it is no hard to obtain the corresponding $I_{out,n}$

$$\begin{cases} m_1(\theta) = 1 - \frac{h \sec(k_1\pi/(2f_n)) \cos(k_1(\pi - 2f_n\theta)/(2f_n)) + \tan(\pi/(2f_n)) \sin(\theta) + \cos(\theta)}{h+1} \\ j_1(\theta) = \frac{-hk_1 \sec(k_1\pi/(2f_n)) \sin(k_1(\pi - 2f_n\theta)/(2f_n)) - \tan(\pi/(2f_n)) \cos(\theta) + \sin(\theta)}{h+1} \\ m_2(\theta) = \frac{h(\tan(k_1\pi/(2f_n)) \sin(k_1\theta) - \tan(\pi/(2f_n)) \sin(\theta) + \cos(k_1\theta) - \cos(\theta))}{h+1} \\ j_2(\theta) = \frac{k_1 \tan(k_1\pi/(2f_n)) \cos(k_1\theta) - \tan(\pi/(2f_n)) \cos(\theta) - k_1 \sin(k_1\theta) + \sin(\theta)}{h+1}. \end{cases} \quad (30)$$



(a)



(b)

Fig. 10. Modes distribution and the maximum output power P_{\max} at certain frequency of CLLC in f_n - M plane and f_n - P_{out_n} plane. (a) f_n - M plane. (b) f_n - P_{out_n} plane.

in (34), which is exactly the output current of the critical P mode in

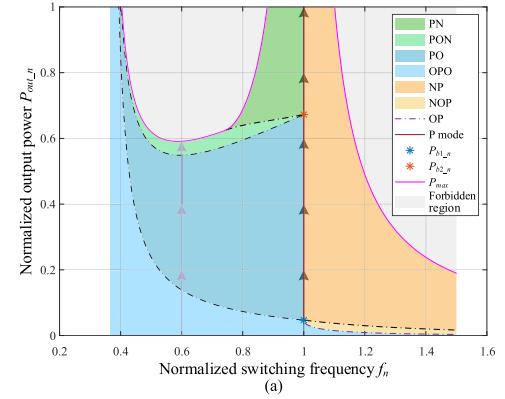
$$I_{\text{out}_n} = \frac{2k}{(hk + h + 1)\pi} = I_{b1_n}. \quad (34)$$

Similarly, it is not hard to derive the normalized output current of PO/PON and PON/PN boundaries intersection in

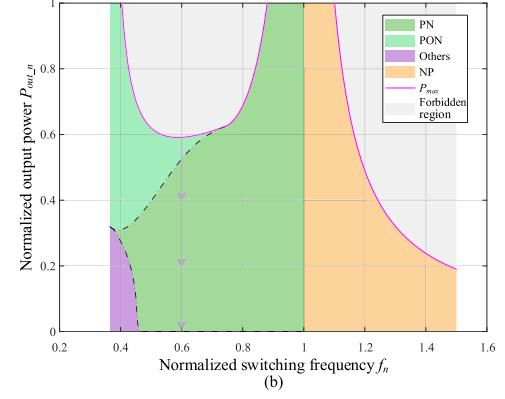
$$I_{b2_n} = \frac{2(k+2)}{(hk + h + 1)\pi} \quad (35)$$

$$P_{\text{out}_n} = MI_{\text{out}_n}. \quad (36)$$

The normalized output power of (21) is redrawn in (36). Similarly, as shown in Fig. 10 and Fig. 11, where P_{b1_n} and P_{b2_n} are the normalized output power of certain P modes corresponding to I_{b1_n} and I_{b2_n} . For a CLLC converter operating at a specific frequency, as voltage gain M gradually decreases from a large value to zero, the normalized output current monotonically increases to the maximum value. The operating mode of the circuit starts in O mode, then passes through several modes, and finally reaches the state of short circuit on the output side. During this process, the normalized output power is zero in the O mode and the output side short-circuit state, which means that the normalized output power first increases from 0 to a certain maximum value P_{\max} and then decreases to 0. However, for the CLLC converter operating at the resonance point $f_n = 1$, when M gradually reduces from a large value to 1, the operating



(a)



(b)

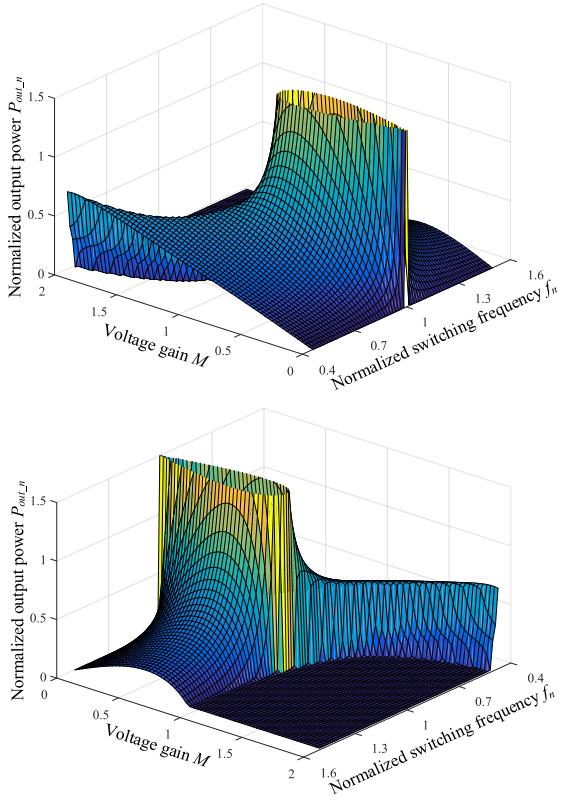
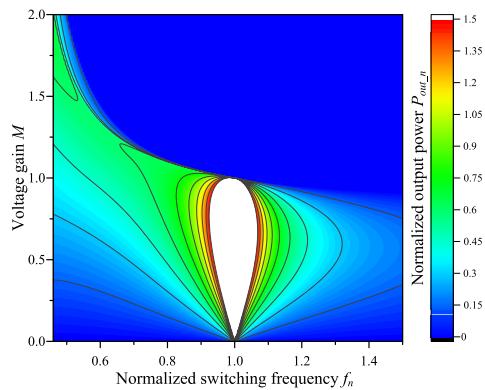
Fig. 11. Variation of P_{out_n} with M decreases at certain frequency. (a) Where P_{out_n} increases monotonically with M decreases. (b) Where P_{out_n} decreases monotonically with M decreases.

mode of the resonant tank sequentially undergoes O mode, OPO mode, and finally enters P mode. As analyzed before, the CLLC resonant converter operating in P mode can output infinite current, which means there is no maximum output power during the process, the output power increases monotonically during this process. In other words, the CLLC resonant converter operating in P mode can output infinite power. Through numerical calculation, it is easy to obtain the normalized output power of operating point for the entire f_n - M plane in Fig. 12, and the maximum output power P_{\max} at certain frequency, as shown in Figs. 10 and 11. Moreover, the projection of constant P_{out_n} gain curves on f_n - M plane is also obtained in Fig. 13.

For OBC applications, the battery is usually charged in a constant P_{out_n} mode. By analyzing Figs. 10–13, it is not difficult to conclude that if a CLLC converter that operates in constant P_{out_n} mode and the voltage gain increases monotonically with the decreasing f_n , then the maximum P_{out_n} should no bigger than the minimum value of the maximum output power P_{\max} at certain frequency in BRR of the CLLC converter, otherwise, the gain curves under constant P_{out_n} mode will be nonmonotonic in BRR.

For CLLC converter operates in forward mode, the constraint for inverting side to achieve ZVS can be described in

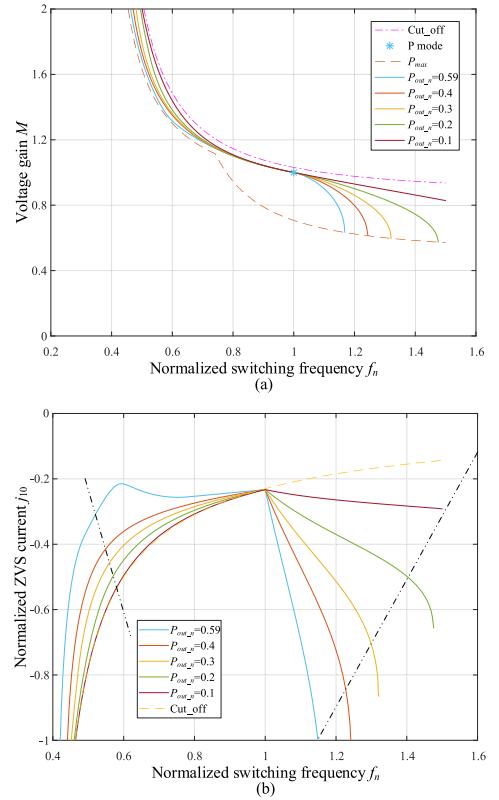
$$\begin{aligned} |j_{10}| I_{\text{base}} t_{\text{dead}} &\geq 2C_{\text{oss}} U_1 \\ |j_{10}| t_{\text{dead}} &\geq 2C_{\text{oss}} Z_r \end{aligned} \quad (37)$$

Fig. 12. Variation of P_{out_n} with M and f_n from different perspectives.Fig. 13. Projection of constant P_{out_n} gain curves on f_n - M plane.

where j_{10} is the normalized value of i_1 at the start moment of the positive half cycle in forward mode, C_{oss} is the output capacitor of corresponding MOSFETs, and t_{dead} is the dead time.

Through numerical calculation, it is easy to obtain the gain curves and the ZVS current j_{10} of the corresponding operating point when *CLLC* converter is operating under constant P_{out_n} mode, as shown in Fig. 14.

It is not difficult to find that ZVS is most likely to be lost when the P_{out_n} reaches the maximum in BRR or the minimum (even O mode) in ARR for *CLLC* converters operating in constant P_{out_n} mode.

Fig. 14. Gain curves under different P_{out_n} (a) and corresponding ZVS current j_{10} (b).

For typical resonant converter analysis, both equivalent output resistance R_{eq} and quality factor Q are, respectively, defined in

$$R_{eq} = \frac{nU_2}{I_{out_n} I_{base}} \quad (38)$$

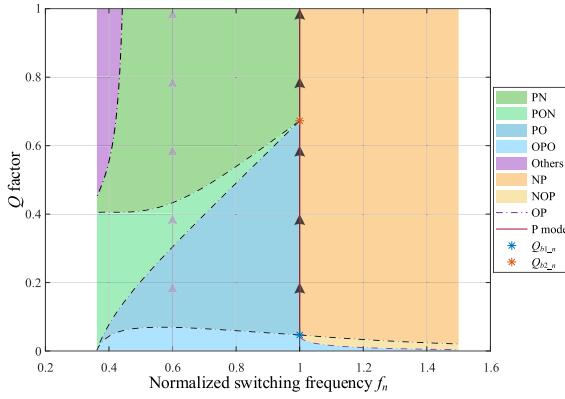
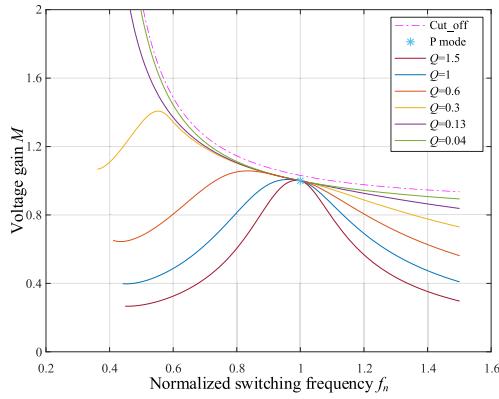
$$Q = \frac{\sqrt{L_p/C_p}}{R_{eq}} = \frac{I_{out_n} I_{base} \sqrt{L_p/C_p}}{nU_2} = \frac{I_{out_n}}{M}. \quad (39)$$

Therefore, for a *CLLC* converter operating at a specific frequency, as M gradually decreases from a large value to zero, the normalized output current monotonically increases to the maximum value. The operating state of the circuit starts in O mode, then passes through several modes, and finally reaches the state of a short circuit on the output side. During this process, the quality factor Q increases monotonically from 0 to infinity, as shown in Figs. 8 and 15. Where Q_{b1_n} and Q_{b2_n} are the quality factor Q of certain P modes corresponding to I_{b1_n} and I_{b2_n} .

By solving the mode equations and mode boundary equations, the gain curves of the resonant tank under different quality factor Q can be accurately obtained, as shown in Fig. 16.

B. Reverse Mode

When *CLLC* converter operates in reverse mode, energy is transferred from U_2 to U_1 . As shown in Fig. 17, similar to

Fig. 15. Modes distribution of CLLC in f_n - Q plane.Fig. 16. Gain curves under different quality factor Q .

forward mode, we have following definitions in:

$$\begin{cases} k' = L_{se}/L_m = hk \\ h' = L_p/L_{se} = 1/h \end{cases} \quad (40)$$

$$\begin{aligned} Z_{base_R} &= Z_{r_R} = \sqrt{L_{se}/C_{se}} \\ &= hZ_r, U_{base_R} = nU_2, \\ I_{base_R} &= U_{base_R}/Z_{base_R}, \omega_{base_R} \\ &= \omega_r = (L_{se}C_{se})^{-1/2} = (L_pC_p)^{-1/2} \end{aligned} \quad (41)$$

where subscript R indicates for corresponding normalization bases for reverse operation.

However, for OBC applications, U_2 varies as battery discharged, which violates the definition of normalization base. In order to be consistent with the forward mode, the voltage and current normalization bases defined by the forward mode in (42) are still adopted in reverse mode analysis

$$U_{base} = U_1, I_{base} = U_{base}/Z_{base}. \quad (42)$$

It is not difficult to derive that there is a conversion coefficient between the voltage base of forward mode and reverse mode, and there is also a conversion coefficient between the current base of forward mode and reverse mode, as shown in (43), where M_R

is the voltage gain of reverse mode

$$\begin{cases} \frac{U_{base}}{U_{base_R}} = \frac{U_1}{nU_2} = M_R \\ \frac{I_{base}}{I_{base_R}} = \frac{U_{base}/Z_{base}}{U_{base_R}/Z_{base_R}} = hM_R. \end{cases} \quad (43)$$

After all definitions have been established, it is easy to obtain the analytical solutions of P stage for reverse mode in (44).

Where $k'_1 = (h'k'(h'k'+k'+1))^{1/2}$, m_{1P0_R} , m_{2P0_R} , j_{1P0_R} , and j_{2P0_R} are the normalized initial value of primary resonant capacitor voltage, secondary resonant capacitor voltage, primary resonant inductor current, and secondary resonant inductor current during reverse mode. $m_{1P_R}(\theta)$, $m_{2P_R}(\theta)$, $j_{1P_R}(\theta)$, and $j_{2P_R}(\theta)$ are the normalized value, respectively, of u_{1P_R} , u_{2P_R} , i_{1P_R} , and i_{2P_R}

Correspondingly, the analytical solutions of the N stage and O stage in reverse mode can be obtained, which will not be repeated here. Compared with the forward operation, only the relevant parameters (h' , k') are different when CLLC converter operates in reverse operation. Therefore, the corresponding operation modes and mode distribution are similar to the forward operation, which will not be repeated further.

Similar to forward operation, the normalized output current $I_{out_n_R}$ and output power $P_{out_n_R}$ of reverse mode can be described in (45) and (46), respectively. Where $m_{1_R}(\theta)$, $m_{2_R}(\theta)$, $j_{1_R}(\theta)$, and $j_{2_R}(\theta)$ are the normalized value of u_{1_R} , u_{2_R} , i_{1_R} , and i_{2_R} , respectively, and subscript R denotes for reverse mode. θ_{P0} and θ_P represent the start and end moment of P stage, θ_{N0} and θ_N represent the start and end moment of N stage

$$\begin{aligned} I_{out_n_R} &= f_n \int_0^{\pi/f_n} |j_{1_R}(\theta)| d\theta / \pi \\ &= f_n \left(\int_{\theta_{P0}}^{\theta_P} j_{1P_R}(\theta) d\theta - \int_{\theta_{N0}}^{\theta_N} j_{1N_R}(\theta) d\theta \right) / \pi \\ &= f_n (m_{1P_R}(\theta_P) - m_{1P_R}(\theta_{P0}) + m_{1N_R}(\theta_N) \\ &\quad - m_{1N_R}(\theta_N)) / \pi \end{aligned} \quad (45)$$

$$\begin{aligned} P_{out_n_R} &= 1I_{out_n_R} \\ &= I_{out_n_R} \\ &= \frac{1}{M_R} f_n \int_0^{\pi/f_n} j_{2_R}(\theta) d\theta / \pi \\ &= \frac{1}{hM_R} f_n (m_{2_R}(\pi/f_n) - m_{2_R}(0)) / \pi \\ &= \frac{-2}{hM_R} f_n m_{2_R}(0) / \pi. \end{aligned} \quad (46)$$

Accordingly, both Q_R and R_{eq_R} for reverse mode are defined in

$$R_{eq_R} = \frac{U_1}{I_{out_n_R} I_{base}} \quad (47)$$

$$Q_R = \frac{h\sqrt{L_p/C_p}}{R_{eq_R}} = \frac{I_{out_n_R} I_{base} h \sqrt{L_p/C_p}}{U_1} = I_{out_n_R} h. \quad (48)$$

Considering that h is a constant, then the three operating conditions of constant $I_{out_n_R}$, constant $P_{out_n_R}$ and constant

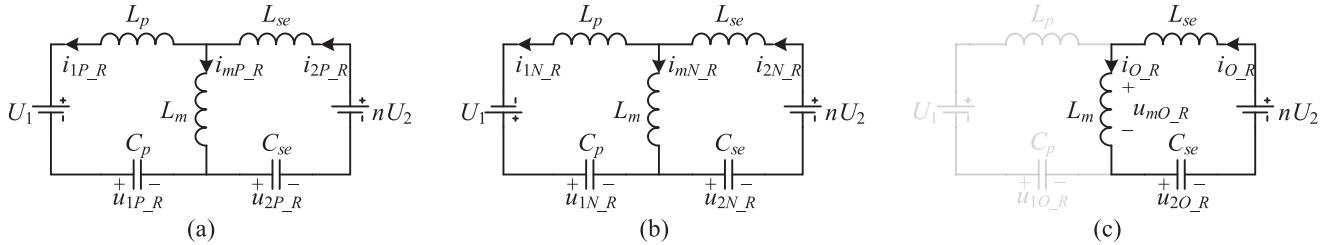


Fig. 17. Equivalent circuit of the CLLC resonant tank in different operating stages of reverse mode. (a) P stage. (b) N stage. (c) O stage.

resistive load (Q_R) for the CLLC converter operating in reverse mode can be regarded as the same situation for analysis. The following analysis takes constant $P_{\text{out_}n_R}$ as an example.

Similarly, for a CLLC converter in reverse mode operating at a certain frequency, as the voltage gain M_R gradually decreases from a large value to zero, the normalized output power monotonically increases from zero to infinity. The operating state of the circuit starts in O mode, then passes through several modes, and finally reaches the state of a short circuit on the output side. As shown in Fig. 18, where $P_{b1_n_R}$ and $P_{b2_n_R}$ are defined in (49) similar to forward mode

$$\begin{cases} P_{b1_n_R} = \frac{2k'}{h(h'k'+h'+1)\pi} \\ P_{b2_n_R} = \frac{2(k'+2)}{h(h'k'+h'+1)\pi}. \end{cases} \quad (49)$$

For CLLC converter operates in reverse mode, the constraint for inverting side to achieve ZVS can be described in (50). Where j_{20_R} is the normalized value of i_{2_R} at the start moment of the positive cycle in reverse mode

$$\begin{aligned} n |j_{20_R}| I_{\text{base}} t_{\text{dead}} &\geq 2C_{\text{oss}} U_2 \\ h M_R |j_{20_R}| &\geq \frac{2C_{\text{oss}} Z_{r_R}}{n^2 t_{\text{dead}}}. \end{aligned} \quad (50)$$

For the convenience of the ZVS derivation, the generalized ZVS current $j_{\text{ZVS_}R}$ in (51) is adopted

$$j_{\text{ZVS_}R} = h M_R j_{20_R}. \quad (51)$$

Through numerical calculation, it is easy to obtain the gain curves and the generalized ZVS current $j_{\text{ZVS_}R}$ of the corresponding operating point when the CLLC converter is operating under constant $P_{\text{out_}n_R}$ mode in reverse mode, as shown in Fig. 19.

TABLE V
DESIGN SPECIFICATIONS FOR CLLC RESONANT CONVERTER

Parameter	Symbol	Value
Bus voltage	U_1	400 V
Battery voltage range	$U_{2m} \sim U_{2M}$	250 V–450 V
Rated power	P_{rated}	1 kW
Resonant frequency	f_r	100 kHz
Operating frequency range	$f_{s,\min} \sim f_{s,\max}$	50 kHz–200 kHz

It is easy to derive that for CLLC converters operates under constant $P_{\text{out_}n_R}$ mode in reverse operation that ZVS is most likely to be lost when the $P_{\text{out_}n_R}$ reaches the maximum in BRR or the minimum (even O mode) in ARR.

IV. DESIGN METHODOLOGY

According to Section III, the characteristics of CLLC converter are determined by parameters h and k . Although the wide-range voltage of battery brings great challenges to the design of the bidirectional CLLC converter, through reasonable design of parameters h and k , the optimal S-type CLLC that satisfies the design specification can be obtained. In this section, the design methodology will be explained elaborately.

The following design process takes a bidirectional CLLC converter with a rated power of 1 kW as an example, and the corresponding design specifications are listed in Table V.

Considering voltage and power grades for bidirectional operations, SCT3080AL MOSFET from ROHM semiconductor is chosen for both sides. It is not difficult to find that the C_{oss} of SCT3080AL decreases monotonically with the increase of the drain-source voltage through datasheet. Considering that the V_{ds} on the primary side is constantly 400 V, the corresponding C_{oss} can be obtained by data interpolation to be approximately

$$\left\{ \begin{array}{l} m_{2P_R}(\theta) = \frac{1}{M_R} \left(\frac{M_R(\cos(\theta)-\cos(k'_1\theta))}{h'+1} + 1 + \frac{1}{h'+1} ((m_{2P0_R} + m_{1P0_R} - 1) \cos(\theta) + (j_{2P0_R} + h'j_{1P0_R}) \sin(\theta) + (h'm_{2P0_R} - h' - m_{1P0_R}) \cos(k'_1\theta) + \frac{h'(j_{2P0_R} - j_{1P0_R}) \sin(k'_1\theta)}{k'_1}) \right) \\ j_{2P_R}(\theta) = \frac{1}{hM_R} \left(\frac{M_R(k'_1 \sin(k'_1\theta) - \sin(\theta))}{h'+1} + \frac{1}{h'+1} ((1 - m_{2P0_R} - m_{1P0_R}) \sin(\theta) + (j_{2P0_R} + h'j_{1P0_R}) \cos(\theta) + k'_1 (h' + m_{1P0_R} - h'm_{2P0_R}) \sin(k'_1\theta) + h'(j_{2P0_R} - j_{1P0_R}) \cos(k'_1\theta)) \right) \\ m_{1P_R}(\theta) = \frac{1}{M_R} \left(\frac{M_R(\cos(\theta)h' + \cos(k'_1\theta))}{h'+1} - M_R + \frac{1}{h'+1} (h' (m_{2P0_R} + m_{1P0_R} - 1) \cos(\theta) + h'(j_{2P0_R} + h'j_{1P0_R}) \sin(\theta) + \frac{h'(j_{1P0_R} - j_{2P0_R}) \sin(k'_1\theta)}{k'_1}) \right) \\ h'(j_{2P0_R} + h'j_{1P0_R}) \sin(\theta) + (h' + m_{1P0_R} - hm_{2P0_R}) \cos(k'_1\theta) + \frac{h'(j_{1P0_R} - j_{2P0_R}) \sin(k'_1\theta)}{k'_1} \\ j_{1P_R}(\theta) = \frac{1}{hM_R} \left(- \frac{M_R(h'\sin(\theta) + k'_1 \sin(k'_1\theta))}{h'(h'+1)} + \frac{1}{h'+1} ((1 - m_{2P0_R} - m_{1P0_R}) \sin(\theta) + (j_{2P0_R} + h'j_{1P0_R}) \cos(\theta) + \frac{k'_1(h'm_{2P0_R} - h' - m_{1P0_R})}{h'} \sin(k'_1\theta) + (j_{1P0_R} - j_{2P0_R}) \cos(k'_1\theta)) \right). \end{array} \right. \quad (44)$$

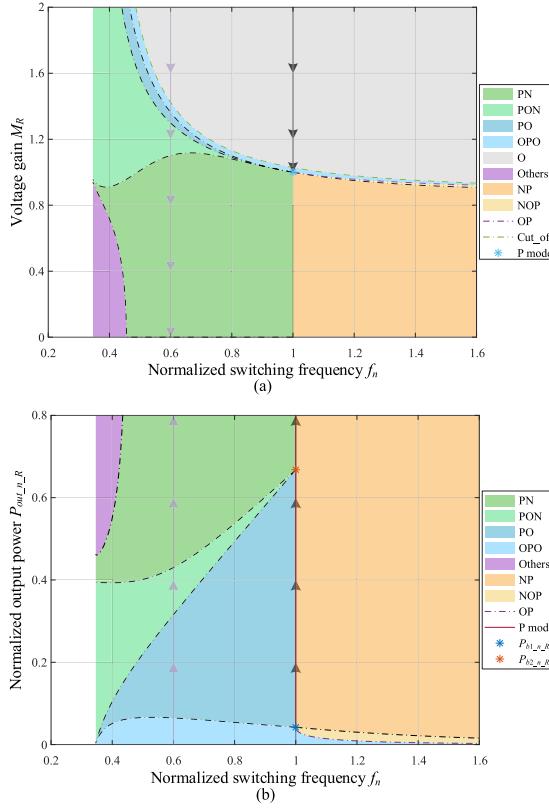


Fig. 18. Modes distribution of CLLC for reverse mode in f_n - M_R plane and f_n - $P_{out,n,R}$ plane. (a) f_n - M_R plane. (b) f_n - $P_{out,n,R}$ plane.

64.8298 pF, and the V_{ds} on the secondary side fluctuates within 250 V–450 V, and the corresponding maximum C_{oss} can be obtained by data interpolation to be approximately 80.0486 pF when V_{ds} on the secondary side is 250 V. In the following analysis, reasonable margin is reserved, the output capacitor C_{oss1} of primary side is set to 70 pF, and the output capacitor C_{oss2} of secondary side is set to 85 pF. Meantime, considering the device characteristics and switching frequency, the designed dead time is 200 ns, as shown in

$$\begin{cases} C_{oss1} = 70 \text{ pF} \\ C_{oss2} = 85 \text{ pF} \\ t_{dead} = 200 \text{ ns.} \end{cases} \quad (52)$$

First, set the transformer ratio n as an undetermined value, and the influence of n on the bidirectional voltage gain of the CLLC converter can be described in (53). Assuming that there are both voltage boost and step down during bidirectional operation, the range of n can be obtained in

$$\begin{cases} M_m = \frac{nU_{2m}}{U_1} < 1 < M_M = \frac{nU_{2M}}{U_1} \\ M_{Rm} = \frac{1}{M_M} < 1 < M_{RM} = \frac{1}{M_m} \end{cases} \Rightarrow \frac{8}{9} < n < 1.6 \quad (53)$$

where M_m and M_M are the minimum and maximum voltage gain for forward operation, M_{Rm} and M_{RM} are the minimum and maximum voltage gain for reverse operation, respectively.

As shown in Fig. 20, which illustrated the typical gain curves of CLLC under different load conditions for forward operation, where M_{rated} represents the gain curve for rated power, M_O

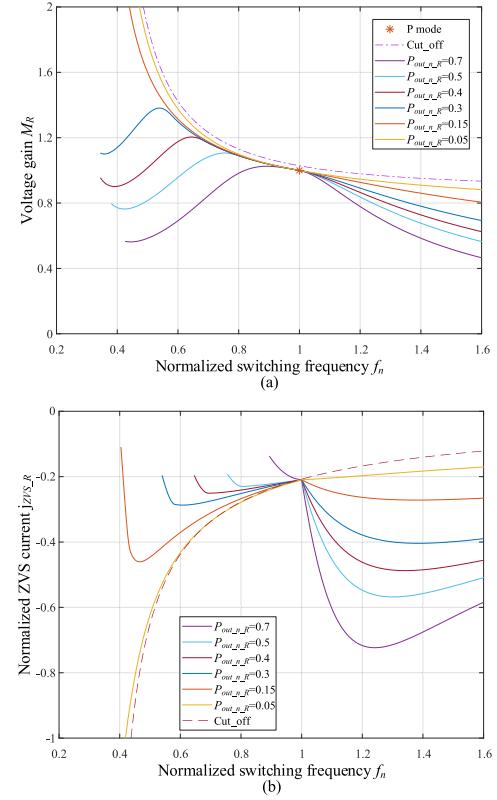


Fig. 19. Gain curves under different $P_{out,n,R}$ (a) and corresponding ZVS current $j_{ZVS,R}$ (b).

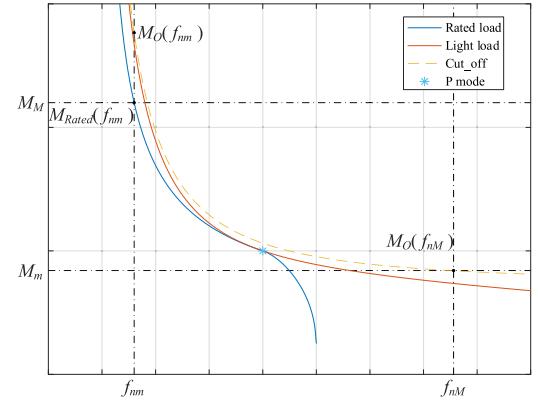


Fig. 20. Typical gain curve of CLLC under different load conditions.

indicates the gain curve for O mode under zero-load condition or Cut-off boundary, f_{nM} and f_{nm} are the maximum and minimum normalized frequency according to design specifications. According to Section III, within the desired operating frequency range of both forward and reverse mode, the heavier the load, the more difficult it is to boost voltage in BRR; the lighter the load, the more difficult it is to step down voltage in ARR. In other words, as long as the CLLC can achieve the designed maximum voltage gain M_M and M_{RM} within the designed frequency range in BRR under rated load condition, then the CLLC can reach the designed maximum voltage gain M_M and

M_{RM} under any load condition. Similarly, as long as the *CLLC* can achieve the designed minimum voltage gain M_m and M_{Rm} within the designed frequency range in ARR under the lightest load condition, then the *CLLC* can reach the designed minimum voltage gain M_m and M_{Rm} under any load condition. The most extreme light-load condition is the O mode under zero-load condition. At this time, *CLLC* has the strongest capability to boost voltage and the weakest capability to step down voltage. The gain capability of the critical O mode is M_O shown in (54), which is the lower boundary of (28). Therefore, for *CLLC* with parameters that satisfy the forward design voltage gain, it is not difficult to obtain the following constraints in (55) and (56), where $M_{\text{Rated}}(f_{nm})$ is the voltage gain for rated power at f_{nm} and $M_O(f_{nM})$ is the voltage gain for zero-load O mode at f_{nM}

$$M_O = \frac{\sec(k_2\pi/(2f_n))}{k+1} \quad (54)$$

$$M_{\text{Rated}}(f_{nm}) \geq M_M \quad (55)$$

$$M_O(f_{nM}) \leq M_m. \quad (56)$$

Unfortunately, the gain curve for rated power M_{rated} can only be obtained by numerical calculation, which cannot be adopted for further analytical analysis. Considering that gain curve M_O for zero-load O mode can be expressed analytically and *CLLC* has the strongest capability to boost voltage at this time, (55) is compromised and transformed into (57) for further analysis, where $M_O(f_{nm})$ is the voltage gain for zero-load O mode at f_{nm} . Note that (57) is a necessary but insufficient constraint at this time

$$M_O(f_{nm}) \geq M_{\text{Rated}}(f_{nm}) \geq M_M \Rightarrow M_O(f_{nm}) \geq M_M. \quad (57)$$

So far, the gain constraints for forward operation have been obtained, as shown in (56) and (57), which are expanded in (58) and (59), respectively. Here, (58) is a necessary and sufficient condition, and (59) is a necessary but insufficient condition

$$\frac{\sec(k_2\pi/(2f_{nM}))}{k+1} \leq M_m \quad (58)$$

$$\frac{\sec(k_2\pi/(2f_{nm}))}{k+1} \geq M_M. \quad (59)$$

By taking M_O as Taylor expansion, inequalities in (60) and (61) hold. Therefore, more stringent constraints are established in (62) and (63) to ensure that (58) and (59) hold

$$\frac{\sec(k_2\pi/(2f_n))}{k+1} \leq \frac{1}{(k+1)(1 - \frac{\pi^2 k_2^2}{8f_n^2})} \quad (60)$$

$$\frac{\sec(k_2\pi/(2f_n))}{k+1} \geq \frac{1}{(k+1)(1 - \frac{\pi^2 k_2^2}{8f_n^2} + \frac{\pi^4 k_2^4}{384f_n^4})} \quad (61)$$

$$\frac{1}{(k+1)(1 - \frac{\pi^2 k_2^2}{8f_n^2})} \leq M_m \quad (62)$$

$$\frac{1}{(k+1)(1 - \frac{\pi^2 k_2^2}{8f_n^2} + \frac{\pi^4 k_2^4}{384f_n^4})} \geq M_M. \quad (63)$$

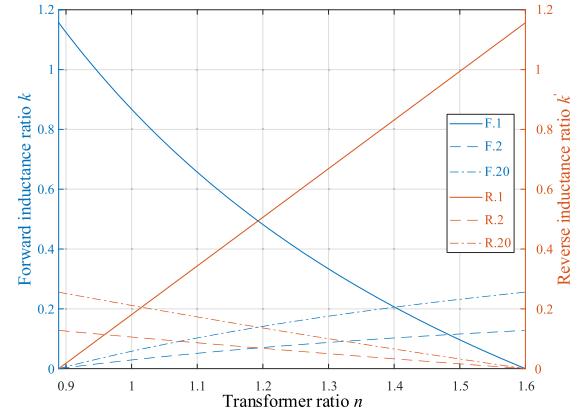


Fig. 21. Gain constraints for forward and reverse mode. F.1 indicates the forward voltage step down constraint refer to (64), F.2 denotes the forward pseudovoltage boost constraint refer to (65), and F.20 illustrates the genuine voltage boost constraint related to (55) for forward operation. R.1 indicates the reverse voltage step down constraint refer to (66), R.2 denotes the reverse pseudo voltage boost constraint refer to (67), and R.20 illustrates the genuine voltage boost constraint related to (55) for reverse operation.

Furthermore, (62) and (63) are further simplified into (64) and (65). Correspondingly, there are constraints similar to (64) and (65) in (66) and (67) for *CLLC* operates in the reverse mode, where M_m , M_M , M_{Rm} , and M_{RM} are defined in (53)

$$k \geq \left(\frac{1}{M_m} - 1 \right) \frac{8f_{nM}^2}{8f_{nM}^2 - \pi^2} \quad (64)$$

$$k \geq \frac{24(16f_{nm}^4 M_M - \pi^2 f_{nm}^2 M_M - 8f_{nm}^4)}{M_M (384f_{nm}^4 - 48\pi^2 f_{nm}^2 + \pi^4)} \\ - 8\sqrt{3} \sqrt{\frac{\pi^4 f_{nm}^4 M_M^2 - 48\pi^2 f_{nm}^6 M_M + 2\pi^4 f_{nm}^4 M_M + 192f_{nm}^8}{M_M^2 (384f_{nm}^4 - 48\pi^2 f_{nm}^2 + \pi^4)^2}} \quad (65)$$

$$k' \geq \left(\frac{1}{M_{RM}} - 1 \right) \frac{8f_{nM}^2}{8f_{nM}^2 - \pi^2} \quad (66)$$

$$k' \geq \frac{24(16f_{nm}^4 M_{RM} - \pi^2 f_{nm}^2 M_{RM} - 8f_{nm}^4)}{M_{RM} (384f_{nm}^4 - 48\pi^2 f_{nm}^2 + \pi^4)} \\ - 8\sqrt{3} \sqrt{\frac{\pi^4 f_{nm}^4 M_{RM}^2 - 48\pi^2 f_{nm}^6 M_{RM} + 2\pi^4 f_{nm}^4 M_{RM} + 192f_{nm}^8}{M_{RM}^2 (384f_{nm}^4 - 48\pi^2 f_{nm}^2 + \pi^4)^2}}. \quad (67)$$

The constraints corresponding to (64)–(67) have been plotted in Fig. 21, where the dash-dot line (F.20 and R.20) described the genuine voltage boost constraint related to (55) for bidirectional operation with different colors, which in fact cannot be obtained analytically.

For *CLLC* converters, the typical value of the inductance ratio is generally 0.1–0.3. Excessive k or k' will increase the circulating reactive power and reduce the system efficiency. It can be seen from Fig. 21 that if the *CLLC* can achieve the zero-load minimum voltage gain under bidirectional operation within the designed frequency range, then one of the forward or reverse inductance ratio k or k' will be always bigger than 0.5, which should be avoided in practice. Considering that in

TABLE VI
POSSIBLE CRITICAL VALUE

Iteration values	$M_m \sim M_M$	$M_{Rm} \sim M_{RM}$
$n = 1.48, k = 0.12$	0.925–1.665	0.6–1.081
$n = 1.47, k = 0.13$	0.918–1.654	0.604–1.089
$n = 1.46, k = 0.14$	0.912–1.643	0.608–1.096
$n = 1.45, k = 0.15$	0.906–1.632	0.613–1.104
$n = 1.44, k = 0.161$	0.9–1.62	0.617–1.112
$n = 1.43, k = 0.172$	0.893–1.61	0.621–1.119
...

OBC applications, the zero-load step-down requirements during forward charging operation are more practical. In contrast, the zero load or even light-load step-down requirements during reverse discharge operation are not indispensable. Therefore, it can be considered to partially sacrifice the reverse light-load voltage step down capability to mitigate the forward and reverse inductance ratio k and k' at appropriate value. The following analysis assumes that the minimum load condition for reverse operation to achieve the minimum voltage step-down M_{Rm} is 50% of the rated load.

As illustrated in Fig. 21, since the genuine voltage boost constraint (F.20) must be more demanding than the pseudovoltage boost constraint (F.2) for forward operation, the minimum k that satisfies the forward regulation voltage constraint must be on the boundary of the forward zero-load voltage step down constraint (F.1) and locate on the left side of the intersection of forward pseudo voltage boost constraint (F.2) and forward zero-load voltage step down constraint (F.1). It is not difficult to derive the coordinate of the intersection in

$$\begin{cases} n = 1.4832 \\ k = 0.1138 \end{cases}. \quad (68)$$

A series of possible values of (n, k) and the corresponding voltage gain range of bidirectional operation can be obtained by taking values to the left of the intersection (68) on the forward zero-load voltage step down boundary constraint (F.1), as shown in Table VI.

So far, for each possible design value (n, k, h) , only h is still missing. The iterative process of h value is explained in detail as follows.

Step 1: Given the initial iteration value h_0 , design values n , k , and the corresponding voltage gain range $M_m \sim M_M$ and $M_{Rm} \sim M_{RM}$. TDM is adopted to solve iteratively within the designed frequency range for the maximum normalized power P_{nMt} that can achieve the maximum voltage boost gain M_M in forward mode, the maximum normalized power P_{nRMt} that can realize the maximum voltage boost gain M_{RM} during reverse operation, and the minimum normalized power P_{nRm} that can achieve the minimum voltage step down gain M_{Rm} in reverse mode. Finally, the designed normalized rated power P_n is defined as the smaller between P_{nRMt} and P_{nMt} in

$$P_n = \min(P_{nMt}, P_{nRMt}). \quad (69)$$

Step 2: Judging whether the minimum normalized power P_{nRm} for reverse mode is less than 50% of the rated power P_n .

TABLE VII
ITERATION RESULTS

Iteration point	h	P_n	P_{nRm}	Z_r	L_m
$n = 1.48, k = 0.12$	5.82	0.03848	0.0192	6.1568	$51.3/\omega_r$
$n = 1.47, k = 0.13$	4.16	0.09296	0.0464	14.8736	$114.412/\omega_r$
$n = 1.46, k = 0.14$	1.63	0.32919	0.16405	52.67	$376.217/\omega_r$
$n = 1.45, k = 0.15$	1.04	0.469	0.2342	75.04	500.26/ω_r
$n = 1.44, k = 0.161$	0.87	0.5	0.2488	80	496.89/ ω_r
$n = 1.43, k = 0.172$	0.79	0.515	0.2563	82.4	479.06/ ω_r
...

Meantime, the lower limit of P_{nRm}/P_n is also limited to 0.5-tolerance, where tolerance is the iteration error limit, the value in this article is 0.005. If $P_{nRm}/P_n > 0.5$, increase the value of h and return to Step 1 to continue iteration; if $P_{nRm}/P_n < 0.5$ -tolerance, decrease the value of h and return to Step 1 to continue iteration.

Step 3: Calculate the corresponding characteristic impedance Z_r according to the rated normalized power P_n and rated power P_{rated} , and comprehensively consider the minimum normalized ZVS current $|j_{ZVS_R}|_{\min}$ and $|j_{10}|_{\min}$ obtained by TMD and Z_r to judge whether the bidirectional full range ZVS is realized. The corresponding constraints are shown in

$$\begin{cases} Z_r = P_n U_1^2 / P_{\text{rated}} \\ |j_{ZVS_R}|_{\min} n^2 t_{\text{dead}} \geq 2C_{\text{oss2}} h Z_r \\ |j_{10}|_{\min} t_{\text{dead}} \geq 2C_{\text{oss1}} Z_r \end{cases} \quad (70)$$

where $|j_{ZVS_R}|_{\min}$ and $|j_{10}|_{\min}$ are the minimum ZVS current during discharging and charging operations, respectively. If the verification finds that the full range of ZVS has been achieved, then the current iteration is ended and the corresponding design value is accepted. Meantime, another set of (n, k) value iteration starts. Otherwise, increase the value of h and start Step 4.

Step 4: Similar to Step 1, recalculate P_{nMt} , P_{nRMt} , P_{nRm} , P_n , and P_{nRm} is also recorded as P_{nRm0} . Note that there should be $P_{nRm}/P_n < 0.5$ -tolerance at this time.

Step 5: While keeping P_n unchanged, adjust P_{nRm} so that 0.5 -tolerance $\leq P_{nRm}/P_n \leq 0.5$ is satisfied.

Step 6: Similar to Step 3, verify whether the full range of ZVS has been achieved. If the verification finds that the full range of ZVS has been achieved, then the current iteration is ended and the corresponding design value is accepted. Meantime, another set of (n, k) value iteration starts. Otherwise, continue with Step 7.

Step 7: While reducing P_n , adjust P_{nRm} to maintain 0.5 -tolerance $\leq P_{nRm}/P_n \leq 0.5$. Meantime, always observe whether P_{nRm} is not less than P_{nRm0} . Otherwise, increase the value of h and return to Step 4.

Step 8: Similar to Step 3, verify whether the full range of ZVS has been achieved. If the verification finds that the full range of ZVS has been achieved, then the current iteration is ended and the corresponding design value is accepted, meantime, another set of (n, k) value iteration starts. Otherwise, return to Step 7.

The overall iterative process is shown in Fig. 22, and the iteration results are listed in Table VII. For each set of (n, k)

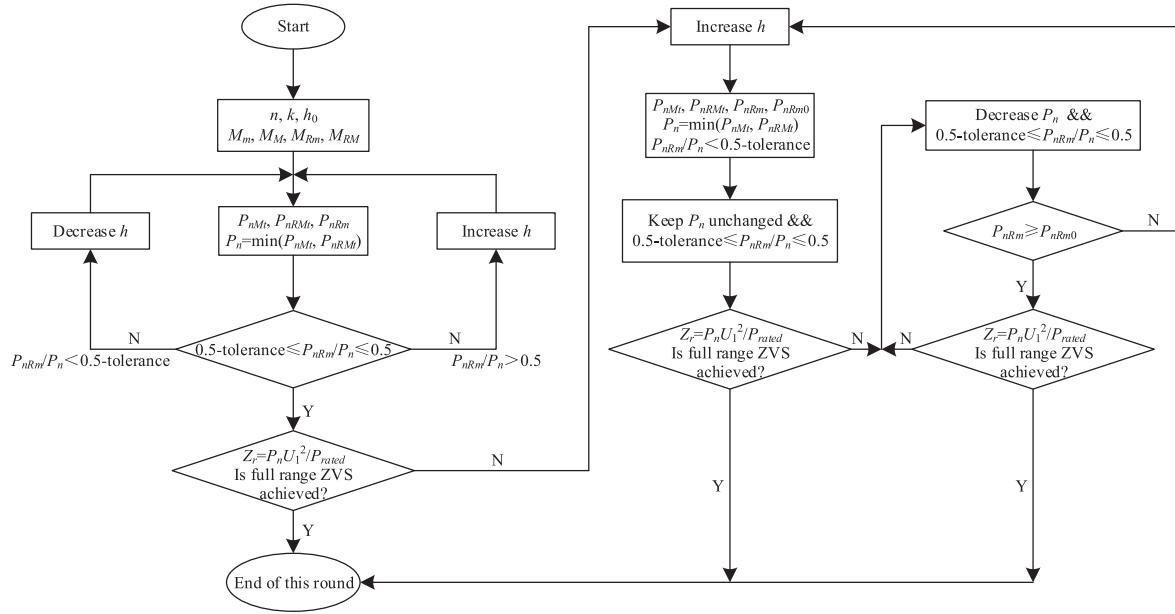


Fig. 22. Design flowchart of the proposed design methodology.

values, after the iterative process is done, the corresponding h , P_n , P_{nRm} , and Z_r can be obtained, which can always guarantee the achievement of the designed bidirectional voltage gain and full range of ZVS.

For different set of (n, k) values, this article chooses the iteration result with the maximum magnetizing inductance L_m as the optimal design, because the maximum magnetizing inductance means the minimum circulating reactive power. The corresponding magnetizing inductance can be calculated through

$$L_m = \frac{L_p}{k} = \frac{\sqrt{L_p C_p} \sqrt{L_p / C_p}}{k} = \frac{Z_r}{k \omega_r}. \quad (71)$$

Traverse the iterative results, the optimal design parameters can be obtained in

$$\left\{ \begin{array}{l} n = 1.45 \\ k = 0.15 \\ h = 1.04 \\ Z_r = 75.04\Omega \\ f_r = 100 \text{ kHz} \end{array} \right. \Rightarrow \left\{ \begin{array}{l} L_p = \frac{Z_r}{\omega_r} = 119.429 \text{ uH} \\ L_m = \frac{Z_r}{k\omega_r} = 796.19 \text{ uH} \\ C_p = \frac{1}{h\omega_r} = 21.21 \text{ nF} \\ L_s = \frac{hL_p}{n^2} = \frac{hZ_r}{n^2\omega_r} = 59.076 \text{ uH} \\ C_s = \frac{n^2C_p}{h} = \frac{n^2}{hZ_r\omega_r} = 42.877 \text{ nF.} \end{array} \right. \quad (72)$$

The initial value of h_0 for the iteration is generally obtained by trial and error. A rough method to estimate h_0 is introduced in this article. It is not difficult to obtain the constraint boundary that satisfies the bidirectional zero-load voltage step down in (73). Assuming that the minimum load condition that can achieve the designed step-down gain during reverse operation is part of the rated load, as shown in (74). Considering that only need to achieve light-load step-down during reverse operation, the boundary constraint of the reverse inductance ratio k' can be relatively alleviated, and $1-F$ in (75) is used to approximately denotes the corresponding alleviation effect. Therefore, it is not difficult to derive the corresponding initial value of h_0 in (76) as

follows:

$$\begin{cases} k = \left(\frac{1}{M_m} - 1\right) \frac{8f_{nM}^2}{8f_{nM}^2 - \pi^2} \\ k' = \left(\frac{1}{M_{Rm}} - 1\right) \frac{8f_{nM}^2}{8f_{nM}^2 - \pi^2} \end{cases} \quad (73)$$

$$P_{nRm}/P_n = F \quad (74)$$

$$k' = h_0 k = (1 - F) \left(\frac{1}{M_{Rm}} - 1 \right) \frac{8f_{nM}^2}{8f_{nM}^2 - \pi^2} \quad (75)$$

$$h_0 = \frac{(1-F)\left(\frac{1}{M_{Rm}} - 1\right) \frac{8f_{nM}^2}{8f_{nM}^2 - \pi^2}}{\left(\frac{1}{M_m} - 1\right) \frac{8f_{nM}^2}{8f_{nM}^2 - \pi^2}} = \frac{(1-F)\left(\frac{1}{M_{Rm}} - 1\right)}{\left(\frac{1}{M_m} - 1\right)}. \quad (76)$$

With $F = 50\%$, in this article, the initial value of h_0 can be further simplified in

$$h_0 = \frac{\left(\frac{1}{M_{Rm}} - 1\right)}{2\left(\frac{1}{M_m} - 1\right)} = \frac{5n(9n - 8)}{16(8 - 5n)}. \quad (77)$$

V. AREA PRODUCT (AP) OPTIMIZATION

According to Section II, for a certain given S-type *CLLC*, when the symmetry coefficient H varies from 0 to infinity, there are infinite kinds of D-type *CLLC* equivalent to it. Since the equivalent process is externally equivalent, the inflow current and port voltage of the resonant tank remain unchanged, and only the voltage of the magnetic components and the current of the magnetizing inductance changed, which means that in the infinite number of equivalent D-type *CLLCs*, there must exist a parameter design that minimizes the total loss or the sum of the AP capacity of the magnetic components. Considering that AP is the multiplication of effective cross-sectional area of magnetic core (A_e) and window area of magnetic core (A_w), the AP maximum capacity is adopted to denotes the volume

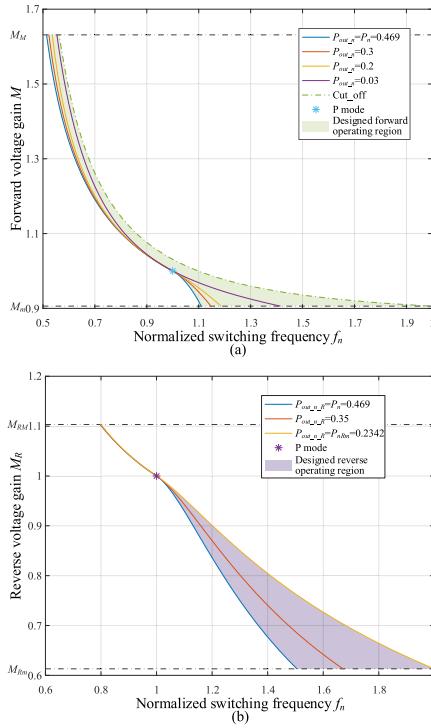


Fig. 23. Gain curves of the designed CLLC for bidirectional operation. (a) Charging mode. (b) Discharging mode.

and cost of the magnetic components of CLLC. In this article, the AP capacity is selected as the optimization target, and TDM is adopted to find the optimum equivalent D-type CLLC, which minimizes the sum of the AP capacity of the magnetic components.

For transformers and inductors, AP capacity have different definitions, as indicated in (78), where k_c is filling factor, J is wire current density, B_m is the magnetic flux peak density for inductor core, and ΔB is the magnetic flux peak to peak density for transformer core. In order to guarantee the consistency of the comparison results, it is assumed that k_c , J , and B_m are the same for the inductance and transformer in the following analysis. Where I_{rms} and I_{peak} are the root mean square (rms) value and peak value of the inductor current, respectively. u_m is the voltage on the magnetizing inductor and $t_0 \sim t_0 + T_s/2$ is half a switching cycle when u_m is positive. $I_{p,\text{rms}}$ and $I_{s,\text{rms}}$ are the rms value of primary coil current i_p and secondary coil current i_s , respectively. $I_{m,\text{peak}}$ is peak value of the magnetizing current i_m . N is the transformer ratio

$$\left\{ \begin{array}{l} \text{AP}_L = \frac{LI_{\text{rms}}I_{\text{peak}}}{k_cB_mJ} \\ \text{AP}_T = \frac{(I_{p,\text{rms}} + \frac{I_{s,\text{rms}}}{N}) \int_{t_0}^{t_0+T_s/2} u_m dt}{k_c\Delta B J} \\ = \frac{(I_{p,\text{rms}} + \frac{I_{s,\text{rms}}}{N}) L_m i_m|_{t_0}^{t_0+T_s/2}}{k_c 2B_m J} \\ = \frac{(I_{p,\text{rms}} + \frac{I_{s,\text{rms}}}{N}) L_m 2I_{m,\text{peak}}}{k_c 2B_m J} = \frac{(I_{p,\text{rms}} + \frac{I_{s,\text{rms}}}{N}) L_m I_{m,\text{peak}}}{k_c B_m J} \end{array} \right. \quad (78)$$

According to Section II, compared with S-type CLLC, the magnetizing current in equivalent D-type CLLC has been changed, and the current of the primary resonant L_{ap} and secondary resonant inductor L_{as} remain unchanged. For forward

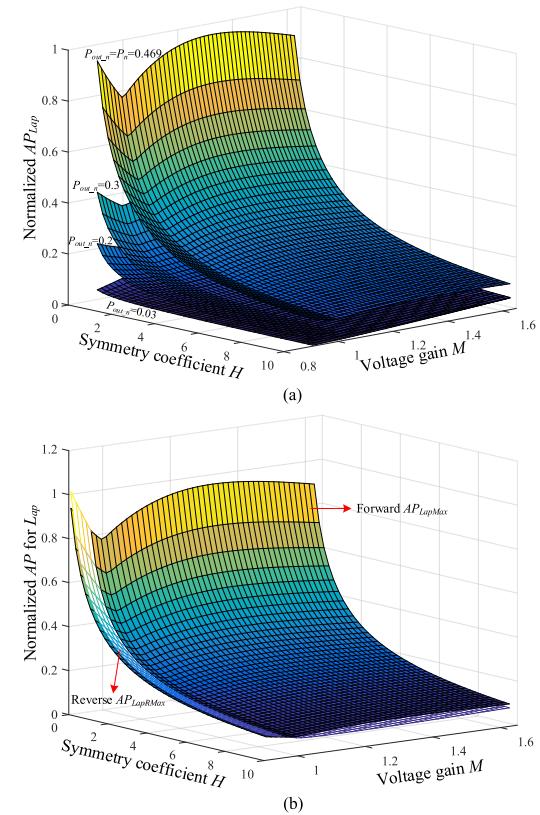


Fig. 24. Variations of AP capacity for L_{ap} . (a) Variations of AP capacity for L_{ap} in forward mode under different load conditions. (b) Maximum AP capacity AP_{LapMax} and $AP_{LapRMax}$ for L_{ap} during bidirectional operations.

mode, it is no hard to derive the magnetizing current i_{am} of the equivalent D-type CLLC in (79). Where i_1 and i_2 are the resonant inductor current in Fig. 4, respectively, for primary and secondary side

$$i_{am} = i_p - i_s/N = i_1 - ni_2/N. \quad (79)$$

Furthermore, the AP capacity of each magnetic component during forward mode can be obtained in (80). Where AP_{Lap} , AP_{Las} , and AP_T are the AP capacity of L_{ap} , L_{as} and transformer T of equivalent D-type CLLL during forward operation, respectively.

Similarly, it is easy to derive the magnetizing current i_{amR} of the equivalent D-type CLLC and the AP capacity of each component during reverse mode in (81) and (82), respectively. Where i_{1R} and i_{2R} are the resonant inductor current in Fig. 17 for primary and secondary side, respectively. AP_{LapR} , AP_{LasR} , and AP_{TR} are the AP capacity of L_{ap} , L_{as} and transformer T of equivalent D-type CLLL during reverse operation, respectively.

It is not difficult to find that all AP capacity contain $C_p U_1^2 (k_c B_m J)^{-1}$ terms, therefore, normalizing the AP capacity based on $C_p U_1^2 (k_c B_m J)^{-1}$ to simplify the following analysis.

Through time-domain calculations, it is no difficult to obtain the gain curves on the f_n - M plane and f_n - M_R plane when the designed S-type CLLC operates in both forward and reverse modes under constant power (e.g., P_{out_n} and $P_{out_n_R}$) conditions, as shown in Fig. 23. Furthermore, it can also obtain the

variations of the AP capacity of magnetic components when the *CLLC* converter operates in both forward and reverse mode under different load conditions within the designed voltage gain and the symmetry coefficient H of equivalent D-type *CLLC* varies from 0 to infinity. The AP capacity of L_{ap} is taken as an example here, as shown in Fig. 24(a). It is not difficult to find that the maximum AP capacity is always achieved with the maximum output power considering only the effect of output power (e.g., P_{out_n} and $P_{out_n_R}$) on AP capacity, which applies to L_{ap} , L_{as} and transformer T for bidirectional operations.

Similarly, by traversing the output power (e.g., P_{out_n} and $P_{out_n_R}$), it is not difficult to obtain the maximum AP capacity (e.g., AP_{LapMax} and $AP_{LapRMax}$ for L_{ap}) that the magnetic

$$\left\{ \begin{aligned} AP_{Lap} &= \frac{L_{ap} I_{p,\text{rms}} I_{p,\text{peak}}}{k_c B_m J} = \frac{L_p}{k_c B_m J} \frac{2k(hk+h+1)+H+1-\xi_1}{2k(hk+1)} \\ &\quad j_{1,\text{rms}} \frac{U_1}{\sqrt{L_p/C_p}} j_{1,\text{peak}} \frac{U_1}{\sqrt{L_p/C_p}} \\ &= \frac{C_p U_1^2}{k_c B_m J} \frac{2k(hk+h+1)+H+1-\xi_1}{2k(hk+1)} j_{1,\text{rms}} j_{1,\text{peak}} \\ AP_{Las} &= \frac{L_{as} I_{s,\text{rms}} I_{s,\text{peak}}}{k_c B_m J} = \frac{L_p}{k_c B_m J} \frac{2hHk^2+2(h+1)Hk+H+1-\xi_1}{2Hk(k+1)n^2} \\ &\quad nj_{2,\text{rms}} \frac{U_1}{\sqrt{L_p/C_p}} nj_{2,\text{peak}} \frac{U_1}{\sqrt{L_p/C_p}} \\ &= \frac{C_p U_1^2}{k_c B_m J} \frac{2hHk^2+2(h+1)Hk+H+1-\xi_1}{2Hk(k+1)} j_{2,\text{rms}} j_{2,\text{peak}} \\ AP_T &= \frac{(I_{p,\text{rms}} + \frac{I_{s,\text{rms}}}{N}) L_{am} I_{am,\text{peak}}}{k_c B_m J} \\ &= \frac{L_p}{k_c B_m J} \frac{\xi_1-H+1}{2k(hk+1)} (i_{1,\text{rms}} + \frac{n i_{2,\text{rms}}}{N})(i_1 - \frac{n i_2}{N})_{\text{peak}} \\ &= \frac{C_p U_1^2}{k_c B_m J} \frac{\xi_1-H+1}{2k(hk+1)} (j_{1,\text{rms}} + \frac{2hk+2}{\xi_1-H+1} j_{2,\text{rms}})(j_1 - \frac{2hk+2}{\xi_1-H+1} j_2)_{\text{peak}} \end{aligned} \right. \quad (80)$$

$$i_{amR} = i_{sR}/N - i_{pR} = ni_{2R}/N - i_{1R} \quad (81)$$

$$\left\{ \begin{aligned} AP_{LapR} &= \frac{L_{ap} I_{pR,\text{rms}} I_{pR,\text{peak}}}{k_c B_m J} = \frac{L_p}{k_c B_m J} \frac{2k(hk+h+1)+H+1-\xi_1}{2k(hk+1)} \\ &\quad j_{1R,\text{rms}} \frac{U_1}{\sqrt{L_p/C_p}} j_{1R,\text{peak}} \frac{U_1}{\sqrt{L_p/C_p}} \\ &= \frac{C_p U_1^2}{k_c B_m J} \frac{2k(hk+h+1)+H+1-\xi_1}{2k(hk+1)} j_{1R,\text{rms}} j_{1R,\text{peak}} \\ AP_{LasR} &= \frac{L_{as} I_{sR,\text{rms}} I_{sR,\text{peak}}}{k_c B_m J} \\ &= \frac{L_p}{k_c B_m J} \frac{2hHk^2+2(h+1)Hk+H+1-\xi_1}{2Hk(k+1)n^2} \\ &\quad nj_{2R,\text{rms}} \frac{U_1}{\sqrt{L_p/C_p}} nj_{2R,\text{peak}} \frac{U_1}{\sqrt{L_p/C_p}} \\ &= \frac{C_p U_1^2}{k_c B_m J} \frac{2hHk^2+2(h+1)Hk+H+1-\xi_1}{2Hk(k+1)} j_{2R,\text{rms}} j_{2R,\text{peak}} \\ AP_{TR} &= \frac{(I_{pR,\text{rms}} + \frac{I_{sR,\text{rms}}}{N}) L_{am} I_{amR,\text{peak}}}{k_c B_m J} \\ &= \frac{L_p}{k_c B_m J} \frac{\xi_1-H+1}{2k(hk+1)} (i_{1R,\text{rms}} + \frac{n i_{2R,\text{rms}}}{N})(\frac{n i_{2R}}{N} - i_{1R})_{\text{peak}} \\ &= \frac{C_p U_1^2}{k_c B_m J} \frac{\xi_1-H+1}{2k(hk+1)} \left(j_{1R,\text{rms}} + \frac{2hk+2}{\xi_1-H+1} j_{2R,\text{rms}} \right) \\ &\quad \left(\frac{2hk+2}{\xi_1-H+1} j_{2R} - j_{1R} \right)_{\text{peak}} \end{aligned} \right. \quad (82)$$

components may reach under the condition of certain voltage gain M and specific symmetry coefficient H when the *CLLC* converter operates in both forward and reverse mode, as shown in Fig. 24(b). In order to facilitate comparison, the bidirectional voltage gain ranges $M_m \sim M_M$ and $M_{Rm} \sim M_{RM}$ are uniformly converted to forward voltage gain range $M_m \sim M_M$ in Figs. 24(b)

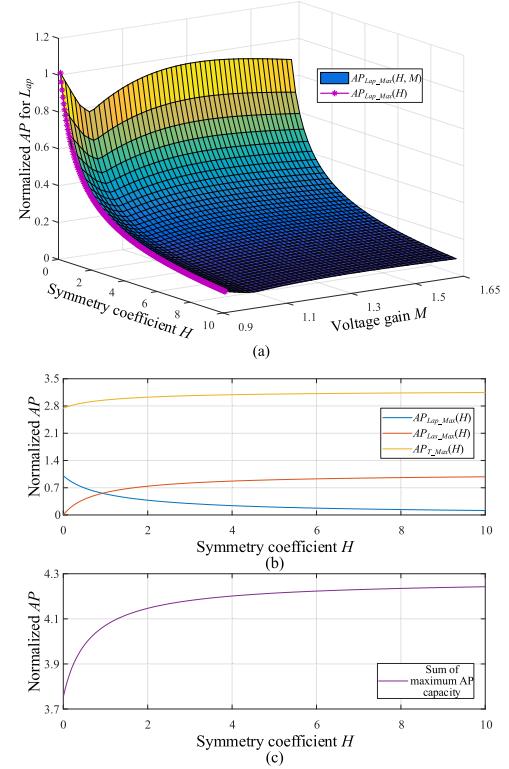


Fig. 25. Variations of AP capacity. (a) Variations of maximum AP capacity $AP_{Lap_Max}(H, M)$ and $AP_{LapR_Max}(H)$ for L_{ap} . (b) Variations of maximum AP capacity with H for each magnetic component. (c) Variations of sum of maximum AP capacity for magnetic components with H .

and 25(a). Where axis M also denotes $1/M_R$ for reverse operation. Moreover, by comparing the maximum AP capacity (e.g., AP_{LapMax} and $AP_{LapRMax}$ for L_{ap}) during bidirectional operation comprehensively, the variations of maximum AP capacity of the magnetic components ($AP_{Lap_Max}(H, M)$ for L_{ap}) are obtained, and by traversing the voltage gain M , the variation of the maximum AP capacity of the magnetic components with symmetry coefficient H (e.g., $AP_{Lap_Max}(H)$ for L_{ap}) can be obtained, as shown in Fig. 25(a) and (b).

By adding the variations of the maximum AP capacity of each magnetic component (e.g., L_{ap} , L_{as} , T) with H in Fig. 25(b), the variation of the total maximum AP capacity of the magnetic components with H for *CLLC* converter can be obtained, as shown in Fig. 25(c).

Obviously, when $H=0$, the total maximum AP capacity of the magnetic components is minimized, the secondary inductance L_{as} is 0 at this time, and the corresponding design parameters of equivalent D-type *CLLC* are shown in

$$\left\{ \begin{aligned} L_{ap} &= L_p \frac{hk+h+1}{hk+1} = 226.875 \text{ uH} \\ L_{as} &= 0 \\ L_{am} &= \frac{L_p}{k(hk+1)} = 688.754 \text{ uH} \\ N &= \frac{n}{hk+1} = 1.254 \\ C_p &= \frac{1}{Z_r \omega_r} = 21.21 \text{ nF} \\ C_s &= \frac{n^2 C_p}{h} = \frac{n^2}{h Z_r \omega_r} = 42.877 \text{ nF}. \end{aligned} \right. \quad (83)$$

TABLE VIII
KEY DESIGN PARAMETERS OF THE CLLC PROTOTYPE

Components	Parameter/Part#
Primary voltage U_1	400 V
Secondary voltage U_2	250 V–450 V
Primary resonant inductance L_{ap}	226.875 μH
Secondary resonant inductance L_{as}	0
Magnetizing inductance L_{am}	688.754 μH
Primary resonant capacitance C_p	21.21 nF
Secondary resonant capacitance C_s	42.877 nF
Turns ratio N	1.254
Resonant frequency f_r	100 kHz
Switching frequency f_s	50 kHz–200 kHz
Rated power	1 kW
MOSFETs	ROHM SOT3080AL

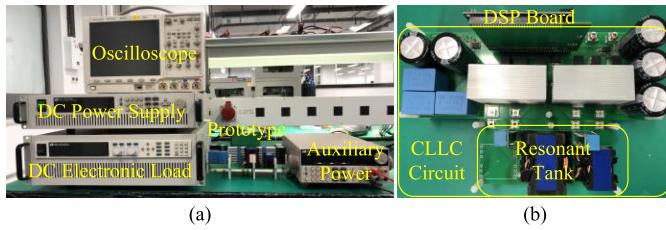


Fig. 26 Experimental environment. (a) Experimental test platform. (b) CLLC prototype.

VI. EXPERIMENTAL RESULTS

To demonstrate the proposed design methodology, a D-type CLLC resonant converter with parameters in (83) was established based on specifications given in Table V. The key circuit components and the semiconductor device are listed in Table VIII. The picture of the prototype is shown in Fig. 26(b), and the corresponding experimental platform is shown in Fig. 26(a).

A. Forward Mode

In the forward charging mode, the dc power supply connected to U_1 is fixed at 400 V, and the electronic load connected to U_2 is programmed to vary from 250–450 V under several load conditions to simulate the charging process.

Fig. 27 illustrated typical waveforms during dead time t_{dead} when CLLC achieve ZVS for forward mode. Where $V_{GSp1}(V_{GSp3})$ is the drive signal of $S_{p1}(S_{p3})$, $V_{GSp4}(V_{GSp2})$ is the drive signal of $S_{p4}(S_{p2})$, $V_{DSp1}(V_{DSp3})$ is the drain-source voltage of $S_{p1}(S_{p3})$, $V_{DSp4}(V_{DSp2})$ is the drain-source voltage of $S_{p4}(S_{p2})$, V_{AB} denotes the inverting voltage of primary side and i_{Cp} indicates the resonant current of C_p . Considering that the drive signals V_{GSp1} and V_{GSp3} are identical, the electrical quantities associated with S_{p1} (e.g., V_{GSp1} , V_{DSp1}) and S_{p3} (e.g., V_{GSp3} , V_{DSp3}) should be identical. Similarly, the electrical quantities associated with S_{p4} (e.g., V_{GSp4} , V_{DSp4}) and S_{p2} (e.g., V_{GSp2} , V_{DSp2}) should be identical too. As shown in Fig. 27, at the beginning of t_{dead} , i_{Cp} starts discharging the C_{oss} of $S_{p1}(S_{p3})$ and charging the C_{oss} of $S_{p4}(S_{p2})$. If $V_{DSp1}(V_{DSp3})$ can decrease to 0 or $V_{DSp4}(V_{DSp2})$ can increase to U_1 before

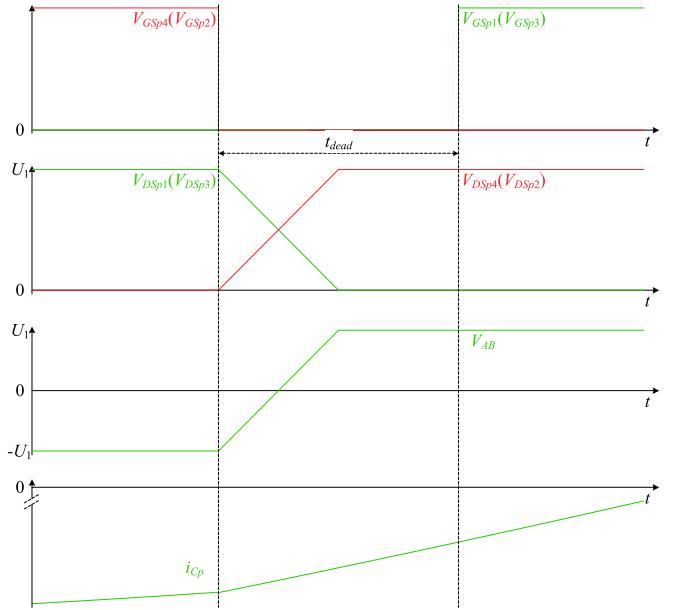


Fig. 27. Typical waveforms during t_{dead} when CLLC achieve ZVS for forward mode.

the ending of t_{dead} , then corresponding antiparallel diodes start to conduct and $S_{p1}(S_{p3})$ can switching with zero voltage at the ending of t_{dead} , which is how the ZVS achieves. While $V_{DSp4}(V_{DSp2})$ increases or $V_{DSp1}(V_{DSp3})$ decreases in t_{dead} , the voltage polarity of V_{AB} is reversing (e.g., from $-U_1$ to U_1) and the relationship among $V_{DSp4}(V_{DSp2})$, $V_{DSp1}(V_{DSp3})$ and U_{AB} are shown in (84). Obviously, If $V_{DSp1}(V_{DSp3})$ can decrease to 0 or $V_{DSp4}(V_{DSp2})$ can increase to U_1 before the ending of t_{dead} , then V_{AB} can reverse the voltage polarity within t_{dead} too. Therefore, this manuscript selects whether V_{AB} can reverse the voltage polarity in t_{dead} as an indication of whether ZVS is achieved or not

$$\begin{cases} V_{DSp4} + V_{DSp1} = U_1 \\ V_{DSp4} - V_{DSp1} = V_{AB} \end{cases} \Rightarrow V_{AB} = U_1 - 2V_{DSp1} = 2V_{DSp4} - U_1. \quad (84)$$

Fig. 28 shows measured voltage and current waveforms of the designed D-type CLLC operating in forward mode at several typical voltage gains with 1 kW load condition. To be consistent with the analysis in Sections III and IV, the voltage gain $M = nU_2/U_1$ in Figs. 28–30 and $M_R = U_1/(nU_2)$ in Fig. 31 and 32 are defined by S-type CLLC parameters in (72). It is not difficult to find that for all typical operating points in Fig. 28, the primary inverting voltage V_{AB} can always reverse the voltage polarity within the dead time t_{dead} . Therefore, ZVS for the inverting side MOSFETs are achieved. Similar waveforms can also be observed in Fig. 29, which shows key waveforms of the prototype operating at several typical voltage gains with 250 W load condition. For zero-load O mode in charging mode, as shown in Fig. 30, except for Fig. 30(e), all typical operating points fully realized ZVS. As the switching frequency continues

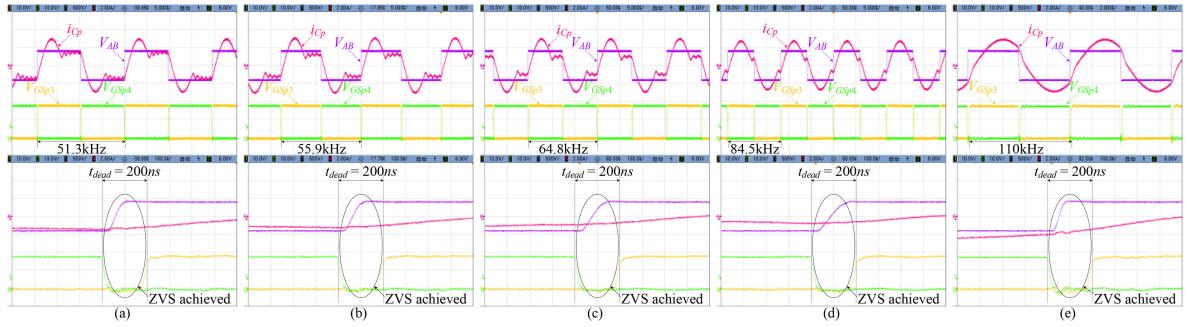


Fig. 28. Key waveforms of the CLLC prototype under 1 kW load condition in forward mode. (a) $U_1 = 400$ V, $U_2 = 450$ V, $M = 1.63125$. (b) $U_1 = 400$ V, $U_2 = 399.37$ V, $M = 1.448$. (c) $U_1 = 400$ V, $U_2 = 348.73$ V, $M = 1.264$. (d) $U_1 = 400$ V, $U_2 = 298.1$ V, $M = 1.08$. (e) $U_1 = 400$ V, $U_2 = 250$ V, $M = 0.90625$.

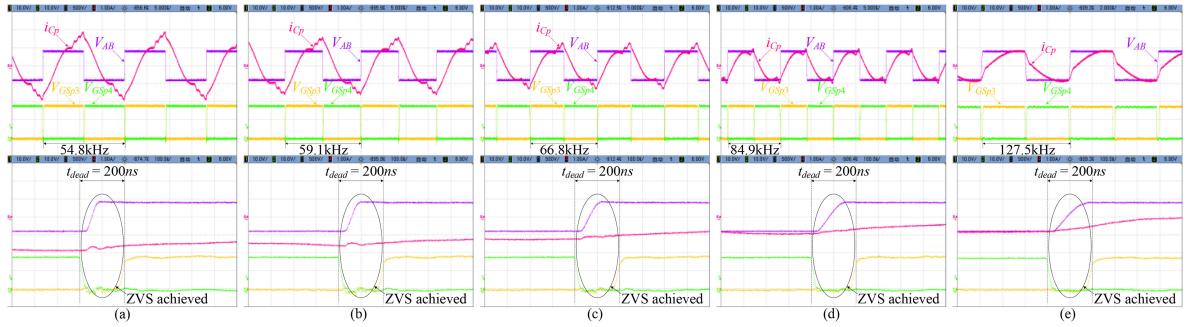


Fig. 29. Key waveforms of the CLLC prototype under 250 W load condition in forward mode. (a) $U_1 = 400$ V, $U_2 = 450$ V, $M = 1.63125$. (b) $U_1 = 400$ V, $U_2 = 399.37$ V, $M = 1.448$. (c) $U_1 = 400$ V, $U_2 = 348.73$ V, $M = 1.264$. (d) $U_1 = 400$ V, $U_2 = 298.1$ V, $M = 1.08$. (e) $U_1 = 400$ V, $U_2 = 250$ V, $M = 0.90625$.

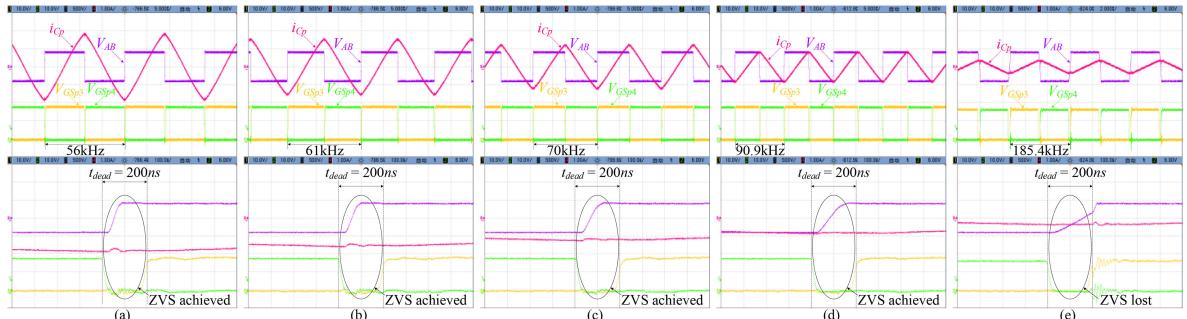


Fig. 30. Key waveforms of the CLLC prototype in forward O mode. (a) $U_1 = 400$ V, $U_2 = 450$ V, $M = 1.63125$. (b) $U_1 = 400$ V, $U_2 = 399.37$ V, $M = 1.448$. (c) $U_1 = 400$ V, $U_2 = 348.73$ V, $M = 1.264$. (d) $U_1 = 400$ V, $U_2 = 298.1$ V, $M = 1.08$. (e) $U_1 = 400$ V, $U_2 = 250$ V, $M = 0.90625$.

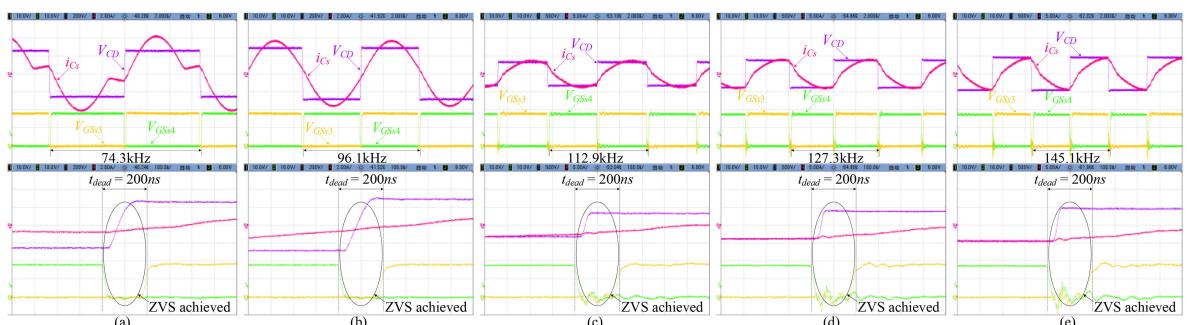


Fig. 31. Key waveforms of the CLLC prototype under 1kW load condition in reverse mode. (a) $U_2 = 250$ V, $U_1 = 400$ V, $M_R = 1.10345$. (b) $U_2 = 281.69$ V, $U_1 = 400$ V, $M_R = 0.979$. (c) $U_2 = 322.6$ V, $U_1 = 400$ V, $M_R = 0.855$. (d) $U_2 = 377.39$ V, $U_1 = 400$ V, $M_R = 0.731$. (e) $U_2 = 450$ V, $U_1 = 400$ V, $M_R = 0.613$.

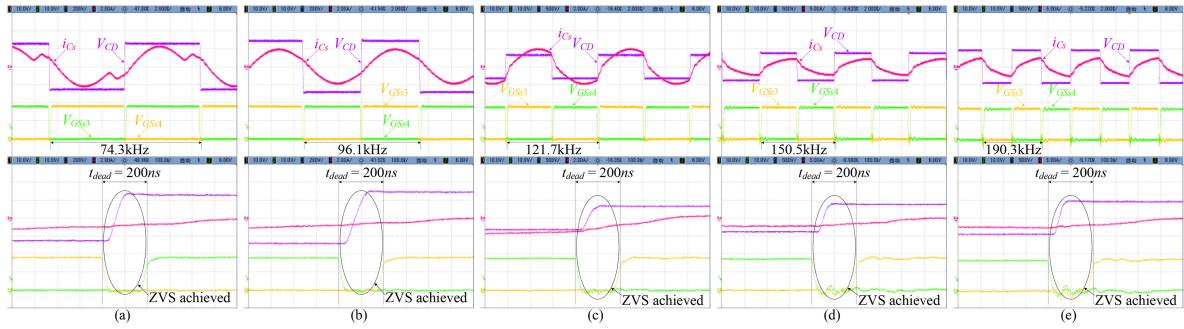


Fig. 32. Key waveforms of the *CLLC* prototype under 500W load condition in reverse mode. (a) $U_2 = 250$ V, $U_1 = 400$ V, $M_R = 1.10345$. (b) $U_2 = 281.69$ V, $U_1 = 400$ V, $M_R = 0.979$. (c) $U_2 = 322.6$ V, $U_1 = 400$ V, $M_R = 0.855$. (d) $U_2 = 377.39$ V, $U_1 = 400$ V, $M_R = 0.731$. (e) $U_2 = 450$ V, $U_1 = 400$ V, $M_R = 0.613$.

to increase, due to the actual device parameters deviate from the design parameters and the existing of corresponding parasitic parameters, the inverting side MOSFETs start to achieve ZVS partly, as shown in Fig. 30(e). By observing the typical waveforms of the forward mode, it is not difficult to conclude that the D-type *CLLC* prototype obtained by the proposed design method is definitely able to achieve the designed voltage gain and ZVS when operating in forward mode within the preset frequency range and under full range of load conditions.

B. Reverse Mode

In the reverse discharging mode, the dc power supply connected to U_2 is programmed to vary from 450–250 V to simulate the discharging process, and the electronic load connected to U_1 is fixed at 400 V under several load conditions.

Fig. 31 shows the key waveforms of the designed D-type *CLLC* operating in reverse mode at several typical voltage gains with 1 kW load condition. It is no difficult to find that ZVS for the inverting side MOSFETs are achieved. Similar waveforms can also be observed in Fig. 32, which shows key waveforms of the prototype operating at several typical voltage gains with 500 W load condition. Therefore, it is not difficult to conclude that the D-type *CLLC* prototype obtained by the proposed design method is definitely able to achieve the designed voltage gain and ZVS within the preset frequency range and under designed range of load conditions when operating in reverse mode.

C. Efficiency Test

Finally, the efficiency curves of the D-type *CLLC* prototype operates in forward and reverse mode under different load conditions and voltage gains are shown in Figs. 33 and 34, respectively. Due to the realization of synchronous rectification refer to our previous research [9], the highest efficiency of the prototype in charging mode and discharging mode are 98.84% and 98.91%, respectively. According to the trend of the efficiency curves in Figs. 33 and 34, the prototype can obtain higher bidirectional efficiency when the voltage gain is around 1 due to operating near the resonance frequency. Besides, when the voltage gains deviate from 1, both the efficiency of charging mode and discharging mode begin to drop gradually.

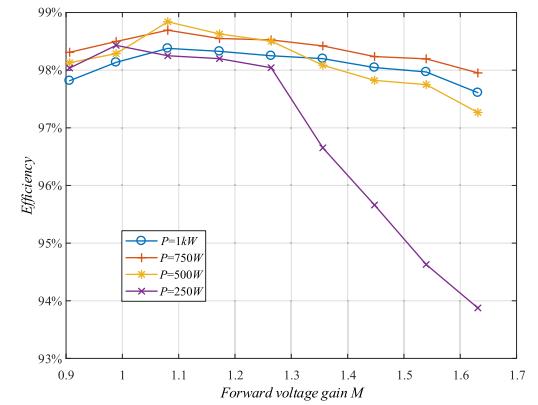


Fig. 33. Efficiency curves of forward operating mode.

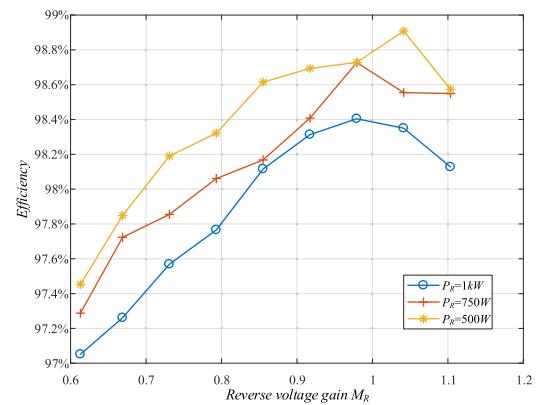


Fig. 34. Efficiency curves of reverse operating mode.

VII. CONCLUSION

This article proposed a novel design methodology for *CLLC* converters. First, based on the port characteristics of the *CLLC* resonant tank, the parameter equivalent principle is presented to convert D-type *CLLC* and S-type *CLLC*. Then, TDM is used to analyze the voltage gain and output characteristics of S-type *CLLC* in forward and reverse modes in typical OBC applications. With the conclusions of TDM analysis, a novel

design methodology is proposed, which can guarantee the required bidirectional voltage gain and ZVS is achieved with the minimum reactive power within the designed frequency range under required load conditions. With the parameters equivalent principle introduced before, a method to minimizes the AP capacity of the magnetic part of the equivalent D-type *CLLC* is provided. Finally, a D-type *CLLC* prototype based on the optimized design parameters was established, the experimental waveforms verified that the designed D-type *CLLC* converter can achieve the required bidirectional voltage gain and ZVS within the preset frequency range under required load conditions.

REFERENCES

- [1] A. Emadi, Y. J. Lee, and K. Rajashekara, "Power electronics and motor drives in electric, hybrid electric, and plug-in hybrid electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2237–2245, Jun. 2008.
- [2] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DC–DC converter for high-frequency-link power-conversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.
- [3] L. Xue, Z. Shen, D. Boroyevich, P. Mattavelli, and D. Diaz, "Dual active bridge-based battery charger for Plug-in hybrid electric vehicle with charging current containing low frequency ripple," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7299–7307, Dec. 2015.
- [4] S. Zou, J. Lu, A. Mallik, and A. Khaligh, "3.3kW CLLC converter with synchronous rectification for plug-in electric vehicles," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, 2017, pp. 1–6.
- [5] Y. Xuan, X. Yang, W. Chen, T. Liu, and X. Hao, "A novel three-level CLLC resonant DC–DC converter for bidirectional EV charger in DC microgrids," *IEEE Trans. Ind. Electron.*, vol. 68, no. 3, pp. 2334–2344, Mar. 2021.
- [6] C. Zhang, P. Li, Z. Kan, X. Chai, and X. Guo, "Integrated half-bridge CLLC bidirectional converter for energy storage systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp. 3879–3889, May 2018.
- [7] R. Emamalipour and J. Lam, "A hybrid string-inverter/rectifier soft-switched bidirectional DC/DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8200–8214, Aug. 2020.
- [8] L. Qu, X. Wang, Z. Bai, and Y. Liu, "Variable CLLC topology structure technique for a bidirectional on board charger of electric vehicle," in *Proc. 4th Int. Conf. Power Renewable Energy*, 2019, pp. 185–189.
- [9] L. Pei *et al.*, "A time-domain-model-based digital synchronous rectification algorithm for CLLC resonant converters utilizing a hybrid modulation," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 2815–2829, Mar. 2022.
- [10] C. Liu, J. Wang, K. Colombage, C. Gould, and B. Sen, "A CLLC resonant converter based bidirectional EV charger with maximum efficiency tracking," in *Proc. 8th IET Int. Conf. Power Electron., Mach. Drives*, 2016, pp. 1–6.
- [11] B. Li, Q. Li, F. C. Lee, Z. Liu, and Y. Yang, "A high-efficiency high-density wide-bandgap device-based bidirectional on-board charger," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1627–1636, Sep. 2018.
- [12] W. Chen, P. Rong, and Z. Lu, "Snubberless bidirectional DC–DC converter with new CLLC resonant tank featuring minimized switching loss," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3075–3086, Sep. 2010.
- [13] J. Jung, H. Kim, M. Ryu, and J. Baek, "Design methodology of bidirectional CLLC resonant converter for high-frequency isolation of DC distribution systems," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1741–1755, Apr. 2013.
- [14] Z. Lv, X. Yan, Y. Fang, and L. Sun, "Mode analysis and optimum design of bidirectional CLLC resonant converter for high-frequency isolation of DC distribution systems," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 1513–1520.
- [15] J. Huang *et al.*, "Robust circuit parameters design for the CLLC-Type DC transformer in the hybrid AC–DC microgrid," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 1906–1918, Mar. 2019.
- [16] B. Zhao, X. Zhang, and J. Huang, "AI algorithm-based two-stage optimal design methodology of high-efficiency CLLC resonant converters for the hybrid AC–DC microgrid applications," *IEEE Trans. Ind. Electron.*, vol. 66, no. 12, pp. 9756–9767, Dec. 2019.
- [17] J. Huang, X. Zhang, and B. Zhao, "Simplified resonant parameter design of the asymmetrical CLLC-type DC transformer in the renewable energy system via semi-artificial intelligent optimal scheme," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1548–1562, Feb. 2020.
- [18] J. Huang, X. Zhang, and Z. Zhang, "Three-step switching frequency selection criteria for the generalized CLLC-Type DC transformer in hybrid AC–DC microgrid," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 980–991, Feb. 2020.
- [19] J. Huang, X. Zhang, and C. Wen, "Two-stage parameter design methodology of a generalized resonant DC transformer in hybrid AC/DC microgrid with optimum active power transmission," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2313–2325, Sep. 2020.
- [20] J. Huang, X. Zhang, A. Zhang, and P. Wang, "Comprehensive coordinated frequency control of symmetrical CLLC-DC transformer in hybrid AC/DC microgrids," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10374–10384, Oct. 2020.
- [21] Y.-F. Wang, B. Chen, Y. Hou, Z. Meng, and Y. Yang, "Analysis and design of a 1-MHz bidirectional Multi-CLLC resonant DC–DC converter with GaN devices," in *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1425–1434, Feb. 2020.
- [22] T. Zhu, F. Zhuo, F. Zhao, F. Wang, H. Yi, and T. Zhao, "Optimization of extended phase-shift control for full-bridge CLLC resonant converter with improved light-load efficiency," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 11129–11142, Oct. 2020.
- [23] Z. U. Zahid, Z. M. Dalala, R. Chen, B. Chen, and J. -S. Lai, "Design of bidirectional DC–DC resonant converter for Vehicle-to-Grid (V2G) applications," *IEEE Trans. Transp. Electrific.*, vol. 1, no. 3, pp. 232–244, Oct. 2015.
- [24] J. Min and M. Ordóñez, "Bidirectional resonant CLLC charger for wide battery voltage range: Asymmetric parameters methodology," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6662–6673, Jun. 2021.
- [25] J. Sun, L. Yuan, Q. Gu, R. Duan, Z. Lu, and Z. Zhao, "Design-Oriented comprehensive time-domain model for CLLC class isolated bidirectional DC–DC converter for various operation modes," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3491–3505, Apr. 2020.
- [26] S. Ditzé, "Steady-state analysis of the bidirectional CLLC resonant converter in time domain," in *Proc. IEEE 36th Int. Telecommun. Energy Conf.*, 2014, pp. 1–9.



Lie Zhao (Student Member, IEEE) was born in Shaanxi, China, in 1996. He received the B.S. degree from Northwestern Polytechnical University, Xi'an, China, in 2017, and the M.S. degree in 2020 from Xi'an Jiaotong University, Xi'an, China, where he is currently working toward the Ph.D. degree all in electrical engineering.

His current research interests include power electronics, resonant power conversion, and bidirectional dc–dc converters.



Yunqing Pei (Member, IEEE) was born in 1969. He received the B.S. and M.S. degrees in electrical engineering, and the Ph.D. degree in power electronics all from Xi'an Jiaotong University, Xi'an, China, in 1991, 1994, and 1999, respectively.

He is currently a Professor with Xi'an Jiaotong University. From February 2006 to February 2007, he was a Visiting Scholar with the Center of Power Electronics Systems, Virginia Polytechnic Institute and State University. His research interests include on the high-power inverters, switch mode power supply, and converters in distributed generation systems.

Dr. Pei was a faculty member with Xi'an Jiaotong University.



Laili Wang (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an, China, in 2004, 2007, and 2011, respectively.

Since 2011, he has been a Postdoctoral Research Fellow with the Department of Electrical Engineering, Queen's University, Kingston, ON, Canada. From 2014 to 2017, he was an Electrical Engineer with Sumida, Kingston, ON, Canada. In 2017, he was a Full Professor with Xi'an Jiaotong University. His research interests include wide bandgap power

devices, package and integration, high density power conversion, wireless power transfer, and energy harvesting.

Dr. Wang is the recipient of Outstanding Young Scholar Award from China Power Supply Society (CPSS), China Electric Power Excellent Young Technological Talent Award from Chinese Society of Electrical Engineering. He is currently an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He is the Co-Chair of System Integration and Application in International Technology Roadmap for Wide Band-Gap Power Semiconductor, and the Chair of CPSS and IEEE Power Electronics Society Joint Chapter in Xi'an, China.



Long Pei (Student Member, IEEE) was born in Hunan, China, in 1995. He received the B.S. degree in electrical automatization in 2018 from Xi'an Jiaotong University, Xi'an, China, where he is currently working toward the Ph.D. degree in electrical engineering and automation.

His research interests include design and control of dc–dc resonant power converters and power factor correction ac–dc converters.



Wei Cao was born in Hebei, China, in 1998. He received the B.S. degree from Northwestern Polytechnical University, Xi'an, China, in 2020. He is currently working toward the Ph.D. degree with Xi'an Jiaotong University, Xi'an, China, all in electrical engineering.

His current research interests include high frequency resonant converters, wide range dc–dc conversion, and control technique.



Yongmei Gan (Member, IEEE) was born in 1971. She received the B.S. and M.S. degrees in control engineering from the Xi'an University of Technology, Xi'an, China, in 1993 and 1996, respectively, and the Ph.D. degree in control theory and control engineering from Northwestern Polytechnical University, Xi'an, in 1999.

Since 2000, she has been with the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an, China, where she is currently an Associate Professor. From February 2008 to February 2009, she was a Visiting Scholar of the Electrical and Computer Engineering, University of Toronto. Her research interests include package and integration of wide-bandgap power semiconductor devices, energy harvesting, and supervisory control of discrete-event systems.