	Cycle 0	Cycle 1	Cycle 2	Cycle 3
MULT Reg0	B * F	E * Reg3	Reg3 * Reg0	DONT CARE
MULT Reg1	DONT CARE	A * E	Reg1 * Reg2	DONT CARE
ALU Reg2	DONT CARE	Reg3 + (Reg0 /4)	DONT CARE	DONT CARE
ALU Reg3	C + D	A + Reg0	DONT CARE	Reg0 - Reg1
Reg2 has a 2 bit shifter on second operand				