

# Paging / Segmentation - Exercises

Logical Addresses:

- 64 Pages of 1024 bytes

Physical Memory:

- 32 Frames

a) How many bits in the logical address

$$2^6 \times 2^{10} = 2^{16} \quad \text{R.: 16 bits}$$

b) How many bits in the physical address

5 bits to address the frames  
10 bits to the frame offset  
Total: 15 bits

Page and frame typically have the same size.

32 bit logical address  $2^5$

4KB page size  $2^{12}$  bytes  $2^9$

512 MB physical memory  $2^{32}$  bytes

a) # entries normal 1 lvl page table

$$\frac{2^{32}}{2^{12}} = 2^{20} \quad \text{32 bits}$$

$$\frac{2^{28}}{2^{12}} = 2^{16}$$

200 m for memory references  
a) 100 ns  $\rightarrow$  1 to hit the table + 1 for the needed instruction  
b) How with TLB, 3% of all references are found in the TLB, which the memory reference time?

$$T = (T_{hit} \times T_{TLB} + T_{miss} \times T_{TLB})$$

$$= 0.75 \times (100 + 0.15 \times 100) + 100 \times 100 = 100 + 100 = 200 \text{ ns}$$

$$128 \text{ KB} = 2^{17} \text{ bits}$$

Exercise 2

Physical Memory  $\rightarrow$  256 MBytes  $\rightarrow 2^8 \times 2^{23} = 2^{31}$

Virtual Memory  $\rightarrow$  2 GBytes  $\rightarrow 2 \times 2^{30} = 2^{31}$

Logical address:

Number of pages	Offset
20 bits	2 bits

• Max number of pages:  $2^{20}$

• Size of each page:  $\frac{2^{34}}{2^{20}} = 2^{14} = 2 \times 2^{13} = 2 \text{ KB}$

• PTE occupies 8 bytes

$\hookrightarrow$  Max size of table of pages:  $2^{20} \times 2^6 = 2^{26} = 8 \text{ MB}$

If inverted  $\Rightarrow$  Capped to physical memory size

$$\frac{2^{31}}{2^{14}} = 2^{17} \quad 2^{17} \times 2^6 = 2^{23} \text{ bits}$$

$$\frac{2^{26}}{2^{14}} = 2^{12} = 4096$$

32 bit logical addresses

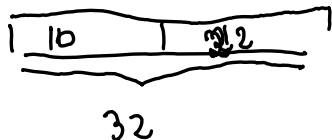
1024 entries 128 frames

} LRU Page replacement algorithm

char A[2\*1024\*1024]

for (int i=0; i < sz(A); ++i) A[i]=0

$\log_2 1024 = 10 \rightarrow$  bits for addressing



1 Page Fault

$$2^{22} = 2^2 \times 2^{10} \times 2^{10}$$

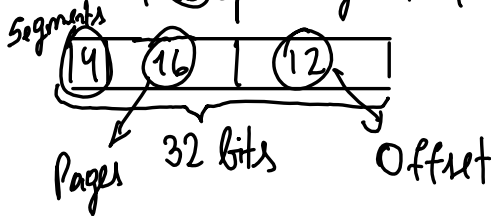
Size of the page

⑥ Segmentation + Paging → 4 bits to address them

Virtual Address: 32 bits

PTE: 4 bytes

⑥ equal segments | Each page has 4KB  
2<sup>12</sup> bytes



a) R:  $2^{32} = 4GB$

b) 4, 16, 12

c)  $2^{16} \times 2^2 = 2^{18} \text{ bytes} = 256KB$

d)  $\frac{2^{18}}{2^{12}} = 2^6 \text{ Pages}$

// Segmentation //

a)  $\begin{array}{r} 430 \\ + 219 \\ \hline 649 \end{array}$  b) 2310 c) Illegal Reference  $\Rightarrow$  Trap to OS

d)  $\begin{array}{r} 1927 \\ + 400 \\ \hline 1727 \end{array}$

// Demanding Paging //

Page Fault  $\begin{cases} 8ms \rightarrow \text{Replaced page not modified} \\ 20ms \rightarrow \text{Replaced page modified} \end{cases}$  MAT = 100 ns

Page to be replaced if modified 75% of the time

What's the maximum acceptable page fault rate for an effective access time of no more than 200 ns?

$$EAT = (1-p) \times MAT + p \times (0.3 \times 8000000 \text{ ns} + 0.7 \times 20000000 + 100)$$

$$\Rightarrow 200 = (1-p) \times 100 + p \times 16400100$$

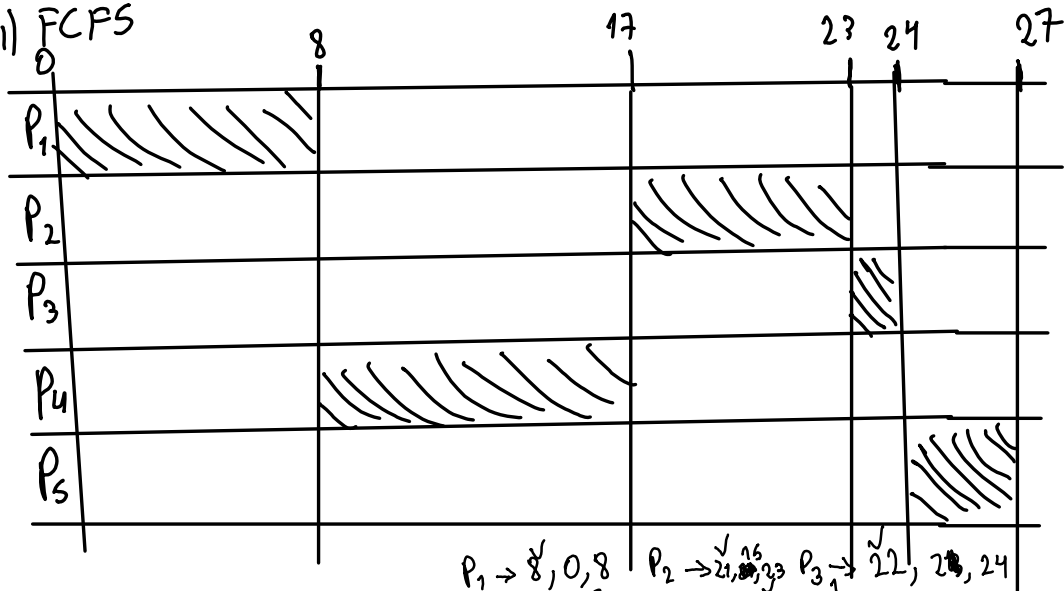
$$\Rightarrow 200 = 100 - 100p + 16400100p$$

$$\Rightarrow 100 = 16400100p$$

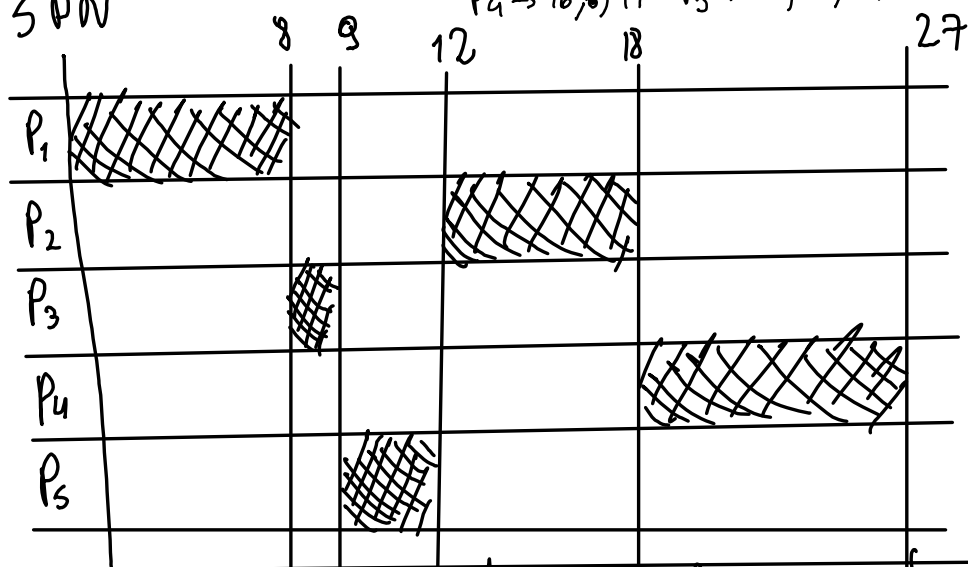
$$\Rightarrow p = \frac{1}{164001}$$

# Scheduling Exercises

(i) FCFS



SPN










	$P_1$	$P_2$	$P_3$	$P_4$	$P_5$
WT	0	10	6	17	6
TT	8	16	7	26	9

	8	14	23	24	27
P <sub>1</sub>					
P <sub>2</sub>					
P <sub>3</sub>					
P <sub>4</sub>					
P <sub>5</sub>					
WT	P <sub>1</sub> 0	P <sub>2</sub> 6	P <sub>3</sub> 21	P <sub>4</sub> 13	P <sub>5</sub> 21
TT	8	12	22	22	24

	0	1	2	8	17	20	27
✓ P <sub>1</sub>							
✓ P <sub>2</sub>							
✓ P <sub>3</sub>							
✓ P <sub>4</sub>							
✓ P <sub>5</sub>							
		P <sub>1</sub>		P <sub>2</sub>	P <sub>3</sub>	P <sub>4</sub>	P <sub>5</sub>
WT		19		0	6	7	14
TT		27		6	7	16	17



0	1,5	2,5	4,5	6,5	10,5	15	20	
$P_1$								$WT = 9$ $TT = 15$
$P_2$								$WT = 1$ $TT = 5$
$P_3$								$WT = 3$ $TT = 7$
$P_4$								$WT = 0$ $TT = 1$
$P_5$								$WT = 8,5$ $TT = 13,5$

$P_1$	
$P_2$	
$P_3$	
$P_4$	
$P_5$	

MAX - ALLOCATION

← what we will need

	A	B	C	D	
P <sub>1</sub>	0	0	0	0	✓
P <sub>2</sub>	0	7	5	0	X
P <sub>3</sub>	1	0	0	2	✓
P <sub>4</sub>	0	0	2	0	✓
P <sub>5</sub>	0	6	4	2	✓

Available: [1, 5, 2, 0]

→ [1, 5, 3, 2] → ✓  
 → [2, 8, 8, 6]  
 → [2, 14, 11, 8]  
 → [2, 14, 12, 12]

a) Safe State Sequence: P<sub>1</sub>, P<sub>3</sub>, P<sub>4</sub>, P<sub>5</sub>, P<sub>2</sub>

b) ALLOC

	A	B	C	D
P <sub>1</sub>	0	0	1	2
P <sub>2</sub>	1	4	2	0
P <sub>3</sub>	1	3	5	4
P <sub>4</sub>	0	6	3	2
P <sub>5</sub>	0	0	1	4

NEED

	A	B	C	D
P <sub>1</sub>	0	0	0	0
P <sub>2</sub>	0	3	3	0
P <sub>3</sub>	1	0	0	2
P <sub>4</sub>	0	0	2	0
P <sub>5</sub>	0	6	4	2

AVAILABLE: [1, 5, 2, 0]

R: YES

A	loc	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	R <sub>4</sub>
P <sub>1</sub>		0	0	1	0
P <sub>2</sub>		0	0	1	1
P <sub>3</sub>		2	0	0	1
P <sub>4</sub>		0	1	2	0

Vector Available

R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	R <sub>4</sub>
2	1	0	0

→ [2, 2, 2, 0]

→ [2, 2, 3, 0]

Req	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	R <sub>4</sub>
<del>P<sub>1</sub></del>	<del>1</del>	<del>0</del>	<del>2</del>	<del>0</del>
P <sub>2</sub>	2	0	0	1
P <sub>3</sub>	1	0	1	1
<del>P<sub>4</sub></del>	<del>2</del>	<del>1</del>	<del>0</del>	<del>0</del>

R: {P<sub>2</sub>, P<sub>3</sub>}

[2\*, 1\*, 3\*]  
 4 2\* 1\*  
 2\* 4 2  
 1

Page faults: 1111111111

Swap-Outs: 111111