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CS 1555 HW 7

1)

a)

With respect to x:

H1: W2(x)->R1(x)->R3(x)->W1(x)

H2: W2(x)->W1(x)->R3(x)->R1(x)

So H1 and H2 cannot be conflict equivalent because they differ for R3(x)->W1(x) versus W1(x)->R3(x).

H3: W2(x)->W1(x)->R1(x)->R3(x)

H2 and H3 are conflict equivalent so far… (both the W2 and W1 writes will happen with respect to x before either of the R1(x) or R3(x); R1(x) and R3(x) do not conflict and can be safely swapped, leading to identical histories with respect to x).

H4: W1(x)->R3(x)->W2(x)->R1(x).

H4 cannot be conflict equivalent to any of H1-H3 (because the leading W1(x) breaks conflict equivalence with any of the three others)

With respect to y:

H1: W2(y)->R3(y)

H2: W2(y)->R3(y)

H3: W2(y)->R3(y)

H4: R3(y)->W2(y)

So H2-H3 remain conflict equivalent with respect to y; H4 further cannot be conflict equivalent to the others.

With respect to z:

H1: R3(z)->R2(z)

H2: R3(z)->R2(z)

H3: R2(z)->R3(z)

H4: R2(z)->R3(z)

Read-only produce no conflicts, so H2-H3 remain conflict equivalent with respect to z.

**Only H2 and H3 are conflict equivalent.**

b)

SG(H1):

T2->T1 (due to W2(x), R1(x))

T3->T1 (due to R3(x), W1(x))

T2->T3 (due to W2(y), R3(y) and W2(x), R3(x))

**So T2->T3->T1 is the equivalent serial history:**

**W2(x)R2(z)W2(y)R3(z)R3(x)R3(y)R1(x)W1(x)**

SG(H2):

T2->T1 (due to W2(x), W1(x))

T2->T3 (due to W2(x), R3(x))

T1->T3 (due to W1(x), R3(x))

So **T2->T1->T3** **is the equivalent serial history:**

**W2(x)W2(y)R2(z)W1(x)R1(x)R3(x)R3(z)R3(y)**

SG(H3):

T2->T1 (due to W2(x), W1(x))

T2->T3 (due to W2(x), R3(x))

T1->T3 (due to W1(x), R3(x))

So **T2->T1->T3** **is the equivalent serial history:**

**W2(y)W2(x)R2(z)W1(x)R1(x)R3(y)R3(x)R3(z)**

SG(H4):

T3->T2 (due to R3(y), W2(y))

T1->T3 (due to W1(x), R3(x))

T2->T1 (due to W2(x), R1(x))

T3->T2->T1->T3 is a cycle, so **NOT SERIALIZABLE**

2)

1.5 ms-> go to sector 3, 1.5ms-> to sector 2, 1.5ms -> to sector 1, 1.5 ms-> to sector 0

6 ms total.