A guide to using FETs for voltage controlled circuits, Part 2

- 26 January 2018
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This article looks at applying feedback in basic VCR circuits, and improving distortion reduction circuits.

In Part 1 of this five-part series, we examined FET voltage controlled resistors, basic voltage controlled resistor circuits, and a balanced or push pull voltage controlled resistor (VCR) circuit. Next, let's take a look at an N-Channel JFET attenuator circuit with feedback (**Figure 8**).

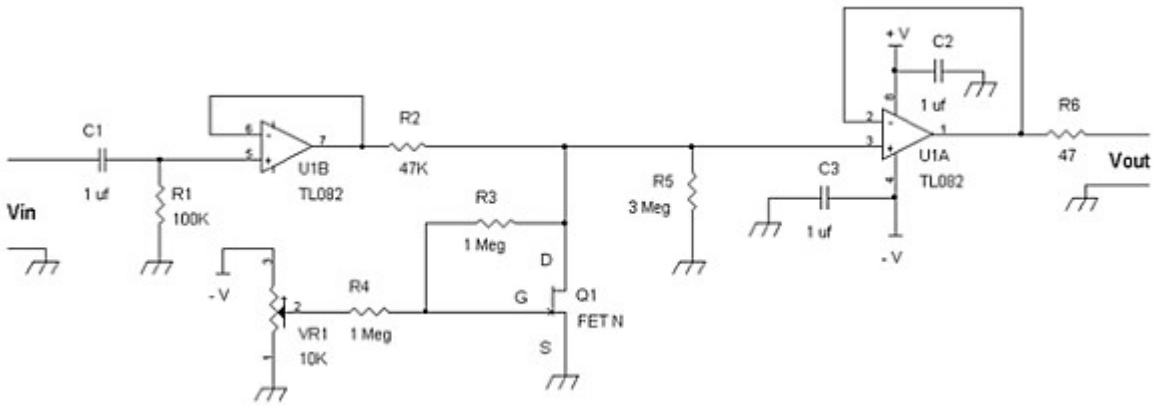

Figure 8 Feedback resistors R3 and R4 provide distortion reduction.

If we refer back to Figure 2 in Part 1, for a voltage controlled resistor without feedback resistors, we see that for VDS > 0 volt, the resistance is higher than when VDS < 0 volts via the S1 and S2 slopes.

Intuitively, if VDS > 0 volt or positive in **Figure 8**, a portion of VDS (voltage across the drain and source of Q1) positive voltage via R3 gets added to the gate voltage. This makes the gate less negative when combined with VR1's slider voltage, which means that the drain to source resistance drops for VDS > 0 volt.

When VDS < 0 volt, there is additional negative voltage added to the gate via R3, which makes the gate voltage more negative resulting in higher resistance across the drain and source of Q1.

Therefore, the resistances at VDS > 0 volt and VDS < 0 volt become closer in value using the feedback resistor network R3 and R4, which will then reduce distortion.

Note that when R3 = R4, R3 and R4 provide half of the VDS voltage back to gate. Let's see why this is good for cancelling out distortion.

Let's take a look at the drain current equation (1):

$$I_d = I_{DSS}\left[2\left(1 - \frac{Vgs}{Vp}\right)\left(\frac{Vds}{-Vp}\right) - \left(\frac{Vds}{Vp}\right)\left(\frac{Vds}{Vp}\right)\right] \quad (1)$$

We will want to eliminate the terms related to (V_{DS}/V_P) (V_{DS}/V_P) so that the conductance (g_{ds}) is only a function of V_{GS} when we take the derivative of I_d with respect to V_{ds}. For a linear conductance, we still want a V_{ds} term in the drain current equation that is multiplied by a constant or a factor related to a control voltage.

Let $V_{gs} = Vc + k\,V_{ds}$, where Vc is the control voltage, $0 < k < 1$, and k is the feedback factor.

This leads to:

$$I_d = I_{DSS}\left[2\left(1 - \frac{Vc + kVds}{Vp}\right)\left(\frac{Vds}{-Vp}\right) - \left(\frac{Vds}{Vp}\right)\left(\frac{Vds}{Vp}\right)\right]$$

$$I_d = I_{DSS}\left[2\left(1 - \frac{Vc + kVds}{Vp}\right)\left(\frac{Vds}{-Vp}\right)\right] - I_{DSS}\left(\frac{Vds}{Vp}\right)\left(\frac{Vds}{Vp}\right)$$

$$I_d = I_{DSS}\left[2\left(1 - \frac{Vc}{Vp} - \frac{kVds}{Vp}\right)\left(\frac{Vds}{-Vp}\right)\right] - I_{DSS}\left(\frac{Vds}{Vp}\right)\left(\frac{Vds}{Vp}\right)$$

$$I_d = I_{DSS}\left[2\left(1 - \frac{Vc}{Vp}\right)\left(\frac{Vds}{-Vp}\right)\right] + I_{DSS}\left[2\left(-\frac{kVds}{Vp}\right)\left(\frac{Vds}{-Vp}\right)\right] - I_{DSS}\left(\frac{Vds}{Vp}\right)\left(\frac{Vds}{Vp}\right) \quad (7)$$

We would like to set the last two terms to cancel each other, that is:

$$I_{DSS}\left[2\left(-\frac{kVds}{Vp}\right)\left(\frac{Vds}{-Vp}\right)\right] - I_{DSS}\left(\frac{Vds}{Vp}\right)\left(\frac{Vds}{Vp}\right) = 0$$

$$I_{DSS}\left[2\left(\frac{kVds}{Vp}\right)\left(\frac{Vds}{Vp}\right)\right] - I_{DSS}\left(\frac{Vds}{Vp}\right)\left(\frac{Vds}{Vp}\right) = 0$$

Or alternatively,

$$I_{DSS}\left[2\left(\frac{kVds}{Vp}\right)\left(\frac{Vds}{Vp}\right)\right] = I_{DSS}\left(\frac{Vds}{Vp}\right)\left(\frac{Vds}{Vp}\right)$$

If we divide both sides by I_{DSS}, and then multiply both sides by (V_p) (V_p), we get:

$$2(kVds)(Vds) = (Vds)(Vds)$$

Dividing by (V_{ds})(V_{ds}) on both sides and solving for k we get

$2k = 1$

$k = 1/2$

For the feedback resistors R3 and R4

$k = 1/2 = R4/(R3 + R4)$

This means R3 = R4 for a feedback factor of $k = 1/2$.

With V_{gs} = Vc + kVds

$k = 1/2$

$k = 0.5$

Vgs = Vc + $0.5\ Vds$

Now let's go back to equation (7)

$$I_d = I_{DSS}\left[2\left(1 - \frac{Vc}{Vp}\right)\left(\frac{Vds}{-Vp}\right)\right] + I_{DSS}\left[2\left(-\frac{kVds}{Vp}\right)\left(\frac{Vds}{-Vp}\right)\right] - I_{DSS}\left(\frac{Vds}{Vp}\right)\left(\frac{Vds}{Vp}\right) \quad (7)$$

With $k = 1/2$, the last two terms disappear in equation (7).

$$I_d = I_{DSS}\left[2\left(1 - \frac{Vc}{Vp}\right)\left(\frac{Vds}{-Vp}\right)\right] \quad (8)$$

$$g_{ds} = \frac{d}{dVds} I_d = \frac{d}{dVds} I_{DSS}\left[2\left(1 - \frac{Vc}{Vp}\right)\left(\frac{Vds}{-Vp}\right)\right] \quad (9)$$

$$g_{ds} = I_{DSS}\left[2\left(1 - \frac{Vc}{Vp}\right)\left(\frac{1}{-Vp}\right)\right]$$

$$g_{ds} = I_{DSS}\left[-2\left(\frac{1}{Vp}\right)\left(1 - \frac{Vc}{Vp}\right)\right] \quad (10)$$

$$R_{ds} = 1/g_{ds} = 1/\{I_{DSS}\left[-2\left(\frac{1}{Vp}\right)\left(1 - \frac{Vc}{Vp}\right)\right]\}$$

$$R_{ds} = 1/\{I_{DSS}\left[-2\left(\frac{1}{Vp}\right)\left(1 - \frac{Vc}{Vp}\right)\right]\} \quad (11)$$

With a given Vp and I_{DSS}, equation (11) then shows that the drain to source resistance R_{ds} is only dependent on the control voltage V_C and without any dependence on V_{ds}. Thus, using the feedback resistors R3 and R4, on a first approximation, provides a linear voltage controlled resistor.

Figure 9 shows a P-Channel JFET version with feedback resistors to lower distortion.

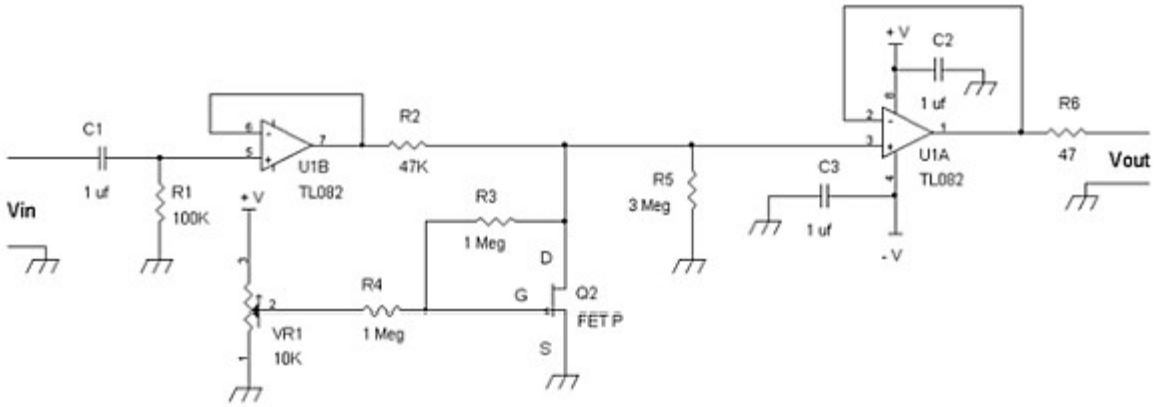

Figure 9 An example P-Channel voltage controlled resistor circuit with a feedback resistor network R3 and R4 to lower distortion.

If you will note that in **Figures 8 and 9**, the feedback resistor network uses high resistance values to allow the FET's (e.g., Q1 and Q2 in **Figures 8 and 9**) drain to source resistance to dominate in forming the voltage divider with R2.

For example, if R3 and R4 = 22KΩ, then there will be approximately a 44KΩ resistor in parallel with the R5 and the FET's drain to source resistance. This 2KΩ resistance will then "wash" out some of the FET's R_{ds} effects. This will not allow the input signal, Vin, to pass substantially unattenuated when the FET is at cut-off (e.g., at infinite resistance) with R2 = 47KΩ.

Using a feedback network to reduce distortion can also be applied to enhancement mode MOSFETs (**Figure 10**).

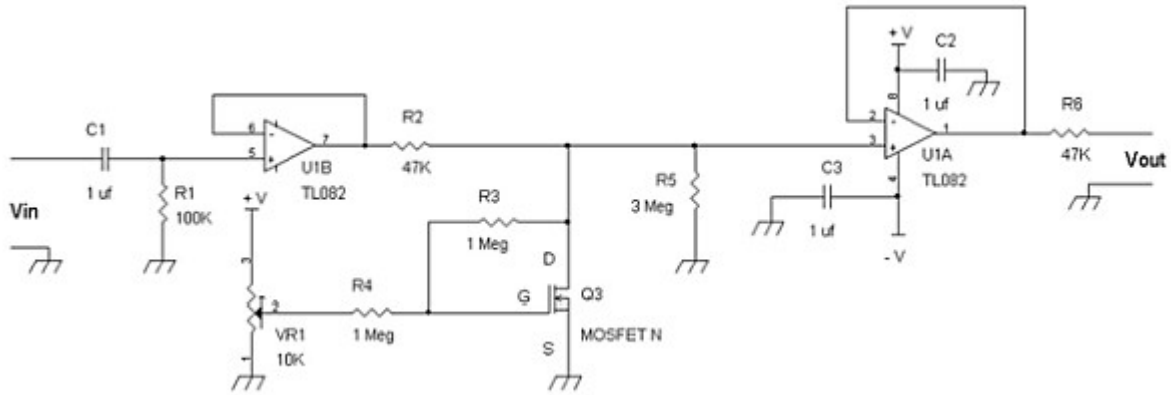

Figure 10 An N-Channel MOSFET voltage controlled attenuator circuit with a feedback network to reduce distortion.

As shown in Appendix A, the feedback network, R3 and R4 should be equal resistance for cancelling distortion for enhancement devices. However, in some cases, the distortion reduction worked even better with a buffer amplifier (e.g., **Figure 14**).

A P-Channel version is shown in **Figure 11**.

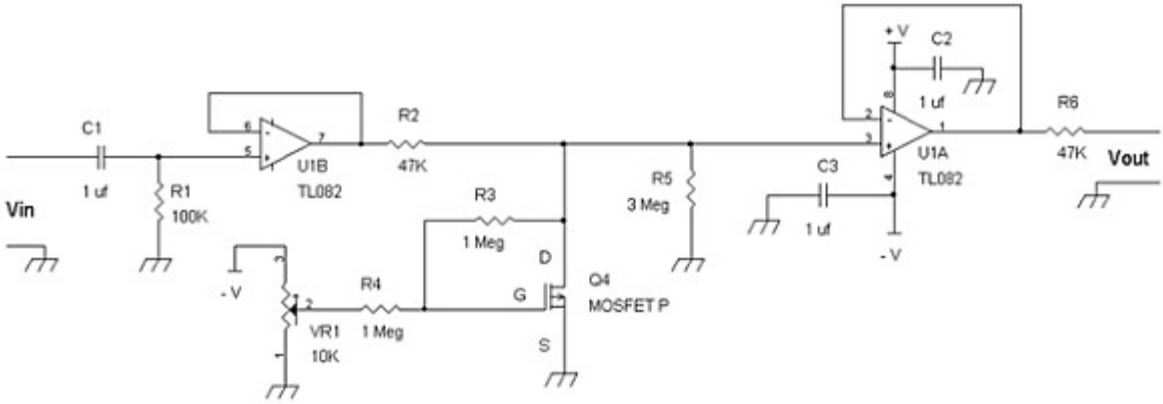

Figure 11 A P-Channel MOSFET voltage controlled attenuator with distortion reduction network R3 and R4.

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