21/10/21

POA
TT-1

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TE COMPS A4

Q1 a Compute (-16)*(-29) using Booth's Restoring Multiplication Algorithm.

ANS

$-16 * -29$

$(-16)_{10} = (110000)_2$

$(-29)_{10} = (100011)_2$

Let M = -29 = $(100011)_2$

Q = -16 = $(110000)_2$

Taking 2's complement of $(-29)_{10}$ = 011100 [1's complement

+ 1

$-M$ = 011101

N	A	Q	Q_{-1}	OPERATION
6	000000	110000	0	Initialization
	000000	011000	0	ARS
5	000000	001100	0	ARS
4	000000	000110	0	ARS
3	000000	000011	0	ARS
2	000000	000011	0	A-M
	+ 011101			
	011101	000011	0	ARS
	001110	100001	1	

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N	A	Q	Q_{-1}	OPERATION
7	000111	010000	1	ARS

$\therefore$ Result = $(000111\ 010000)_2$

= $(464)_{10}$

$\therefore (-29)_{10} \times (-16)_{10} = (464)_{10}$

$(100011)_2 \times (110000)_2 = (000111\ 010000)_2$.

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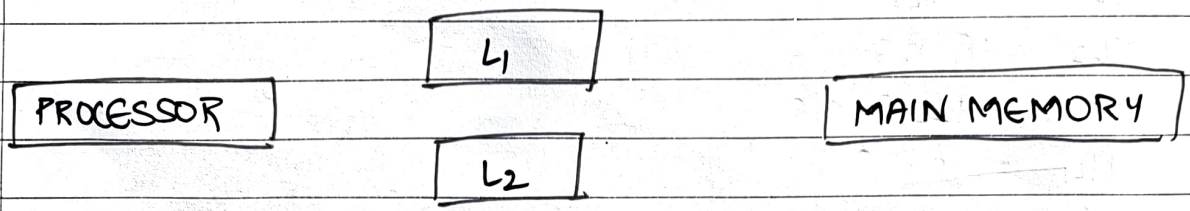
Q2



L_1 and L_2 are in parallel. So their average time is

$$(T_{avg})_1 = H_{L_1} + T_{L_1} + (1 - H_{L_1}) T_{L_2}$$

Let us replace L_1 and L_2 cache with a single block

All three are in series
Average time is cache consist of 2 blocks

$$\therefore (T_{avg})_2 = H_{cache} (T_{avg})_1 + (1 - H_{cache}) ((T_{avg})_1 + T_{MM})$$

$1 - H_{cache}$ = Hit ratio of main memory
$1 - H_{cache} = H_{MM}$
$1 - H_{MM} = H_{cache}$

$$\therefore (T_{avg})_2 = (1 - H_{MM}) (T_{avg})_1 + H_{MM} ((T_{avg})_1 + T_{MM})$$

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$T_{L1} = 15$ ns

$T_{L2} = 18$ ns

$T_{MM} = 1225$ ns

$H_{L1} = 0.75$

$H_{L2} = 0.95$

$H_{L3} = 0.65$

$\therefore T_{avg} = H_{L1} \times T_{L1} + (1 - H_{L1}) T_{L2}$

$= 0.75 \times 15 + (1 - 0.75) 18$

$= 0.75 \times 15 + 0.25 \times 18$

$= 11.25 + 4.5$

$= 15.75$ ns

$(T_{avg})_2 = (1 - H_{MM}) T_{avg.} + H_{MM} (T_{avg} + T_{MM})$

$= 0.35 \times 15.75 + 0.65 (15.75 + 1225)$

$= 5.5125 + 806.4875$

$= 812$ ns

$\therefore$ Average Memory Access Time = 812 ns.

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Q3 Differentiate between Von Neumann and Harvard Architecture

ANS

VON NEUMANN	HARVARD
• It is an ancient computer architecture based on stored program computer concept.	• It is modern computer architecture based on Harvard Mark I relay based model
• same physical memory address is used for instructions and data	• separate physical memory address is used for instructions and data
• there is a common bus for data and instruction transfer	• separate buses are used for transferring data and instruction.
• two clock cycles are required to execute single instruction	• An instruction is executed in a single cycle
• It is cheaper in cost	• It is costlier than Von Neumann Architecture
• CPU cannot access instructions and read/write at the same time.	• CPU can access instructions and read/write at the same time.
• It is used in personal computers and small computers	• It is used in micro controllers and signal processing.

Q4 b A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

a] calculate the number of bits in each of the Tag, Block, and word fields of the memory address

ANS Block size = 64 bytes
$= 2^6$ bytes
$= 2^6$ words [$\because$ 1 byte = 1 word]

$\therefore$ Number of bits in word field = 6

Cache size = 2K-byte
$= 2^{11}$ bytes

Number of cache blocks = Cache size $\div$ Block size
$= 2^{11} \div 2^6$
$= 2^5$

$\therefore$ Number of bits in the block fied = 5

Total number of address bits = 16

$\therefore$ Number of bits in the tag field = 16 - 6 - 5
= 5

$\therefore$ Number of bits in tag field = 5
Number of bits in block field = 5
Number of bits in word field = 6