

DE

JUNAID GIRKAR

24.09.2020

EXPERIMENT NO: 3

60004190057

→ AIM: To verify the truth table of half adder and full adder by using EX-OR and NAND gates respectively

→ THEORY:

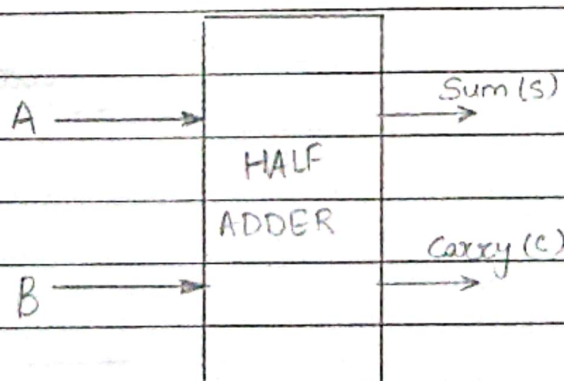
1 HALF ADDER: Half adder is a combinational circuit that performs simple addition of two binary numbers

* TRUTH TABLE:

• If we assume A & B as the two bits whose addition is to be performed, truth table for half adder with A, B as inputs and sum, carry as outputs can be tabulated as follows

• The sum output of the binary addition carried out above is similar to that of an EX-OR operation while carry output is similar to that of an AND operation.

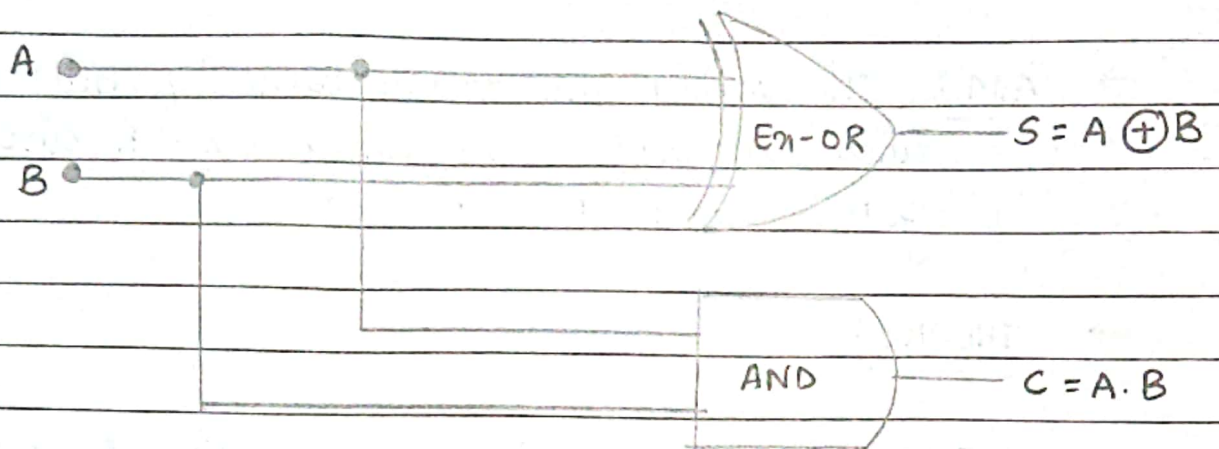
BLOCK DIAGRAM



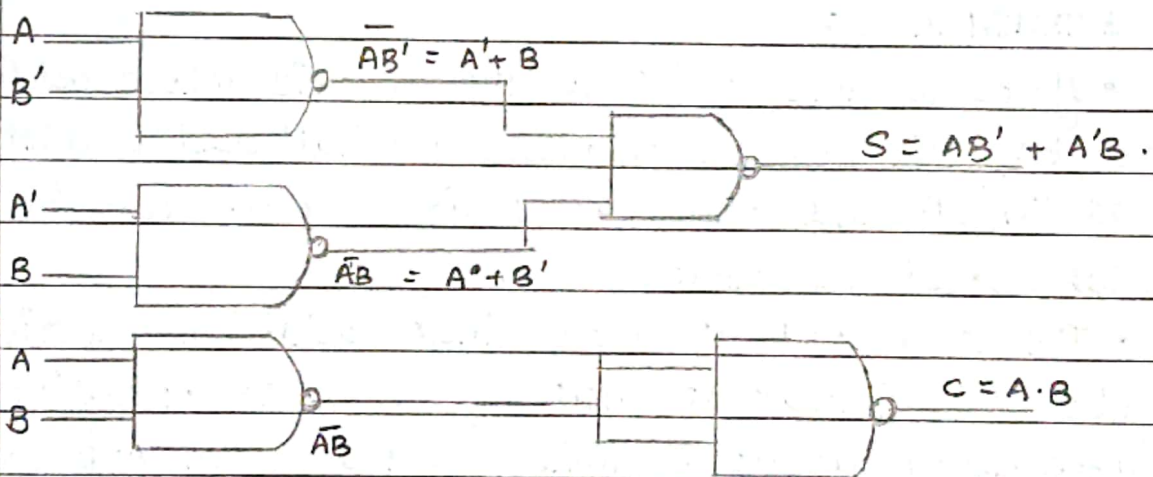
TRUTH TABLE

INPUT		OUTPUT	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

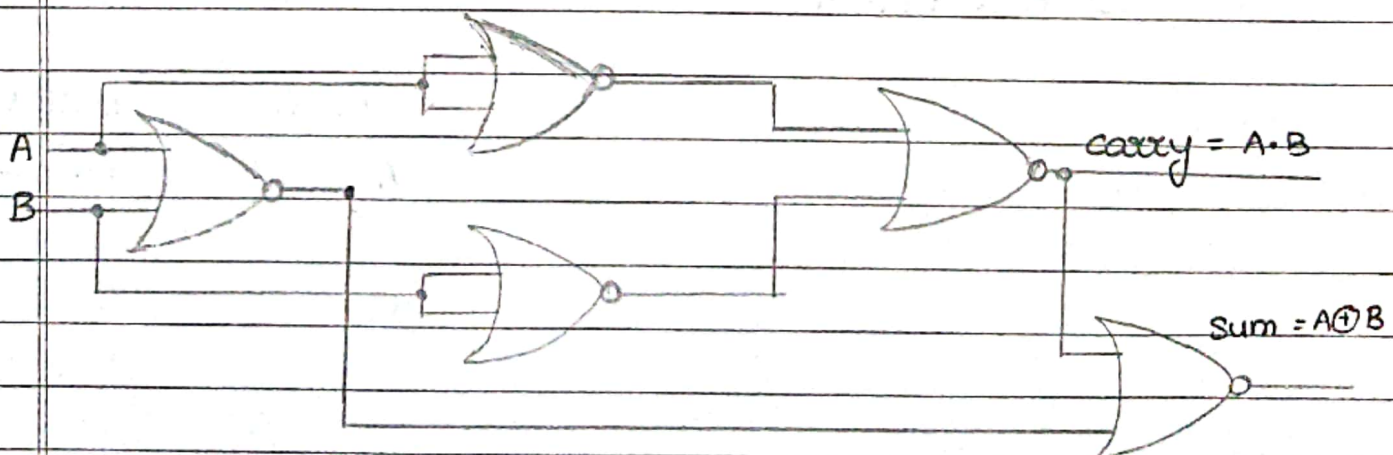
* HALF - ADDER LOGIC DIAGRAM :



* HALF - ADDER USING NAND GATES :



* HALF ADDER USING NOR GATES :

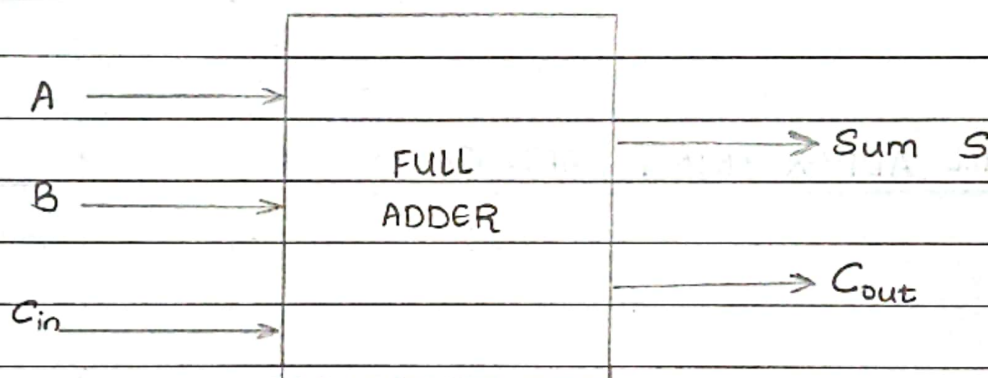


II FULL ADDER : Full adder is a digital circuit used to calculate the sum of three binary bits.

* TRUTH TABLE :

• Two of the three bits are same as before which are A and B. The additional is carry bit from the previous stage and is called carry : represented by C_{in} . It calculates sum of three bits along with carry. The output carry is called C_{out} .

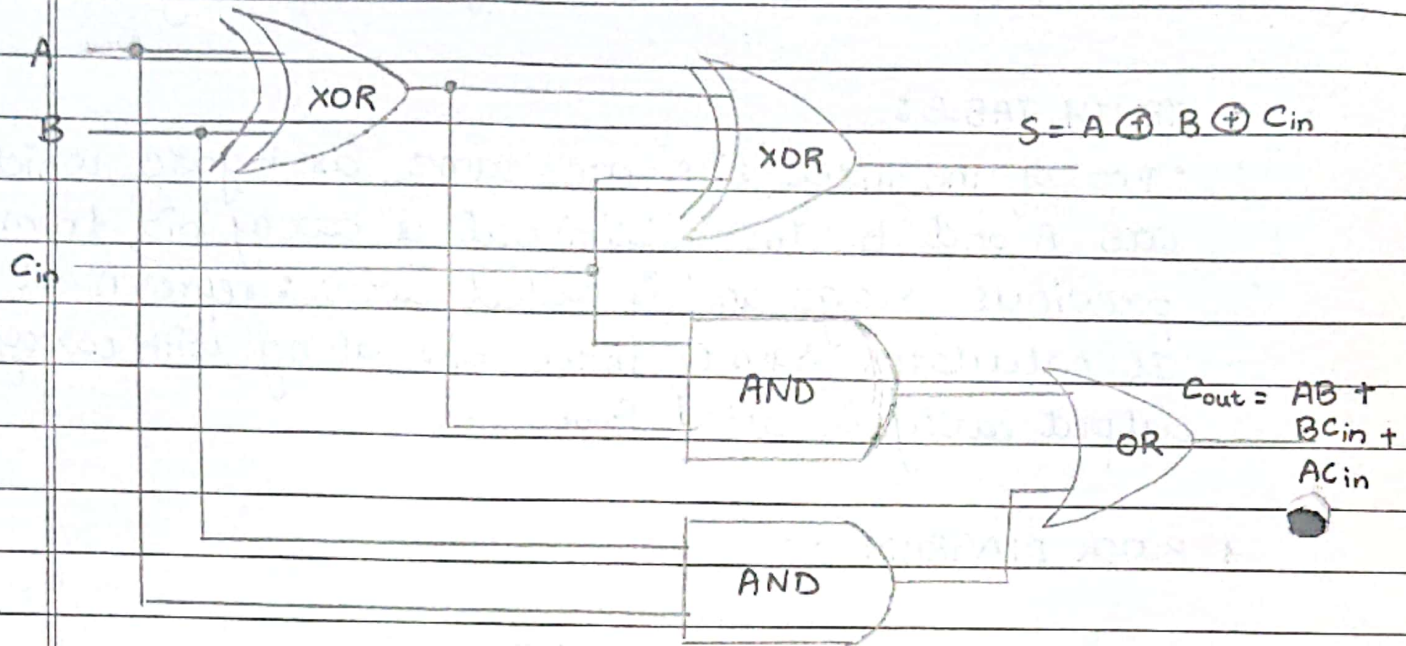
* BLOCK DIAGRAM :



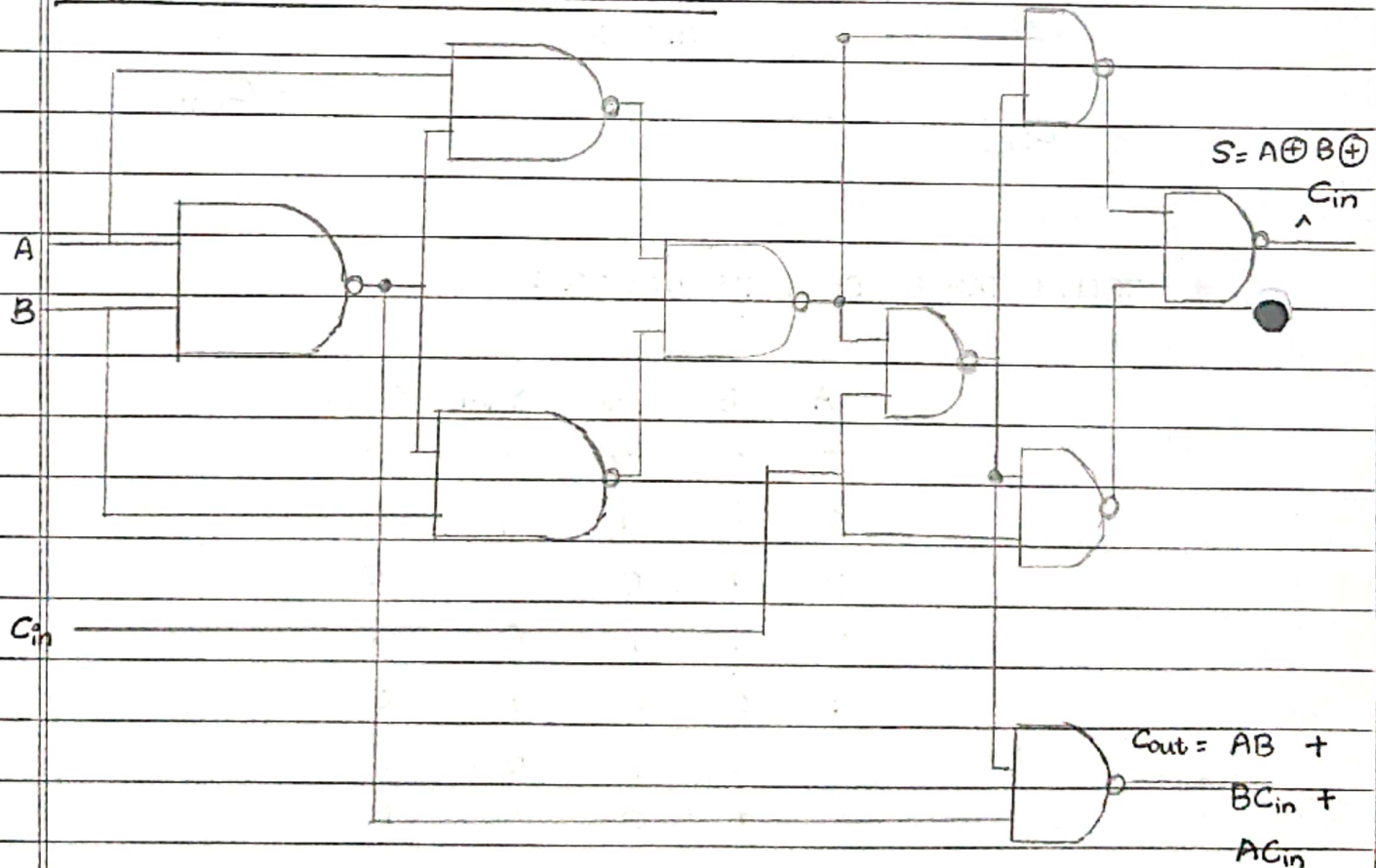
* TRUTH TABLE OF FULL ADDER :-

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

* FULL ADDER LOGIC DIAGRAM:



* FULL ADDER USING NAND GATES



* FULL ADDER USING NOR GATES

$$C_{out} = AB + BC_{in} + AC_{in}$$

