Instructions

4-Bit Synchronous Parallel Counter using J-K Flip-Flop

Print

Q1

Q0

Q2

Q3

| 1K | 1Q | 1Q̄ | GND | 2K | 2Q | 2Q̄ | 2J |
| 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 |

CLEAR · K · CLOCK · J · Q̄ · Q

CLEAR · J · CLOCK · K · Q̄ · Q

IC 7476

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 1CK | 1PR | 1CLR | 1J | VCC | 2CK | 2PR | 2CLR |

| 1K | 1Q | 1Q̄ | GND | 2K | 2Q | 2Q̄ | 2J |
| 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 |

CLEAR · K · CLOCK · J · Q̄ · Q

CLEAR · J · CLOCK · K · Q̄ · Q

IC 7476

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 1CK | 1PR | 1CLR | 1J | VCC | 2CK | 2PR | 2CLR |

Q3 Q2 Q1 Q0

Switch

16

Negatively Triggered Clock

Clock pulse
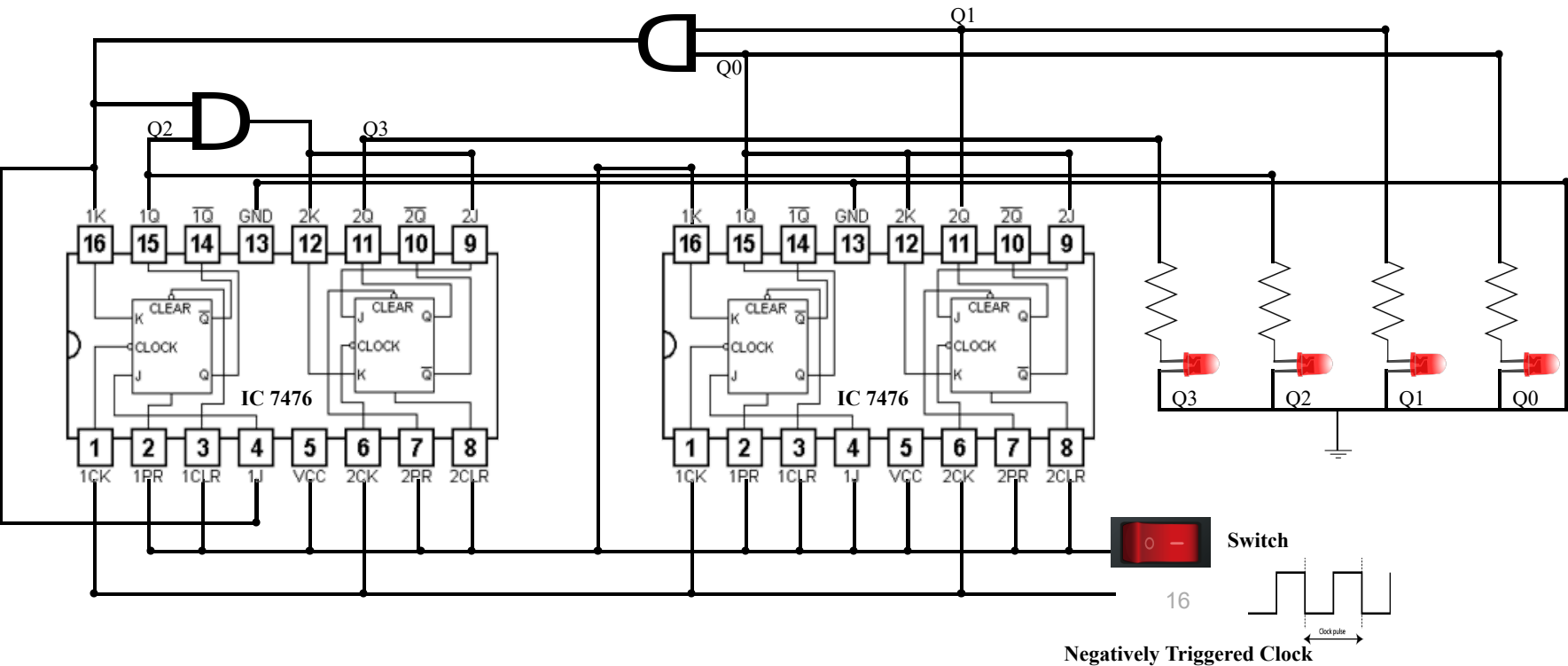
TRUTH TABLE

Serial No.	Clock	Q3	Q2	Q1	Q0
1	1	0	0	0	0
2	2	0	0	0	1
3	3	0	0	1	0
4	4	0	0	1	1

TIMING DIAGRAM

Generate Waveform

Timing Diagram

CLK

Trial Version 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16   CanvasJS.com

Q0
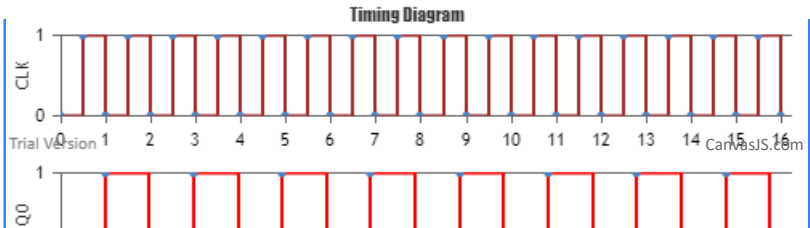
5	5	0	1	0	0
6	6	0	1	0	1
7	7	0	1	1	0
8	8	0	1	1	1
9	9	1	0	0	0
10	10	1	0	0	1
11	11	1	0	1	0
12	12	1	0	1	1
13	13	1	1	0	0
14	14	1	1	0	1
15	15	1	1	1	0
16	16	1	1	1	1