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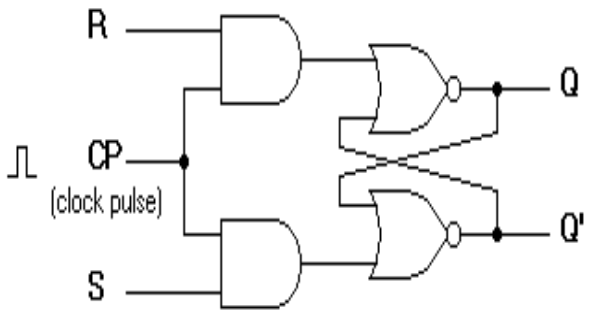
PRACTICAL NO: 8

A flip flop is an electronic circuit with two stable states that can be used to store binary data. The stored data can be changed by applying varying inputs. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.

Let's look at the types of flip-flops to understand better.

SR Flip Flop

There are majorly 4 types of flip flops, with the most common one being SR flip flop. This simple flip flop circuit has a set input (S) and a reset input (R). In this circuit when you Set "S" as active the output "Q" would be high and "Q‵" will be low. Once the outputs are established, the wiring of the circuit is maintained until "S" or "R" go high, or power is turned off.

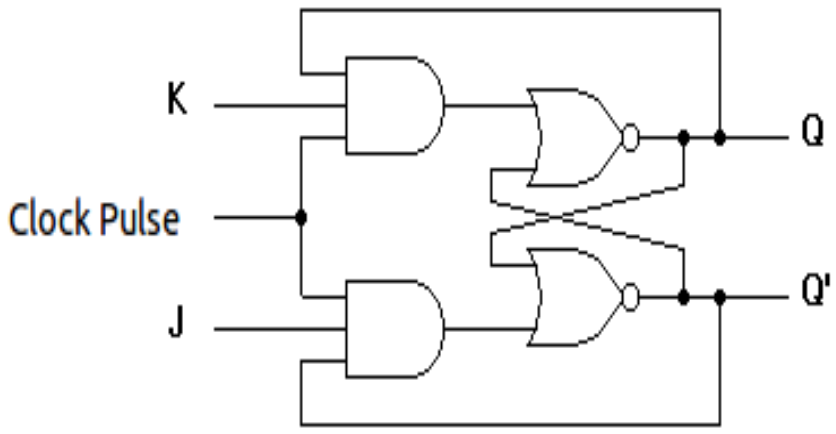


As shown above, it is the simplest and easiest to understand. The two outputs, as shown above, are the inverse of each other. The truth table of SR Flip Flop is highlighted below.

INPUTS			OUTPUT	STATE
CLK	S	R	Q	
X	0	0	No Change	Previous
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	-	Forbidden

JK Flip-flop

Due to the undefined state in the SR flip flop, another flip flop is required in electronics. The JK flip flop is an improvement on the SR flip flop where S=R=1 is not a problem.



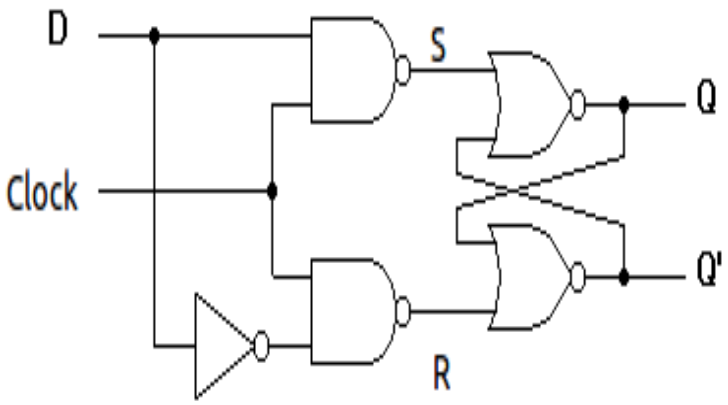
The input condition of J=K=1, gives an output inverting the output state. However, the outputs are the same when one tests the circuit practically.

Trigger	Inputs		Output				Inference
			Present State		Next State		
CLK	J	K	Q	Q'	Q	Q'	
⊠	x	x	-		-		Latched
⊓	0	0	0	1	0	1	No Change
⊓			1	0	1	0	
⊓	0	1	0	1	0	1	Reset
⊓			1	0	0	1	
⊓	1	0	0	1	1	0	Set
⊓			1	0	1	0	
⊓	1	1	0	1	1	0	Toggles
⊓			1	0	0	1	

In simple words, If J and K data input are different (i.e. high and low) then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K are both high at the clock edge then the output will toggle from one state to the other. JK Flip Flop can function as Set or Reset Flip flop

D Flip Flop

D flip flop is a better alternative that is very popular with digital electronics. They are commonly used for counters and shift-registers and input synchronisation.



In a D flip flop, the output can be only changed at the clock edge, and if the input changes at other times, the output will be unaffected.

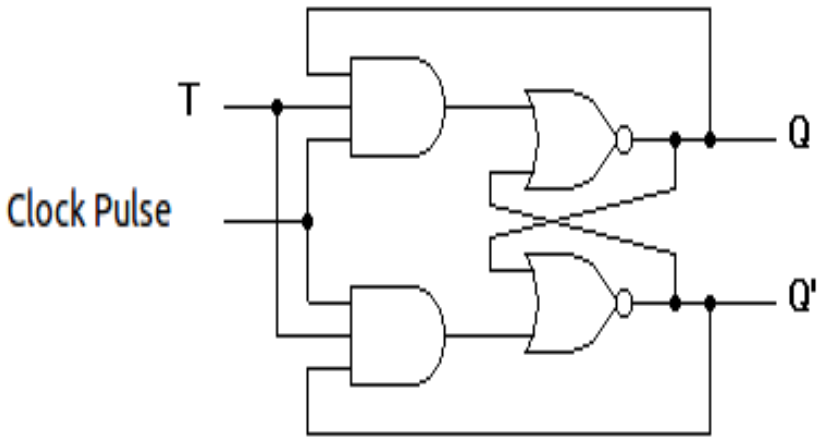
Figure-3:Circuit diagram of D flip flop

Input			Output	
D	reset	clock	Q	Q’
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

The change of state of the output is dependent on the rising edge of the clock. The output (Q) is same as the input and can only change at the rising edge of the clock.

T Flip Flop

A T flip flop is like JK flip-flop. These are basically a single input version of JK flip flop. This modified form of JK flip-flop is obtained by connecting both inputs J and K together. This flip-flop has only one input along with the clock input.



These flip-flops are called T flip-flops because of their ability to complement its state (i.e.) Toggle, hence the name Toggle flip-flop.

T flip-flop

T	Clock	Q	Q'
0	↑	Q	Q'
1	↑	Q'	Q
X	↓	Q	Q'

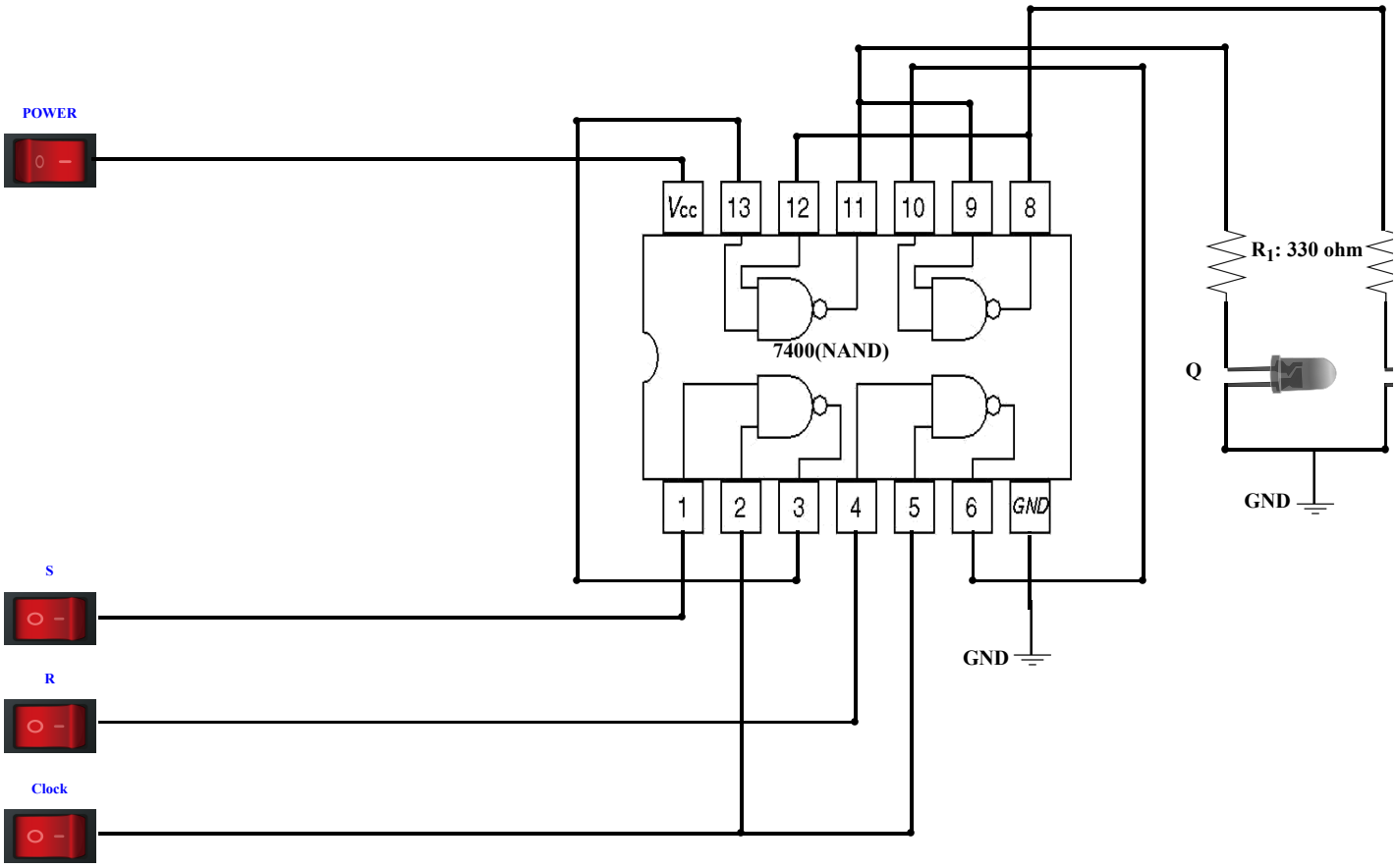
Applications of Flip-Flops

These are the various types of flip-flops being used in digital electronic circuits and the applications of Flip-flops are as specified below.

- Counters
- Frequency Dividers
- Shift Registers
- Storage Registers

INSTRUCTIONS

Experiment to perform SR Flip Flop on kit



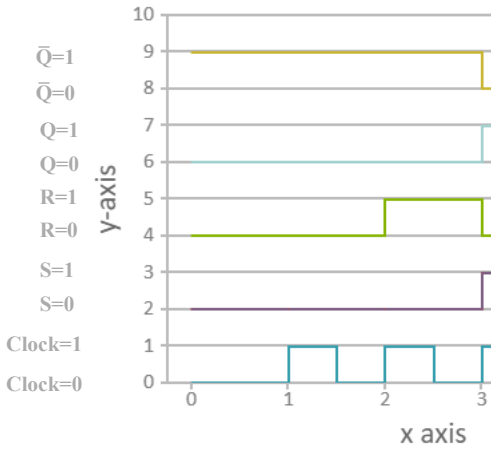
TRUTH TABLE

PRINT

Add

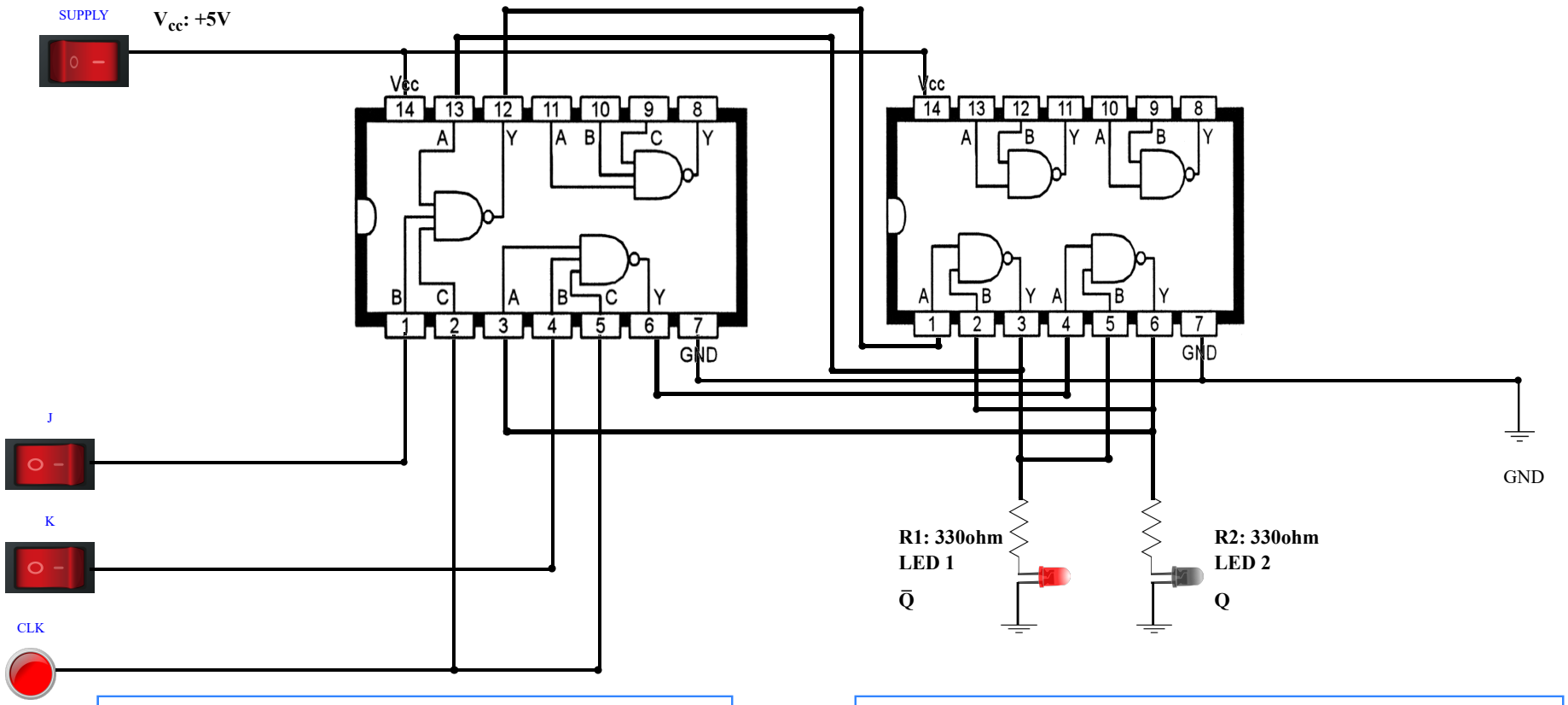
Serial No.	clock	S	R	Q(n-1)	$\bar{Q}$(n-1)	Q	$\bar{Q}$	Remark
1	0	0	0	X	X	0	1	No Change
2	1	0	0	0	1	0	1	No change
3	1	0	1	0	1	0	1	Reset
4	1	1	0	0	1	1	0	set
5	1	1	1	1	0	0	0	INVALID

CLOCK DIAGRAM



INSTRUCTIONS

Experiment to perform logic of JK FLIP FLOP on kit



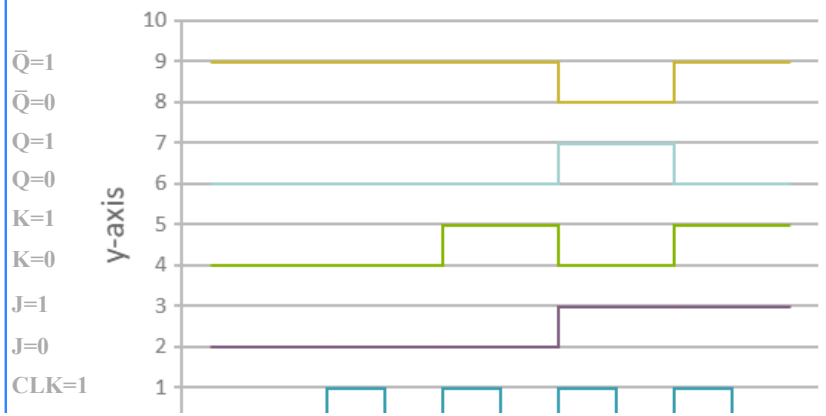
TRUTH TABLE

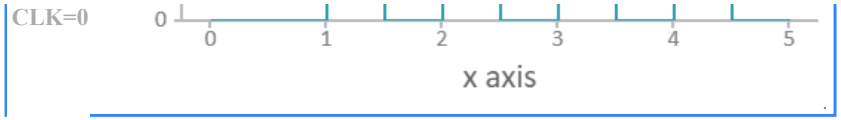
PRINT

Add

Serial No.	clock	J	K	Q(n-1)	Q̄(n-1)	Q	Q̄	Remark
1	0	0	0	X	X	0	1	No Change
2	1	0	0	0	1	0	1	No change
3	1	0	1	0	1	0	1	Reset
4	1	1	0	0	1	1	0	set
5	1	1	1	1	0	0	1	toggle

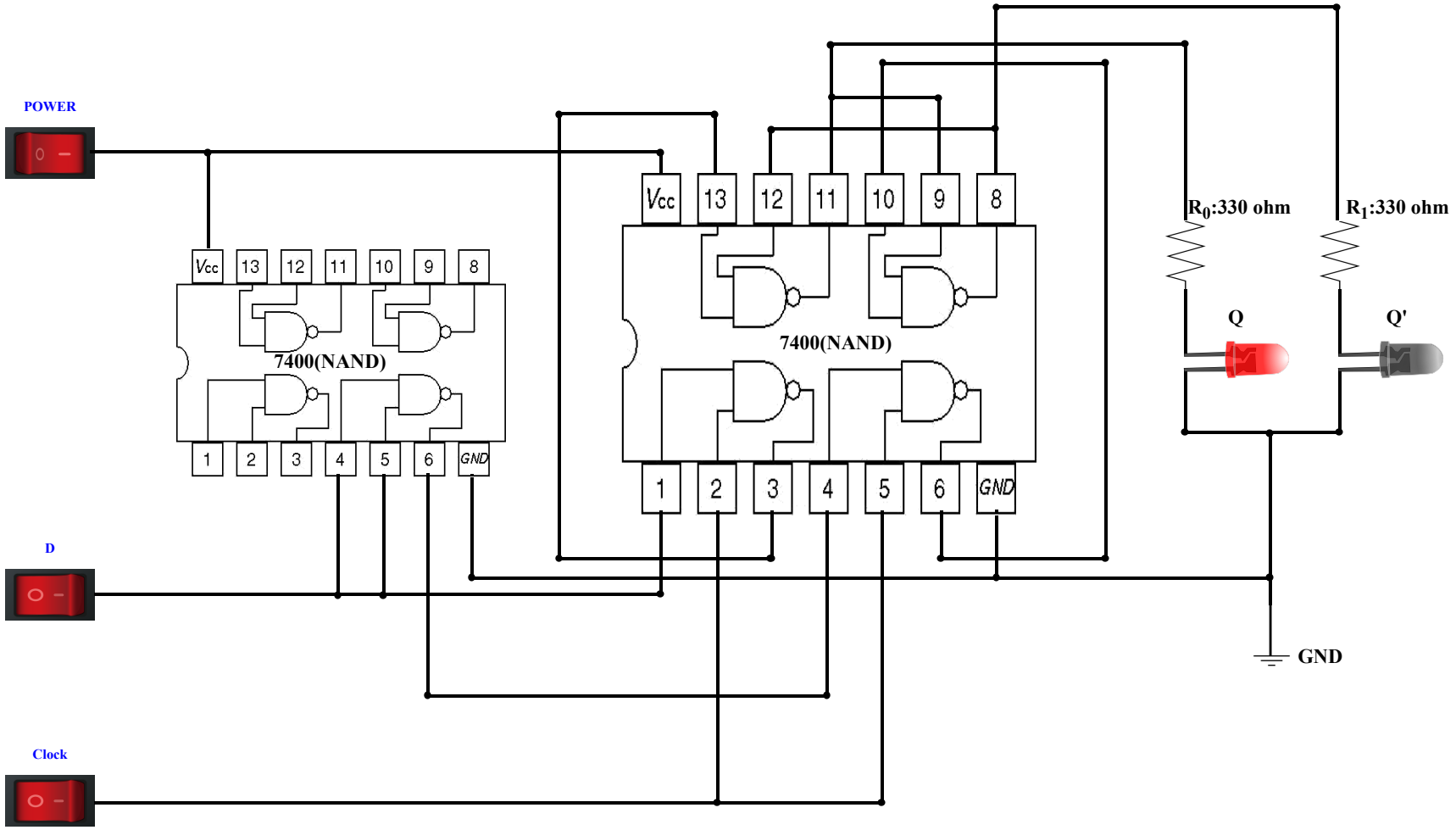
CLOCK DIAGRAM




CLK=0
0
0
1
2
3
4
5
x axis

INSTRUCTIONS

Experiment to perform logic of D - Flipflop on kit

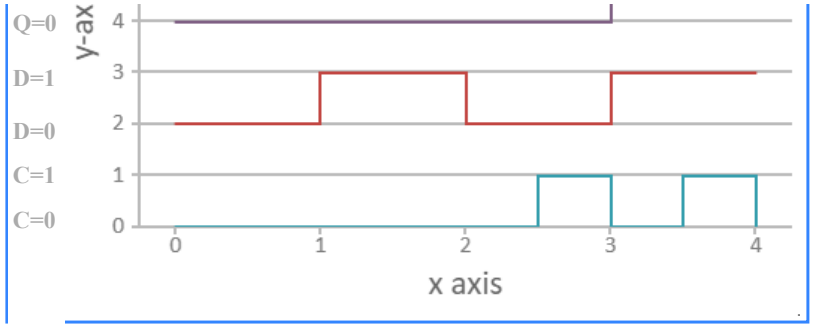


TRUTH TABLE

PRINT Add

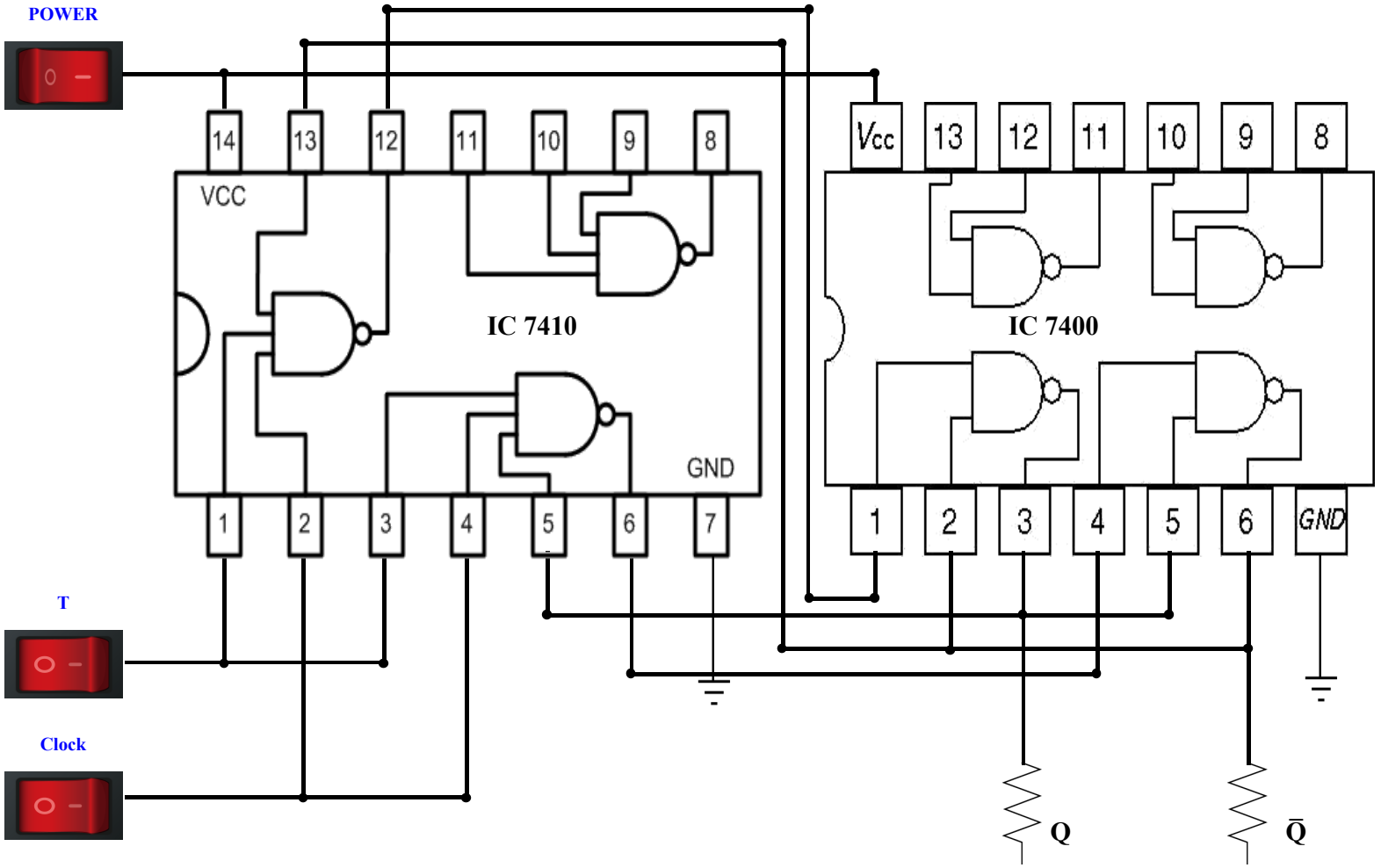
Serial No.	clock	D	Q(n-1)	Q'(n-1)	Q	Q'	Remark
1	0	0	X	X	0	1	No Change
2	0	1	0	1	0	1	No change
3	1	0	0	1	0	1	Reset
4	1	1	0	1	1	0	set

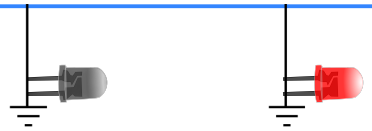
CLOCK DIAGRAM


Q=0
D=1
D=0
C=1
C=0
y-ax
4
3
2
1
0
0
1
2
3
4
x axis

INSTRUCTIONS

Experiment to perform T Flip Flop on kit





TRUTH TABLE

Add Print

Serial No.	Clock	T	Q_{n-1}	$\bar{Q}_{n-1}$	Q	$\bar{Q}$	Remarks
1	0	0	X	X	0	1	No Change
2	0	1	0	1	0	1	No Change
3	1	0	0	1	0	1	No change
4	1	1	0	1	1	0	Toggle

TIMING DIAGRAM