EXPERIMENT NO 6

NAME: JUNAID GIRKAR

SAP ID: 60004190057

AIM: To Verify the truth table of one bit and two bit comparator using logic gates.

THEORY:

A magnitude digital comparator is a combinational circuit that compares two digital or binary numbers in order to find out whether one binary number is equal, less than or greater than the other binary number. We logically design a circuit for which we will have two inputs one for A and other for B and have three output terminals, one for A > B condition, one for A = B condition and one for A < B condition.

There are 2 types of comparators:

- 1 bit comparator
- 2 bit comparator

1 BIT MAGNITUDE COMPARATOR:

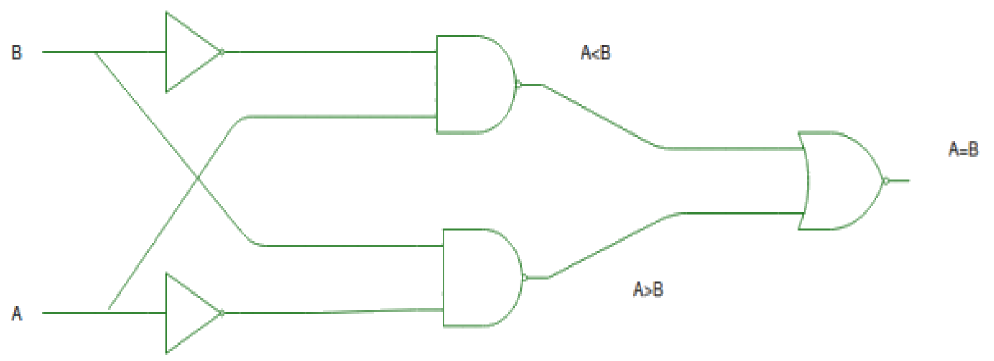
This type of comparator compares single bit from 2 numbers to display the output if the numbers are equal or which number is greater.

The truth table is:

A	B	A<B	A=B	A>B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

From the above truth table logical expressions for each output can be expressed as follows:
A > B : AB'
A < B : A'B
A = B : A'B' + AB

By using these Boolean expressions, we can implement a logic circuit for this comparator as given below :



2 BIT MAGNITUDE COMPARATOR:

This type of comparator compared two bits from two numbers to display the out as the numbers are equal or which of the number is greater.

The truth table for a 2-bit comparator is given below:

INPUT				OUTPUT		
A1	A0	B1	B0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

From the above truth table logical expressions for each output can be expressed as follows:

A > B : $A_1B_1' + A_0B_1'B_0' + A_1A_0B_0'$

A = B : $A_1'A_0'B_1'B_0' + A_1'A_0B_1'B_0 + A_1A_0B_1B_0 + A_1A_0'B_1B_0'$

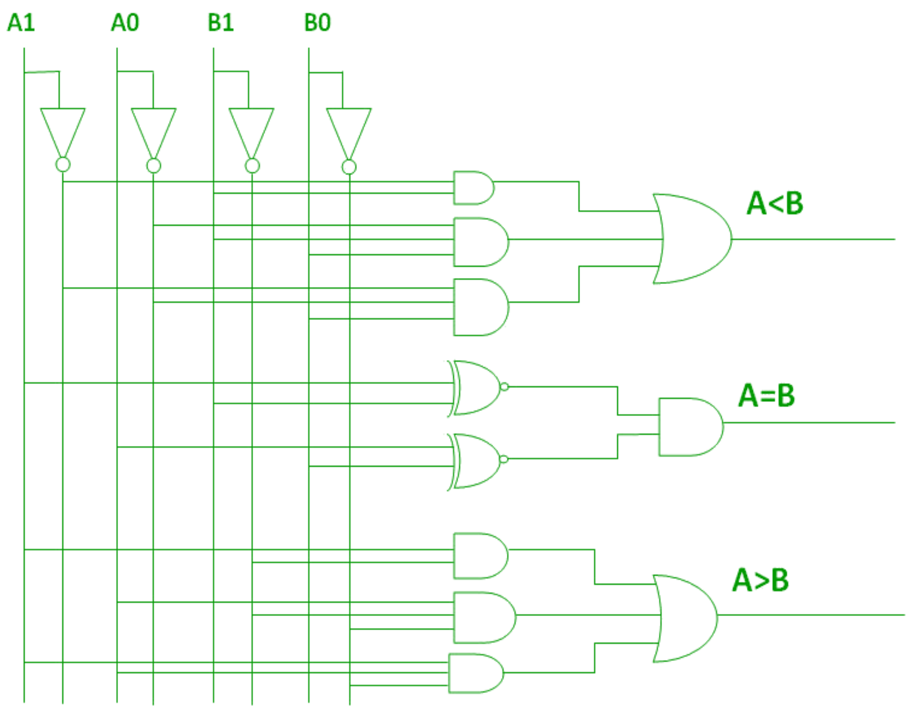
: $A_1'B_1' (A_0'B_0' + A_0B_0) + A_1B_1 (A_0B_0 + A_0'B_0')$

: $(A_0B_0 + A_0'B_0') (A_1B_1 + A_1'B_1')$

: $(A_0$ Ex-Nor $B_0) (A_1$ Ex-Nor $B_1)$

A < B : $A_1'B_1 + A_0'B_1B_0 + A_1'A0'B0$

By using these Boolean expressions, we can implement a logic circuit for this comparator as given below :



Instructions

Construction of 1-Bit Comparator and verification of its operation

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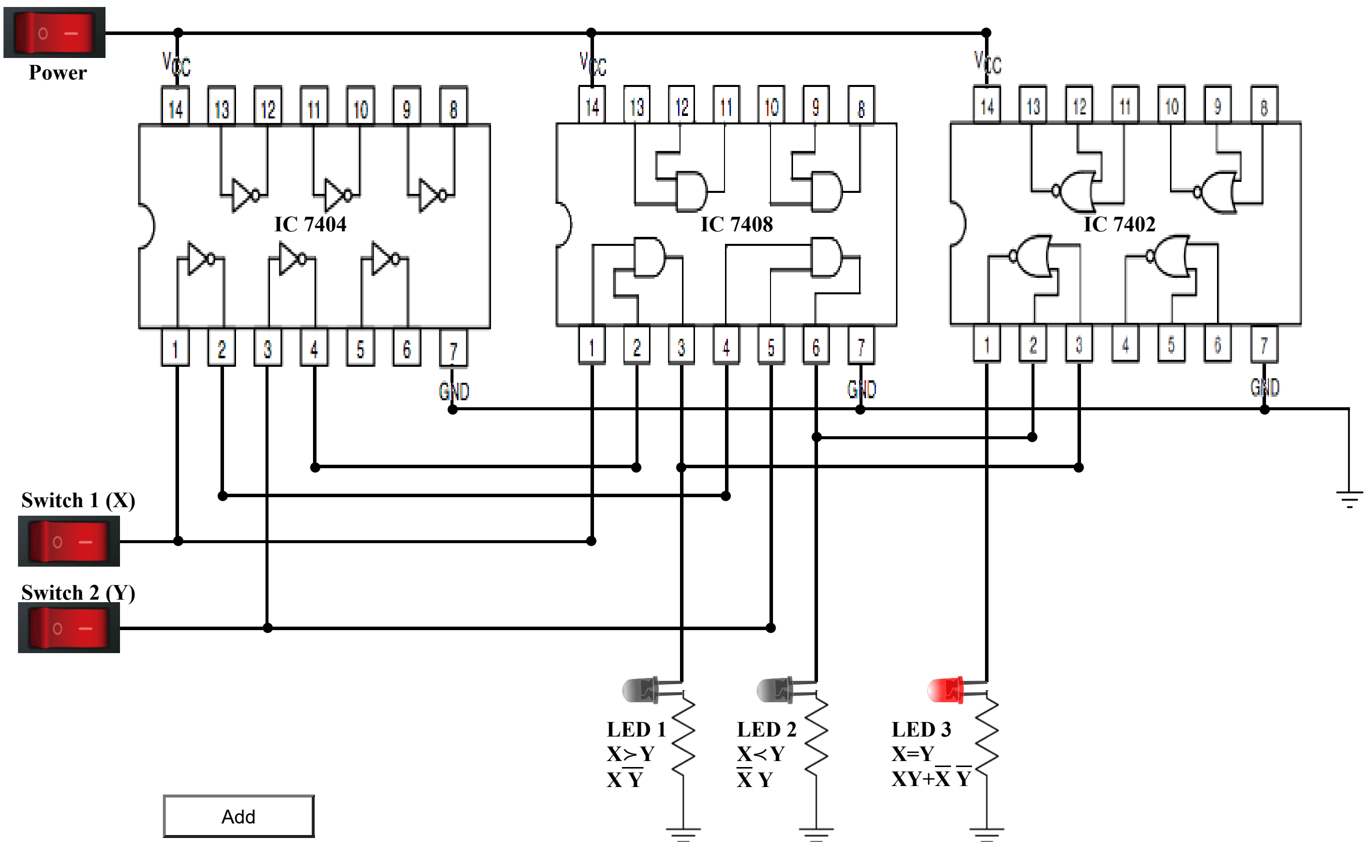

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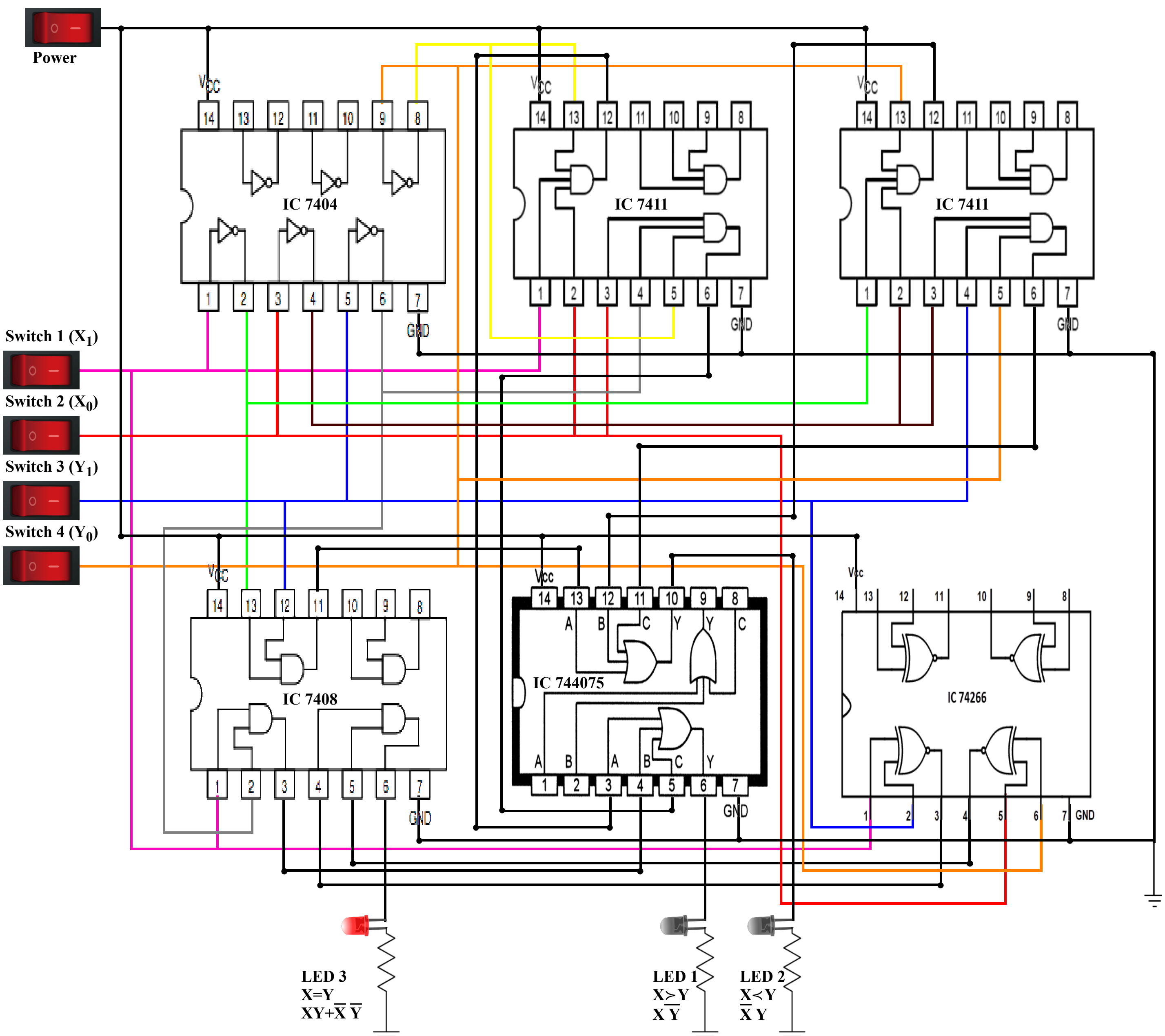
TRUTH TABLE

Serial No.	X	Y	X>Y	X<Y	X=Y
1	0	0	0	0	1
2	0	1	0	1	0
3	1	0	1	0	0
4	1	1	0	0	1

Instructions

Construction of 2-Bit Comparator and verification of its operation



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TRUTH TABLE

Serial No.	X_1	X_0	Y_1	Y_0	X>Y	X<Y	X=Y
1	0	0	0	0	0	0	1
2	0	0	0	1	0	1	0
3	0	0	1	0	0	1	0
4	0	0	1	1	0	1	0
5	0	1	0	0	1	0	0
6	0	1	0	1	0	0	1

COLOR OF INPUTS

Color	Inputs
	X_1
	$\bar{X}_1$
	X_0
	$\bar{X}_0$
	Y_1

7	0	1	1	0	0	1	0
8	0	1	1	1	0	1	0
9	1	0	0	0	1	0	0
10	1	0	0	1	1	0	0
11	1	0	1	0	0	0	1
12	1	0	1	1	0	1	0
13	1	1	0	0	1	0	0
14	1	1	0	1	1	0	0
15	1	1	1	0	1	0	0
16	1	1	1	1	0	0	1

	$\overline{Y_1}$
	Y_0
	[illegible]