Page: 1 ()
Date: / /

	DIGITAL ELECTRONICS JUNAID - GIRKAR
	EXPERIMENT - 2 60004190057
	'A d' b A
*	AIM: To implement the logic functions i.e. AND, OR, NOT, EM-DR.
	En-Nor and a logical empression with the help of
	NAND and NOR universal gates respectively.
	togders i together to the together to
米	THEORY: logic gates are electronic circuits which perform
	logical functions on one or more inputs to produce
	one output. There are seven logic gates when all
	the input combinations of a logic gate are written
	in a series and their corresponding outputs written
3	along them, the input combination is called Truth Table.
triate	THE STORE A PROPERTY OF THE LOCAL PROPERTY OF THE
1	NAND GATE AS UNIVERSAL GATE :
•	NAND gate is actually a combination of two logic gates
	(AND followed by NOT). So, the output is the complement
	of the AND gate. This gate can have minimum 2 inputs;
2	output is always one.
•	By using only NAND gates, we can realize all logic
	By using only NAND gates, we can realize all logic functions: AND, OR, NOT, X-OR, X-NOR, NOR. SO this gate is
	also called a universal gate.
	<u> </u>
$\rightarrow$	NAND gates as NOT gate
•	A NOT produces the complement of the input. It can have only
	one input, tie the inputs of a NAND gate together. It will
1	work as a NOT gate with the output.
•	EXPRESSION: Y = (A.A)'
	= A'

(OP	age:			7
Vo	ate:	1	1	

Mina 3

		A11 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1
	DIAGRAM :	1412
	Α	DA'
	L. AD LONG DEL ENGLISH SIGNA	de Jany temi di
ļ.	ded pro on bong NOT (	nverter

A A STATE OF THE S		11	,
TRUTH TABLE:	Input	output	
e aid elikaritte, mildek ge	Α	A.	,
ed the contract	0	لدر الريان	
122 Jajun Stand mare	71 I 11 4	0	

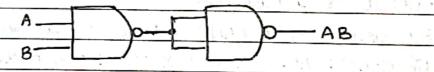
→ NAND gates as AND gate.

• A NAND produces complement of the AND gate so, if the output of a NAND gate is inverted, overall output will be that of AND gate.

• EXPRESSION : Y = ((A.B)')' = A.B

2 Y = A.B

## · DIAGRAM :



AND

-					
	TRUTH TABLE:	Input	50 / A /	Output	Jagar e
	Company than a second	A	B	F=A·B	11 12 .
	The second of the second	0	0 ~	<b>b</b> 1.	A
	and the second second	1 · O	, ,1 -	, <u>o</u>	
		ı	0	0	
		·	1 5	: 1.	
		١.			

6	Page:	2	. 5	7
0	Date:	/	1	$\mathcal{I}$

		and the street of the		and the second second		_
<b>→</b>	NAND gates as	OR gate.	81. T	(EA, A))		
	From De Morgan	3 Theor	em:	(A·B)' = A	4' + B'	
	(Carmal + Car	may +	(SA)	(A'B') = A	"+B" = A + B	
•	so give the inverted					
	or operation at o	utput.		SIA + SIA		
	EXPRESSION : Y					
				1 11. 11.	17783 1	
			!	1.7	482.331 *	
		¬ ^'				
	A -	p-i		2	A	
				b(A: 8	3')'= A + B	
3A V		7 6		<b>1</b>		
	8		1 17	V •	194	
	-	0R	- 1			
	TRUTH TABLE :	9 <b>A</b> A	В	X = A + B	Albin.	
	2 2	0	0	0		
	1	ಲಿ	1	1		
		1 2	0	1		
	, )	1 1	1			
Contract of the second		1				
$\rightarrow$	The output of two	EM-OR 9	ate	the contract	111.1	_
411	The output of two	input En	n-OR	gate is sh	own by Y=A'B+AB	
	Karaman a tr	oth i was	A V I	-2-	1111 T	_
-315	Gate No		vput		OUTPUT	_
	1		, B		(AB)	_
	2	-	, IAB		(A(AB)')'	_
	3		3)', B		(B(AB)')'	_
	4		The state of the s	(AB)')'	A'B + AB'	_
	The output from 9	ate 4 is	the ove	exall out	out of the	_
	enjiguration.	1. 1 1 - m				_

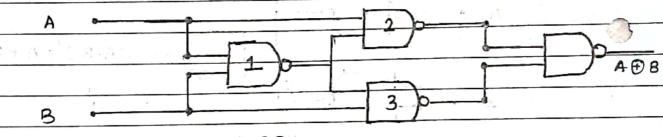
		11 19 11
Y =	((A (AB)')' · (B(AB)')') =	(A (AB)')" + (B (AB)')

$$Y = A(AB)' + B(AB') = (A(A'+B)') + (B(A'+B'))$$
  
 $Y = AA' + AB' + BA' + BB' = O + AB' + BA' + O$ 

$$Y = AB' + A'B$$

EXPRESSION: Y = AB' + A'B

DIAGRAM



X	-	0	R

TRUTH TABLE	A	B	: A⊕ B	ι.,	
	0	0	0		
	0	1	į.		
Y	1 .	0	1		
1-	1 :	1	0		

NAND gates as En-NOR gate

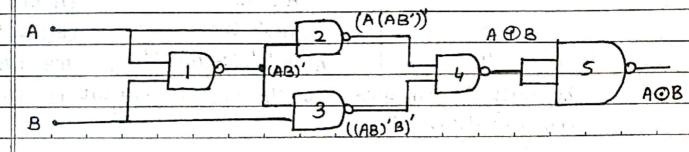
• En-NOR gate is the En-OR gate jollowed by the

NOT gate so given the output of En-OR gate to

a NOT gate, overall output is that of En-NOR gate.

• EXPRESSION: Y-AR+A'R'

EXPRESSION : Y = AB + A'B'



X-NOR

Page: 3 | ()
Date: / /

TRUTH TABLE :	A	В	У	When dean I ha
	0	0	1	
de bound on the straight of the	0	N.	. 0	Control geria
action Control no No let 2	1.0	0	0	or a company
and the second of the second	133	1	In	thus were

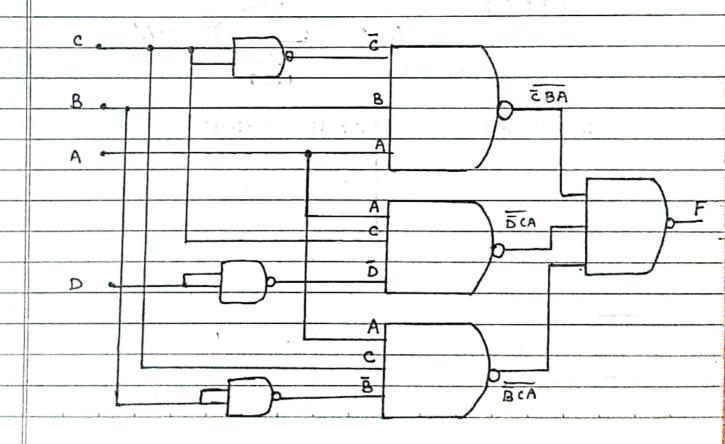
-> IMPLEMENTING THE SIMPLIFIED FUNCTIONS WITH NAND GATES DNLY

· EXPRESSION: F = ((C'.B.A)'(D'.C.A)'(C.B'.A)')'

• The entire empression is inverted and we have three terms

ANDed. This means that we must use a 3-input NAND gate.

Each of the three terms is itself a NAND empression. Finally, negated single terms can be generated with a 2-input NAND gate acting inverted.



Page:			7
Date:	1	1	$\cup$

2-		NOR	GATE	AS	UNIVERSAL	GATE
----	--	-----	------	----	-----------	------

NOR gate is actually a combination of two logic gates: OR gate followed by NOT gate. So its output is complement of the output of an OR gate. This gate can have minimum two inputs; output is always one. By using NOR gates, we can realize all logic junctions: AND, OR, NOT, EX-OR, EX-NOR, NAND. So, this gate is also called a universal gate.

→ NOR gates as NOT gate:

• A NOT produces complement of the input It can have only one input, and after trying the inputs of a NOR gate together, it will work as a NOT gate.

· EXPRESSION : Y = (A + A)' = A'

· DIAGRAM:



TRUTH TABLE: INP UT TUTTUO O

Page	:	4		7
Date	:	1	1	

$\rightarrow$	NOR GATES AS OR GATE :							
0	A NOR produces complement of or gate. so, if the output of a NOR gate is inverted, overall output will be that of an or gate.							
	or a NOR gate is inverted overall output will be							
	that of an or gate.							
٥	EXPRESSION: Y = ((A+B)')' = A+B							
	(A+B)'							
ه								
	8 -	-57	1	L V . 4708				
			OR					
0	- Tuestus	£1 &	, Ar g * 1		.1.42			
•		A	В	X=A+B	*			
171,	TRUTH TABLE	0	0	0				
Q 1	A) TS)	.0	o / MI	1				
	1 (6:3)			1				
( )	/W = 3) (163 + A) - 1	- J'	-1	s hachina	3			
	Gajar(Ars)Ar			ar sead for	$A_{ij} = Y_{ij}$			
$\rightarrow$								
0		w:	(A + B	)' = A'B'	(A) (C) (A)			
	9	(	A' + B'	)' = A·B				
	so give the invexted	linpu	uts to	a NOR gate	e, obtain AND			
	operation at outpu	it		0				
	EXPRESSION: Y =	A·E	3	A second	a water the			
8								
l v l	A A							
	(A'+B') = AB							
3 1	В		7					
	•		B	,				
1 1 4	1 ( ) :			A 1				
			AND	* [*]				

Page:

Contract of the Contract of th	INPUT	0	OUTPUT	- HOM K
TRUTH TABLE:	A	В	F = A. B.	84 6
North to spile flicters	0	0	0 0	
	0	1_0	0	s suris
5. F.A	1 Ja +	A 0	0	Enter of
	1	1	1	

NOR gates as En-NOR gate:

• EXPRESSION: Y = AB + A'B'

_			
	Gate No	Inputs	output
	1 57	A-B	(A+B)
	2	A. (A+B)'	(A+ (A+B)')'
	3	(A+B)'.B	(B + (A+B)')'
	4	(A+(A+B)')'. (B+(A+B)')'	AB + A'B'

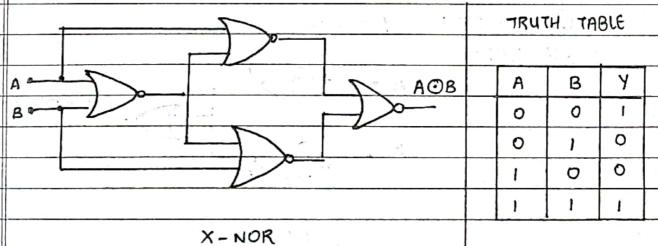
Y = ((A+(A+B)')'. (B+(A+B)')') = (A+(A+B)')(B+(A+B)')

Y = (A+A')(A+B')(B+A')(B+B') = A(B+A') + B'(B+A')

Y = AB + AA' + B'B + B'A' = AB + B'A'

Y = AB + A'B'

## DIAGRAM



Page: 5 Date: / /

				/Date: / /			
<b>→</b>	NOR gates as ex-OR gate	ટ :					
	town district hours h		6		1		
0	En-OR gate is actually En-	dor o	gate jol	lowed by	NOT		
	gate so give the output of Ex-NOR gate to a wor gate:						
	Gn-OR gate is actually En-NOR gate jollowed by NOT gate so give the output of Ex-NOR gate to a NOT gate; overall output is that of an En-OR gate.						
o							
	DIAGRAM:						
	(A+ (A+B	3)')					
	1 (4.0) (3)		AO B	~			
	A A	1	- F	1	A+B		
	В	一					
			1	, ,			
	IR+ IA+B	)')'					
	(B+ (A+B)')' X - OR.						
-7 F T	-1	/					
	TRUTH TABLE	A	В	A 🗗 B			
		0	0	0			
	a sig _ f	ō	1	1			
		KIT.	0	1			
		1	1	0			
0							
	I NEW -	,					
	Land .						
-							
<del></del>							
			<u> </u>		-		

6	Page:			7
V	Date:	1	1	

-> CONSTRUCTING A CIRCUIT WITH NOR GATES ONLY

· F = (((c.B.A) + (D.Z.A) + (c.B.A))))

· DIAGRAM :

