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DE TT2

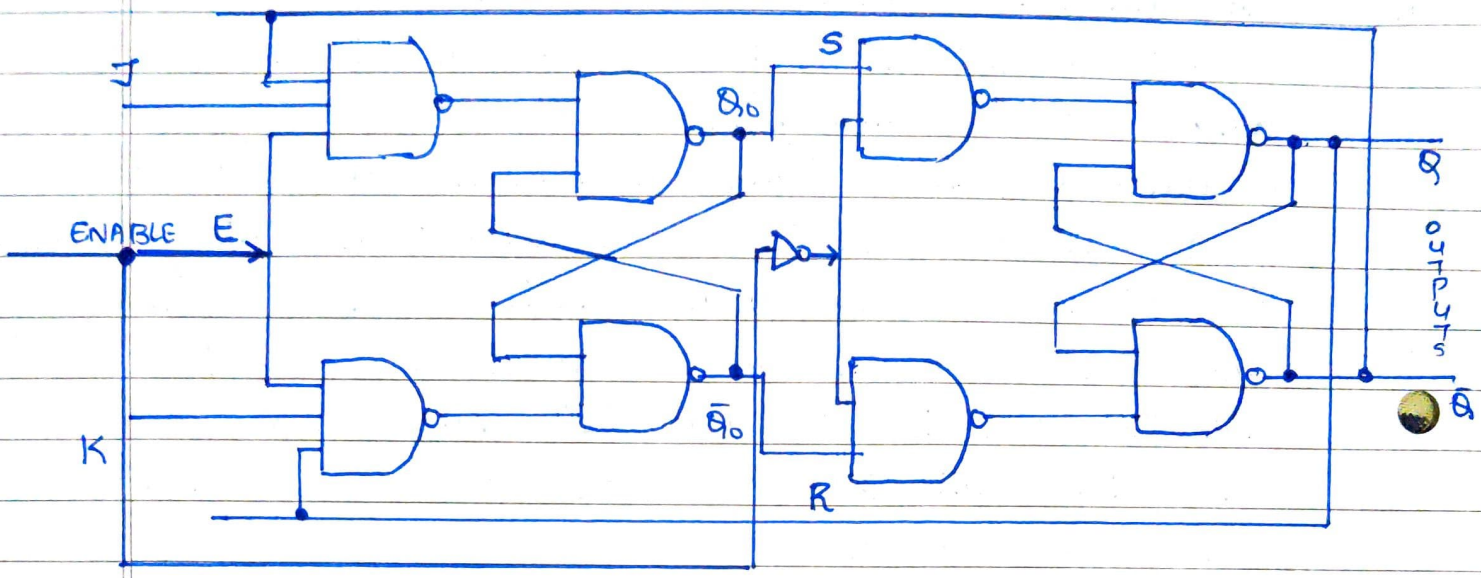
Q1

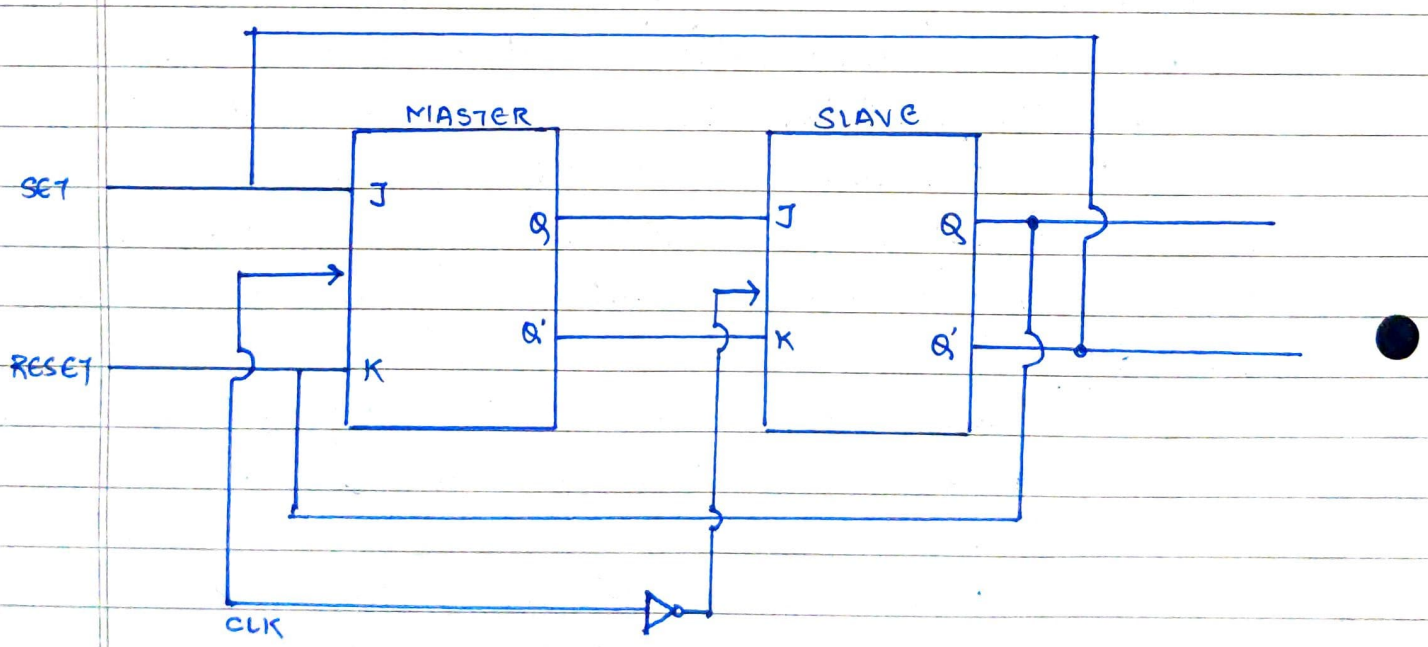
ANS RACE AROUND CONDITION IN JK FLIP-FLOP

For JK flip-flop, if J=K=1, and if clk=1 for a long period of time, then Q output will toggle as long as CLK is high, which makes the output of the flip-flop unstable or uncertain. This problem is called race around condition in J-K flip-flop. The whole problem can be avoided by ensuring that the clock is at logic '1' only for a very short time. This introduced the concept of master slave JK flip-flop.

The master slave flip-flop is basically a combination of two JK flip-flops connected together in a series configuration. Out of these, one acts as the "MASTER" and the other as a "SLAVE". The output from the master flip-flop is connected to the two inputs of the slave flip-flop. whose output is fed back to inputs of the master flip-flop.

In addition to these flip-flops, the circuit also includes an inverter. The inverter is also connected to clock pulse in such a way that the inverted clock pulse is given to the slave flip-flop. In other words if clock pulse = 0 for a master flip-flop, then clock pulse = 1 for a slave flip-flop and if clock pulse = 1 for master flip-flop then it becomes 0 for slave flip-flop





Q2

ANS STEP 1: Since we have to design MOD-9 counter, 4 flip-flops are needed

STEP 2: TRUTH TABLE

State	Flip-flop output				output of Reset logic
	Q_D	Q_C	Q_B	Q_A	
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	0

States 0 to 8 are valid states and output of reset logic is inactive for them.

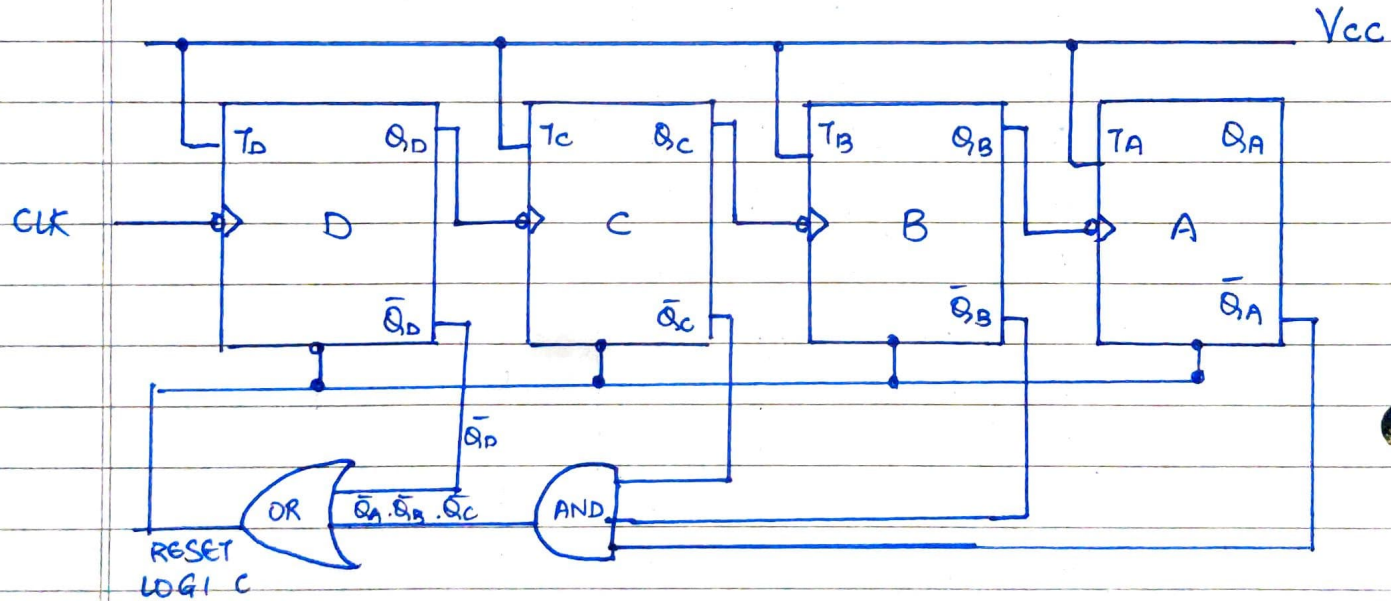
States 9 to 15 are invalid states. If counter enters any of these states then it will reset all flip-flops

STEP 3: K-Map

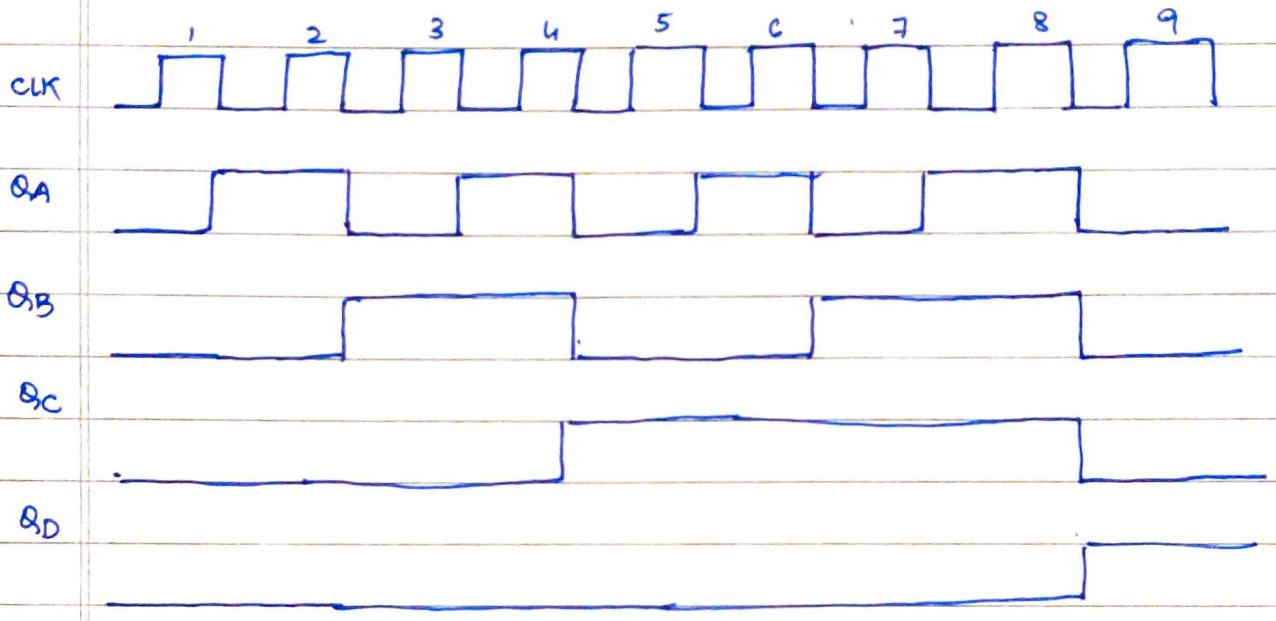
$Q_D Q_C$ \ $Q_A Q_B$	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	0	0	0	0
10	1	0	0	0

$$Y = \bar{Q}_D + \bar{Q}_A \cdot \bar{Q}_B \cdot \bar{Q}_C$$

STEP 4: LOGIC DIAGRAM



Timing Diagram.



Q3

ANS $F(A,B,C,D) = \Sigma_m (0,1,3,6,9,11,12,13,15)$

The design table is as follows

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\bar{A}$	(0)	(1)	2	(3)	4	5	(6)	7
A	8	(9)	10	(11)	(12)	(13)	14	(15)

Input to Multiplexer	$\bar{A}$	1	0	1	A	A	$\bar{A}$	$\bar{A}$

The corresponding logic diagram is: