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PRACTICAL NO: 9

In digital logic and computing, a Counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. Counters are used in digital electronics for counting purpose, they can count specific event happening in the circuit. For example, in UP counter a counter increases count for every rising edge of clock. Not only counting, a counter can follow the certain sequence based on our design like any random sequence 0,1,3,2… .They can also be designed with the help of flip flops.

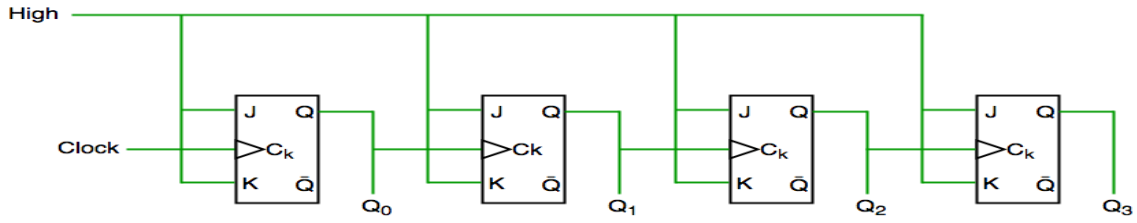
Counter Classification

Counters are broadly divided into two categories

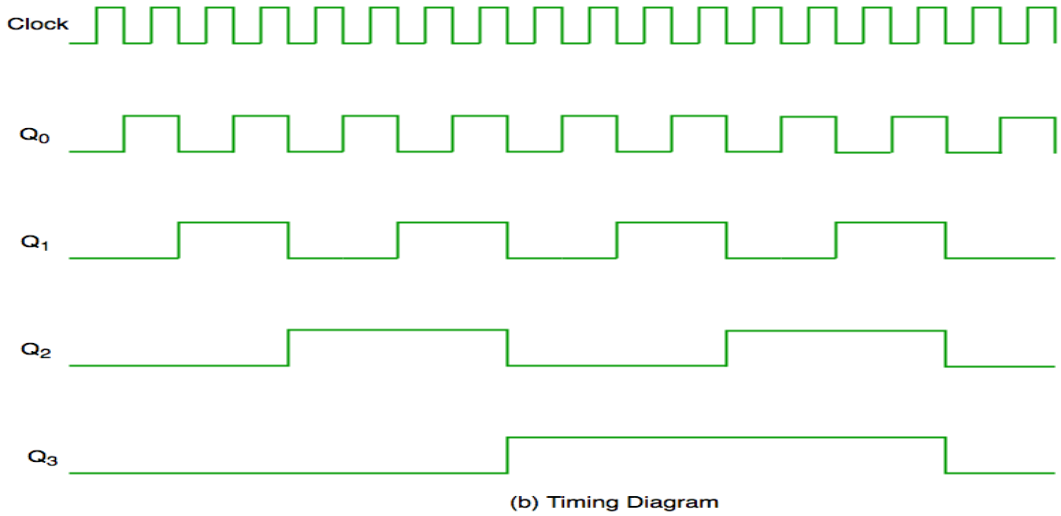
1. Asynchronous counter
2. Synchronous counter

1. Asynchronous Counter

In asynchronous counter we don't use universal clock, only first flip flop is driven by main clock and the clock input of rest of the following flip flop is driven by output of previous flip flops. We can understand it by following diagram-



(a) Asynchronous counter

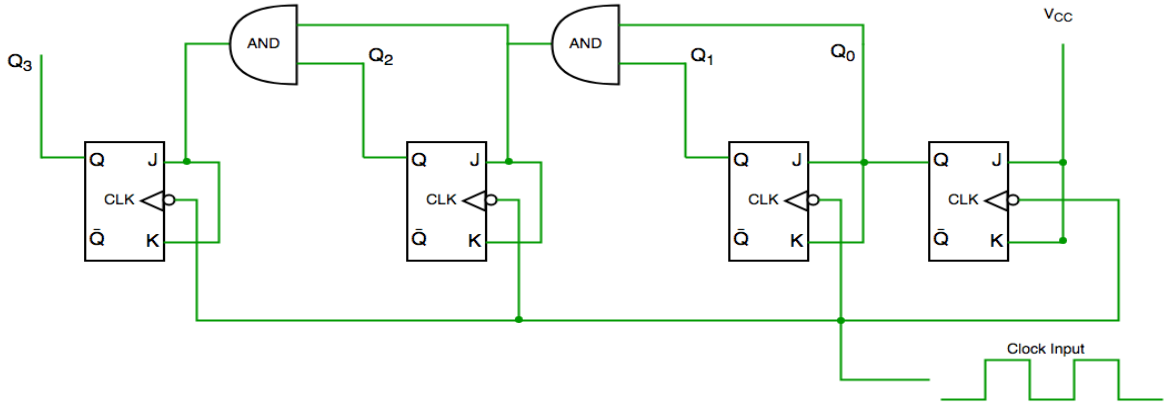


(b) Timing Diagram

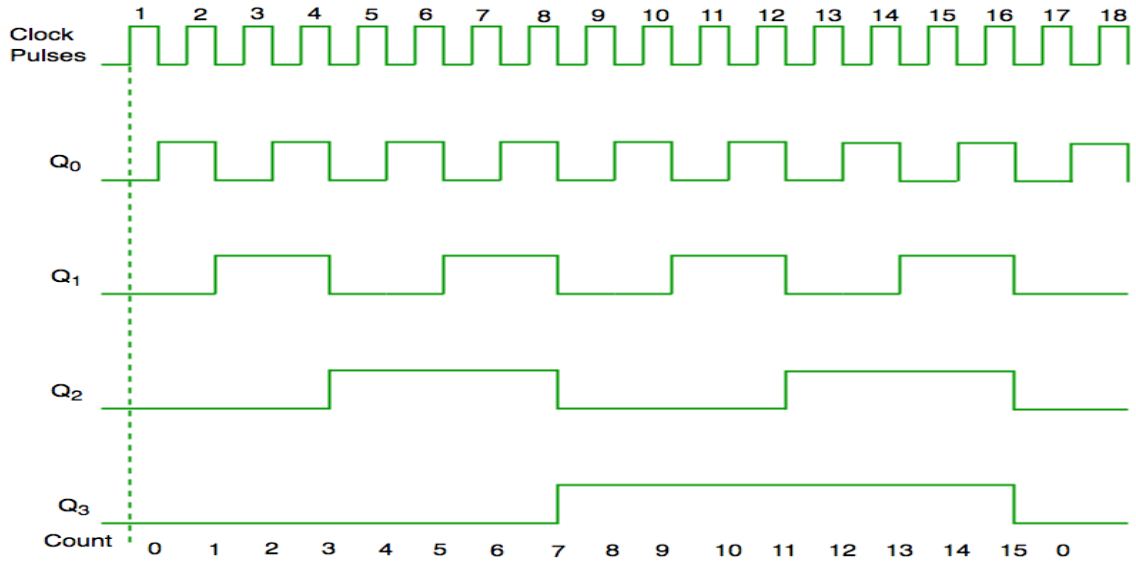
It is evident from timing diagram that Q0 is changing as soon as the rising edge of clock pulse is encountered, Q1 is changing when rising edge of Q0 is encountered(because Q0 is like clock pulse for second flip flop) and so on. In this way ripples are generated through Q0,Q1,Q2,Q3 hence it is also called **RIPPLE counter.**

3. **Synchronous Counter**

Unlike the asynchronous counter, synchronous counter has one global clock which drives each flip flop so output changes in parallel. The one advantage of synchronous counter over asynchronous counter is, it can operate on higher frequency than asynchronous counter as it does not have cumulative delay because of same clock is given to each flip flop.



Synchronous counter circuit



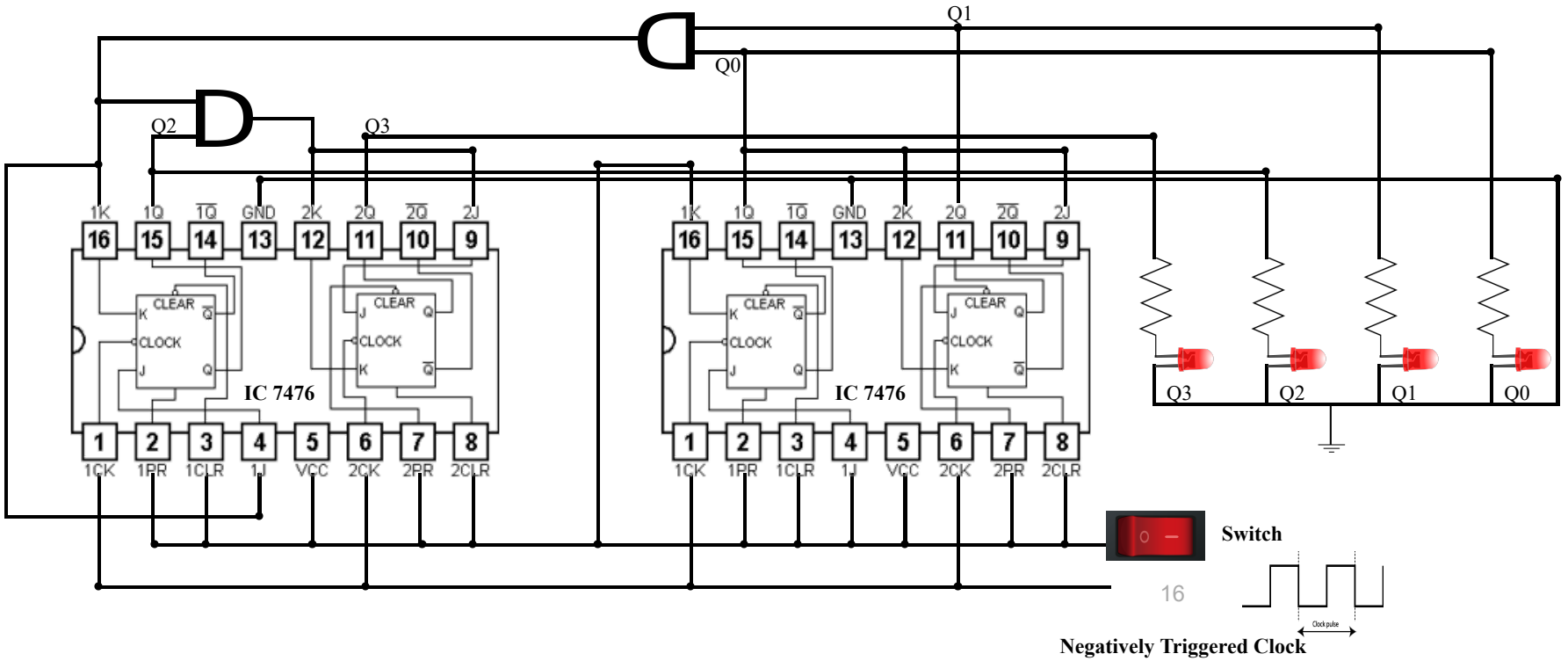
Timing diagram synchronous counter

From circuit diagram we see that Q0 bit gives response to each falling edge of clock while Q1 is dependent on Q0, Q2 is dependent on Q1 and Q0 , Q3 is dependent on Q2,Q1 and Q0.

Instructions

Print

4-Bit Synchronous Parallel Counter using J-K Flip-Flop

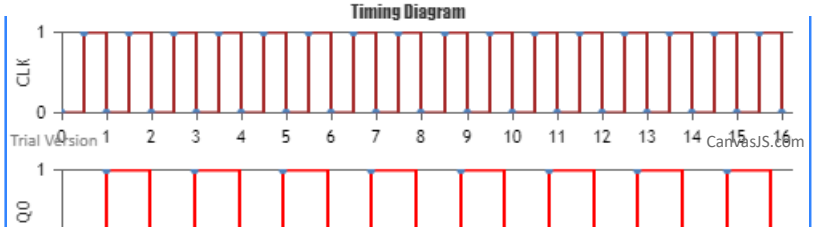


TRUTH TABLE

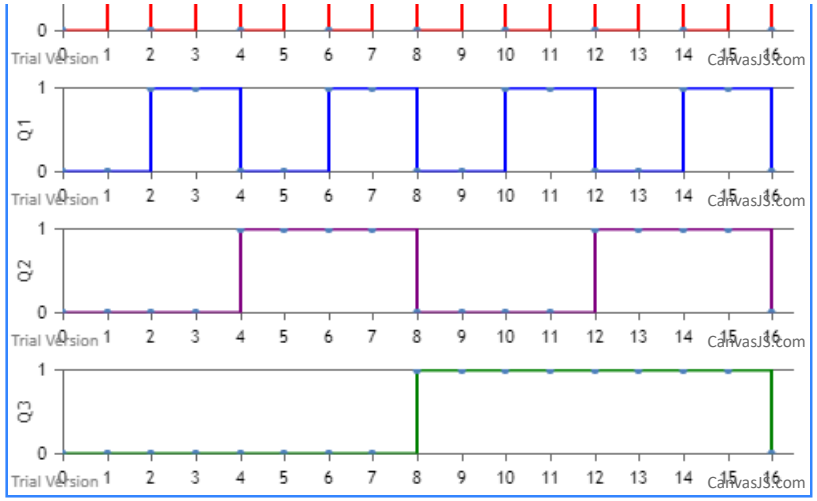
Serial No.	Clock	Q3	Q2	Q1	Q0
1	1	0	0	0	0
2	2	0	0	0	1
3	3	0	0	1	0
4	4	0	0	1	1

TIMING DIAGRAM

Generate Waveform



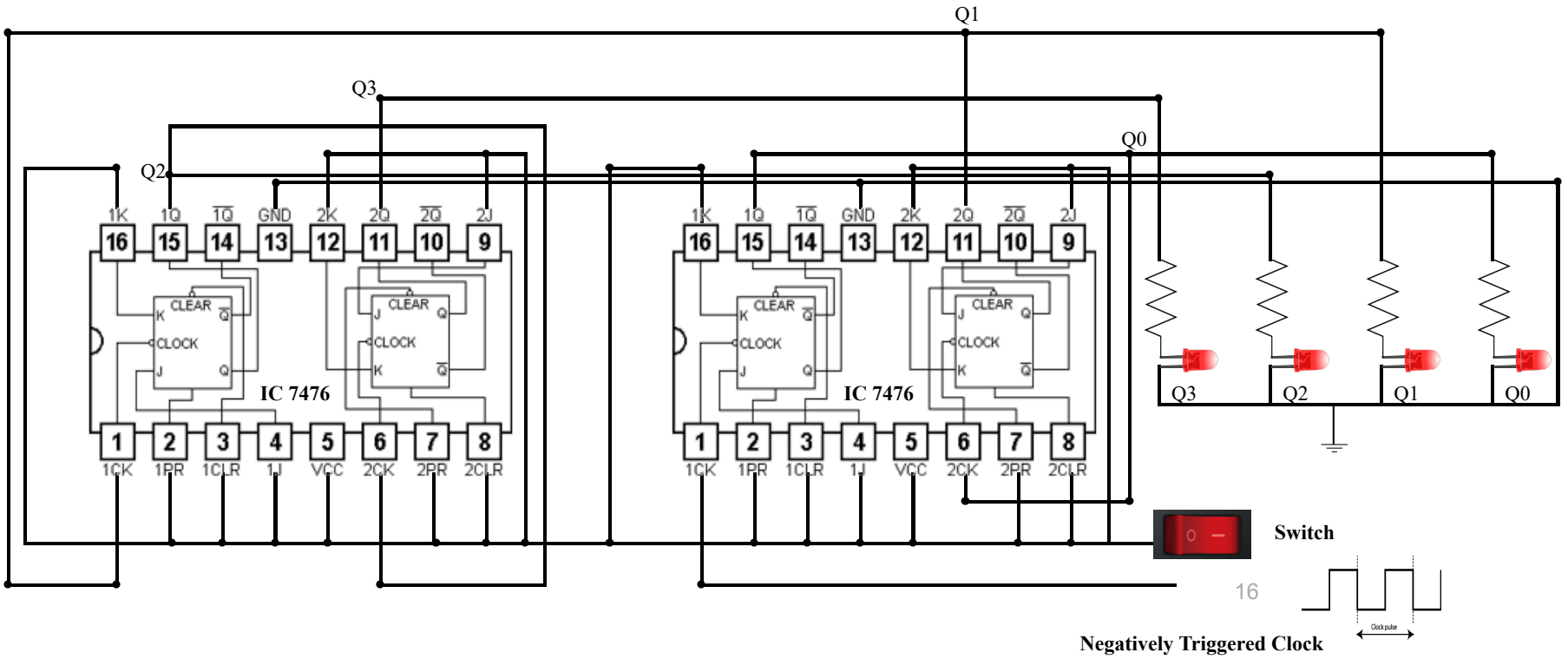
5	5	0	1	0	0
6	6	0	1	0	1
7	7	0	1	1	0
8	8	0	1	1	1
9	9	1	0	0	0
10	10	1	0	0	1
11	11	1	0	1	0
12	12	1	0	1	1
13	13	1	1	0	0
14	14	1	1	0	1
15	15	1	1	1	0
16	16	1	1	1	1



Instructions

Print

4-Bit Asynchronous Parallel Counter using J-K Flip-Flop

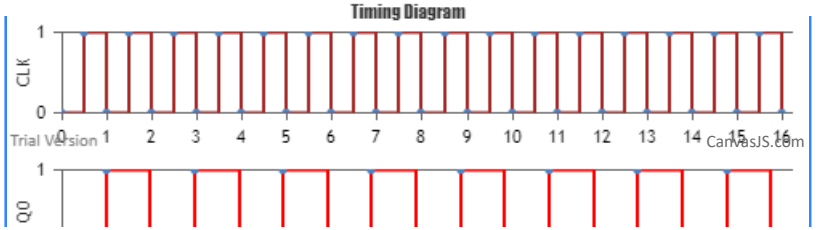


TRUTH TABLE

Serial No.	Clock	Q3	Q2	Q1	Q0
1	1	0	0	0	0
2	2	0	0	0	1
3	3	0	0	1	0
4	4	0	0	1	1

TIMING DIAGRAM

Generate Waveform



5	5	0	1	0	0
6	6	0	1	0	1
7	7	0	1	1	0
8	8	0	1	1	1
9	9	1	0	0	0
10	10	1	0	0	1
11	11	1	0	1	0
12	12	1	0	1	1
13	13	1	1	0	0
14	14	1	1	0	1
15	15	1	1	1	0
16	16	1	1	1	1