21/10/21			POA		JUNAID GIRKAR GOOOU190057 TE COMPS A4
Q1 a	0	+- / */-0	-21	- u 2- (	- 0
\(\alpha\)	·	te (-16)*(-2	9) using	Booth's t	Restoring
	Multip	olication Alg	orithm.	1	
ANS		C 4 - 20			Carlo and the second of the se
MINO		6 + -29			
		$\frac{1}{10000} = \frac{110000}{110000}$	Control of the Contro		
	(- 29	)10 = (10 <u>0</u> 0	11/2		
		20 - 410			
	+	= -29 = (10)	Secretary of the second of the		
	l G	= -16 = (110	2000 12 /		
	Taking	2's complemen	1+ 0 (-24)	110 = 011	1100 [is complement
	1 · · · · · · · · · · · · · · · · · · ·				
			-M	= 011	101
				•	
	N	Α	8	Q -1	OPERATION
	6	000 000	11 00 00	0	Initialization
		000000	011000	0	ARS
3					
	5	000000	001100	0	ARS
	4	000 000	000110	) <u>O</u>	ARS
4 (1) (1) (1) (1) (1) (1) (1) (1) (1) (1)					
	3	000 000	000011	0	ARS
	2	000000	000011	D	A-M
	1/200	+011101			
		011101	11 0000	0	ARS
		ا ا ا ا ا ا ا ا ا ا ا ا ا ا ا ا ا ا ا	100001	1	
					<u> </u>
Sundaram®	4-		FOR EDUCAT	TONAL USE	

JUNALD GIRKAR

							_
	N. S.	A	8	V V	Q -1	OPERATION	\'
				KS.1/0	102111		
Evipe ville NNAS : Evipe :	1 00	00111	010000		J	ARS	
				66011		2 , 3 ,	
	: Result	= (0001	11 010000	),		N <sub>ije</sub>	
		= (464	The control of the co	<u>,                                    </u>			_
The state of the s	(-29)10	x (-16)10	= (464)	10			)
							_
	(100011)2	X (1100	00)2 = (0	001110	10000)		_
							_
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		A			, A		_
							_
	18 A 44 A 54 A 54 A 54 A 54 A 54 A 54 A 5						_
	5,30,000						_
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		<u>. 1</u>					
300 S		,				Constitution of the Consti	
	- 370	1					
	3137					4.00 MARIA	
						590.** P03.**	
V VIII	1 1	7. 7	(4)	(1.5%)	0.00		
			Series Asserting and a		L.		
N. Carlos	1 1			Section of the second	***		

Q2							
	PROCESSOR				MAIN MEMORY		
	**************************************		[ L2 ]		24		
	4 and 12 are in parallel. So their average						
	HME is				V		
			2.2				
	(Tang), =	: HL, +	TL, +	(1-HLI)7L2			
	let us repl	ace L	and L	2 cache u	oith a single	block	
					O .		
	PROCESSOR		CACHE	MAIN	J MEMORY		
	Au three are in series						
	Average time is cache consist of 2 blocks						
	: (Tang)2	= H cac	he (Tavg)	, + (1 - Ho	ache ) ((Tang)1+	TMM)	
		ANNA SAME THE SECOND STREET		main men	nory		
	1-4 cache						
	1-HMM	= Hcac	he				
	∴ (7avg)2 =	: (1- <del> </del>	1mm) (7	avg), + Hr	1M ((Tavg), + T	mm)	
	100 Miles		yur				
	Maria de la compania	lajet.					
	The first factor of the state of						

```
Tu = 15 ns
762 = 18 ns
TMM = 1225 ns
H4 = 0.75
HLZ = 0.95
HL3 = 0.65
: Tavg = HL1 * TL1 + (1-HL1) TL2
      = 0.75 × 15 + (1-0.75) 18
      = 0.75 x15 + 0.25 x18
       = 11.25 + 4.5
      = 15.75 ns
(Tang)2 = (1 - Hmm) Tang, + Hmm (Tang + Tmm)
       = 0.35 × 15.75 + 0.65 (15.75 + 1225)
      = 5.5125 + 806.4875
        = 812 ns
: Average Memory Accels Time = 812 ns.
```

<b>Q</b> 3	Differentiate between von N Axchitecture	Jeumann and Harvard
	Ancutecture	
ANS	VON NEUMANN	HARVARD
•		
Λ.	It is an ancient computer	· It is modern computer
	architecture based on	architecture based on
	Stored program computer	Harward Mark I relay
	concept.	based model
	Same physical memory	· separate physical
	address is used for	memory address is used
	instructions and data	for instructions and data
	there is a common bus	separate buses are
- July	for data and instruction	used for transjeving
	transper	data and instruction.
	7100 clock cycles are	· An instruction is
	required to enecute	enecuted in a single
	single instruction	cycle
	It is cheaper in cost	· It is costiler than
		von Neumann Architecture
•	cpu cannot access	· CPU can access instructions
	instructions and read/	and slead / write at the
	write at the same time.	same time.
•	It is used in personal	· It is used in micro
	computers and small	controllers and signal
	computeres	processing.
(a)		

Q4 b	A computer system uses 16-bit memory addresses
	It has a 2k-byte cache organized in a
	It has a 2x-byte cache organized in a direct-mapped manner with 64 bytes per
	cache block Assume that the size of each
	memory word is 1 byte.
	a] calculate the number of bits in each of the
	Tag, Block, and word jields of the memory
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	memory word is 1 byte.  a] calculate the number of bits in each of the tag, Block, and word yields of the memory address
ANS	Block size = G4 bytes  = 26 bytes  = 26 words [: 1 byte = 1 word]
	= 26 64+68
	= 26 words [: 1 byte = 1 word]
	: Number of bits in word field = 6
	Cache size = 2K-byte =
	= 2" bytes
	= 2" bytes Number of cache blocks = cache size : Block size
	= 2" = 26
	= 25
	: Number of bits in the block fied [= 5]
NEW TO	rotal number of address bits = 16  : Number of bits in the tag field = 16-6-5
	: Number of bits in the tag field = 16-6-5
	= 5
	Number of bits in tag field = 5  Number of bits in block field = 5  Number of bits in word field = 6
	Number of bits in block field = 5
	Number of bits in word field = 6
	TAG(S) BLOCK(S) WORD (G)
- A	9 15
·	TOD TIVE