Built-in Self-Test for on-chip testing of Digital IC's

VHDL Code:

(A) Top Module (Assembly) Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity TopModule is
   Port ( Enable,Select1  : in  STD_LOGIC;
          Clk : in  STD_LOGIC;
                                MISR_Out : inout STD_LOGIC_VECTOR(7 downto 0);
                                        Nibble1,Nibble2 : inout STD_LOGIC_VECTOR(3 downto 0)
                                        --MUL_Result : out  STD_LOGIC_vector(7 downto 0);
                                        );
        --MUL_Result : out  STD_LOGIC_vector(7 downto 0));
end TopModule;

architecture Behavioral of TopModule is


signal MUL_Result : STD_LOGIC_VECTOR(7 downto 0);

component mul
  port(Nibble1, Nibble2: in std_logic_vector(3 downto 0);
       Result: out std_logic_vector(7 downto 0));
end component;

component LFSR
   Port (clk,enable : in  STD_LOGIC;
                                LFSR_Out  : inout  STD_LOGIC_vector(7 downto 0));
end component;

component MISR
port ( clk,select1 : in std_logic;
       M : in std_logic_vector(7 downto 0);
                               MISR_Out : inout std_logic_vector(7 downto 0));
end component;

begin

Mod1 : LFSR port map (clk=>Clk, enable=>Enable,LFSR_Out(7 downto 4)=>Nibble1(3 downto 0),LFSR_Out(3 downto
0)=>Nibble2(3 downto 0));
Mod2 : mul port map (Nibble1(3 downto 0)=>Nibble1(3 downto 0), Nibble2(3 downto 0)=>Nibble2(3 downto 0),
Result=>MUL_Result);
Mod3 : MISR port map (clk=>Clk,select1=>Select1,M(7 downto 0)=>MUL_Result(7 downto 0), MISR_Out(7 downto
0)=>MISR_Out(7 downto 0));
end Behavioral;
```

Top Module Test Bench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY TopModule_Test IS
END TopModule_Test;
```

```
ARCHITECTURE behavior OF TopModule_Test IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT TopModule
    PORT(
         Enable : IN  std_logic;
         Select1 : IN  std_logic;
         Clk : IN  std_logic;
         MISR_Out : INOUT  std_logic_vector(7 downto 0);
         Nibble1 : INOUT  std_logic_vector(3 downto 0);
         Nibble2 : INOUT  std_logic_vector(3 downto 0)
        );
    END COMPONENT;


   --Inputs
   signal Enable : std_logic := '0';
   signal Select1 : std_logic := '0';
   signal Clk : std_logic := '0';

            --BiDirs
   signal MISR_Out : std_logic_vector(7 downto 0);
   signal Nibble1 : std_logic_vector(3 downto 0);
   signal Nibble2 : std_logic_vector(3 downto 0);

   -- Clock period definitions
   constant Clk_period : time := 10 ns;

BEGIN
            -- Instantiate the Unit Under Test (UUT)
   uut: TopModule PORT MAP (
          Enable => Enable,
          Select1 => Select1,
          Clk => Clk,
          MISR_Out => MISR_Out,
          Nibble1 => Nibble1,
          Nibble2 => Nibble2
        );

   -- Clock process definitions
   Clk_process :process
   begin
                        Clk <= '0';
                        wait for Clk_period/2;
                        Clk <= '1';
                        wait for Clk_period/2;
   end process;


   -- Stimulus process
   stim_proc: process
   begin
      -- hold reset state for 100 ns.
      wait for 30ns;
Enable<='1';
Select1<='1';

      -- insert stimulus here
```

```
    wait;
  end process;

END;
```

(B) Multiplier Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity mul is
  port
  (
    Nibble1, Nibble2: in std_logic_vector(3 downto 0);

    Result: out std_logic_vector(7 downto 0)
  );
end entity mul;

architecture Behavioral of mul is
begin

  Result <= std_logic_vector(unsigned(Nibble1) * unsigned(Nibble2));

end architecture Behavioral;
```

Multiplier Test Bench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY mul_test IS
END mul_test;

ARCHITECTURE behavior OF mul_test IS

   -- Component Declaration for the Unit Under Test (UUT)

   COMPONENT mul
   PORT(
        Nibble1 : IN  std_logic_vector(3 downto 0);
        Nibble2 : IN  std_logic_vector(3 downto 0);
        Result : OUT  std_logic_vector(7 downto 0)
       );
   END COMPONENT;


  --Inputs
  signal Nibble1 : std_logic_vector(3 downto 0) := (others => '0');
  signal Nibble2 : std_logic_vector(3 downto 0) := (others => '0');

          --Outputs
  signal Result : std_logic_vector(7 downto 0);

BEGIN
```

```
        -- Instantiate the Unit Under Test (UUT)
  uut: mul PORT MAP (
       Nibble1 => Nibble1,
       Nibble2 => Nibble2,
       Result => Result
      );


  -- Stimulus process
stim_proc: process
begin
        wait for 100 ns;
                Nibble1<= "0101";
                Nibble2<= "1100";

        wait for 100 ns;
                Nibble1<= "0111";
                Nibble2<= "1110";

end process;

END;
```

(C) LFSR Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity LFSR is
   Port (
        clk,enable : in  STD_LOGIC;
                        LFSR_Out  : inout  STD_LOGIC_vector(7 downto 0));
end LFSR;

architecture Behavioral of LFSR is
begin
process (clk,enable)
begin
        if (rising_edge (clk)) then
                if (enable = '0') then
                        LFSR_Out <= "11111111";
                else
                        LFSR_Out(7) <= LFSR_Out(0) xor LFSR_Out(1) xor LFSR_Out(5) xor LFSR_Out(6);
                        LFSR_Out(6) <= LFSR_Out(7);
                        LFSR_Out(5) <= LFSR_Out(6);
                        LFSR_Out(4) <= LFSR_Out(5);
                        LFSR_Out(3) <= LFSR_Out(4);
                        LFSR_Out(2) <= LFSR_Out(3);
                        LFSR_Out(1) <= LFSR_Out(2);
                        LFSR_Out(0) <= LFSR_Out(1);
                end if;
        end if;
end process;
end Behavioral;
```

LFSR Test Bench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY LFSR_Test IS
END LFSR_Test;

ARCHITECTURE behavior OF LFSR_Test IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT LFSR
    PORT(
         clk : IN  std_logic;
         enable : IN  std_logic;
         LFSR_Out : INOUT  std_logic_vector(7 downto 0)
        );
    END COMPONENT;


   --Inputs
   signal clk : std_logic := '0';
   signal enable : std_logic := '0';

            --BiDirs
   signal LFSR_Out : std_logic_vector(7 downto 0);

   -- Clock period definitions
   constant clk_period : time := 10 ns;

BEGIN

            -- Instantiate the Unit Under Test (UUT)
   uut: LFSR PORT MAP (
         clk => clk,
         enable => enable,
         LFSR_Out => LFSR_Out
        );

   -- Clock process definitions
   clk_process :process
   begin
                        clk <= '0';
                        wait for clk_period/2;
                        clk <= '1';
                        wait for clk_period/2;
   end process;


   -- Stimulus process
   stim_proc: process
   begin
      wait for 10 ns;
enable <='1';
      wait;
   end process;
```

```
END;
```

(D) MISR Code:

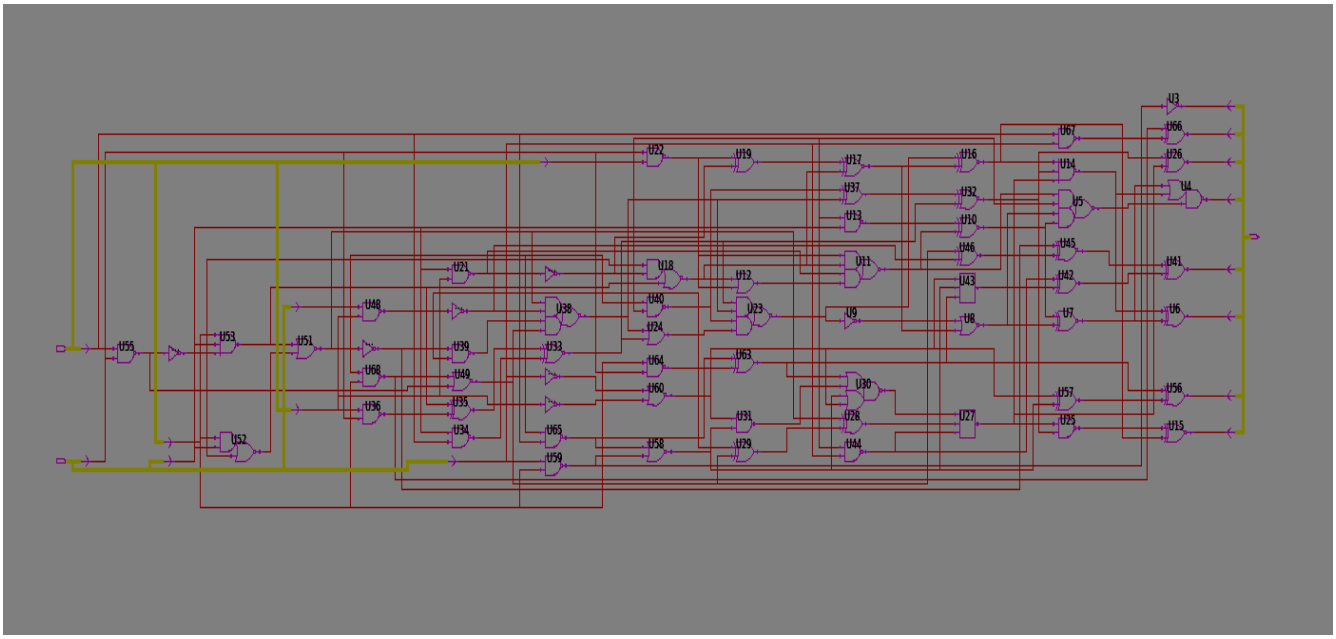
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity MISR is
port ( clk,select1 : in std_logic;
       M : in std_logic_vector(7 downto 0);
                              MISR_Out : inout std_logic_vector(7 downto 0)
       );

end MISR;

architecture Behavioral of MISR is

begin
process (clk)
begin
 if (rising_edge(clk)) then
           if (select1='0') then
                     MISR_Out <="00000000";
           else
                     MISR_Out (7) <= M(7) xor MISR_Out(6);
                     MISR_Out (6) <= M(6) xor MISR_Out(5) xor MISR_Out(7);
                     MISR_Out (5) <= M(5) xor MISR_Out(4) xor MISR_Out(7);
                     MISR_Out (4) <= M(4) xor MISR_Out(3);
                     MISR_Out (3) <= M(3) xor MISR_Out(2);
                     MISR_Out (2) <= M(2) xor MISR_Out(1);
                     MISR_Out (1) <= M(1) xor MISR_Out(7) xor MISR_Out(0);
                     MISR_Out (0) <= M(0) xor MISR_Out(7);
           end if;
end if;
end process;
end Behavioral;
```

MISR Test Bench:

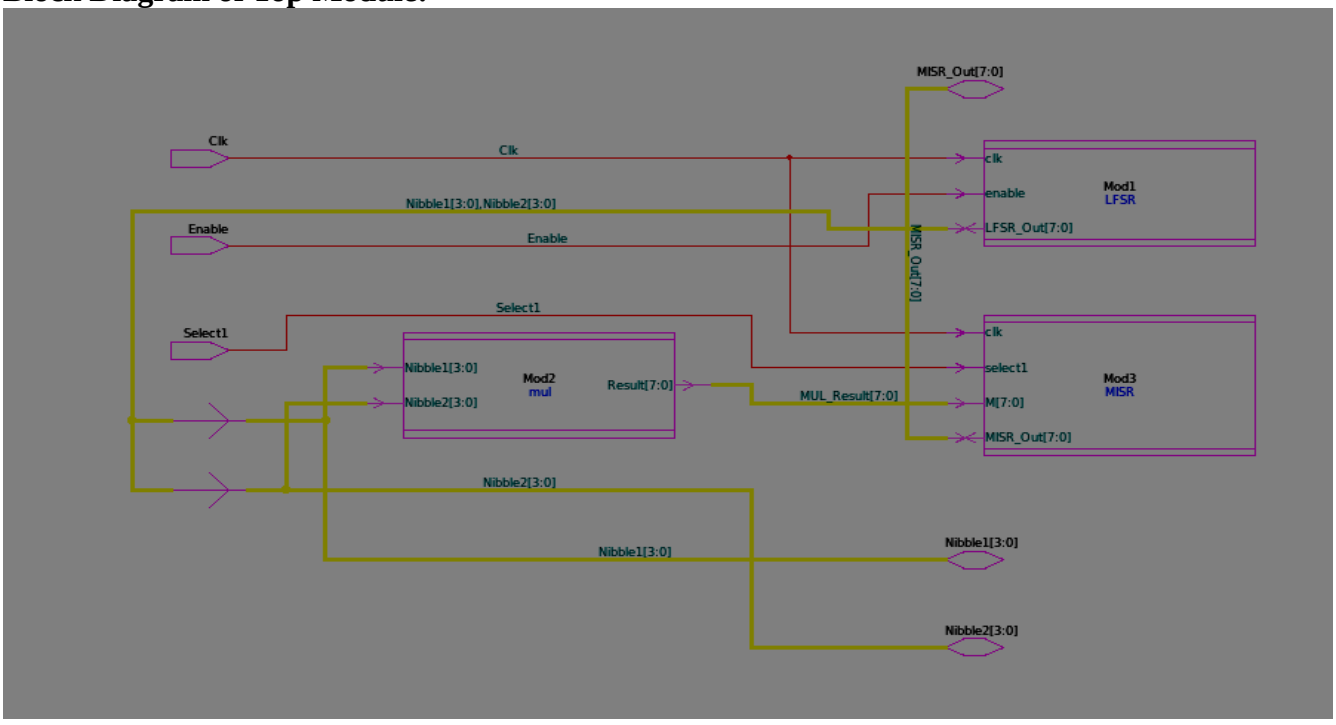
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY MISR_Test IS
END MISR_Test;

ARCHITECTURE behavior OF MISR_Test IS

   -- Component Declaration for the Unit Under Test (UUT)

   COMPONENT MISR
   PORT(
       clk,select1 : IN  std_logic;
       M : IN  std_logic_vector(7 downto 0);
```

```
        MISR_Out : INOUT  std_logic_vector(7 downto 0)
       );
    END COMPONENT;


   --Inputs
   signal clk,select1 : std_logic := '0';
   signal M : std_logic_vector(7 downto 0) := (others => '0');

            --BiDirs
   signal MISR_Out : std_logic_vector(7 downto 0);

   -- Clock period definitions
   constant clk_period : time := 10 ns;

BEGIN

            -- Instantiate the Unit Under Test (UUT)
   uut: MISR PORT MAP (
         clk => clk,
                                  select1=>select1,
         M => M,
         MISR_Out => MISR_Out
        );

   -- Clock process definitions
   clk_process :process
   begin
                        clk <= '0';
                        wait for clk_period/2;
                        clk <= '1';
                        wait for clk_period/2;
   end process;


   -- Stimulus process
   stim_proc: process
   begin
      -- hold reset state for 100 ns.
      wait for 20ns;
select1<='1';
M<="10101010";
wait for 10ns;
M<="11100010";
wait;
      -- insert stimulus here

      wait;
   end process;

END;
```

Circuit of Multiplier (Design Vision):

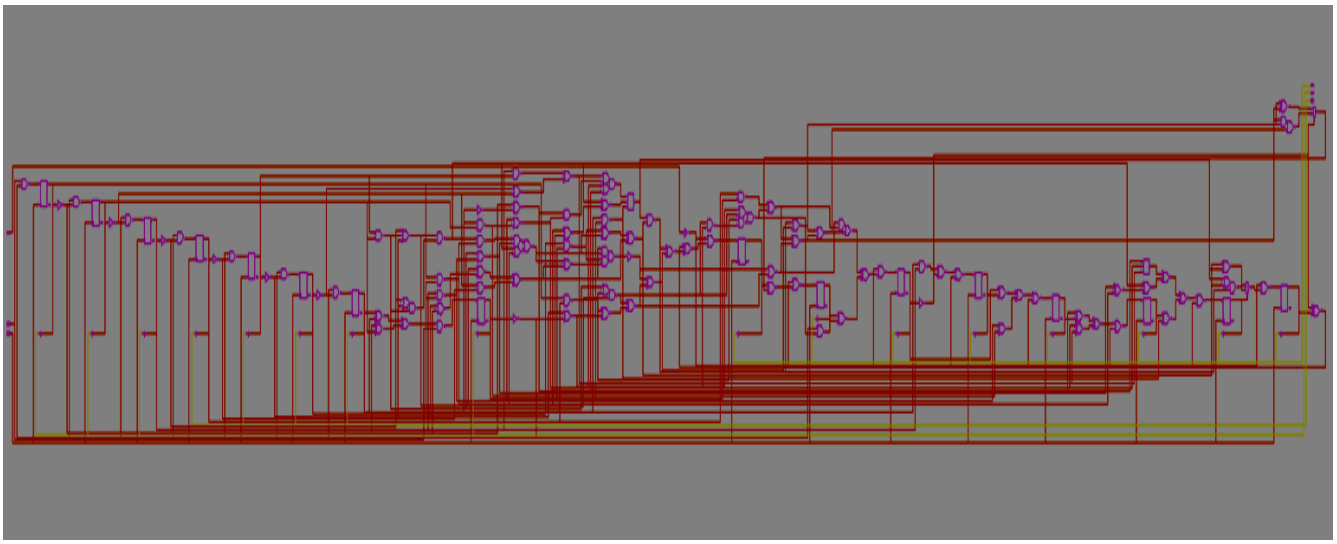


Block Diagram of Top Module:



The testable system is controlled by only one pin N/T (Normal/Test) and of the clock by giving the Enable and Clk Signal respectively as input to the LFSR. Nibble1 and Nibble2, which are the inputs to multiplier and outputs of LFSR have been pulled out as additional signals to observe them at the output of the system and to observe the LFSR patterns.

Circuit Diagram of Top Module using Design Vision and after compiling with class.v:



ATPG Report of Multiplier before inserting BIST:

```
run atpg -ndetects 1
 ATPG performed for stuck fault model using internal pattern source.
 ------------------------------------------------------------
 #patterns     #faults     #ATPG faults  test      process
 stored     detect/active  red/au/abort  coverage  CPU time
 ---------  -------------  ------------  --------  --------
 Begin deterministic ATPG: #uncollapsed_faults=446, abort_limit=10...
 19           438      8        0/0/0    98.21%      0.00
 25             8      0        0/0/0   100.00%      0.00

    Uncollapsed Stuck Fault Summary Report
 -----------------------------------------------
 fault class                    code   #faults
 -------------------------------  ----  ---------
 Detected                        DT       446
 Possibly detected               PT         0
 Undetectable                    UD         0
 ATPG untestable                 AU         0
 Not detected                    ND         0
 -----------------------------------------------
 total faults                          446
 test coverage                         100.00%
 fault coverage                        100.00%
 -----------------------------------------------
          Pattern Summary Report
 -----------------------------------------------
 #internal patterns                     25
    #basic_scan patterns                25
 -----------------------------------------------
TEST> run pattern_compression

 Pass 1: Reverse order pattern compression performed on 25 patterns.
```

```
 ---------------------------------------------
 #patterns     #faults     test      process
 stored     detect/active  coverage  CPU time
 ---------  -------------  --------  --------
 17           446      0   100.00%      0.00
 Compression pass 1 completed: #patterns_deleted=8, CPU time=0.00
```

ATPG Report after inserting BIST :

The 255 Patterns of LFSR were noted down and first 10 patterns followed by 20 patterns and then 30 patterns were tested on the multiplier by inserting an external pattern files in Tetramax.

The external pattern source file is as follows:

```
STIL 1.0 { Design 2005; }
Header {
  Title "  TetraMAX (TM)  A-2007.12-SP1-i080111_232011 STIL output";
  Date "Sun Apr 24 06:50:43 2016";
  History {
    Ann {*     Uncollapsed Stuck Fault Summary Report *}
    Ann {* ----------------------------------------------- *}
    Ann {* fault class                  code   #faults *}
    Ann {* ------------------------------  ----  --------- *}
    Ann {* Detected                      DT       446 *}
    Ann {* Possibly detected             PT         0 *}
    Ann {* Undetectable                  UD         0 *}
    Ann {* ATPG untestable               AU         0 *}
    Ann {* Not detected                  ND         0 *}
    Ann {* ----------------------------------------------- *}
    Ann {* total faults                        446 *}
    Ann {* test coverage                      100.00% *}
    Ann {* fault coverage                     100.00% *}
    Ann {* ----------------------------------------------- *}
    Ann {*  *}
    Ann {*           Pattern Summary Report *}
    Ann {* ----------------------------------------------- *}
    Ann {* #internal patterns                      17 *}
    Ann {*     #basic_scan patterns                17 *}
    Ann {* ----------------------------------------------- *}
    Ann {*  *}
    Ann {* rule  severity  #fails  description *}
    Ann {* ----  --------  ------  ---------------------------------- *}
    Ann {* N2    warning        1  unsupported construct *}
    Ann {*  *}
    Ann {* There are no clocks *}
    Ann {* There are no constraint ports *}
    Ann {* There are no equivalent pins *}
    Ann {* There are no net connections *}
  }
}
Signals {
  "Nibble1(3)" In; "Nibble1(2)" In; "Nibble1(1)" In; "Nibble1(0)" In; "Nibble2(3)" In;
  "Nibble2(2)" In; "Nibble2(1)" In; "Nibble2(0)" In; "Result(7)" Out; "Result(6)" Out;
  "Result(5)" Out; "Result(4)" Out; "Result(3)" Out; "Result(2)" Out; "Result(1)" Out;
  "Result(0)" Out;
}
```

```
SignalGroups {
  "_default_In_Timing_" = '"Nibble1(3)" + "Nibble1(2)" + "Nibble1(1)" +
  "Nibble1(0)" + "Nibble2(3)" + "Nibble2(2)" + "Nibble2(1)" + "Nibble2(0)"'; // #signals=8
  "_pi" = '"Nibble1(3)" + "Nibble1(2)" + "Nibble1(1)" + "Nibble1(0)" +
  "Nibble2(3)" + "Nibble2(2)" + "Nibble2(1)" + "Nibble2(0)"'; // #signals=8
  "_in" = '"Nibble1(3)" + "Nibble1(2)" + "Nibble1(1)" + "Nibble1(0)" +
  "Nibble2(3)" + "Nibble2(2)" + "Nibble2(1)" + "Nibble2(0)"'; // #signals=8
  "_default_Out_Timing_" = '"Result(7)" + "Result(6)" + "Result(5)" +
  "Result(4)" + "Result(3)" + "Result(2)" + "Result(1)" + "Result(0)"'; // #signals=8
  "_po" = '"Result(7)" + "Result(6)" + "Result(5)" + "Result(4)" + "Result(3)" +
  "Result(2)" + "Result(1)" + "Result(0)"'; // #signals=8
  "_out" = '"Result(7)" + "Result(6)" + "Result(5)" + "Result(4)" + "Result(3)" +
  "Result(2)" + "Result(1)" + "Result(0)"'; // #signals=8
}
Timing {
  WaveformTable "_default_WFT_" {
    Period '100ns';
    Waveforms {
      "_default_In_Timing_" { 0 { '0ns' D; } }
      "_default_In_Timing_" { 1 { '0ns' U; } }
      "_default_In_Timing_" { Z { '0ns' Z; } }
      "_default_In_Timing_" { N { '0ns' N; } }
      "_default_Out_Timing_" { X { '0ns' X; } }
      "_default_Out_Timing_" { H { '0ns' X; '40ns' H; } }
      "_default_Out_Timing_" { T { '0ns' X; '40ns' T; } }
      "_default_Out_Timing_" { L { '0ns' X; '40ns' L; } }
    }
  }
}
ScanStructures {
  // Uncomment and modify the following to suit your design
  // ScanChain "chain_name" { ScanIn "chain_input_name"; ScanOut "chain_output_name"; }
}
PatternBurst "_burst_" {
  PatList { "_pattern_" {
  }
}}
PatternExec {
  PatternBurst "_burst_";
}
Procedures {
  "capture" {
    W "_default_WFT_";
    C { "Nibble1(1)"=0; "Nibble2(1)"=0; "Nibble1(0)"=0; "Nibble2(0)"=0; "Nibble1(3)"=0; "Nibble2(3)"=0;
      "Nibble1(2)"=0; "Nibble2(2)"=0; }
    "forcePI": V { "_pi"=\r8 # ; "_po"=\r8 X ; }
    "measurePO": V { "_po"=\r8 # ; }
  }
  // Uncomment and modify the following to suit your design
  // load_unload {
    // V { } // force clocks off and scan enable pins active
    // Shift { V { _si=#; _so=#; }} // pulse shift clocks
  // }
}
MacroDefs {
}
Pattern "_pattern_" {
  W "_default_WFT_";
  "precondition all Signals": C { "_pi"=\r8 0 ; "_po"=\r8 X ; }
```

"pattern 0": Call "capture" {
"_pi"=11111111; "_po"=HHHLLLLH; }
"pattern 1": Call "capture" {
"_pi"=01111111; "_po"=LHHLHLLH; }
"pattern 2": Call "capture" {
"_pi"=00111111; "_po"=LLHLHHLH; }
"pattern 3": Call "capture" {
"_pi"=10011111; "_po"=HLLLLHHH; }
"pattern 4": Call "capture" {
"_pi"=01001111; "_po"=LLHHHHLL; }
"pattern 5": Call "capture" {
"_pi"=10100111; "_po"=LHLLLHHL; }
"pattern 6": Call "capture" {
"_pi"=11010011; "_po"=LLHLLHHH; }
"pattern 7": Call "capture" {
"_pi"=11101001; "_po"=LHHHHHHL; }
"pattern 8": Call "capture" {
"_pi"=11110100; "_po"=LLHHHHLL; }
"pattern 9": Call "capture" {
"_pi"=01111010; "_po"=LHLLLHHL; }
"pattern 10": Call "capture" {
"_pi"=10111101; "_po"=HLLLHHHH; }
"pattern 11": Call "capture" {
"_pi"=01011110; "_po"=LHLLLHHL; }
"pattern 12": Call "capture" {
"_pi"=00101111; "_po"=LLLHHHHHL; }
"pattern 13": Call "capture" {
"_pi"=10010111; "_po"=LLHHHHHH; }
"pattern 14": Call "capture" {
"_pi"=01001011; "_po"=LLHLHHLL; }
"pattern 15": Call "capture" {
"_pi"=10100101; "_po"=LLHHLLHL; }
"pattern 16": Call "capture" {
"_pi"=01010010; "_po"=LLLL1LHL; }
"pattern 17": Call "capture" {
"_pi"=00101001; "_po"=LLLHLLHL; }
"pattern 18": Call "capture" {
"_pi"=00010100; "_po"=LLLLLHLL; }
"pattern 19": Call "capture" {
"_pi"=00001010; "_po"=LLLLLLLL; }
"pattern 20": Call "capture" {
"_pi"=10000101; "_po"=LLHLHLLL; }
"pattern 21": Call "capture" {
"_pi"=11000010; "_po"=LLLHHLLL; }
"pattern 22": Call "capture" {
"_pi"=01100001; "_po"=LLLLLHHL; }
"pattern 23": Call "capture" {
"_pi"=10110000; "_po"=LLLLLLLL; }
"pattern 24": Call "capture" {
"_pi"=11011000; "_po"=LHHLHLLL; }
"pattern 25": Call "capture" {
"_pi"=11101100; "_po"=HLHLHLLL; }
"pattern 26": Call "capture" {
"_pi"=01110110; "_po"=LLHLHLHL; }
"pattern 27": Call "capture" {
"_pi"=10111011; "_po"=LHHHHLLH; }
"pattern 28": Call "capture" {
"_pi"=11011101; "_po"=HLHLHLLH; }
"pattern 29": Call "capture" {

"_pi"=01101110; "_po"=LHLHLHLL; }

}

(A). ATPG Report obtained with first 10 patterns:

```
run atpg -ndetects 1
 ATPG performed for stuck fault model using external pattern source.
 Simulation performed for 446 faults on circuit size of 105 gates.
 ----------------------------------------------
 #patterns     #faults     test      process
 stored     detect/active  coverage  CPU time
 ---------  -------------  --------  --------
 10           425     21    95.29%      0.00
 Fault simulation completed: #patterns=10, CPU time=0.00

    Uncollapsed Stuck Fault Summary Report
 -------------------------------------------------
 fault class                    code   #faults
 -------------------------------  ----  ---------
 Detected                       DT        425
 Possibly detected              PT          0
 Undetectable                   UD          0
 ATPG untestable                AU          0
 Not detected                   ND         21
 -------------------------------------------------
 total faults                            446
 test coverage                          95.29%
 fault coverage                         95.29%
 -------------------------------------------------
          Pattern Summary Report
 -------------------------------------------------
 #internal patterns                      10
    #basic_scan patterns                 10
 #external patterns (/home/eng/m/mrs150330/bistpatterns)     10
    #basic_scan patterns                 10
 -------------------------------------------------
TEST> run pattern_compression

 Pass 1: Reverse order pattern compression performed on 10 patterns.
 ----------------------------------------------
 #patterns     #faults     test      process
 stored     detect/active  coverage  CPU time
 ---------  -------------  --------  --------
 10           425     21    95.29%      0.00
 Compression pass 1 completed: #patterns_deleted=0, CPU time=0.00
```

(B). ATPG Report obtained with first 20 patterns:

```
run atpg -ndetects 1
 ATPG performed for stuck fault model using external pattern source.
 Simulation performed for 446 faults on circuit size of 105 gates.
 ----------------------------------------------
 #patterns     #faults     test      process
 stored     detect/active  coverage  CPU time
```

```
---------  -------------  --------  --------
13           432     14    96.86%      0.00
Fault simulation completed: #patterns=20, CPU time=0.00

    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                   code   #faults
------------------------------  ----  ---------
Detected                       DT       432
Possibly detected              PT         0
Undetectable                   UD         0
ATPG untestable                AU         0
Not detected                   ND        14
-----------------------------------------------
total faults                            446
test coverage                          96.86%
fault coverage                         96.86%
-----------------------------------------------
         Pattern Summary Report
-----------------------------------------------
#internal patterns                      13
   #basic_scan patterns                 13
#external patterns (/home/eng/m/mrs150330/bistpatterns)     20
   #basic_scan patterns                 20
-----------------------------------------------
TEST> run pattern_compression

Pass 1: Reverse order pattern compression performed on 13 patterns.
-------------------------------------------
#patterns     #faults     test      process
stored     detect/active  coverage  CPU time
---------  -------------  --------  --------
13           432     14    96.86%      0.00
Compression pass 1 completed: #patterns_deleted=0, CPU time=0.00
```

(C). ATPG Report obtained with first 30 patterns:

```
run atpg -ndetects 1
ATPG performed for stuck fault model using external pattern source.
Simulation performed for 446 faults on circuit size of 105 gates.
-------------------------------------------
#patterns     #faults     test      process
stored     detect/active  coverage  CPU time
---------  -------------  --------  --------
16           439     7    98.43%      0.00
Fault simulation completed: #patterns=30, CPU time=0.00

    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                   code   #faults
```

```
------------------------------  ----  ---------
Detected                      DT       439
Possibly detected             PT         0
Undetectable                  UD         0
ATPG untestable               AU         0
Not detected                  ND         7
-------------------------------------------------
total faults                            446
test coverage                         98.43%
fault coverage                        98.43%
-------------------------------------------------
          Pattern Summary Report
-------------------------------------------------
#internal patterns                       16
    #basic_scan patterns                 16
#external patterns (/home/eng/m/mrs150330/bistpatterns)     30
-------------------------------------------------
TEST> run pattern_compression

 Pass 1: Reverse order pattern compression performed on 16 patterns.
 -----------------------------------------
 #patterns     #faults     test      process
 stored     detect/active  coverage  CPU time
 ---------  -------------  --------  --------
 15           439      7    98.43%      0.00
 Compression pass 1 completed: #patterns_deleted=1, CPU time=0.00
```

Result:

10 Patterns: fault coverage 95.29%
20 Patterns: fault coverage 96.86%
30 Patterns: fault coverage 98.43%

Area Report before inserting BIST:

```
****************************************
Report : area
Design : mul
Version: H-2013.03-SP4
Date   : Sun Apr 24 21:27:49 2016
****************************************

Library(s) Used:

    class (File: /proj/cad/synopsys/synopsys-2013.lnx86_64/syn/libraries/syn/class.db)

Number of ports:                        16
Number of nets:                         74
Number of cells:                        66
Number of combinational cells:          66
Number of sequential cells:              0
Number of macros/black boxes:            0
Number of buf/inv:                       8
Number of references:                   14

Combinational area:             127.000000
Buf/Inv area:                     8.000000
Noncombinational area:            0.000000
```

Macro/Black Box area: 0.000000
Net Interconnect area: undefined (Wire load has zero net area)

Total cell area: 127.000000

Timing Report before inserting BIST:

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : mul
Version: H-2013.03-SP4
Date   : Sun Apr 24 21:23:02 2016
****************************************

Operating Conditions: nom_pvt   Library: class
Wire Load Model Mode: top

  Startpoint: Nibble1[1] (input port)
  Endpoint: Result[6] (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  mul                05x05                 class

  Point                                   Incr       Path
  ------------------------------------------------------------
  input external delay                    0.00       0.00 f
  Nibble1[1] (in)                         0.00       0.00 f
  U55/Z (ND2)                             0.85       0.85 r
  U54/Z (IV)                              0.37       1.23 f
  U53/Z (AN3)                             1.07       2.30 f
  U51/Z (NR2)                             1.52       3.82 r
  U50/Z (IV)                              0.30       4.12 f
  U39/Z (ND2)                             0.69       4.81 r
  U38/Z (AO2)                             0.86       5.68 f
  U24/Z (OR2)                             0.93       6.61 f
  U23/Z (AO2)                             1.49       8.10 r
  U9/Z (IV)                               0.23       8.33 f
  U8/Z (NR2)                              1.48       9.81 r
  U7/Z (EN)                               1.31      11.12 r
  U6/Z (EO)                               1.09      12.21 f
  Result[6] (out)                         0.00      12.21 f
  data arrival time                                 12.21
  ------------------------------------------------------------
  (Path is unconstrained)
```

Area Report After BIST:

```
****************************************
```

```
Report : area
Design : TopModule
Version: H-2013.03-SP4
Date   : Sat Apr 23 21:40:32 2016
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    class (File: /proj/cad/synopsys/synopsys-2013.lnx86_64/syn/libraries/syn/class.db)

Number of ports:                19
Number of nets:                122
Number of cells:               119
Number of combinational cells:         103
Number of sequential cells:            16
Number of macros/black boxes:           0
Number of buf/inv:                     11
Number of references:                  17

Combinational area:            196.000000
Buf/Inv area:                   11.000000
Noncombinational area:         112.000000
Macro/Black Box area:            0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:               308.000000
***** End Of Report *****
```

Timing Report After BIST:

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : TopModule
Version: H-2013.03-SP4
Date   : Sat Apr 23 21:45:51 2016
****************************************

Operating Conditions: nom_pvt   Library: class
Wire Load Model Mode: top

  Startpoint: Mod1/LFSR_Out_reg[1]
              (rising edge-triggered flip-flop)
  Endpoint: Nibble2[1] (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
```

TopModule 05x05 class

Point	Incr	Path
Mod1/LFSR_Out_reg[1]/CP (FD1)	0.00	0.00 r
Mod1/LFSR_Out_reg[1]/Q (FD1)	2.16	2.16 r
Nibble2[1] (inout)	0.00	2.16 r
data arrival time	2.16	

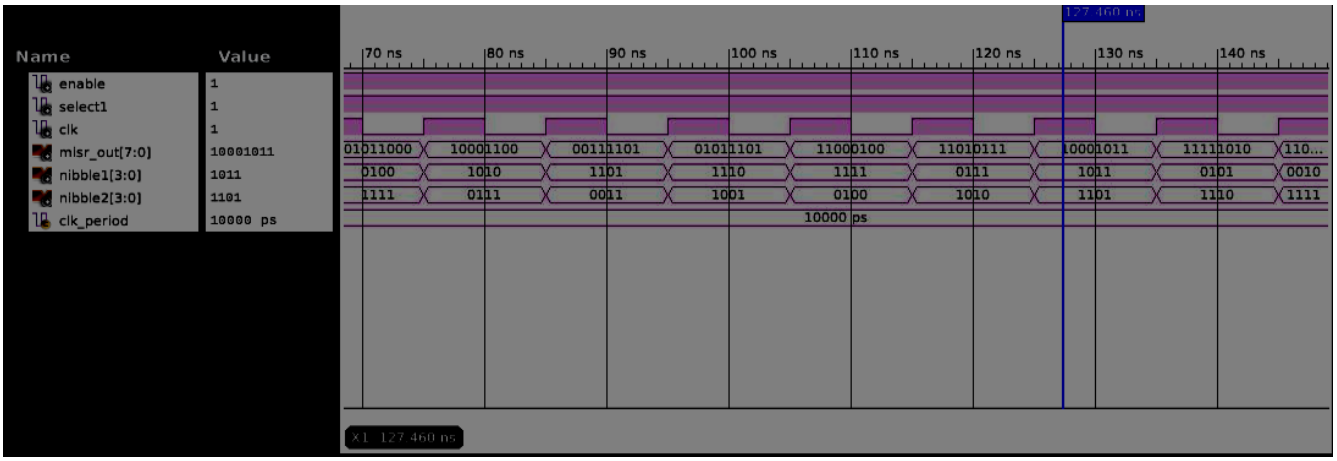
(Path is unconstrained)

Content of the Compressor after applying the following number patterns:
(Note: Nibble1+Nibble2 : corresponds to the LFSR Pattern that is inserted to the multiplier and

the corresponding MISR Output is obtained in the next positive edge clock cycle)

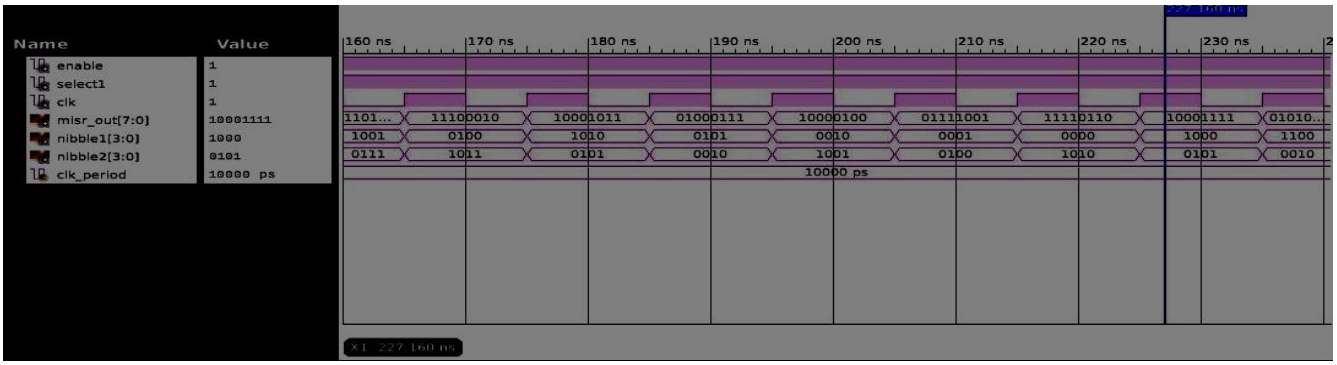
1. 10th pattern : 10001011

The content of compressor after applying first 10 patterns is observed at 125th cycle as shown in the waveform obtained below:



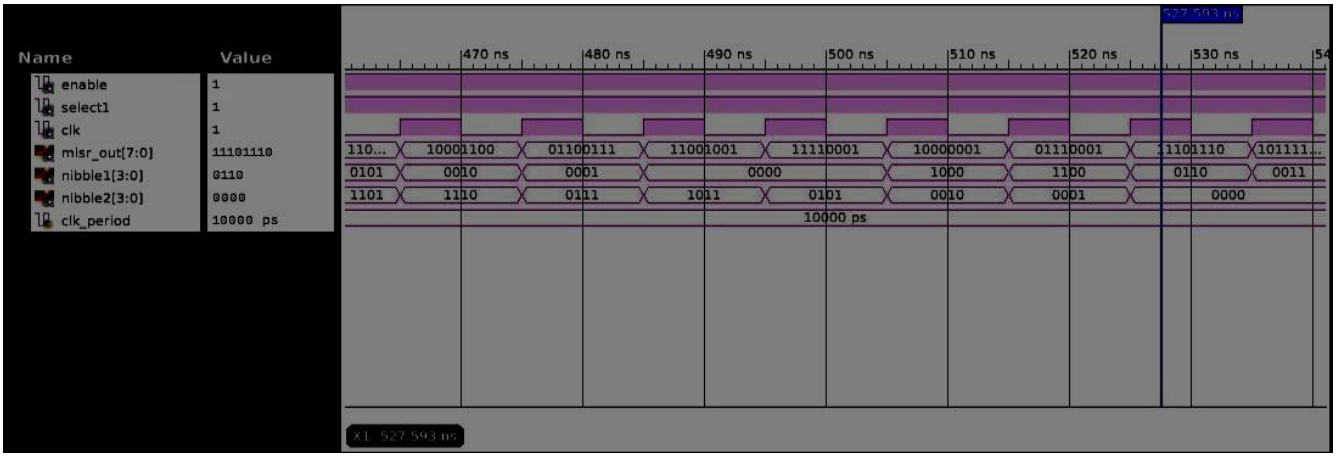
2. 20th Pattern : 10001111

The content of compressor after applying first 20 patterns is observed at 225th cycle as shown in the waveform obtained below:



3. 50th Pattern : 11101110

The content of compressor after applying first 50 patterns is observed at 525th cycle as shown in the waveform obtained below:



4. 100th Pattern : 00100010

The content of compressor after applying first 100 patterns is observed at 1025th cycle as shown in the waveform obtained below: