
STM32
CubeMX

1. Description

1.1. Project

Project Name	STM32F769I_DISCO
Board Name	custom
Generated with:	STM32CubeMX 6.14.1
Date	06/15/2025

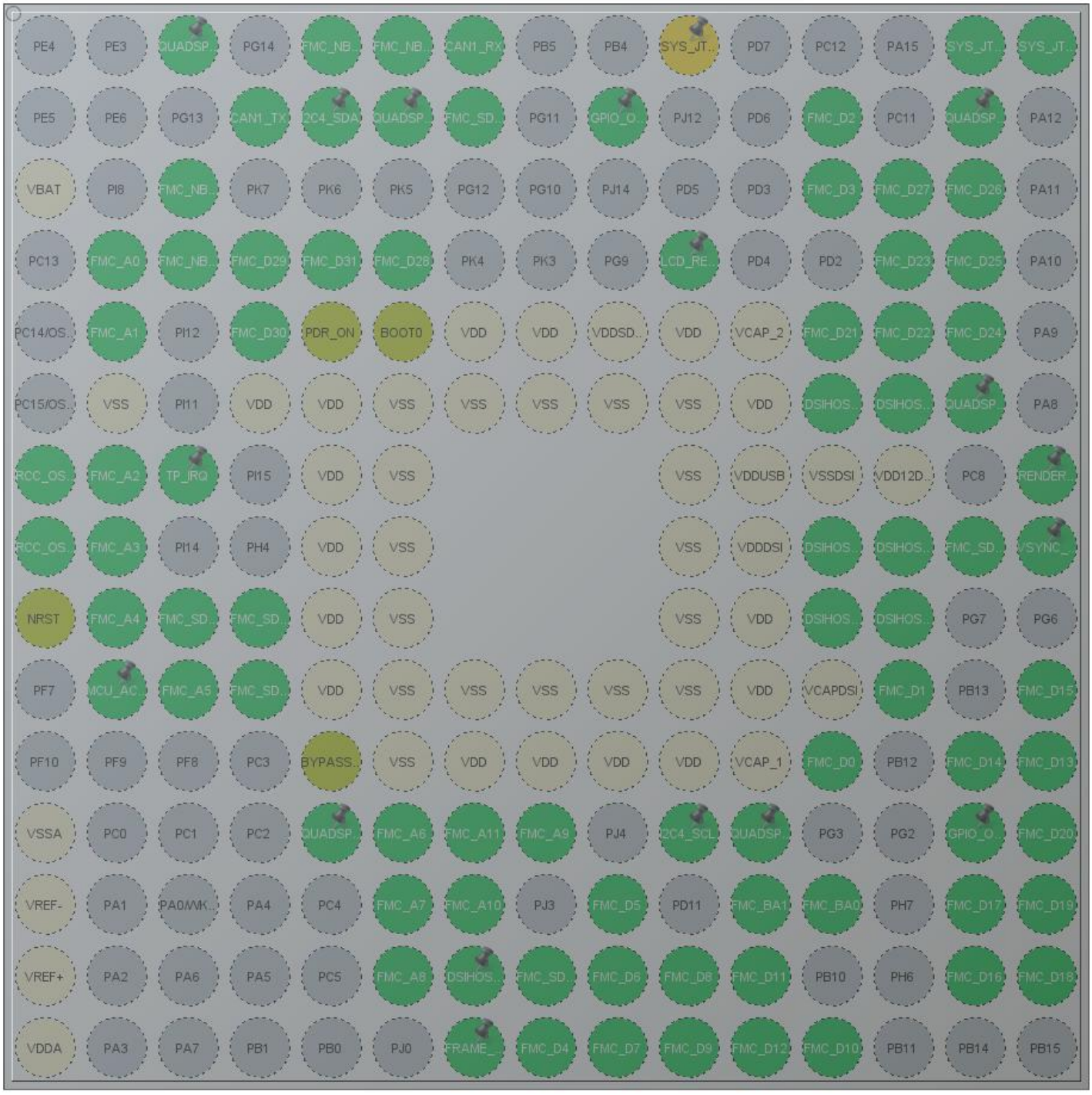
1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x9
MCU name	STM32F769NIHx
MCU Package	TFBGA216
MCU Pin number	216

1.3. Core(s) information

Core(s)	Arm Cortex-M7

2. Pinout Configuration



TFBGA216 (Top view)

3. Pins Configuration

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A3	PE2	I/O	QUADSPI_BK1_IO2	
A5	PE1	I/O	FMC_NBL1	
A6	PE0	I/O	FMC_NBL0	
A7	PB8	I/O	CAN1_RX	
A10	PB3 *	I/O	SYS_JTDO-SWO	
A14	PA14	I/O	SYS_JTCK-SWCLK	
A15	PA13	I/O	SYS_JTMS-SWDIO	
B4	PB9	I/O	CAN1_TX	
B5	PB7	I/O	I2C4_SDA	
B6	PB6	I/O	QUADSPI_BK1_NCS	
B7	PG15	I/O	FMC_SDNCAS	
B9	PJ13 **	I/O	GPIO_Output	
B12	PD0	I/O	FMC_D2	
B14	PC10	I/O	QUADSPI_BK1_IO1	
C1	VBAT	Power		
C3	PI4	I/O	FMC_NBL2	
C12	PD1	I/O	FMC_D3	
C13	PI3	I/O	FMC_D27	
C14	PI2	I/O	FMC_D26	
D2	PF0	I/O	FMC_A0	
D3	PI5	I/O	FMC_NBL3	
D4	PI7	I/O	FMC_D29	
D5	PI10	I/O	FMC_D31	
D6	PI6	I/O	FMC_D28	
D10	PJ15 **	I/O	GPIO_Output	LCD_RESET
D13	PH15	I/O	FMC_D23	
D14	PI1	I/O	FMC_D25	
E2	PF1	I/O	FMC_A1	
E4	PI9	I/O	FMC_D30	
E5	PDR_ON	Reset		
E6	BOOT0	Boot		
E7	VDD	Power		
E8	VDD	Power		
E9	VDDSDMMC	Power		
E10	VDD	Power		
E11	VCAP_2	Power		

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
E12	PH13	I/O	FMC_D21	
E13	PH14	I/O	FMC_D22	
E14	PI0	I/O	FMC_D24	
F2	VSS	Power		
F4	VDD	Power		
F5	VDD	Power		
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F11	VDD	Power		
F12	DSIHOST_D1P	MonoIO	DSIHOST_D1P	
F13	DSIHOST_D1N	MonoIO	DSIHOST_D1N	
F14	PC9	I/O	QUADSPI_BK1_IO0	
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	
G2	PF2	I/O	FMC_A2	
G3	PI13	I/O	GPIO_EXTI13	TP_IRQ
G5	VDD	Power		
G6	VSS	Power		
G10	VSS	Power		
G11	VDDUSB	Power		
G12	VSSDSI	Power		
G13	VDD12DSI	Power		
G15	PC7 **	I/O	GPIO_Output	RENDER_TIME
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
H2	PF3	I/O	FMC_A3	
H5	VDD	Power		
H6	VSS	Power		
H10	VSS	Power		
H11	VDDDSI	Power		
H12	DSIHOST_CKP	MonoIO	DSIHOST_CKP	
H13	DSIHOST_CKN	MonoIO	DSIHOST_CKN	
H14	PG8	I/O	FMC_SDCLK	
H15	PC6 **	I/O	GPIO_Output	VSYNC_FREQ
J1	NRST	Reset		
J2	PF4	I/O	FMC_A4	
J3	PH5	I/O	FMC_SDNWE	
J4	PH3	I/O	FMC_SDNE0	

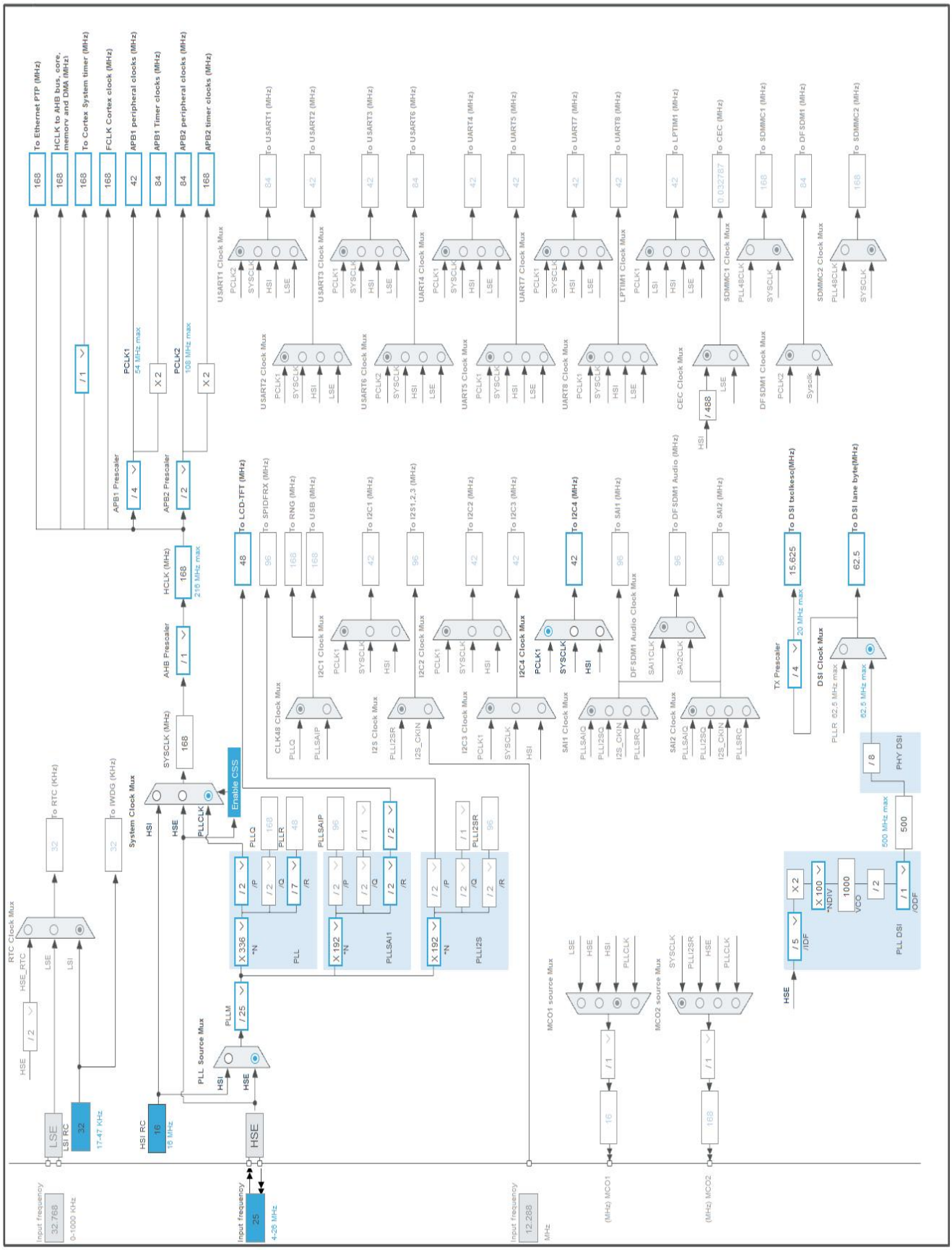
Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
J5	VDD	Power		
J6	VSS	Power		
J10	VSS	Power		
J11	VDD	Power		
J12	DSIHOST_D0P	MonoIO	DSIHOST_D0P	
J13	DSIHOST_D0N	MonoIO	DSIHOST_D0N	
K2	PF6 **	I/O	GPIO_Output	MCU_ACTIVE
K3	PF5	I/O	FMC_A5	
K4	PH2	I/O	FMC_SDCKE0	
K5	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K11	VDD	Power		
K12	VCAPDSI	Power		
K13	PD15	I/O	FMC_D1	
K15	PD10	I/O	FMC_D15	
L5	BYPASS_REG	Reset		
L6	VSS	Power		
L7	VDD	Power		
L8	VDD	Power		
L9	VDD	Power		
L10	VDD	Power		
L11	VCAP_1	Power		
L12	PD14	I/O	FMC_D0	
L14	PD9	I/O	FMC_D14	
L15	PD8	I/O	FMC_D13	
M1	VSSA	Power		
M5	PB2	I/O	QUADSPI_CLK	
M6	PF12	I/O	FMC_A6	
M7	PG1	I/O	FMC_A11	
M8	PF15	I/O	FMC_A9	
M10	PD12	I/O	I2C4_SCL	
M11	PD13	I/O	QUADSPI_BK1_IO3	
M14	PJ5 **	I/O	GPIO_Output	
M15	PH12	I/O	FMC_D20	
N1	VREF-	Power		

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
N6	PF13	I/O	FMC_A7	
N7	PG0	I/O	FMC_A10	
N9	PE8	I/O	FMC_D5	
N11	PG5	I/O	FMC_BA1	
N12	PG4	I/O	FMC_BA0	
N14	PH9	I/O	FMC_D17	
N15	PH11	I/O	FMC_D19	
P1	VREF+	Power		
P6	PF14	I/O	FMC_A8	
P7	PJ2	I/O	DSIHOST_TE	
P8	PF11	I/O	FMC_SDNRAS	
P9	PE9	I/O	FMC_D6	
P10	PE11	I/O	FMC_D8	
P11	PE14	I/O	FMC_D11	
P14	PH8	I/O	FMC_D16	
P15	PH10	I/O	FMC_D18	
R1	VDDA	Power		
R7	PJ1 **	I/O	GPIO_Output	FRAME_RATE
R8	PE7	I/O	FMC_D4	
R9	PE10	I/O	FMC_D7	
R10	PE12	I/O	FMC_D9	
R11	PE15	I/O	FMC_D12	
R12	PE13	I/O	FMC_D10	

** The pin is affected with an I/O function

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x9
MCU	STM32F769NIHx
Datasheet	DS11532_Rev4

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

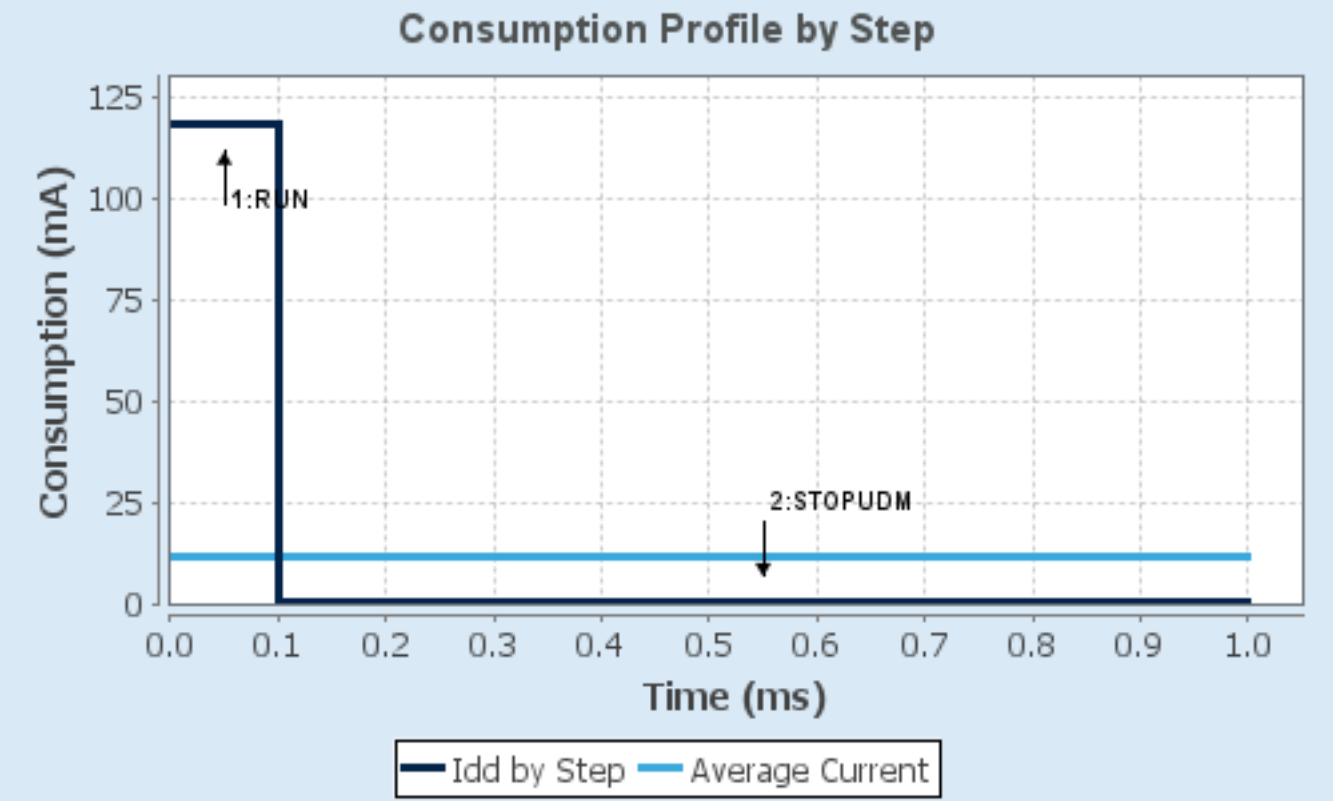
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ICTM FLASH-SingleBank REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	118 mA	130 µA
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	93.71	104.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	11.92 mA
Battery Life	2 days, 4 hours	Average DMIPS	462.24005 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
125
100
75
50
25
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Software Project

2.1. Project Settings

Name	Value
Project Name	STM32F769I_DISCO
Project Folder	D:\workspace_DorcuM\Licenta\MyApplication_2
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.17.2
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x1000
Minimum Stack Size	0x1000

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_DSIHOST_DSI_Init	DSIHOST
4	MX_LTDC_Init	LTDC
5	MX_FMC_Init	FMC
6	MX_QUADSPI_Init	QUADSPI
7	MX_DMA2D_Init	DMA2D
8	MX_I2C4_Init	I2C4
9	MX_LIBJPEG_Init	LIBJPEG
10	MX_CRC_Init	CRC
11	MX_CAN1_Init	CAN1

Rank	Function Name	Peripheral Instance Name
12	MX_TIM14_Init	TIM14
14	MX_TouchGFX_Init	STMicroelectronics.X-CUBE-TOUCHGFX.4.25.0
15	MX_TouchGFX_Process	STMicroelectronics.X-CUBE-TOUCHGFX.4.25.0

3. Peripherals and Middlewares Configuration

3.1. CAN1

mode: Activated

3.1.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**21 ***
Time Quantum	**500.0 ***
Time Quanta in Bit Segment 1	**15 Times ***
Time Quanta in Bit Segment 2	**4 Times ***
Time for one Bit	**10000 ***
Baud Rate	**100000 ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

3.2. CORTEX_M7

3.2.1. Parameter Settings:

Speculation default mode Settings:

Speculation default mode	Disabled

Cortex Interface Settings:

Flash Interface	AXI Interface
ART ACCELERATOR	Disabled
Instruction Prefetch	**Enabled ***
CPU ICache	**Enabled ***
CPU DCache	**Enabled ***

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	**Background Region Privileged accesses only + MPU Disabled**

	during hard fault, NMI and FAULTMASK handlers *

Cortex Memory Protection Unit Region 0 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x20000000 ***
MPU Region Size	**512KB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	level 0
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	**ENABLE ***
MPU Bufferable Permission	**ENABLE ***

Cortex Memory Protection Unit Region 1 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x90000000 ***
MPU Region Size	**512MB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	level 0
MPU Access Permission	ALL ACCESS NOT PERMITTED
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 2 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x90000000 ***
MPU Region Size	**64MB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	level 0
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	**ENABLE ***
MPU Bufferable Permission	**ENABLE ***

Cortex Memory Protection Unit Region 3 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0xC0000000 ***

MPU Region Size	**512MB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	level 0
MPU Access Permission	ALL ACCESS NOT PERMITTED
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 4 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0xC0000000 ***
MPU Region Size	**16MB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	level 0
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	**ENABLE ***
MPU Bufferable Permission	**ENABLE ***

Cortex Memory Protection Unit Region 5 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 6 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region	Disabled

3.3. CRC

mode: Activated

3.3.1. Parameter Settings:

Basic Parameters:

Default Polynomial State	Enable
Default Init Value State	Enable

Advanced Parameters:

Input Data Inversion Mode	None
Output Data Inversion Mode	Disable
Input Data Format	Bytes

3.4. DMA2D

mode: Activated

3.4.1. Parameter Settings:

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	ARGB8888
Output Offset	0

Foreground layer Configuration:

DMA2D Input Color Mode	ARGB8888
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0
DMA2D ALPHA Inversion	Regular Alpha
DMA2D Red and Blue swap	Regular mode (RGB or ARGB)

3.5. DSIHOST

DSIHost: Adapted Command Mode with TE Pin

3.5.1. DSI Clocks:

from PLLDSI:

Pllndiv	100
Pllodf	DSI_PLL_OUT_DIV1
Pllidf	DSI_PLL_IN_DIV5
High Speed Clock - PLLDSI Output	500000
Lane Byte Clock	62500
Tx Escape Ckdiv	4
Transmission Escape Clock	15625
Time Out Clock	62500

from PLLR:

Lane Byte Clock	48000
Transmission Escape Clock	12000
Time Out Clock	48000

3.5.2. Timeout Counters:

Time Out Clock Setting:

Time Out Clock Divider	1
Time Out Clock - from PLLDSI	62500

Contention Error Detection:

High-speed transmission time-out	0
No High-speed transmission time-out	
Low-power reception time-out	0
No Low-power reception time-out	

Peripheral Response:

High-speed read time-out	0
Resulting Timing High-speed read time-out	0
Low-power read time-out	0
Resulting Timing Low-power read time-out	0
High-speed write time-out	0
Resulting Timing High-speed write time-out	0
Low-power write time-out	0
Resulting Timing Low-power write time-out	0
BTA time-out	0
Resulting Timing for BTA time-out	0
High-speed write presp mode	Normal Behavior

3.5.3. Data and Clock Lanes:

Basic Settings:

Number of Lanes	**Two Data Lanes ***
Automatic Clock Lane Control	Clock lane is always provided
Bus Turn Around Request is	Enabled

Flow Control - Configuration:

CRC Reception	Disabled
ECC Reception	Disabled
EoTP Reception is	Disabled
EoTP Transmission is	Disabled
Acknowledge Request after Each Transmission	**Enabled ***
Tearing Effect Acknowledge Request Enable	**Enabled ***

Flow Control - Packet Analyzer Configuration:

CRC Error Interrupt	Disable
ECC Errors Interrupt	Disable
EoTP Error Interrupt	Disable
Packet Size Error Interrupt	Disable

Acknowledge Errors Interrupt	Disable
PHY related Errors Interrupt	Disable

3.5.4. PHY Timings:

LP to HS and HS to LP Transitions Timings:

Minimum wait period to request a HS transmission after the Stop state (min is 1 cycle of escape clock)	0
Resulting Minimum wait period to request a HS transmission after the Stop state (min is 1 cycle of escape clock)	0

3.5.5. Commands:

APB Interface Error Configuration:

Generic Command Error Interrupt	Disable

Transmission Mode for Commands::

Generic Short Write Zero Parameter	**Low Power Transmission ***
Generic Short Write One Parameter	**Low Power Transmission ***
Generic Short Write Two parameters	**Low Power Transmission ***
Generic Short Read Zero parameter	**Low Power Transmission ***
Generic Short Read One parameter	**Low Power Transmission ***
Generic Short Read Two parameters	**Low Power Transmission ***
Generic Long Write	**Low Power Transmission ***
DCS Short Write Zero parameter	**Low Power Transmission ***
DCS Short Write One parameter	**Low Power Transmission ***
DCS Short Read Zero parameter	**Low Power Transmission ***
DCS Long Write	**Low Power Transmission ***
Maximum Read Packet Size Command	**Low Power Transmission ***

3.5.6. Display Interface:

Basic Settings:

Display ID	0
Color Coding	RGB565 (16 bits) - DSI mode

Specific Command Mode Settings:

Maximum Command Size	480
The Refresh of the Display Frame Buffer is Triggered	**manually by Enabling the LTDC ***

Tearing Effect Source	External Source
Polarity of the External Tearing Effect Source	Rising Edge

3.5.7. LTDC Interface:

Clocking:

LTDC Pixel Clock (from Clock tree)	48

Frame Vertical Timings:

VSA: Vertical Synchronism Active duration (set in LTDC)	2
VBP: Vertical Back-Porch duration (set in LTDC)	1
VFP: Vertical Front-Porch duration (set in LTDC)	1
VACT: Vertical Active duration (set in LTDC)	800

Frame Horizontal Timings:

HSA: Horizontal Synchronism Active duration (set in LTDC)	2
HBP: Horizontal Back-Porch duration (set in LTDC)	1
HACT: Horizontal Active duration (set in LTDC)	480
HLINE: Horizontal Line duration (set in LTDC)	484

Polarity of the Control Signals:

VSYNC Polarity (set in LTDC)	DSI_VSYNC_ACTIVE_LOW
HSYNC Polarity (set in LTDC)	DSI_HSYNC_ACTIVE_LOW
Data Enable Polarity (set in LTDC)	DSI_DATA_ENABLE_ACTIVE_HIGH

Interface:

The DSI is halting the LTDC synchronously	On a Falling Edge of VSYNC

Interface Error Configuration:

LTDC FIFO Overflow Error Interrupt is	**Enabled ***

3.6. FMC

SDRAM 1

Clock and chip enable: SDCKE0+SDNE0

Internal bank number: 4 banks

Address: 12 bits

Data: 32 bits

Byte enable: 32-bit byte enable

3.6.1. SDRAM 1:

SDRAM control:

Bank	SDRAM bank 1
Number of column address bits	8 bits
Number of row address bits	12 bits
CAS latency	**3 memory clock cycles ***
Write protection	Disabled
SDRAM common clock	**2 HCLK clock cycles ***
SDRAM common burst read	**Enabled ***
SDRAM common read pipe delay	0 HCLK clock cycle

SDRAM timing in memory clock cycles:

Load mode register to active delay	**2 ***
Exit self-refresh delay	**7 ***
Self-refresh time	**4 ***
SDRAM common row cycle delay	**7 ***
Write recovery time	**2 ***
SDRAM common row precharge delay	**2 ***
Row to column delay	**3 ***

3.7. I2C4

I2C: I2C

3.7.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x00A0A3F7 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

3.8. LTDC

Display Type: RGB565 (16 bits) - DSI mode

3.8.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	**2 ***
Horizontal Back Porch	**1 ***
Active Width	**480 ***
Horizontal Front Porch	**1 ***
HSync Width	1
Accumulated Horizontal Back Porch Width	2
Accumulated Active Width	482
Total Width	483

Synchronization for Height:

Vertical Synchronization Height	**2 ***
Vertical Back Porch	**1 ***
Active Height	**800 ***
Vertical Front Porch	**1 ***
VSync Height	1
Accumulated Vertical Back Porch Height	2
Accumulated Active Height	802
Total Height	803

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

Layer Default Color:

Red	0
Green	0
Blue	0

3.8.2. Layer Settings:

Layer Default Color:

Layer 0 - Alpha	0
Layer 0 - Blue	0
Layer 0 - Green	0

Layer 0 - Red	0

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	**480 ***
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	**800 ***

Pixel Parameters:

Layer 0 - Pixel Format	**RGB565 ***

Blending:

Layer 0 - Alpha constant for blending	**255 ***
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	0
Layer 0 - Color Frame Buffer Line Length (Image Width)	**480 ***
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	**800 ***

Number of Layers:

Number of Layers	**1 layer ***

3.9. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

3.9.1. Parameter Settings:

General Parameters:

Clock Prescaler	**1 ***
Fifo Threshold	**16 ***
Sample Shifting	**Sample Shifting Half Cycle ***
Flash Size	**25 ***
Chip Select High Time	**4 Cycles ***
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

3.10. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

3.10.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Disabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 2

3.11. SYS

Debug: Serial Wire

Timebase Source: TIM6

3.12. TIM14

mode: Activated

3.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**83 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

3.13. FREERTOS

Interface: CMSIS_V2

3.13.1. Config parameters:

API:

FreeRTOS API	CMSIS v2

Versions:

FreeRTOS version	10.2.1
CMSIS-RTOS version	2.00

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	**80000 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	**Enabled ***
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

3.13.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

3.13.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled

Project settings (see parameter description first):

Use FW pack heap file	Enabled

3.14. LIBJPEG

mode: Enabled

3.14.1. Config parameters:

Version:

LIBJPEG version	8d

MW configuration:

Data Stream management type	Stdio
FREERTOS	Enabled
HAVE_BOOLEAN	Undefined

General Settings:

Use FREERTOS Memory Allocator	Enabled

RGB scanline format:

RGB_ORDERING	**BGR ***

3.15. STMicroelectronics.X-CUBE-TOUCHGFX.4.25.0

mode: GraphicsJjApplication

3.15.1. TouchGFX Generator:

Display:

Interface	**Parallel RGB (LTDC) ***
Framebuffer Pixel Format (LTDC)	RGB565
Width (LTDC)	480
Height (LTDC)	800
Use Larger Framebuffer Stride	No
Framebuffer Strategy	**Double Buffer ***
Buffer Location	By Allocation

Driver:

Application Tick Source	Custom
Use DMA2D Accelerator (ChromART)	**Yes ***
Real-Time Operating System	CMSIS_RTOS_V2

Additional Features:

External Data Reader	Disabled
Vector Rendering	**Software ***
Vector Font Rendering	**Enabled ***

Video Decoding:

Type	**Software ***
Concurrent videos	1
Strategy	Direct to Framebuffer
Orientation	**Rotated ***

*** User modified value**

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
CAN1	PB8	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB9	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
DSIHOST	DSIHOST_D1P	DSIHOST_D1P	n/a	n/a	n/a	
	DSIHOST_D1N	DSIHOST_D1N	n/a	n/a	n/a	
	DSIHOST_CKP	DSIHOST_CKP	n/a	n/a	n/a	
	DSIHOST_CKN	DSIHOST_CKN	n/a	n/a	n/a	
	DSIHOST_D0P	DSIHOST_D0P	n/a	n/a	n/a	
	DSIHOST_D0N	DSIHOST_D0N	n/a	n/a	n/a	
	PJ2	DSIHOST_TE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FMC	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI4	FMC_NBL2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI3	FMC_D27	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI2	FMC_D26	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI5	FMC_NBL3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI7	FMC_D29	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI10	FMC_D31	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI6	FMC_D28	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH15	FMC_D23	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI1	FMC_D25	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI9	FMC_D30	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH13	FMC_D21	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH14	FMC_D22	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI0	FMC_D24	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH5	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH3	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH2	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH12	FMC_D20	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH9	FMC_D17	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH11	FMC_D19	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH8	FMC_D16	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH10	FMC_D18	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
I2C4	PB7	I2C4_SDA	Alternate Function Open Drain	**Pull-up ***	**Very High ***	
	PD12	I2C4_SCL	Alternate Function Open Drain	**Pull-up ***	**Very High ***	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
QUADSPI	PE2	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB6	QUADSPI_BK1_NCS	Alternate Function Push Pull	**Pull-up ***	**Very High ***	
	PC10	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC9	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD13	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
Single Mapped Signals	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	
GPIO	PJ13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PJ15	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	LCD_RESET
	PI13	GPIO_EXTI13	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	**n/a**	TP_IRQ
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	RENDER_TIME
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	VSYNC_FREQ
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	MCU_ACTIVE
	PJ5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PJ1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	FRAME_RATE

4.2. DMA configuration

nothing configured in DMA service

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
CAN1 TX interrupts	true	5	0
CAN1 RX0 interrupts	true	5	0
CAN1 RX1 interrupt	true	5	0
CAN1 SCE interrupt	true	5	0
EXTI line[15:10] interrupts	true	5	0
TIM8 trigger and commutation interrupts and TIM14 global interrupt	true	5	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	15	0
LTDC global interrupt	true	3	0
DMA2D global interrupt	true	5	0
I2C4 event interrupt	true	5	0
DSI global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
FMC global interrupt	unused		
FPU global interrupt	unused		
LTDC global error interrupt	unused		
QUADSPI global interrupt	unused		
I2C4 error interrupt	unused		

4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false

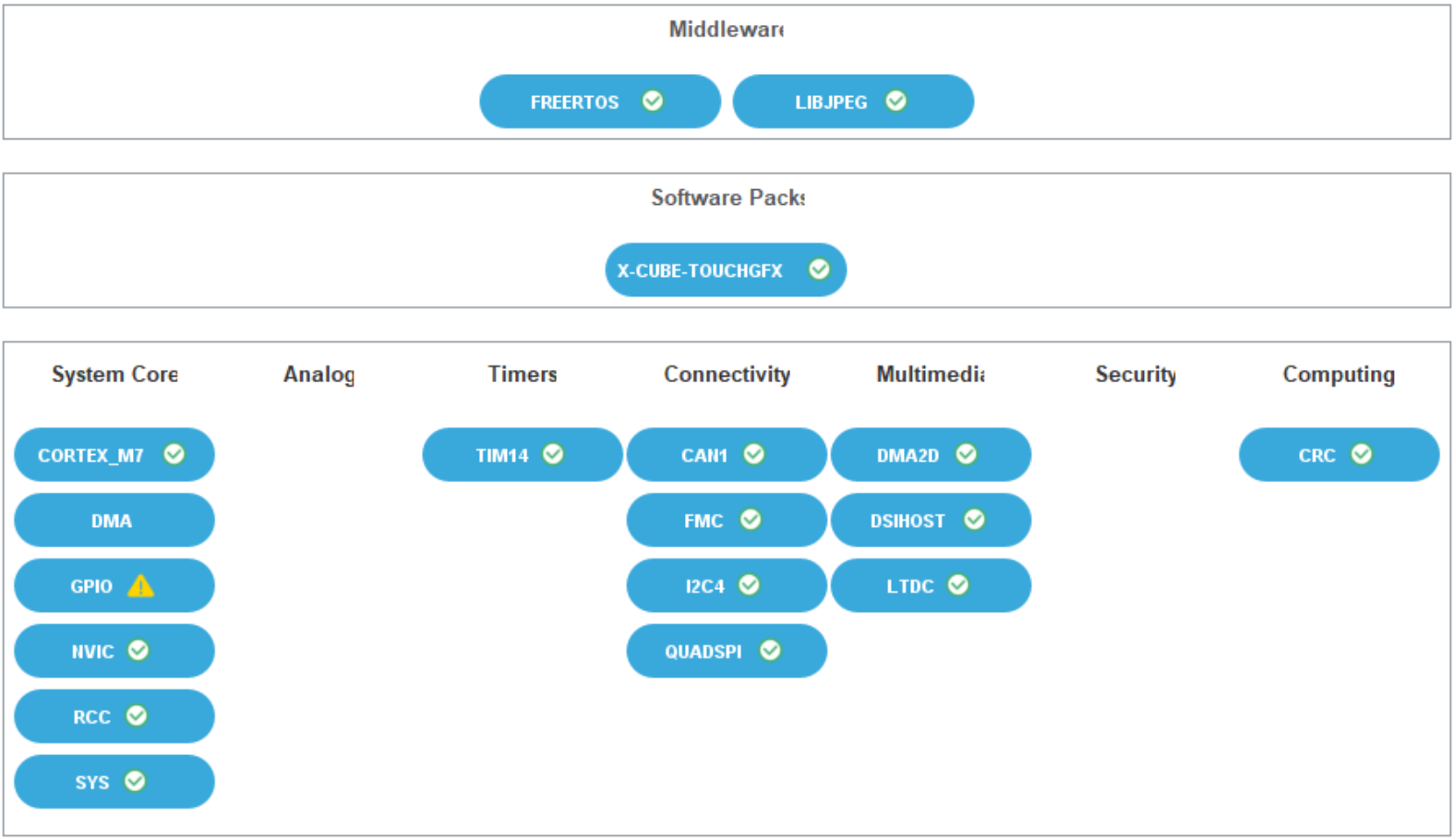
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
CAN1 TX interrupts	false	true	true
CAN1 RX0 interrupts	false	true	true
CAN1 RX1 interrupt	false	true	true
CAN1 SCE interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true
TIM8 trigger and commutation interrupts and TIM14 global interrupt	false	true	true
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	false	true	true
LTDC global interrupt	false	true	true
DMA2D global interrupt	false	true	true
I2C4 event interrupt	false	true	true
DSI global interrupt	false	true	true

*** User modified value**

5. System Views

5.1. Category view

5.1.1. Current



6. Software Pack Report

6.1. Software Pack selected

Vendor	Name	Version	Component
STMicroelectronics	X-CUBE-TOUCHGFX	4.25.0	Class : Graphics Group : Application Variant : TouchGFX Generator Version : 4.25.0

7. Docs & Resources

Type	Link