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Custom Implementation FPGA Code Module

I/O pin mapping and driver configuration

I/O Module	IO316
Simulink Real-Time Target Version	R2016a
Reference	speedgoat_IO316_CI_01547

speedgoat
real-time simulation and testing

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1 Introduction

This manual is an addendum to the User's Manual you have received with your Real-time target machine (with specific serial number).

Your Real-time target machine is equipped with at least one reconfigurable FPGA I/O module for which a default FPGA bitstream and Simulink Real-Time driver blockset has been provided. See the User's Manual for your Real-time target machine for more information on this.

This manual provides information on how to install, configure, and use the specific (custom) FPGA bitstream and Simulink Real-Time driver blockset you have additionally ordered at the time of your Real-time target machine purchase or also possible, at a later time.

2 Implemented Functionality

This custom FPGA bitstream and Simulink Real-Time driver blockset implements the following functionality:

FPGA Code Module	Transceiver Type	No. of modules / channels
SPI master/slave	TTL	2
Digital input/output	TTL	56

Table 1: Implemented functionality IO316- Front I/O

3 Software Installation

The software installation for this custom FPGA bitstream and Simulink Real-Time driver blockset must be installed after the MathWorks software standard installation and the Speedgoat library (speedgoatlib). Therefore, the steps are as follows:

1. Download the custom implementation for your I/O module and Matlab R2016a : http://www.speedgoat.ch/downloads/ci/speedgoat_IO316_CI_01547.zip
2. The archive contains both, the test model (*.slx) and the bitstream (*.mat) of the custom implementation.
3. The content of this archive can be extracted in your current MATLAB workspace. To make the bitstream accessible for all projects and folders, we recommend to add the bitstream in the following directory:

   For Speedgoatlib 8.x.x:
   [matlabroot]\toolbox\rtw\targets\xpc\target\build\xpcblocks\thirdpartydrivers\sg_bitstream

Note: After placing the bitstream file into the *thirdpartydrivers*-folder, please do not forget to type **rehash toolbox** in your MATLAB Command Window!

4 I/O Pin mapping

The I/O pin mapping for this custom FPGA bitstream implementation is shown below. This I/O pin mapping is specific to the reconfigurable FPGA module for which it has been designed and is the reference on how you connect the pins to your hardware under test.

Attention: Speedgoat delivers real-time target machines together with terminal boards pre-wired for the default FPGA bitstream implementation (see User's Manual of your target machine). Therefore, the wires of the terminal board for the reconfigurable FPGA I/O module have to be wired as described in section 7.2 of this document to execute the test model for this specific implementation.

4.1 Front I/O

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Proposed FPGA pin mapping for IO316 I/O module

2x SPI Master, 2x SPI Slave, 56x General purpose digital I/O

Pin	Code Module Channel	Functionality	Direction	Transceiver
1	1	SPI - CLK	IN/OUT	TTL
2		SPI - CS	IN/OUT	TTL
3		SPI - SDO	OUT	TTL
4		SPI - SDI	IN	TTL
5	2	SPI - CLK	IN/OUT	TTL
6		SPI - CS	IN/OUT	TTL
7		SPI - SDO	OUT	TTL
8		SPI - SDI	IN	TTL
9		Ground		
10	1	GPIO	IN/OUT	TTL
11	2	GPIO	IN/OUT	TTL
12	3	GPIO	IN/OUT	TTL
13	4	GPIO	IN/OUT	TTL
14	5	GPIO	IN/OUT	TTL
15	6	GPIO	IN/OUT	TTL
16	7	GPIO	IN/OUT	TTL
17	8	GPIO	IN/OUT	TTL
18	9	GPIO	IN/OUT	TTL
19	10	GPIO	IN/OUT	TTL
20	11	GPIO	IN/OUT	TTL
21	12	GPIO	IN/OUT	TTL
22	13	GPIO	IN/OUT	TTL
23	14	GPIO	IN/OUT	TTL
24	15	GPIO	IN/OUT	TTL
25	16	GPIO	IN/OUT	TTL
26		Ground		
27	17	GPIO	IN/OUT	TTL
28	18	GPIO	IN/OUT	TTL
29	19	GPIO	IN/OUT	TTL
30	20	GPIO	IN/OUT	TTL
31	21	GPIO	IN/OUT	TTL
32	22	GPIO	IN/OUT	TTL
33	23	GPIO	IN/OUT	TTL
34	24	GPIO	IN/OUT	TTL

Pin	Code Module Channel	Functionality	Direction	Transceiver	Port	Pull Resistors
35	25	GPIO	IN/OUT	TTL	1	pull-up 3.3 VDC weak pull-up 5.0 VDC pull-down, or floating
36	26	GPIO	IN/OUT	TTL		
37	27	GPIO	IN/OUT	TTL		
38	28	GPIO	IN/OUT	TTL		
39	29	GPIO	IN/OUT	TTL		
40	30	GPIO	IN/OUT	TTL		
41	31	GPIO	IN/OUT	TTL		
42	32	GPIO	IN/OUT	TTL		
43		Ground				
44	33	GPIO	IN/OUT	TTL	2	pull-up 3.3 VDC weak pull-up 5.0 VDC pull-down, or floating
45	34	GPIO	IN/OUT	TTL		
46	35	GPIO	IN/OUT	TTL		
47	36	GPIO	IN/OUT	TTL		
48	37	GPIO	IN/OUT	TTL		
49	38	GPIO	IN/OUT	TTL		
50	39	GPIO	IN/OUT	TTL		
51	40	GPIO	IN/OUT	TTL		
52	41	GPIO	IN/OUT	TTL	3	pull-up 3.3 VDC weak pull-up 5.0 VDC pull-down, or floating
53	42	GPIO	IN/OUT	TTL		
54	43	GPIO	IN/OUT	TTL		
55	44	GPIO	IN/OUT	TTL		
56	45	GPIO	IN/OUT	TTL		
57	46	GPIO	IN/OUT	TTL		
58	47	GPIO	IN/OUT	TTL		
59	48	GPIO	IN/OUT	TTL		
60		Ground				
61	49	GPIO	IN/OUT	TTL	4	pull-up 3.3 VDC weak pull-up 5.0 VDC pull-down, or floating
62	50	GPIO	IN/OUT	TTL		
63	51	GPIO	IN/OUT	TTL		
64	52	GPIO	IN/OUT	TTL		
65	53	GPIO	IN/OUT	TTL		
66	54	GPIO	IN/OUT	TTL		
67	55	GPIO	IN/OUT	TTL		
68	56	GPIO	IN/OUT	TTL		

Figure 1: Pinout front IO316

5 Simulink Driver Library

To open the library blocks for the custom FPGA bitstream, type
» `speedgoatlib_IO316_CI_01547`

at the MATLAB command line prompt. The blockset looks as follows:

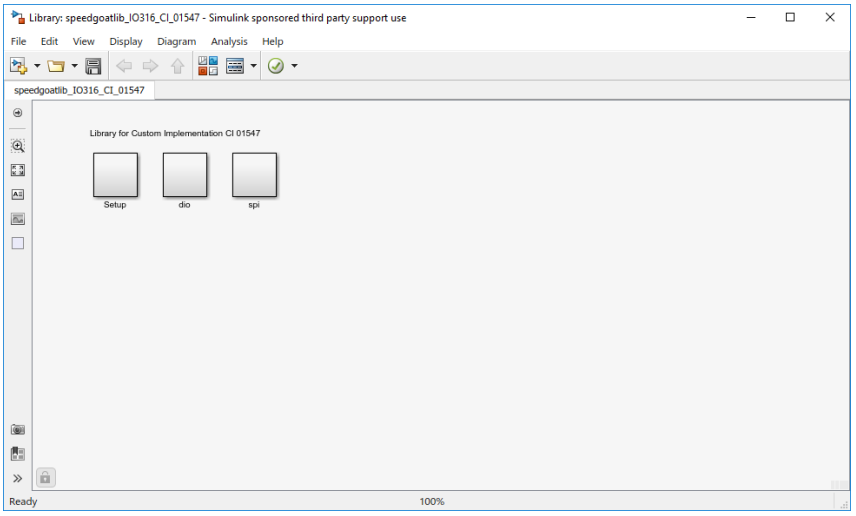

Figure 2: Library for Custom Implementation 01547

6 Bitstream

Using this custom Speedgoat FPGA bitstream and driver blocks is basically identical to using the default FPGA bitstream, as described in the speedgoatlib_fpga User's Manual. The only difference is the configuration of the Setup driver block:

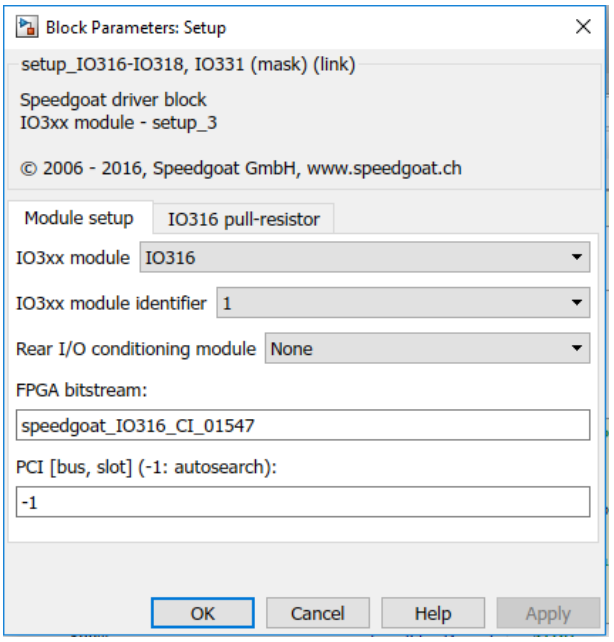

Figure 3: IO316, select I/O module, front I/O plug-in module, rear I/O conditioning module and Custom Implementation Bitstream

7 Test Model

7.1 Test Model description

To test the custom set of FPGA Code Modules, a dedicated test model is included. Note that this test model only tests I/O channels for which the loopback test method is possible. It is required to pre-wire the provided terminal board as described in chapter 7.2 of this manual. The test model doesn't exercise I/O channels requiring additional external hardware. Nevertheless executing this test model will confirm the correct set-up of this implementation.

To open the test model type:
» `speedgoat_IO316_CI_01547`

at the MATLAB command line prompt. The model looks as follows:

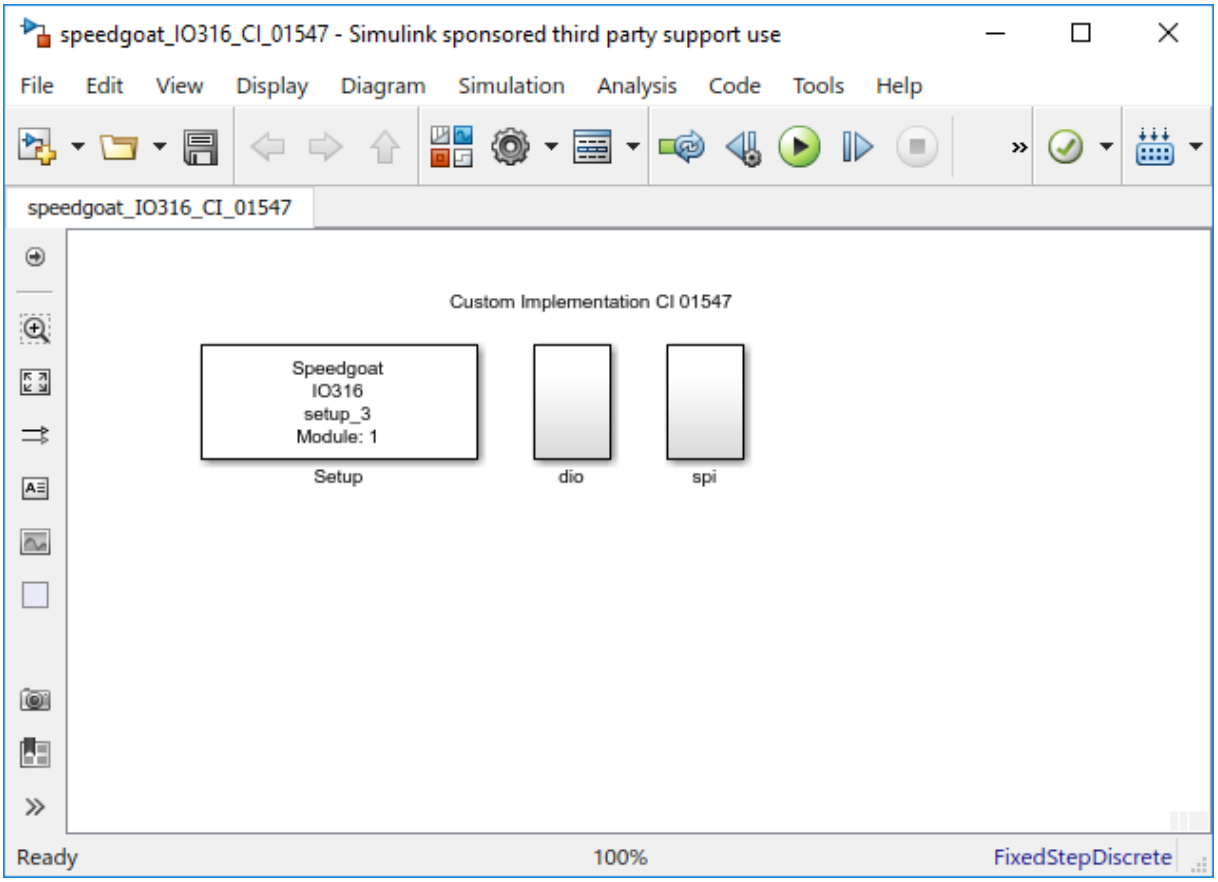

Figure 4: speedgoat_IO316_CI_01547

7.2 Required test wiring of the terminal board

Front I/O:

From Pin	To Pin	Tested functionality
01	05	SPI - SPI1 CLK - SPI2 CLK
02	06	SPI - SPI1 CS - SPI2 CS
03	08	SPI - SPI1 SDO - SPI2 SDI
04	07	SPI - SPI1 SDI - SPI2 SDO
10	18	DO channel 1 - DI channel 9
11	19	DO channel 2 - DI channel 10
12	20	DO channel 3 - DI channel 11
13	21	DO channel 4 - DI channel 12
30	35	DO channel 20 - DI channel 25
31	36	DO channel 21 - DI channel 26
32	37	DO channel 22 - DI channel 27
33	38	DO channel 23 - DI channel 28

Table 2: Front I/O Terminal Board wiring

8 Target Screen

If you start the test model (speedgoat_IO316_CI_01547.slx) with the wired board (according to section 7.2) you see the following target screen.

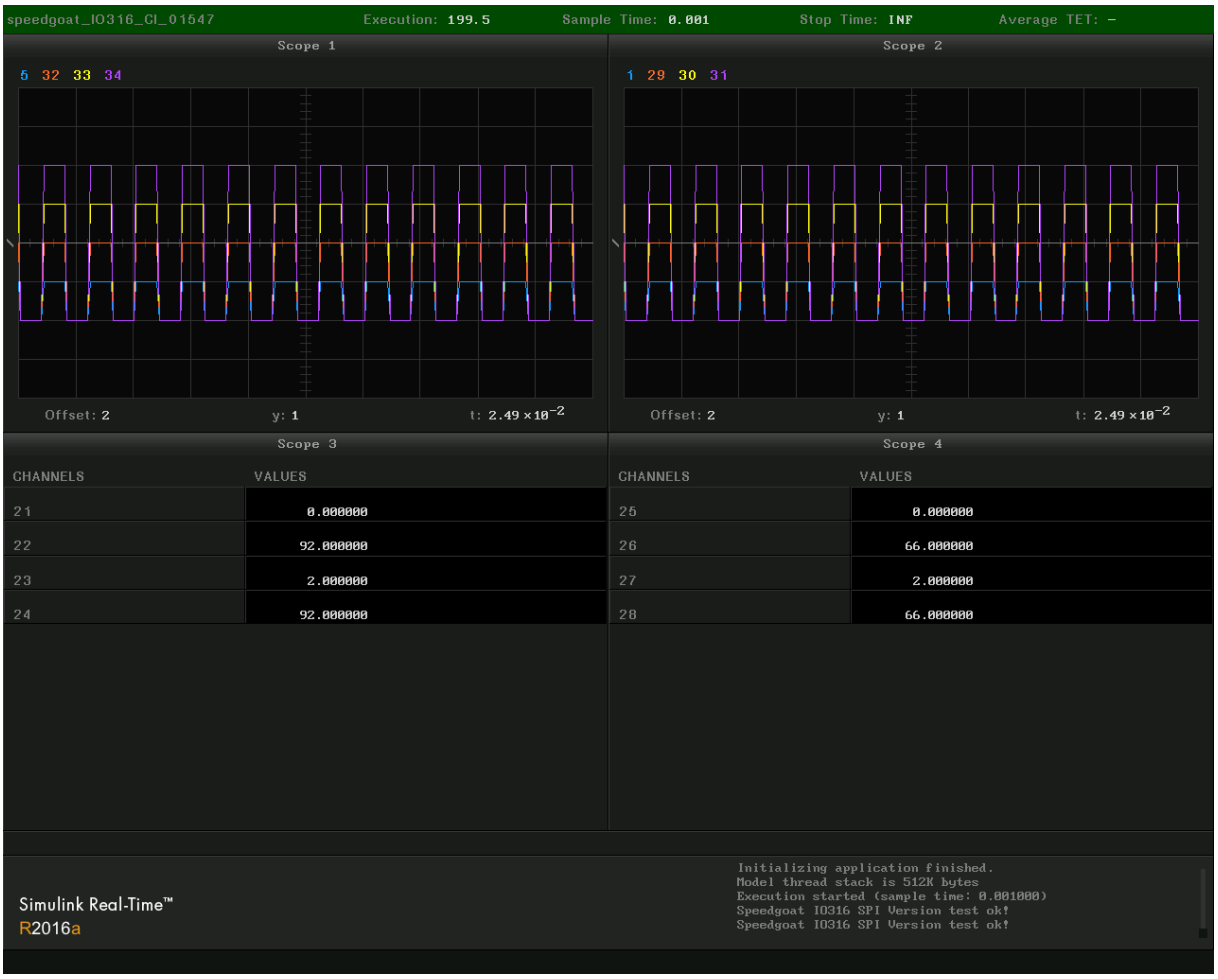

Figure 5: Target Screen with Test Signals