EEE2408 INTEGRATED CIRCUITS

IC design philosophy, special techniques for implementing analogue and digital IC circuits. Medium Scale Integration (MSI), Large scale integration (LSI), Very Large Scale Integration (VLSI) manufacture techniques and Computer Aided Manufacturing (CAM). Fabrication of IC, computer aided design of IC, special devices; e g MOSFET, VMOS, read only memory elements, Charge Coupled Devices (CCDs), bubble memories, solid state lasers.

References:

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Baker, *CMOS Circuit Design*, *Layout and Simulation*, IEEE Press, 1997
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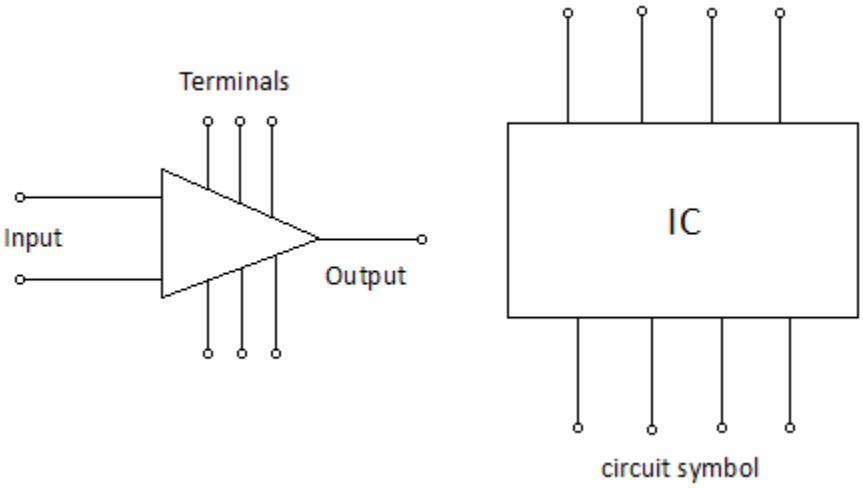
S. Campbell, *The Science and Engineering of Microelectronic Fabrication*, Oxford Univ. Press, New York, 2001.

Circuit – a combination of components put together to perform a specific function.

Integrated circuit – components put together in one piece of material to perform a function. It is in one package.

Components that can be integrated are like: resistors, capacitors, inductors and diodes which are referred to as passive components. Transistors which are referred to as active components.

Circuit symbol for an integrated circuit:



circuit symbol

Historical perspective of the development of ICs

1940 – The p-n junction was invented.

1945 – Transistor was invented.

1955 – First field effect transistor was invented (FET)

1958 – Integrated circuit was invented.

1960 – First MOSFET was invented.

1963 – CMOS was invented.

1971 – Microprocessor was invented

Microprocessors include:

Intel 4004 – Had 2300 transistors, speed of 108 kHz.

1972 – Intel 8008 – 3500 transistors, 200 kHz

1974 – Intel 8080 – 600 transistors, 2MHz.

1978 – Intel 8086/88 – 2900 transistors, 5 – 10 MHz.

1982 – Intel 80286 – 134000 transistors 6 – 12 MHz.

1985 – Intel 80386 – 275000 transistors, 16 – 33 MHZ.

1989 – Intel 80486 – 1.2M transistors, 25 – 30 MHz.

1993 – Intel Pentium – 3.1M transistors, 60 – 66 MHZ.

1995 – Intel Pentium pro – 5.5M transistors, 150 – 200 MHz.

1997 – Intel Pentium II – 7.5M transistors, 233 – 300 MHz.

1999 – Intel Pentium III – 28M transistors, 500 – 733 MHz.

2000 – 2005 – Intel Pentium IV – 42 – 169M transistors, 1.4 – 1.5 GHZ.

2007 – Intel core 2 Duo – 410M transistors.

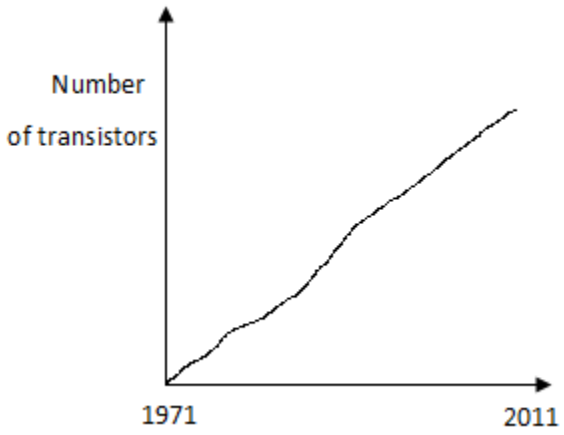
2010 – Intel Core i7 – 810M transistors.

Features of processor integrated circuit:

1. Number of transistors.
2. Speed in terms of Hz.
3. Instruction bits: 4, 8, 16, 32, 64…
4. Power dissipation.
5. Power consumption.
6. Size.

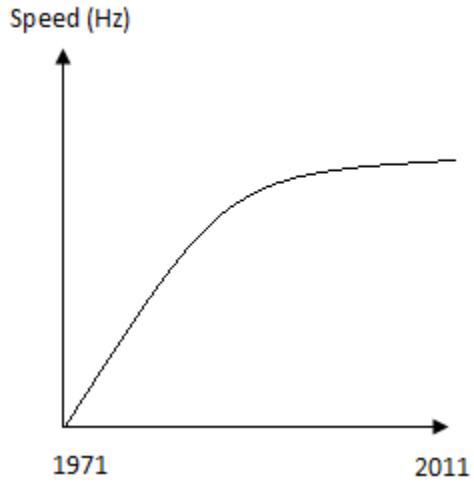
Number of transistors:

Have been growing due to the advancement of technology. According to Moore theory, the number of transistors in a processor was to double in 2 years.



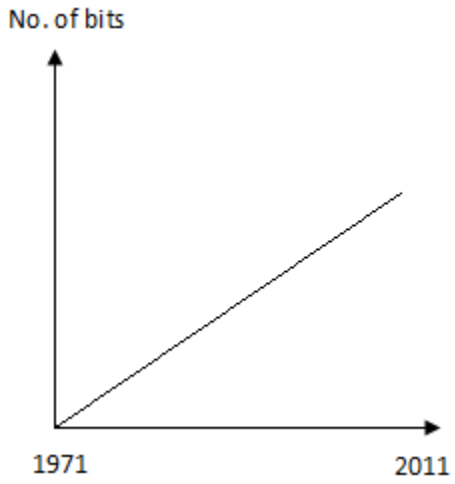
Speed:

Speed increases exponentially.



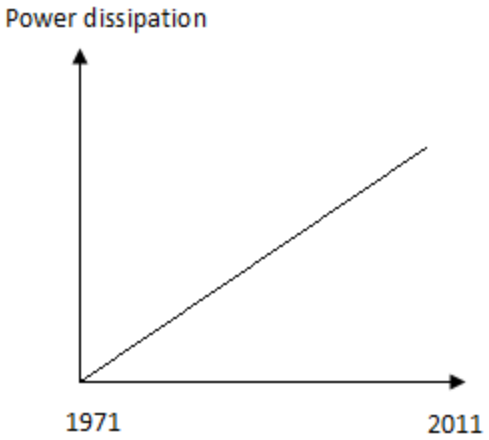
Instruction bits:

It has been increasing with time, but not necessarily linearly:



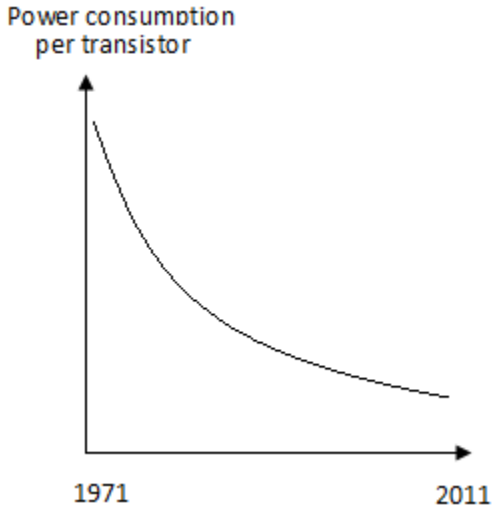
Power Dissipation:

Has been increased with time, almost linearly:



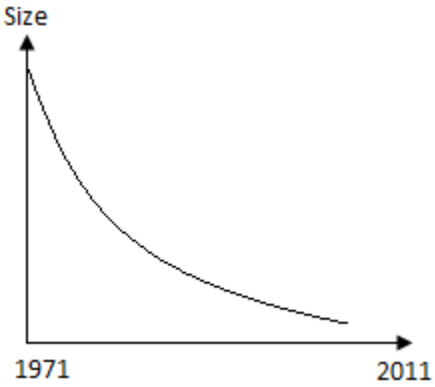
Power Consumption:

Has reduced with time per the given number of transistors.



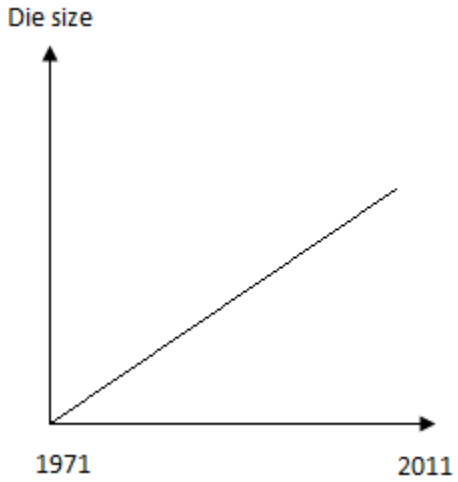
Size:

Reducing with respect to time.



Die size:

Die – Subtrates cut and used to develop integrated circuits.



IC classification:

There are 3 main classifications:

i) According to technique used to develop them.
ii) According to size.
iii) According to application.

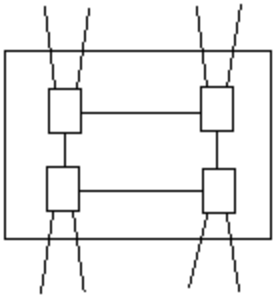
i) Technique:

There are four types:

a) Monolithic.
b) Thin film.
c) Thick film.
d) Hybrid.

a) Monolithic:

All the components are fabricated on a single substrate. For instance, transistors can be fabricated by doping different sections of the substrate to form the transistor. 'Mono' means single while 'litho' means stone.



The technology used to connect these components is called photolithography. This is the most common in IC manufucturing.

Advantages:

1. It is easier to fabricate in mass production.
2. They are cheaper.
3. They are small in size.
4. They are portable.

Disadvantages:

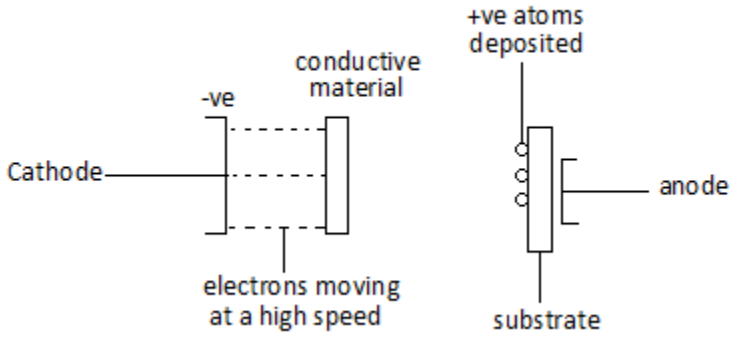
1. Not easy to fabricate passive components like capacitors and inductors.
2. Cannot be used in high power applications.
3. Once one of the components fail, the whole IC fails.
4. Complex technology is used to develop the IC.

b) Thin film:

They are constructed by depositing a thin film of the conductive material to form the required components on a substrate e.g. ceramic.

The techniques used to deposit the thin film are:

1. Sputtering:



This is the process where electrons moving at a high speed from a cathode strike the conductive material knocking off atoms which will be attracted by the anode as they move and get deposited on the surface.

2. Vaporization:

The material is vaporized and allowed to condense on the substrate. This technology is used to fabricate resistors and other passive components.

Advantages:

1. Easier to fabricate passive components.
2. Can be used in high power applications.

Disadvantages:

1. Slow in fabrication.
2. Occupy a large space.
3. Consume more power.

c) Thick film:
The construction is the same as that of thin film ICs. The difference is that the material is deposited on the substrate are put inside a furnace. Because of the high temperature, fusion will take place. Technology used to fabricate passive components.
Advantages:
1. Easier to fabricate passive components.
2. Higher power application than thin film.

Disadvantage:

1. Slow in fabrication.
2. Occupy large space.
3. Consume more power than thin film.

d) Hybrid:

This is where the chipsets mentioned above are combined. They are interconnected. Can handle both analogue and digital signals. They can handle more power (5W – 50W).

BJT and FET technology can be used in the construction of hybrids:

BJT = $\frac{V_{BE}}{I_B}$ FET = $\frac{V_{GS}}{I_G}$ but $I_G \approx 0$ thus has infinite resistance.

i) According to size:

Refers to the scale of integration.

Refers also to the number of components used to construct the IC. They are given by:

a) SSI – Small Scale Integration.
b) MSI – Medium Scale Integration.
c) LSI – Large Scale Integration.
d) VLSI – Very Large Scale Integration.
e) ULSI – Ultra Large Scale Integration.

a) SSI – Small Scale Integration:

These have a small number of components and circuits. The number of components is 100 and less. Applications are in: Single stage amplifiers, Gates, adders, multiplexers, operational amplifiers.

b) MSI – Medium Scale Integration:

They have a moderate number of components. The components are approximately between 100 – 3000. Applications are in: filters, registers.

c) LSI – Large Scale Integration:

Has a large number of components or circuits. The components are approximately between 3000 – 100000. Applications are in: microprocessors, registers, memories.

d) VLSI – Very Large Scale Integration:

They have a very large number of components and circuits. The components are approximately between 10000 – 1M. Applications are in: Signal processors, Computer processors, memories.

e) ULSI – Ultra Large Scale Integration:

They have a very large number of components and circuits. The number of components are more than a million. Applications are in: computers and signal processors.

ii) According to application

There are three types:

a) Linear.
b) Digital
c) Mixed Signals.

a) Linear:

This is the same as analogue. The input and output have a linear relationship. They deal with analogue signals only. E.g. operational amplifiers, filters (analogue), single storage amplifiers.

b) Digital:
They deal with discrete quantities i.e. 0 and 1. They are constructed using gates, Flip flops. Examples are: counters, registers, processors.

c) Mixed Signal:
These are circuits that deal with both analogue and digital signals. They are constructed using linear and digital circuits. Lately Bi-CMOS technology is used to construct them. Examples: ADC – Analogue-to-digital converters, DAC – Digital-to-Analogue converters, mobile phones, DVD writers, VOIP application.

Merits of ICs:

1. Small size.
2. Portability.
3. Low power consumption.
4. No protruding components.
5. Reliable.
6. Versatile – have many applications.
7. Programmable.
8. Cheaper.
9. Durable.

Demerits:

1. If one component fails, the whole IC fails.
2. Used in low power applications.
3. Complex to construct.
4. Expensive technology used to come up with them.
5. Leakage current and voltage since the components are close to each other.
6. Not easy to fabricate components like inductors.

Materials used in IC fabrication:

These are materials that are used to fabricate ICs (in the processor). IC fabrication materials cab be categorized as:

i) Semiconductor Conductor materials.
ii) Metallic materials.
iii) Group III
iv) Group V
v) Acids
vi) Alkalines.

i) Semiconductor materials:

These include

a) Silicon.
b) Germanium.
c) Gallium arsenide – GAAS

a) <u>Silicon:</u>

- Is a group V elements.
- It partly conducts.
- It has an energy gap of 1.1eV.
- It is readily available.
- It is cheap.
- It is used together with other dopants either n-type or p-type semiconductor materials.
- Is used as a substrate (material on which components can be fabricated)
- It can also act as a support material.
- The material can also be used to fabricate elements.

b) <u>Germanium:</u>

- Is a group IV element but has 32 electron s(2.8.18.4)
- Partly conducts – better than Si since it has a lower energy gap and has weaker energy bonds.
- Has an energy gap of 0.7 eV (0.66eV) – Energy required for an elecltron to move from VB to CB.
- It is not readily available.
- Is expensive.
- Not commonly used to develop electronic components since they have high leakage current (due to weak bonds).
- Noise generated is higher.
- Highly affected by temperature changes.
- Used together with other dopants to obtain p-type and n-type materials.
- Can be used as a substrate and making components.
- Mostly applied in photodiodes and photo-conducting materials e.g. solar cells.
- Easily affected by light energy variations.

c) <u>GAAs:</u>

- This is a compound from Gallium – Group III and Arsenic – Group V materials.
- When combined, they form a semiconductor material.
- It partially conducts.
- It has an energy gap of 1.35eV.
- Is not readily available.
- Is expensive.

- Is used in high power applications.
- Can also be applied in devices that require low noise.
- Leakage current is minimal because energy gap is 1.35eV.
- Mostly applied in LED

ii) Metallic materials:

- They are used in metallization i.e. connection of direct components and chipsets in an IC.
- Materials used are Al, Cu, Pb, Au, Silver, Sn – Tin.
- Aluminium and Copper are used in developing lines i.e. interconnecting various chipsets and components. This is because they are all available and are good conductors.
- Gold and Silver are usually applied in the leads of terminals of the IC package
- They are also used in wire bonding:
- They are not readily available and are expensive.
- Lead and Tin are used to develop the solder coated as the leads in order to increase the metal contacts and to reduce the effect of dry joints.

iii) Group III:

- Usually used as dopants to form the p-type materials.
- They include Al, B, Ga.
- They are used to develop substrates together with semiconductors like Si.
- They are also used to develop compounds like GAAS.

iv) Group V:

- They are referred to as pentavalent elements.
- They are used as dopants.
- When doped with semiconductors like Si, they form n-type materials.
- Also used as substrates.
- Together with Group III elements, they form compounds like GAAS, Gallium Phosphide.
- Examples: Phosphorus, Arsenic, Antimony.

v) Acids:

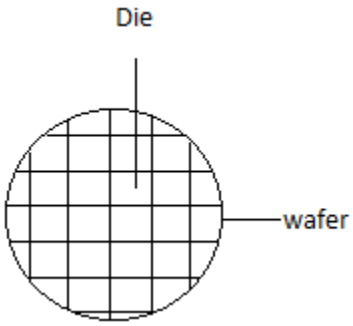
They are used in cleaning semiconductors.

Can also be used in etching. Examples: Sulphuric acid, Nitric acid, Hydrochloric acid.

vi) Alkalines:

Can also be used to clean semiconductor materials and etching. Examples: Sodium Hydroxide, Potassium Hydroxide, Aluminium Hydroxide.

Wafers:



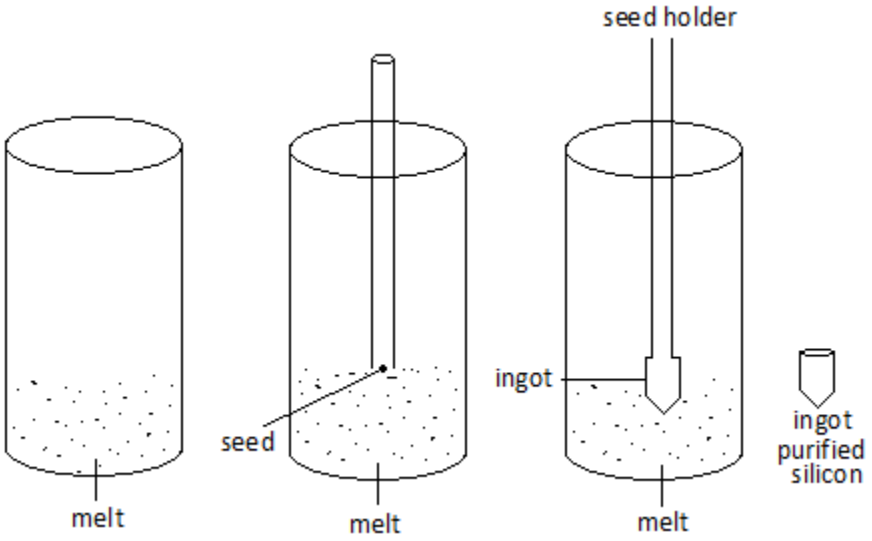
This is a thin, round semiconductor material obtained by purifying the mined materials like Silicon and Germanium. From the wafer, processors and chipsets can be obtained by doping and cutting it appropriately.

Formation:

There are methods used to develop wafers.

i) Czochralski method.
ii) Float zone method.

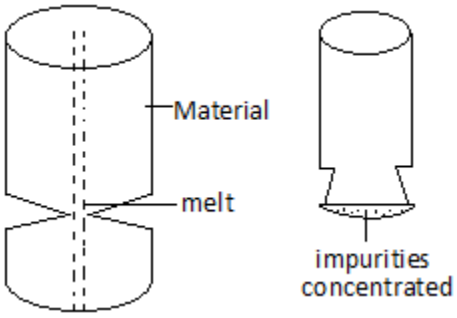
i) Czochralski method:



Steps:

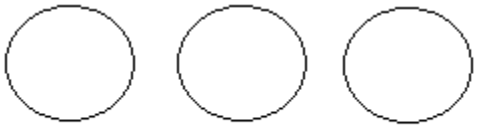
1. Melt the material.
2. Introduce a seed into the melt to facilitate the development of ingot.
3. The seed is rotated to develop the ingot.
4. For a uniform diameter, the speeds of rotation should be controlled.
5. Also for a given length, the speed towards the end should be such that the material comes out without a problem.
6. This develops a cone like shape.

i) Float zone method:



Steps

1. Obtain the material which is round.
2. The material is melted from the upper end.
3. The melt is controlled in a way that it moves down.
4. As it moves down, it moves with impurities.
5. AT the lower end where the concentrate is, it is chopped off.
   This method is better since purity levels are high. For both methods after obtaining the ingot, it is cut into small pieces called wafers by using a saw.



wafers

Wafer properties:

1. Diameter:
   They have been increasing in diameter as follows:
   1", 2", 3", 4", 5", 6", 8", 12" => 18". (research is being done).
   The higher the diameter, the more the die or chips and the higher the yield.
2. Thickness:
   This is important as together with the diameter, they determine the stability of the wafer.
3. Texture:

Most applications require smooth surfaces, but for solar wafers, they need to be rough increases efficiency.

Yield Considerations in IC fabrication:

Yield:

This is the percentage of dice that are fabricated from a wafer without defects. The percentage is from 10 – 90. The yield is a function of several factors:

Die area (A).

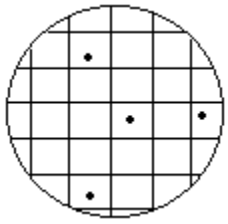
Defect density (D).

Complexity of the technique used to obtain the wafers and die.

Processes the die goes through before use e.g. testing, packaging.

a) Die Area (A)

The more the area, the lower the yield. This is because there is a higher chance more defects will occur.



Total number of dies = 32

Dies in good condition = 26

Yield = (26/35) x 100% = 81.25%

For a case where the area of the die is increased,

Total number of dies = 25.

Total number without defects = 15.

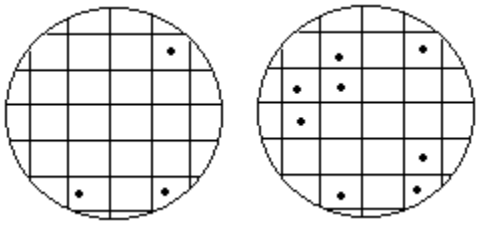
Yield = $\frac{Number\ without\ defects}{Total\ number}\ X\ 100\%$ = $\frac{15}{25}\ X\ 100\%$ = 60%.

Thus the larger the area of each side, the lower the yield.

b) Defect Density (D):

It is given by: $Defect\ Density\ (D) = Number\ of\ defects/m^2$

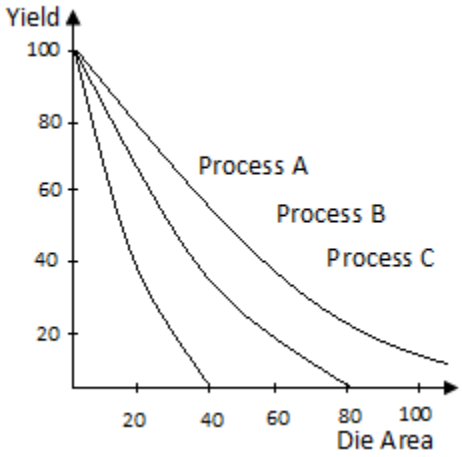
The more the defect density, the less the yield.



Defect density = $\frac{Number\ of\ defects}{Total\ area\ of\ wafer}$

c) Complexity of the technique being used:

The more the steps involved in coming up with an IC, the lower the yield.



Process A – less complex.

Process B – Complex.

Process C – Very complex.

Causes of failure:

1. Defects introduced during cutting of wafers, ingot.
2. Impurities introduced during ingot production.
3. During photolithography: using masks in bad condition.

4. During etching process.
5. When testing, defects/ impurities may be introduced.
6. During packaging.
7. Poor oxidation.
8. Iron implantation.

Yield models:

i) Poisson model.
ii) Murphy's model.
iii) Negative binomial model.
iv) Seed's model.

Each of the above models use the die area and defect density:

i) Poisson model:
Y = e^{-AD} where A – Die Area, D – Defect Density

ii) Murphy's model:
1st equation is given by:

Y = $\frac{1 - e^{-2AD}}{2AD}$ where A – Die Area, D – Defect Density

2nd equation:

Y = $(\frac{1 - e^{-AD}}{AD})^2$

iii) Negative Binomial model
Y = $(1 + \frac{AD}{\alpha})^{-\alpha}$ where α = factor that ranges from 0.3 – 3.

iv) Seed model:
Y = $e^{-\sqrt{AD}}$

Example:

By using the models above, obtain the yield for a die with sides of 6mm and defect density of 0.7/cm^2. Determine the most optimistic yield model.

Area = (6x6) x 10^{-6} = 36 x 10^{-6}m^2

D = $\frac{0.7}{1\ X\ 10^{-4}}$ = 0.7 x 10^4/m^2 = 7 x 10^3/m^2

AD = 36 x 10^{-6} x 7 x 103 = 252 x 10^{-3} = 0.252

Using Poisson model:

$Y = e^{-AD} = e^{-0.252} = 0.777 = 77.7\%$

Using 1st equation of murphy's model:

$Y = \frac{1 - e^{-2AD}}{2AD} = \frac{1 - e^{-2\ X\ 0.252}}{2\ X\ 0.252} = 0.7855 = 78.55\%$

Using 2nd equation of murphy's model:

$Y = (\frac{1 - e^{-AD}}{AD})^2 = = (\frac{1 - e^{-\ 0.252}}{0.252})^2 = 0.7814 = 78.14\%$

Using negative binomial:

$Y = (1 + \frac{AD}{\alpha})^{-\alpha} = (1+ \frac{0.252}{0.3})^{-0.3} = 0.8328 = 83.28\%$

$= (1+ \frac{0.252}{3})^{-3} = 0.7851 = 78.51\%$

Using seed's model:

$Y = e^{-\sqrt{AD}} = e^{-\sqrt{0.252}} = 0.6053 = 60.53\%$

The most optimistic model is negative binomial when $\alpha = 0.3$. The least optimistic model is the seed's model.

Importance of yield models in IC fabrication:

1. To determine or predict the number of working ICs that can be manufactured out of a wafer.
2. Helps in reducing costs incurred in the manufacturing process.
3. Helps in selection of techniques that can be used in IC fabrication.
4. Helps in improving the process of IC fabrication.

Quality metrics in IC design:

These are the factors taken into consideration when designing and fabricating ICs:

1. Cost.
2. Functionality.
3. Robustness.
4. Directivity.

5. Performance.
6. Noise immunity.
7. Power dissipation.
8. Power consumption.
9. Fan in and fan out.

Cost

There are two types of costs:

a) Fixed cost b) Variable cost.

a) Fixed cost:

Cost that does not vary with the volume of production. It is affected by:

1. Research development.
2. Machinery.
3. Premises.
4. Overheads, e.g. electricity, labour.

b) Variable cost:

Cost that varies with the volume being produces. E.g. cost of raw materials.

Total cost = variable cost per IC + Fixed cost per IC.

$$= \frac{Fixed\ Cost}{Volume} + Variable\ IC$$

The cost of ICs should be reasonable to the consumer and also t be able to get a profit out of the ICs. Pricing will be important in this case to take care of the two.

ii) Functionality:

The IC should perform the function it was designed to perform.

It should not fail.

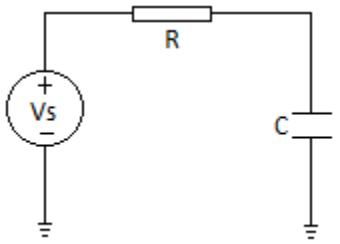
It should be reliable.

iii) Robustness:
Strength: the IC should be able to operate in the presence of noise.
Coupling noise should not affect its operation.
e.g. inter-element capacitance, p-n junction capacitors.

iv) Directivity:
A signal is expected to move from input to output and not vice-versa. There should be no feedback. If there is feedback, there will be instability in the operation.

v) Performance:

Ability of a system (IC) to operate at its optimum.
For instance, a processor should execute a given number of instructions per second.
Can be modeled using an RC network where a delay is expected.



$Vc = Vs(1 - e^{\frac{-t}{RC}})$

$1 - e^{\frac{-t}{RC}} = \frac{V_c}{V_s}$

$e^{\frac{-t}{RC}} = 1 - \frac{V_c}{V_s}$

$-\frac{t}{RC} = \ln(1 - \frac{V_c}{V_s})$

$t = - RC \ln(1 - \frac{V_c}{V_s})$

Example: Calculate the time at which the capacitor charges up to 50%.

$t = -RC\ln(1 - \frac{50}{100})$

$t = - RC\ln\frac{1}{2}$

$t = - RC\ln 2^{-1}$

$t = RC \ln 2.$

vi) <u>Noise immunity:</u>

The IC should be able to reject noise. Examples of noise are: ESDD – Electrostatic Discharge. RFI – Radio Frequency Interference, EMI – Electromagnetic Interference.

The above can be prevented by use of SiO2 insulators, reflectors for RFI.

vii) <u>Power Dissipation:</u>

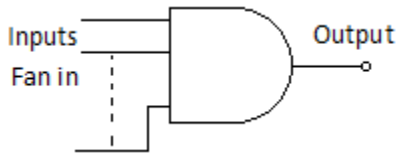
This is power given out as the IC is operating. This is important in considering the mechanism to use to eliminate the heat dissipated: Heat sink size, Fan size.

viii) This is the amount of power required by the IC to operate. This is important to:
Determine the size of batteries.
Determine the power supply unit requirements.

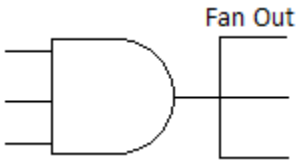
Determine the technology that can be used to reduce the power consumption of the IC.

ix) Fan in and fan out:

Fan in – is the maximum number of inputs into an IC without affecting its operation.



Fan out – is the maximum number of outputs that can be connected to the output of an IC without affecting its operation.



IC Fabrication Process:

These are processes involved in fabricating an IC. They are different steps used to come up with the final product (working IC)

Several processes are involved.

1. Deposition.
2. Oxidation.
3. Photolithography.
4. Etching.
5. Ion implantation.
6. Diffusion.
7. Metallization.
8. Testing.
9. Packaging.

The processes need to follow the sequence given above. Some can be repeated at some point. E.g after metallization, one can test and also after packaging.

1. Deposition:

   A thin film is deposited. This is a process of adding a thin film of material to a substrate. There are two main methods of deposition.

   a) Chemical reaction deposition.
   b) Physical deposition.

a) Chemical reaction deposition:

   This involves a chemical reaction to form the material deposited on the substrate. There are four types of chemical reaction deposition.

   i) Chemical vapour deposition.

ii) Electro-deposition.
iii) Epitaxy deposition.
iv) Oxidation.

i) Chemical Vapour deposition: CVO

Here gases are introduced into a reactor where they react to form a material that will be deposited on the substrate. The reactor will be facilitated to provide necessary conditions for reaction like: vacuum, high temperature, pressure requirements.

There are two main types of CVO:

1. Low pressure CVO.
2. Plasma enhanced CVO.

1. Low pressure CVO:
   Very low pressure.
   High pressure temperature upto 600°C.
   Reaction is slower hence slower deposition is good quality deposition.
2. Plasma enhanced CVO:
   Moderate pressure.
   Low temperature.
   Reaction is faster.
   The quality of deposition is not as good as low pressure CVO.

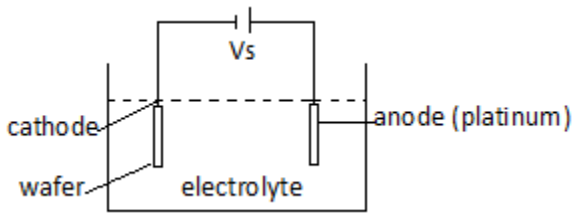
ii) Electro-deposition:
Involves the use of electrolysis.
The requirements include:
Electrical potential.
Electrolyte.
Cathode where the wafer is connected.
Anode (Platinum).

There are two methods:

1. Electroplating.
2. Electroless plating.

1. Electroplating:

This involves an external potential, electrolyte, cathode, anode.



When Vs is switched on electrolysis takes place resulting to deposition of the required material on the wafer. This process is controllable and therefore the thickness and uniformity of the deposit material can also be controlled.

2. Electroless plating:

This has no external voltage supply.

It only requires an electrolyte with a complex solution and a wafer with a starter material where when the wafer is immersed in the electrolyte, there will be spontaneous reaction.

This process is not easy to control. Thus the thickness and uniformity can also be controlled.

Electrodeposition is commonly used when depositing metallic materials such as Cu, Au, Ni.

iii) Epitaxy deposition:

It is similar to CVO, only difference being that the deposition process is controlled. It usually takes place on already existing material of the same kind. If the material is amorphous or crystalline, it will retain the same property. There are several types of epitaxy deposition. However, we shall discuss three.

1. Vapour phase.
2. Liquid phase.
3. Solid phase.

1. Vapour phase:

This is where gases are introduced into a reactor where they react forming the required solid material. This material will get deposited on an existing substrate to form an amorphous or crystalline structure. The gases are usually introduced at high temperatures and controlled pressure. The raw materials include: $SiCl_4$, SiH_4, H_2

For $SiCl_4$ – Silicon Tetrachloride, there will be the following reaction:

$SiCl_4\ (g) + 2H_2\ (g) \longrightarrow Si\ (s) + 4HCl\ (g)$

For SiH4 – Silane – introduce high temperature then Si and H2 will be obtained.

$SiH_4\ (g) \longrightarrow Si\ (s) + 2H_2\ (g)$

The 1st process should be controlled to avoid the etching process that can also take place. The competing etching process is given as:

$SiCl_4\ (g) + Si\ (s) \longrightarrow 2SiCl_2\ (g)$

2. Liquid phase:

- This involves the use of a material liquid / melt form.
- The required material will be dissolved in melt.

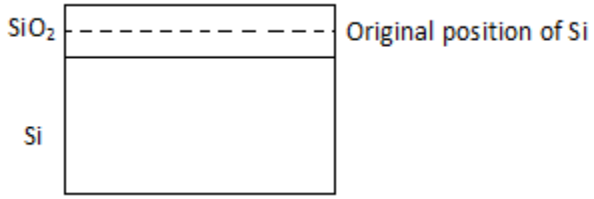
- If the temperatures and concentration of materials are controlled at some point deposition will take place on substrate.
- This process is used in producing compounds like GaAs and Indium phosphate. InP.
- These are Group 3 and 5 elements combined.

3. Solid phase:

- This is where an amorphous material in solid form is deposited on a crystalline material and the two are put in a furnace (high temperatures).
- The amorphous material changes to crystalline.
- This process is mostly applied in wafers after iron implantation to rectify the damaged structure.

iv) Oxidation:

This is the process of introducing oxygen into a material which will react to form an oxide. This is done at high temperatures. Mostly this process is applied when developing Sio2. This process takes place in such a way that it eats into the material i.e. Si.



There are two main methods for oxidation:

1. Dry oxidation.
2. Wet oxidation.

1. Dry Oxidation:

This involves the use of oxygen and Si at high temperatures. This process is slower.

$Si\ (s) + O_2\ (g) \longrightarrow SiO_2\ (s)$

2. Wet oxidation:

This involves the use of water vapour.

$Si\ (s) + 2H_2O\ (g) \longrightarrow SiO_2\ (s) + 2H_2\ (g)$

- This process is faster than dry oxidation.
- Pure water can be used and for better performance H2 and O2 used.
- Growth rate of the oxide:
- This depends on the temperature and the material used like oxygen or water.
- This can be analyzed using the following:

dx – change of oxide.

dt – change in time.

C – constant of proportionality.

X – Oxide size.

The above have the following relation.

$\frac{dx}{dt} = \frac{c}{x}$

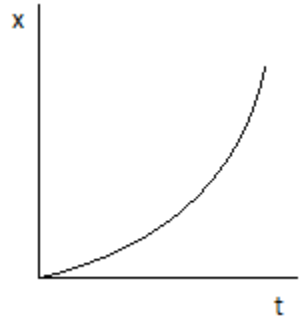
Integrating both sides we get:

$\int_0^x x dx = \int_0^t c dt$

$\frac{x^2}{2}$ = ct

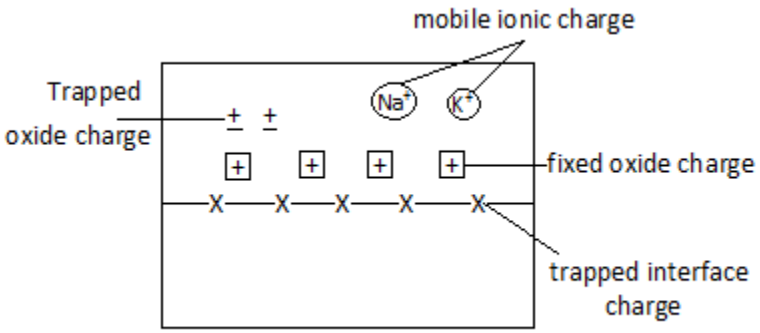
$x^2 = 2ct$

$x = \sqrt{2ct}$



The growth rate depends on the square root of time.

Oxide Charges:



Given as:

1. Trapped interface charge.
2. Trapped oxide charge.
3. Mobile ionic charge.
4. Fixed oxide charge.

a) Trapped interface charge:

These are as a result of the defects during formation of the oxide e.g. due to bonding effects.

b) Trapped oxide charges:

There are as a result of the effects of dopants which form holes and electrons.

c) Mobile ionic charges:

These are as a result of the presence of metallic impurities. For instance Sodium and Potassium.

d) Fixed oxide charges:

- These will result from temperature changes during the oxide formation.
- Effects of impurity on oxidation rate:
- Some of the impurities include:
- Water.
- Sodium.
- Group III and IV elements.
- Halogens.

a) Water:

Presence of water in dry oxidation will increase the oxidation rate. The water acts as a catalyst.

b) Sodium:

Sodium ions will weaken the semiconductor bonds increasing the penetration rate of Oxygen. This will increase the rate of oxidation. The Sodium ions also change the properties of oxides.

c) Group III and V:

Group III e.g. Boron will weaken the semiconductor bonds and thus increase oxidation rate. Group V e.g. Phosphorus will have an opposite effect to that of Group III.

d) Halogens:

- Halogens e.g. Chlorine will reduce the effect of Sodium ions since it chemically combines with them.
- This is because the Sodium ions will reduce in number.
- This stabilizes the properties of the oxide.

Applications of SiO_2:

1. Used as insulator in MOSFETs.
2. Used to protect the underlying materials from corrosion (chemical) and physical wearing.
3. Used as masks in the process of introducing dopants to the semiconductor materal.
4. Used in transferring patterns

Physical Vapour Deposition:

Under physical deposition, the material is deposited physically on the substrate. There is no chemical reaction.

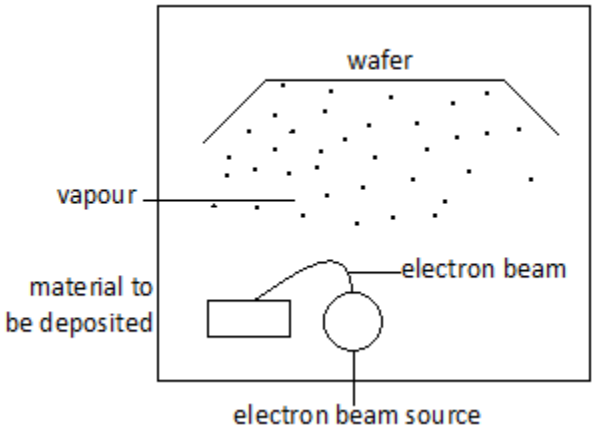
There are three main methods of PVO:

i) Evaporation.
ii) Sputtering.
iii) Casting.
i) Evaporation:

This involves changing the material into gaseous form and allowing it to settle on the wafers. There are 2 methods to achieve this:

a) E beam.
b) Resistive.
a) E beam:

An electron beam is directed on the material at a high speed, heating the materials to the point of evaporation. The vapour is then allowed to settle on the wafers.



b) Resistive:

A lot of current is passed through a tungsten wire with the material. The high current generates a lot of heat which vapourizes the material. The vapour is allowed to settle on the wafer.

ii) Sputtering:

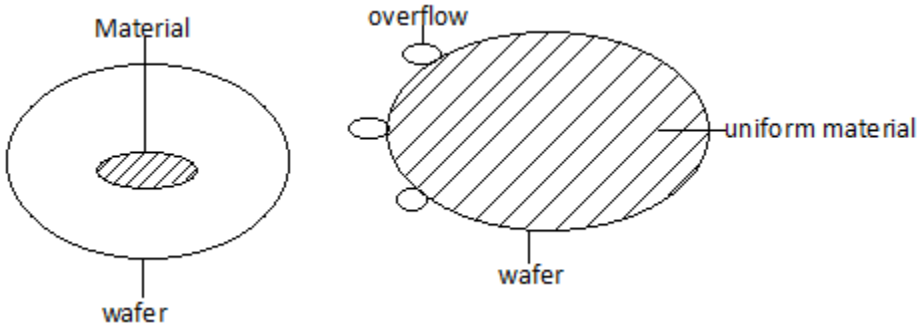
A gas is ionized by using RF.

The ions are accelerated at a high speed towards the material.

As a result, the material atoms are dislodged. These atoms will be allowed to settle on the substrate.

iii) Casting:

- The material in liquid for is deposited on the wafer.
- The wafer is spinned at high speed.
- This will allow the material to spread uniformly.
- This method is commonly applied in photolithography to deposit the photoresist.



Lithography:

- This is the process of transferring patterns to a flat surface by using a mask.
- The process where patterns are transferred by use of light energy is called photolithography.
- Photolithography is done by applying a material called a photoresist onto the surface and then exposing it to light energy which will make it soluble when developed.
- This can either result to a +ve or –ve photoresist.

i) +ve photoresist:
The part which is exposed to light becomes soluble.

ii) –ve photoresist:
The part which is exposed to light becomes insoluble.

Photoresist:

This is a light sensitive material which when exposed to light reacts. A photoresist consists of:

- Polymers.
- Solvent.
- Photo active compound (PAC).

a) Polymer:

A rubber material that changes property when exposed to light to become soluble or insoluble.

b) Solvent:

This helps in dissolving the polymer to make it a liquid and enable it to spread and stick on the wafer.

c) Photoactive compound:
This changes the properties of the polymer when exposed to light energy.

Steps involved in photolithography:

1. Cleaning.
2. Oxidation.
3. Photoresist application.
4. Soft brake.
5. Mask alignment.
6. Exposure.
7. Develop.
8. Hard bake.
9. Cleaning.

a) Cleaning and dehydration:

Cleaning is done to remove particles settled on the wafer like dust and other impurities.

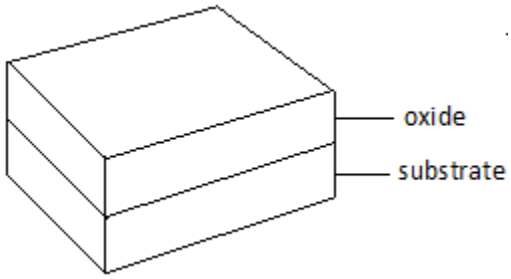
Liquids used are:

1. Water.
2. Weak acid.
3. Alkalis.
4. Dehydration helps in removing any water left on the wafer.
5. Water needs to be eliminated since some materials can stick to it.

b) Oxidation:

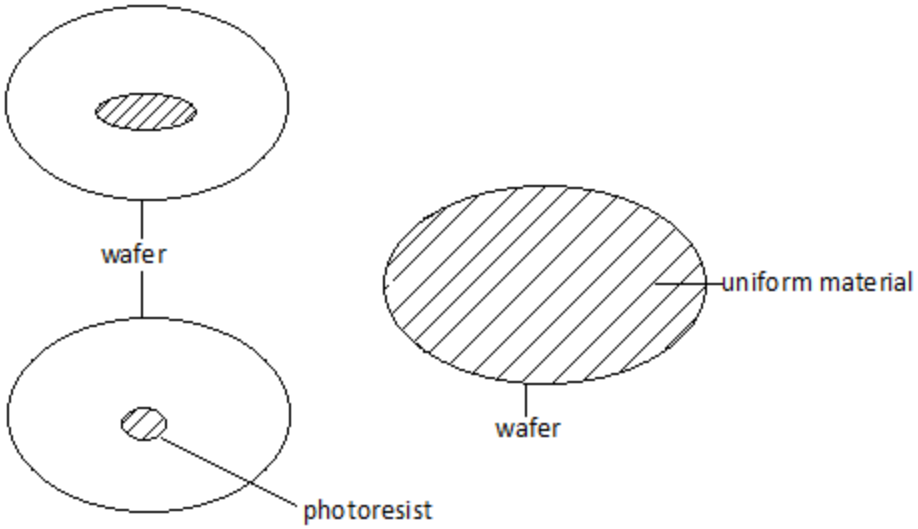
This is done as discussed earlier.

This will result to an oxide.



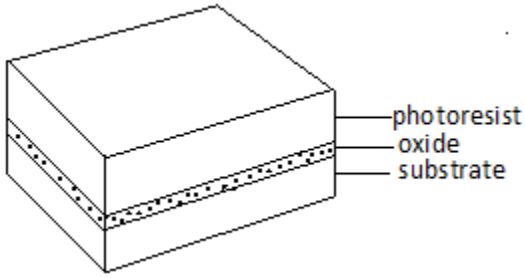
c) Photoresist:

- This is done using casting process.
- The photoresist is applied in droplets and allowed to settle.
- After this it is spinned at a high speed where it spreads uniformly.



The thickness of the of the photoresist will be given by

t = $\frac{kp^2}{\sqrt{w}}$ where k – spinning constant (80-100). p – percentage of solid photoresist. w – spinning rate/1000.

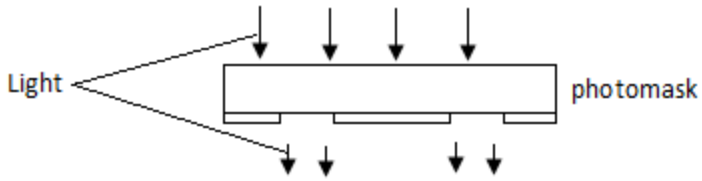


d) <u>Soft bake:</u>

- The photoresist is exposed to high temperature.
- This removes the solid and also prepares the photoresist for exposure.
- The process should be controlled to prevent underbaking or overbaking.
- Underbaking prevents light penetration and thus some sections not required will remain.
- Overbaking allows light penetration.
- The methods are used to prepare the photoresist.
- Hot plate – preferred because it is easier to control, microwave, oven.

e) <u>Mask alignment:</u>

Mask – a mat of glass coated with chrome used to allow light to pass through according to a pattern on the mask.

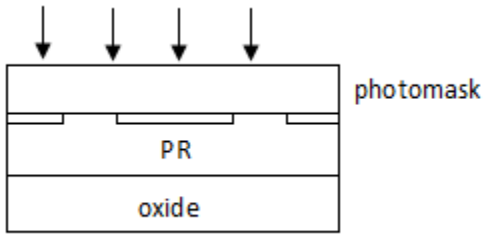


Mask alignment – process of positioning the mask on the photoresist (PR). There are three types of methods for alignment:

i) Contact.
ii) Proximity.
iii) Projected.

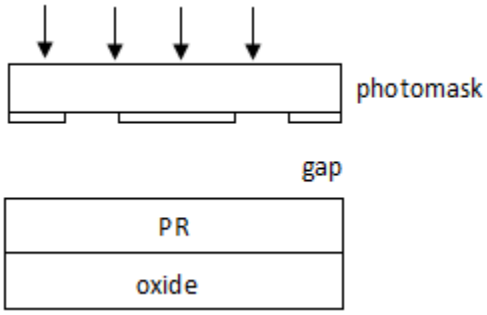
i) <u>Contact:</u>

This is where the mask and photoresist are in contact i.e. there is no gap between them.



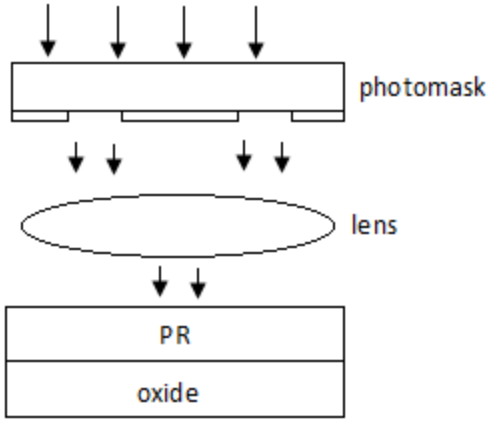
ii) <u>Proximity:</u>

This is characterized by a small gap between the photomask and the photoresist. It reduces chances of the photomask getting damaged.



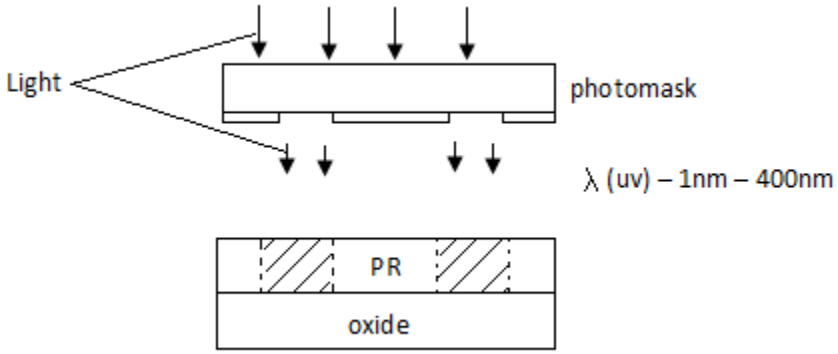
iii) <u>Projected:</u>

There is a gap between the photoresist and photomask. A lens can be put between the two to magnify light energy. The ratio of magnification can be up to 10:1.



f) Exposure:

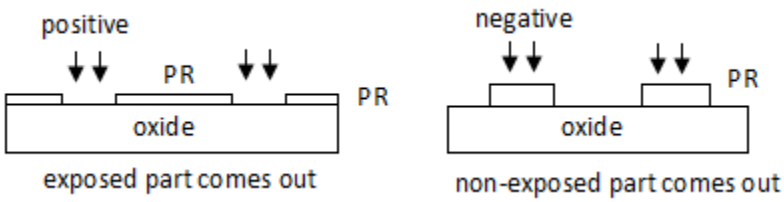
This is the process of exposing the photoresist to light energy to make it soluble.



The most common source of light is ultraviolet because of its small wavelength which can lead to small component structure.

g) Development:

- Process where the photoresist is washed away.
- Depending on whether +ve or –ve photoresist is used, the part that comes out is soluble.
- For the +ve photoresist, the soluble part is the one that is exposed. It is washed away.
- For –ve photoresist, the exposed part is not washed away. It is soluble.

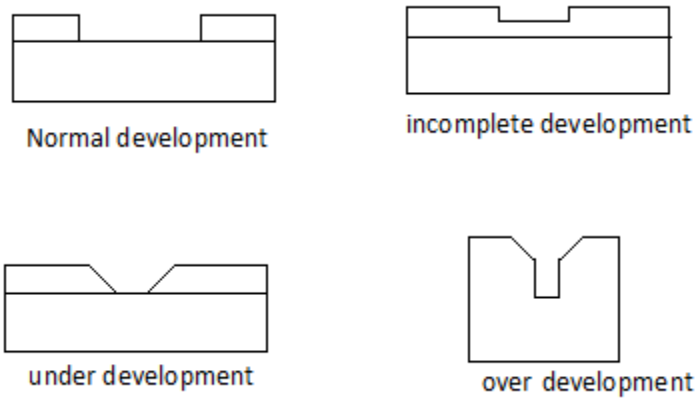


- The first step is to introduce the solvent to wash away the soluble part and then rinse to remove the solvent.
- Lastly, the material is dried up to completely remove any existing liquid.

h) Hard baking:

- The photoresist is exposed to high temperature up to 110°C. This is to prepare the material for etching.
- The process should be controlled to avoid underbaking or overbaking.
- Underbaking will result in the etchant being able to easily remove the photoresist after affecting the formed structure.
- Overbaking will result in a situation where the photoresist will be difficult to remove after all the processes.

NB. One could have normal development, incomplete development, under development and over development.



Incomplete and under development will result from under baking. Over development will result from overbaking (softbaking process).

Pattern Inspection:

- This is done to check whether the pattern formed is as required. If it is not, the photoresist is removed and another is coated to repeat the photolithography process.
- This is important because photolithography is not permanent but the subsequent process like etching, ion implantation and diffusion are.
- It is also done to check for critical dimension (CD).
- Critical dimension is the smallest structure that can be transferred to the PR.

CD = $\sqrt{\lambda g}$ where λ - is wavelength and g – gap between the oxide and photomask.

Example:

Determine the critical dimension given wavelength of 20nm and a gap of 50nm.

CD = $\sqrt{\lambda g}$

= $\sqrt{20\ X\ 10^{-9}\ X\ 50\ X\ 10^{-9}}$ = 31.623 x 10-9 = 31.623nm.

Etching:

This is the process of removing the unwanted sections that have been exposed by photolithography.

There are two methods:

a) Wet etching.
b) Dry etching.
a) Wet Etching:

This is uses a solution which can react with the exposed part, removing it.

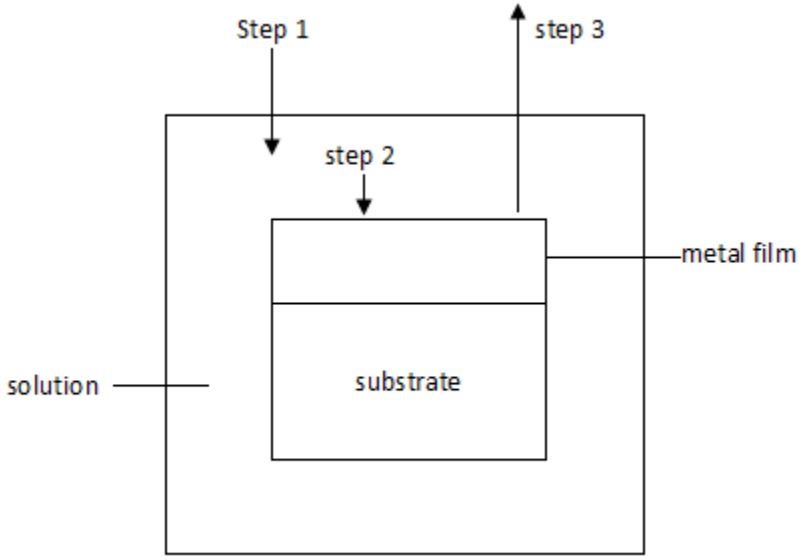
Method 1: One of the simplest etching processes is by coating copper material with wax then using a needle to draw the required pattern. The Copper is then immersed in a solution.

Those sections exposed will come out after reaction with the solution.

Wet etching is a blanket form of etching where the materials are immersed in solution.

Method 2: The other method of wet etching is where the etchant is sprayed on the material.

- This is faster than immersion etching.
- There are three steps in etching:
- Step 1: The reactants are introduced.
- Step 2: The reaction takes place.
- Step 3: The by-products are transported away.



b) Dry Etching:

This involves the use of ions or gases to remove the unwanted sections. There are three methods:

- Reactive ion evaporation.

- Sputtering.
- Vapour phase.

1. Reactive ion evaporation:

Gases are ionized where the ions are accelerated to the material where they react removing the unwanted sector.

2. Sputtering:

The ion are directed at the material at high speed will dislodge the atoms resulting to etching.

3. Vapour phase:

Gases are introduced which react on the surface resulting to other gases and removing the unwanted sections.

Etching can be isotropic or anisotropic.

Isotropic etching: The etching process is uniform in horizontal and vertical directions.

Anisotropic: only takes place in vertical direction.

The level of anisotropic etching can be given as:

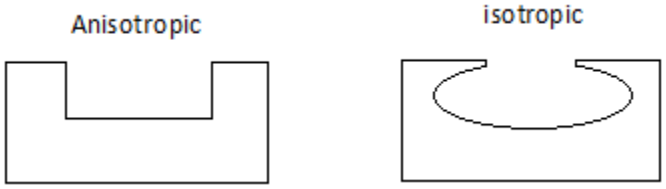
$A_f = 1 - \frac{R_L}{R_V}$ where A_f – Anisotropic level

R_L – Lateral rate.

R_v – Vertical rate.

If $A_f = 0$, then the process is fully isotropic ($\frac{R_L}{R_V} = 1$)

If $A_f = 1$, then it is anisotropic ($\frac{R_L}{R_V} = 0$)



Etching rate uniformly is given by = $\frac{Max\ etching\ rate - Min\ etching\ rate}{Max\ etching\ rate + Min\ etching\ rate}$

Features of dry etching:

1. Faster.
2. Expensive.
3. Complex.
4. Easy to control.
5. Non-isotropic etching.

Diffusion:

This is the process of introducing dopants into a substrate material e.g. silicon.

The most commonly used dopants are:

Boron – to give p-type.

Phosphorus – to give n-type.

The dopants can be in gas, liquid or solid form as compounds with other elements.

Phosphorus - P2O5

Boron – BN.

The dopants are passed through a quartz furnace containing silicon wafers.

The process is similar to oxidation where the high temperature facilitate the diffusion of the dopant into the silicon material.

The dopant flow in a unit area in unit time is given by expression: F = - D $\frac{dc}{dx}$

Where D – diffusion co-efficient.

C – dopant concentration per unit volume.

dx – Change in distance (depth)

substituting the above expression in one dimension expression:

$\frac{dc}{dt}$ = - $\frac{dF}{dx}$

$= \frac{-\, d(-D\, \frac{dc}{dx})}{dx}$

$\frac{dc}{dt}$ = - $\frac{D d^2 C}{dx}$

The expression is called Fick's law or Fick's equation.

D = d_0 exp ($\frac{Ea}{KT}$)

Where Ea – Energy in eV.

D0 – diffusion coefficient obtained by extrapolating to infinity.

K – Boltzmann constant.
T – absolute temperature.

The expression is the concentration rate per unit volume.

Ea ranges from 0.5eV to 2eV.

Ion implantation:

- This involves accelerating ions of the dopant at a high speed to the Si material.
- Because of the high energy levels, they are able to penetrate the Si material to some depth.
- Energy ranges from 1KeV – 1MeV.
- Depth ranges between 10nm - 10μm
- It operates in such a way that the ions are extracted from the source using a voltage of around 40KV.
- The ions are accelerated from the source at a high speed using a voltage of around 180KV.
- They are scanned on the surface of the Si material using electrostatic deflectors.
- The ions get implanted into the Si material obtaining either p-type or n-type semiconductors.

Features of ion implantation:

- Requires low temperature.
- Requires low pressure of around 10^{-4} Pa. Low pressure is to reduce the effect of scattering of ions.
- Complex as compared to diffusion.
- Damages the Si material requiring annealing process after.

Metallization:

- This is the process of reducing ohmic contacts or interconnects on the IC.
- It interconnects the different sections of the IC.
- Aluminum is commonly used since it has high bonding ability with SiO_2
- It is easy to apply.

There are several methods used to introduce the interconnects.

a) Filament evaporation.
b) Flash evaporation.
c) Electron beam evaporation.
d) Sputtering.

a) Filament Evaporation:

The material (aluminium) is evaporated by exposing it to high temperatures then allowed to settle on the substrate. Pallets of the material are used in this process.

b) Flash evaporation:

The material is placed on a ceramic and heated to a high temperature making it evaporate. The gaseous material is then allowed to settle on the substrate.

c) Electron beam evaporation:

An electron beam is directed on the material at high speed.

This will make the material evaporate.

The gaseous material is allowed to settle on the substrate.

d) Sputtering:

Involves ions at high speed striking the material to dislodge atoms which are allowed to settle on substrate.

Basic IC fabrication analysis:

- Electrical properties of intrinsic semiconductor materials:
- Intrinsic semiconductor material.
- At equilibrium, the number of electrons equals to number of hole.
- They are given by n and p.

n – equilibrium concentration of electrons.

p – equilibrium concentration of holes.

The rate of recombination in equilibrium is usually given by:

$R = \gamma np$ where γ is gamma a constant.

Under thermal generation, we have: $G = \gamma n_i^2$ where n_i – intrinsic concentration

Under equilibrium conditions, the rate of recombination and rate of generation are equal i.e.

$R = \gamma np = G = \gamma n_i^2$

$np = n_i^2$

If n increases, p decreases according to the constant np

Conductivity of intrinsic semiconductor materials:

The conductivity is given by:

σ = q($\mu_n n + \mu_p p$)

Where σ - sigma (conductivity)

q – electron charge = 1.6 x 10-19C

μ_n - electron mobility

μ_p - hole mobility.

n – electron concentration.

p – hole concentration

Extrinsic semiconductor material:

If one of the dopants is added to the intrinsic semiconductor, its properties change according to the type of dopant used and its concentration. For n-type material phosphorus atoms are added to come up with more electron charge carriers.

The dopant/ impurities are referred to as dopants and are given as N_p.

The material will have more electrons and thus is called N – type where $n \approx N_D$.

Taking the conduction of intrinsic semiconductor:

σ = q($\mu_n n + \mu_p p$) and taking $n \approx N_D$ and $np = n_i^2$

Substituting n with Np in $np = n_i^2$ obtain

$$N_D P = n_i^2$$

$$P = \frac{n_i^2}{N_D}$$

Substituting the above equation in the conductivity expression we have:

σ = q($\mu_n N_D + \mu_p \frac{n_i^2}{N_D}$)

Taking $\mu_p \frac{n_i^2}{N_D} \approx 0$

$\sigma_n = q\mu_n N_D$

Substituting p with NA

$nN_A = n_i^2$

$n = \frac{n_i^2}{N_A}$

σ = q($\mu_n \frac{n_i^2}{N_A} + \mu_p N_A$)

$\mu_n \frac{n_i^2}{N_A} \approx 0$

$\sigma = q\mu_p N_A$

This is the conductivity of n-type material.

Using the same method, one can obtain conductivity of a p-type material

$\sigma_p = q\mu_p N_A$ where N_A is acceptor concentration.

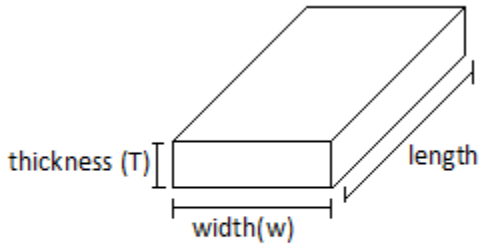
Electrical properties of diffused layers:

For diffused layers, the conductivity can be obtained as above.

From the conductivity, one can get the resistance of a diffused layer.

This is commonly used in analyzing diffused resistors.

For instance, taking the following the following layer one can obtain its resistance.



Resistance = $\frac{\rho L}{A}$

A = T X W

$\rho = \frac{1}{\sigma} = \frac{1}{q\mu_n N_D}$

Resistivity = $\frac{1}{\text{conductivity}}$

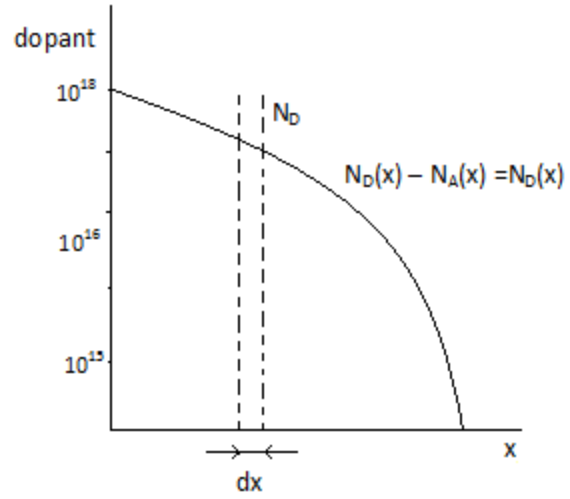
Resistance = $\frac{1}{\text{conductance}}$

Resistance of n-type = $(\frac{1}{q\mu_n N_D})(\frac{L}{WT})$

R = $(\frac{1}{q\mu_n N_D T})(\frac{L}{W})$ = $(\frac{L}{W})$R■

Where R■ - sheet resistance measured in Ω/■

Since most diffused layers are not uniform, the above formula can be changed to take care of the non-uniformity.



The conductance of the material is given by

$$G = \frac{1}{R} = \frac{1}{\frac{L}{W}\left(\frac{1}{q\mu_n N_D T}\right)} = \frac{W}{L}(q\mu_n N_D T)$$

For small changes of distance there will be small changes of conductance:

$$dG = \frac{w}{L}\ (q\mu_n N_D(x)dx)$$

To obtain the total conductance, we integrate the above expression to get

$$\int dG = \int \frac{w}{L}\ (q\mu_n N_D(x)dx)$$

$$G = \int_0^{x_j} \frac{w}{L}\ (q\mu_n N_D(x)dx)$$

Where xj – distance to the junction

$$G = \frac{w}{L}\ q\mu_n \int_0^{x_j} \frac{w}{L}\ (N_D(x)dx)$$

$$R = \frac{1}{G} = \frac{1}{\frac{w}{L} q\mu_n \int_0^{x_j} (N_D(x)dx)}$$

$$= \frac{L}{w}\left[\frac{1}{q\mu_n \int_0^{x_j} \frac{w}{L}(N_D(x)dx)}\right] = \frac{L}{w} R\blacksquare$$

Where $R\blacksquare = \frac{1}{q\mu_n \int_0^{x_j} (N_D(x)dx)}$

$$R\blacksquare = [q\mu_n \int_0^{x_j} (N_D(x)dx)]^{-1}$$

$$R\blacksquare = [q\bar{\mu}_n \int_0^{x_j} (N_D(x)dx)]^{-1}$$ non-uniform diffused layer

where $\bar{\mu}_n - \ average\ mobility$.

Example:

Given a diffused layer with the following parameters:

L = 150μm, w = 50 μm, R■ = 100Ω/■

Calculate the conductance of the material.

R = $\frac{L}{w}$ R■ = $\frac{150\ X\ 10^{-6}}{50\ X\ 10^{-6}}$ X 100

G = $\frac{1}{R}$ = $\frac{1}{300}$ = 3.33mS

Passive components in bipolar integrated circuits:

Passive components can be constructed from diffused layers by using the base, emitter, buried layers, epitaxial layers and pinched epitaxial layers.

Examples of such components are:

- Resistors.
- Capacitors.
- Inductors.
- Diodes.

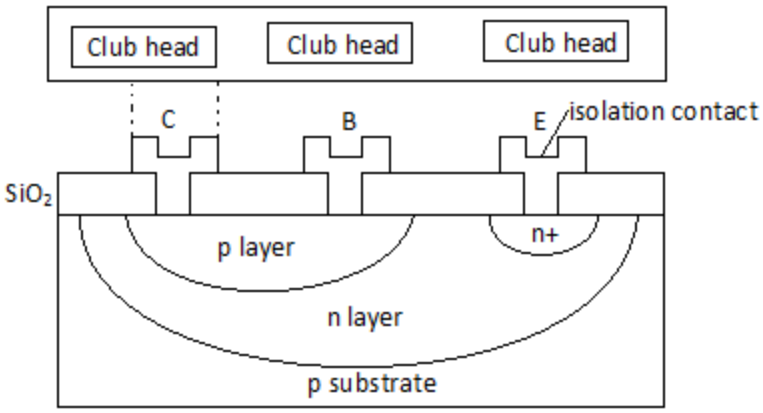
a) Diffused Resistors:

These resistors can be obtained from diffused base, emitter, pinched base, epitaxial and pinched epitaxial layers.

The type of diffused layer to be used depends on:

- Resistance.
- Tolerance.
- Temperature coefficient of the resistor.

Base and emitter diffused resistor:



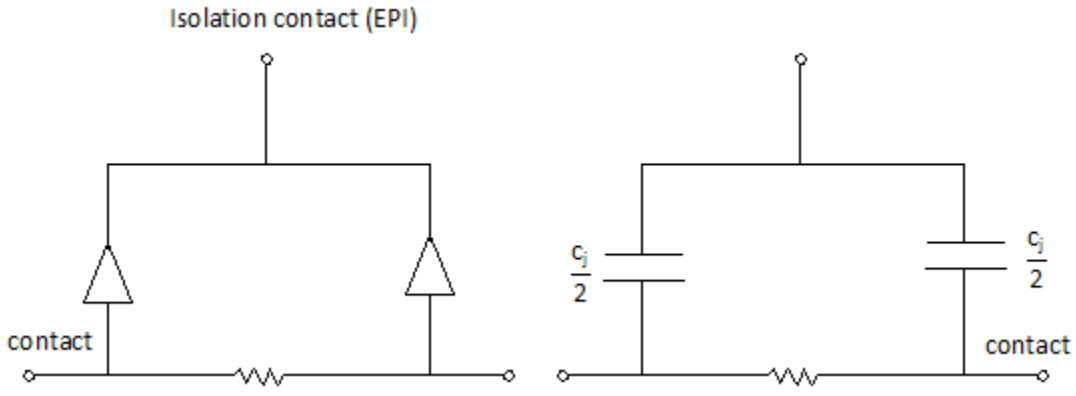
This is formed by a p-type layer from the base of n-p-n transistor technology for it to operate, the p-type material should be isolated from the n-type material by connecting the two n-type materials to a +ve voltage which will form a p-n junction.

The collector-base and base-emitter are reverse biased. This is done by using an isolation contact as given in the diagram.

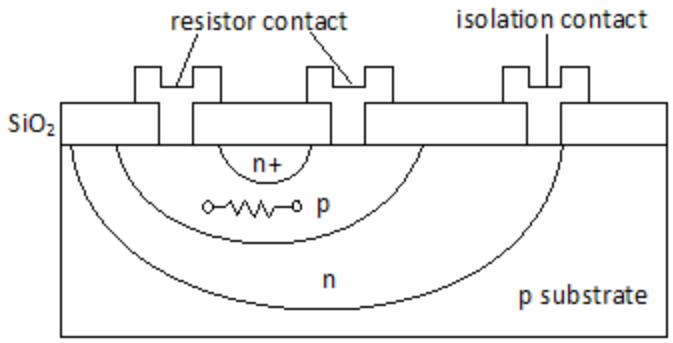
This layer gives low resistance of high tolerances.

There is a limit to the maximum voltage that can be applied across the resistor without breakdown.

It can be modeled using two capacitors and a resistor as shown below since there is a junction formed across the length of the resistor.



Pinched Base:



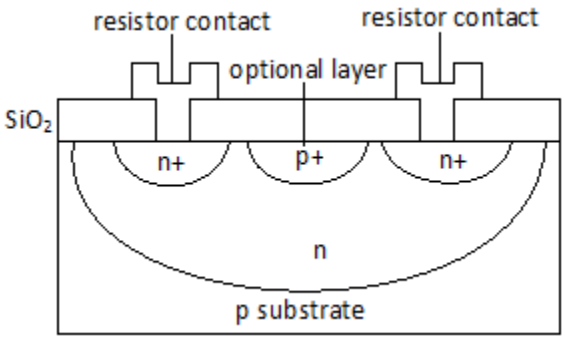
The pinched base has the emitter between the two resistor contacts.

It reduces the thickness of the base and thus increasing resistance.

This sheet resistance can be 1KΩ/■ to 10KΩ/■

It is commonly used in high resistance applications.

Epitaxial and pinched epitaxial layers:



Epitaxial layer does not have the optional p-type.

The n-type layer is used as the resistance.

The one with the optional p-type material has a pinched epitaxial layer.

This will have more resistance than the first one since the thickness of the epitaxial layer is reduced.

The resistors have less resistance and poor temperature coefficient.

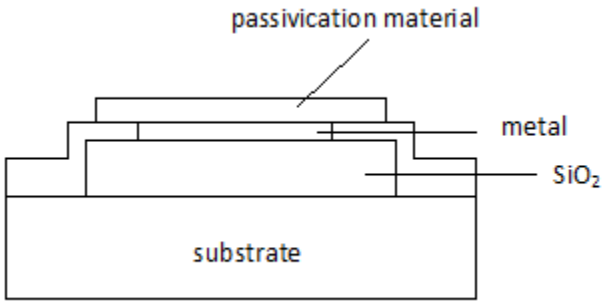
They can be applied in low voltage applications, only up to around 7V.

High performance Resistors:

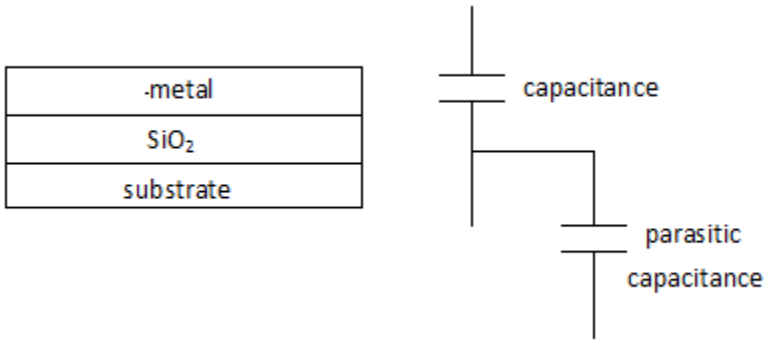
These are constructed using a thin film of metallic material e.g. tantalum or nichrome.

The thin film can be obtained using metallization methods.

They have high resistance and can be used in high voltage applications.



Capacitance:



Constructed by depositing a metallic film on SiO_2 supported by a substrate to form capacitance

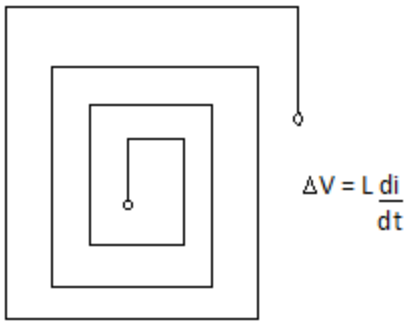
The capacitance is very small ranging from pF to femtoFarads (fF = 10^{-15}F).

These capacitors can be used in high frequency operations.

Inductors:

These have application in high frequency ICs.

They are constructed by depositing a metallic material on a substrate in a spiral form.



The commonly used formula to obtain inductance is a s below:

LC = $\mu\varepsilon$

L = $\mu\varepsilon$/C

L – Inductance.

C – Capacitance.

μ - permeability

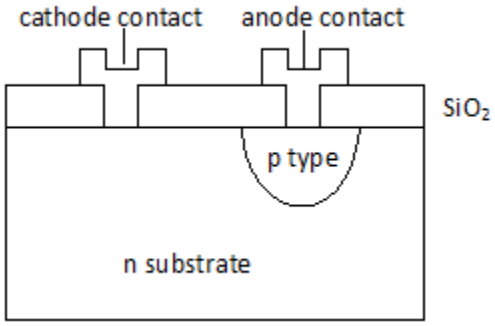
ε – permittivity

In semiconductor materials, capacitance is given by:

C/A = pF/μm2.

C = (C/A)x A

Diode:



This is constructed by doping n type substrate with p-type in a small section.

The p-type section is connected to a contact (anode) and n-type to another contact (cathode).

Parameters:

a) Built in voltage: $\emptyset_o$

This is the voltage across the junction

$\emptyset_o = \emptyset_T \ln(\frac{N_A N_D}{n_i^2})$

Where $\emptyset_T$ - thermal voltage = 25mV.

b) Junction capacitance:

This exists since the depletion layer has immobile ions and is given by:

$C_j = \frac{c_{jo}}{(1-\frac{V_D}{\emptyset_0})^m}$

C_{jo} – capacitance in junction without bias voltage.

V_D – voltage across diode.

$\emptyset_o$ - built in potential.

m – grading coefficient.

m = ½ for abrupt junction.

m = 1/3 for graded junction.

Gradual change of charge carriers or ions.

Example:

Calculate the resistance of a diffused resistor with R■ = 150Ω/■, L = 1μm, w = 10nm.

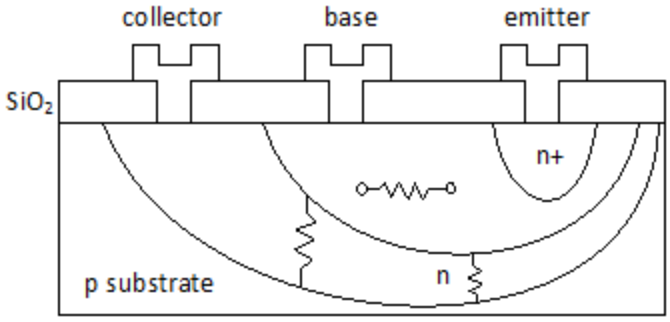
Also calculate capacitance given area = 100 μm^2 and C/A = 10-4 pF/ μm^2

Resistance R = $\frac{L}{w}$ R■ = $\frac{1\mu m}{10nm}\ x\ 100$ = 15KΩ.

Capacitance C = (C/A) x A = 10-4 pF/ μm^2 x 100 μm^2 = 0.01pF.

Active components in bipolar ICs:

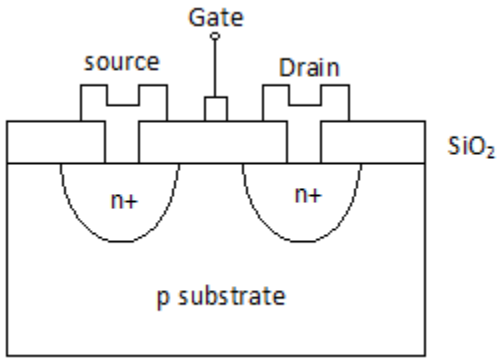
n-p-n transistor:



- It is constructed by heavily doping the emitter with ND dopants.
- The collector and base are lightly doped.
- There are several parameters that affect the operation of this transistor.
- In small signal applications or high frequency applications.
- Saturation current, I_s.
- Parasitic resistances:
- Base resistance.
- Collector resistance.
- Parasitic capacitances:
- Base-Emitter capacitance.
- Collector-base capacitance.
- Collector substrate capacitor.
- Gain.

N-Channel transistor:

<u>MOSFET:</u>



Construction is done in such a way that there are two heavily doped n-type in a p-type substrate.

They are separated by the substrate.

One forms the drain and the other forms the source.

Gate is insulated by SiO_2.

It also has several parameters that need to be considered in high frequency.

Parameters:

- Threshold voltage.
- Effective channel length.
- Effective channel width.
- Gate source capacitance.
- Source substrate capacitance.
- Drain substrate capacitance.

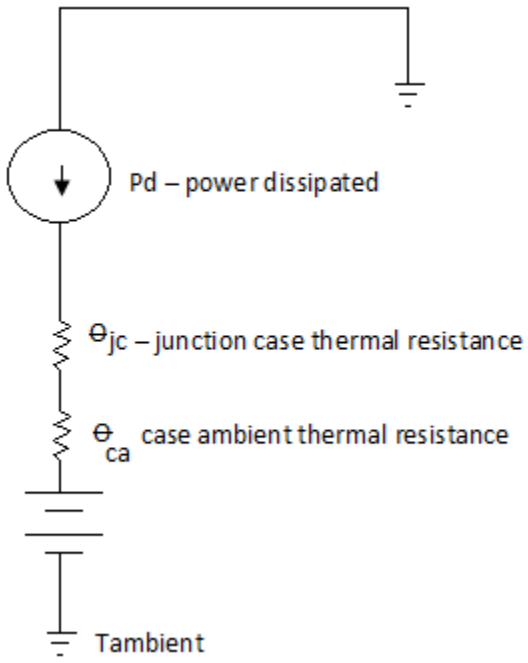
Packaging Consideration:

Packaging is important since it determines the power dissipation and reliability of the component.

Power dissipation:

Depending on the amount of heat generated, a heat sink can be used or the package itself can be enough to dissipate heat.

The power dissipation can be modeled as below.



Chip temperature, $T_{chip} = T_{ambient} + (\theta_{jc} + \theta_{ca})Pd$.

Example:

Calculate the power dissipated if T_{chip} = 70°E, $T_{ambient}$ = 30°, ($\theta_{jc} + \theta_{ca}$) = 120°c/w.

Pd = $\frac{T_{chip} - T_{ambient}}{\theta_{jc} + \theta_{ca}} = \frac{70-30}{120}$ = 40/120 = 0.33W.

Reliability:

This needs to be high and therefore depending on the environmental conditions

Ceramic – strong, expensive.

Plastic – cheap, weak.

CAM, CAD

In the design of ICs

Charge coupled devices.

Light sensitive devices – photoconductive materials applied in cameras.