CSMC 0.5um MM DPTM PDK – st02

Reference Manual

Rev 1.0

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2 Overview

The purpose of this document is to describe the technical details of the CSMC 0.5um MM DPTM Process Design Kit (PDK) provided by Cadence Design Systems, Inc. (Cadence). This PDK requires the UNIX environment variable CDS_Netlisting_Mode to be set to Analog. Training is not provided as part of this PDK.

3 Supported Design Tools

Cadence Design Framework II, version 5.0 Virtuoso Custom Design Platform:

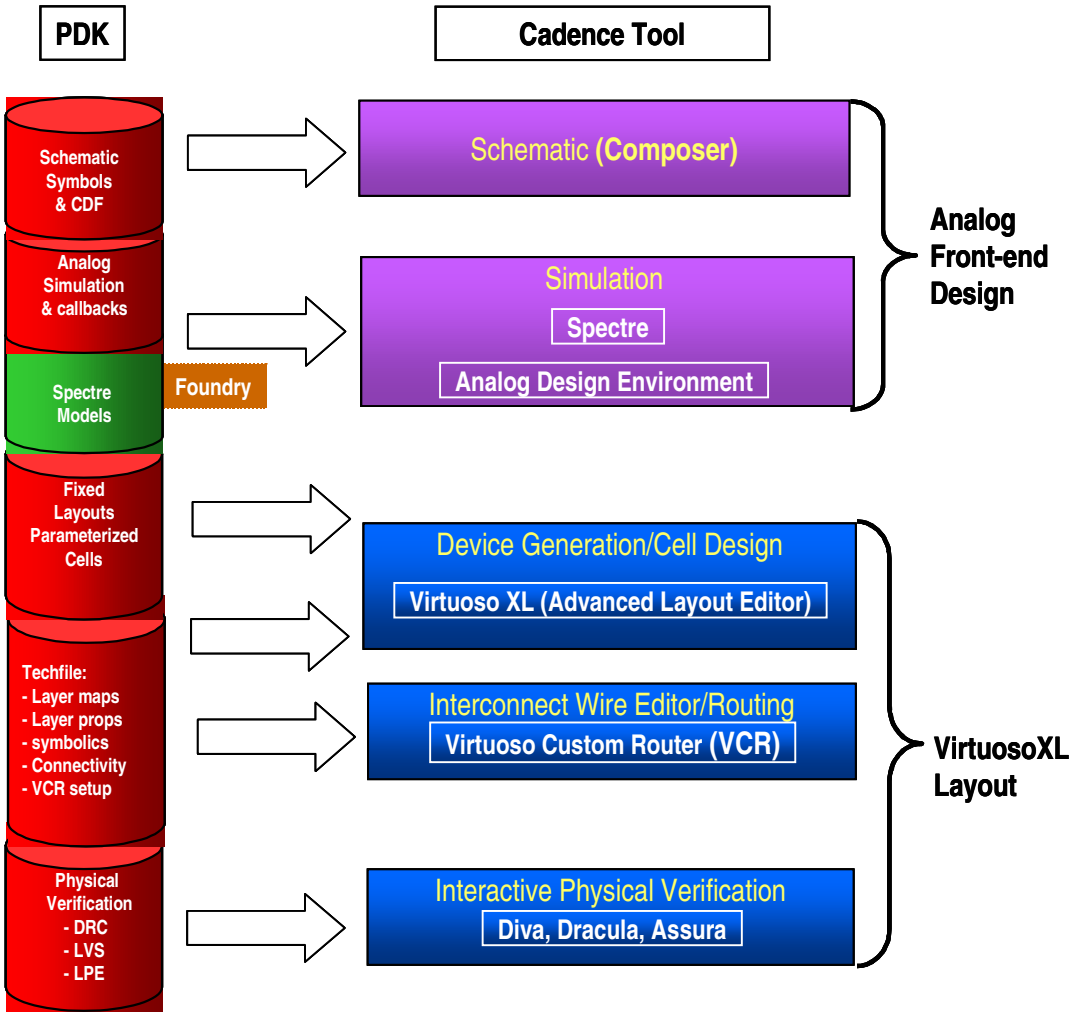
- Virtuoso Schematic Editor
- Virtuoso Analog Design Environment including Spectre and Hspice simulation
- VirtuosoLE, VirtuosoXL and Virtuoso Custom Router
- Dracula DRC, LVS, LPE and PRE
- CDL netlisting
- Stream In/Out

4 Foundry Data

- **WTD-73D22** **Revision 6J07**
  6S05DPTM-STXX Mixed Signal Design Rule
- **WTD-73E60** **Revision 6A06**
  6S05DPTM-ST0200 Process Electrical Design Rule
- **s05mixddst02v23.scs**
  Spectre models
- **h05mixddst02v23.lib**
  Hspice models

5 What makes up a PDK?

PDK stands for Process Design Kit. A PDK Contains the process technology and needed information to do device-level design in the Cadence DFII environment.



6 Installation of the PDK

The PDK is distributed in compressed tar format. The distribution file name contains the PDK name and release time stamp:

st02_*YYYYMMDDhhmm*.tar.gz

To install the PDK, logon to the computer as the user who will own and maintain the PDK.

Choose a disk and directory under which the PDK will be installed. This disk should be exported to all client machines and must be mounted consistently across all client machines.

Change working directory to the location where the PDK will be installed:

cd *<pdk_install_parent_directory>*

Extract the PDK from the archive using the following commands:

gzip -dc …/st02_*YYYYMMDDhhmm*.tar.gz | tar -xvf -

This will produce a single directory with a name similar to following format:

st02_*YYYYMMDDhhmm*

This is the PDK installation directory for the CSMC 0.5um MM DPTM process.

The default permissions on the PDK have already been set to allow only the owner to have write, read and execute access. Other users will have only read and execute access.

7 PDK Install Directory Structure/Contents

st02_reference_manual.pdf – This document.

README – Text file containing delivery information.

cds.lib – Text file defining Cadence libraries.

icc.rules – Virtuoso Custom Router rules file.

st02/ – CSMC 0.5um MM DPTM PDK Cadence library.

st02/display.drf – Text version of display resource file.

st02/techfile.tf – Text version of technology file.

ruledeck/ - Dracula verification files.

8 Creation of a Design Project

A unique directory should be created for each circuit design project. The following command can be executed in UNIX:

```
mkdir ~/circuit_design

cd ~/circuit_design
```

All work by the user should be performed in this circuit design directory. The user should create a "cds.lib" file. Using any text editor, the following entry should be put in the cds.lib file:

```
INCLUDE <pdk_install_directory>/cds.lib
```

Where "pdk_install_directory" is the path to where the CSMC 0.5um MM DPTM PDK was installed.

9 Techfile Methodology

The st02 library techfile will be designated as the **master** techfile. This techfile will contain all required techfile information. There is an ASCII version of this techfile shipped with the PDK. This ASCII version represents the techfile currently compiled into the st02 library.

The **attach** method should be used for any design library that is created. This allows the design database techfile to be kept in sync with the techfile in the process PDK. To create a new library that uses an attached techfile, use the command *File->New->Library* from either the CIW or library manager and select the *Attach to an existing techfile* option. Select the st02 library when asked for the name of the *Attach To Technology Library*.

10 Schematic Design

The user should follow the guidelines listed below while building schematics using Composer:

Project libraries should list the primitive PDK library as a reference library in the library properties form.

Users can add instances from the PDK library to designs stored in the project libraries.

When performing hierarchical copy of schematic designs care should be taken to preserve the references to the PDK libraries. These references should not be copied locally to the project directories and the references set to the local copy of PDK cells. This would prevent your designs from inheriting any fixes done to the PDK library from an upgrade.

Users should exercise caution when querying an instance and changing the name of the cell and replacing it with a reference to another cell. While like parameters will inherit values, callbacks are not necessarily executed. This would cause dependent parameters to have incorrect values.

Schematics should be designed with schematic driven layout methodology in mind. Partitioning of schematics, hierarchical design, input and output ports, should be done in a clean and consistent fashion.

11 Library Device Setup

11.1 MOSFETS

All mosfets in the PDK library are 4 terminal devices, with the body terminal explicitly connected.

Units:
Length and width are in meters, with areas and perimeters in meters squared and meters, respectively. Design variables are allowed for Length and Width entries.

Calculation:
The area and perimeter parameters for the sources and drains are calculated from the width and the number of fingers used. This calculation assumes that the drain will always have the less capacitance (area) when there are an even number of fingers (odd number of diffusion areas). The width per finger is calculated by dividing the width by the number of fingers. This parameter is for viewing by the designer.

Simulation:
These mosfets are netlisted as their predefined device names for simulation purposes. CSMC's model definitions are used for these devices.

11.2 Resistors

All resistors in the PDK library are 2 terminal devices.

Units:
The width is specified in meters for schematic simulation. All parameters entered into the resistor form must be integers or floating point numbers. No design variables are supported due to the calculations that must be performed on the entries.

Calculation:
The length of the resistor segment is calculated from the resistance value, the width, and the number of parallel or series segments specified. These calculations are based on the CSMC data provided in the design rule manuals and SPICE models provided by CSMC. See the Foundry Documents section for document names.

The width and length are snapped to grid, and the resistances are recalculated and updated on the component form based on actual dimensions.

Simulation:
CSMC supplied models are used to model the resistors.

11.3 Bipolar Transistors

All BJTs in the PDK library are 3 terminal devices.

Units:
Only fixed size devices are allowed.

Calculation:
The area is calculated from the emitter size.

Simulation:
These BJTs are netlisted as their predefined device names for simulation purposes. CSMC's model definitions are used for these devices.

11.4 Diodes

All diodes in the PDK library are 2 terminal devices.

Units:
Length and width are in meters. Design variables are not allowed for length and width entries.

Calculation:

The area and perimeter are calculated from the width and length entered.

Simulation:

These diodes are netlisted as their predefined device names for simulation purposes. CSMC's model definitions are used for these devices.

11.5 Capacitors

The capacitor in the PDK library is a 2 terminal device.

Units:
The length and width of pipcaps are specified in meters for schematic simulation. All parameters entered into the capacitor form must be integers or floating point numbers. No design variables are supported due to the calculations that must be performed on the entries.

Calculation:

The capacitance is calculated from the width and length.

Simulation:

CSMC's model definitions are used for these devices.

12 Supported Devices

12.1 MOSFETS

- **mn** 5V normal NMOS transistor
- **mnlvt** 5V low vt NMOS transistor
- **mndep** 5V depletion NMOS transistor
- **mp** 5V normal PMOS transistor
- **mplvt** 5V low vt PMOS transistor
- **mpdep** 5V depletion PMOS transistor

12.2 Resistors

- **rnplus** N+ diffusion resistor
- **rpplus** P+ diffusion resistor
- **rnpoly1** N+ poly1 resistor
- **rppoly1** P+ poly1 resistor
- **rpoly2** Poly2 resistor
- **rhr1k** 1K ohm high resistance poly2 resistor
- **rhr2k** 2K ohm high resistance poly2 resistor
- **rnwell** Nwell resistor

12.3 Bipolars

- **qvp5** Vertical PNP Area=5*5
- **qvp10** Vertical PNP Area=10*10
- **qvp20** Vertical PNP Area=20*20
- **qvn10ba** Vertical NPN with P-base Area=10*10
- **qvn20ba** Vertical NPN with P-base Area=20*20

12.4 Diodes

- **dnppw** N+/Pwell diode
- **dppnw** P+/Nwell diode

12.5 Capacitors

- **cpip** PIP capacitor

12.6 Fuse

- **fp1** Poly1 fuse

13 Views Provided

13.1 MOSFETS

- Four terminals (D, G, S, B)
- symbol, spectre, hspiceD, auLvs, auCdl, ivpcell, layout (Pcell)

13.2 Resistors

- Two terminals (PLUS, MINUS)
- symbol, spectre, hspiceD, auLvs, auCdl, ivpcell, layout (Pcell)

13.3 Bipolar Junction Transistors

- Three terminals (C, B, E)
- symbol, spectre, hspiceD, auLvs, auCdl, ivpcell, layout (Fixed layout)

13.4 Diodes

- Two terminals (PLUS, MINUS)
- symbol, spectre, hspiceD, auLvs, auCdl, ivpcell, layout (Pcell)

13.5 Capacitors

- Two terminals (PLUS, MINUS)
- symbol, spectre, hspiceD, auLvs, auCdl, ivpcell, layout (Pcell)

13.6 Fuse

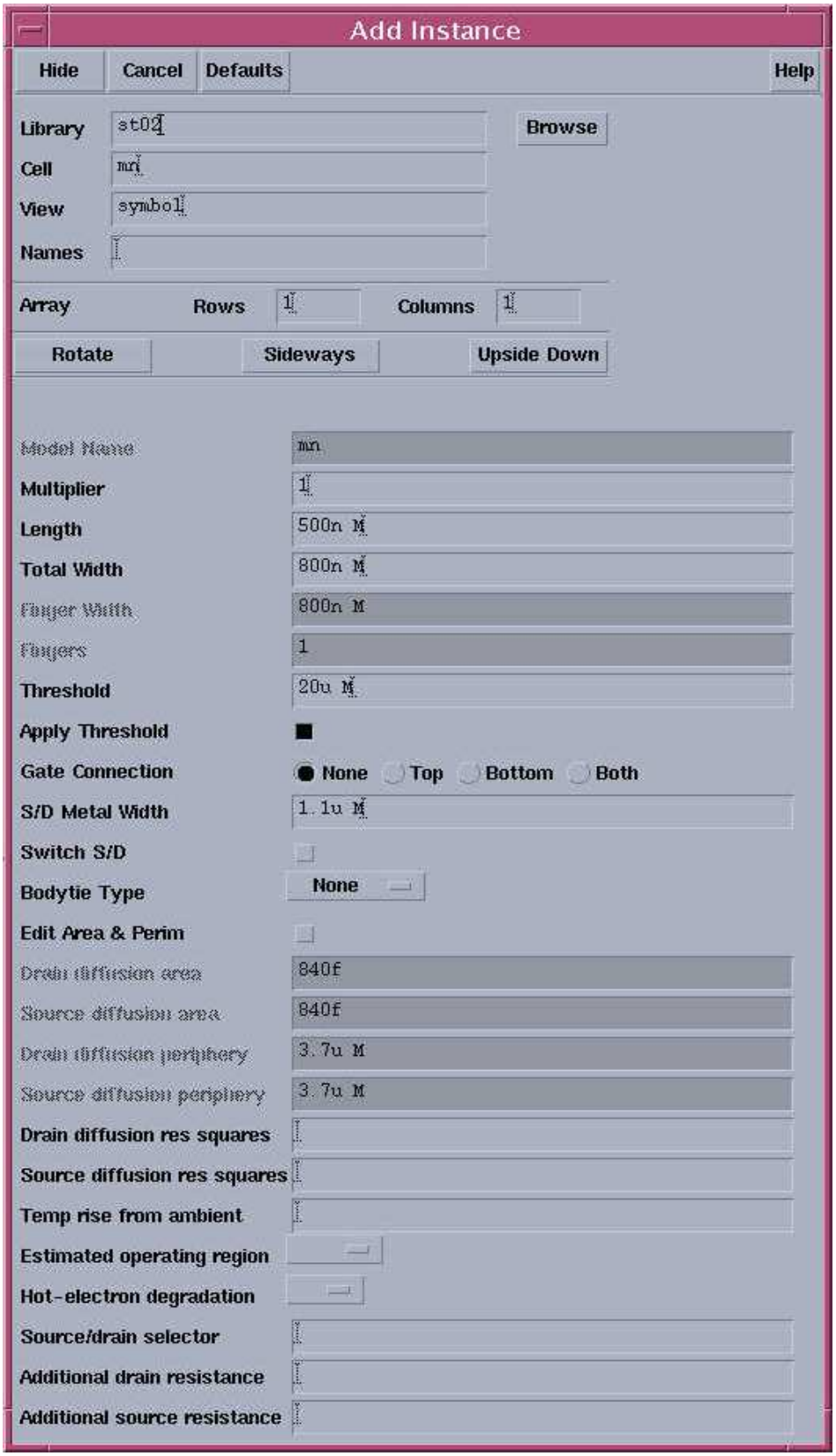
- Two terminals (PLUS, MINUS)
- layout (Fixed layout)

14 CDF parameters

14.1 MOSFETS

- **Model Name** - Spectre model name (non-editable)
- **Multiplier** - Number of parallel devices
- **Length** - Gate length in meters
- **Total Width** - Gate width in meters (sum of all fingers)
- **Finger Width** - Width of each gate finger
- **Fingers** - Number of gate fingers in layout
- **Threshold** – Finger width at which to apply device folding in the layout
- **Apply Threshold** – Button to apply threshold or not
- **Gate Connection** – Allow shorting of multi-finger devices and addition of contact heads to gate ends.
- **S/D Connection** – Allow shorting of source and/or drains on multi-finger devices
- **S/D Metal Width** – Width of source/drain metal
- **Switch S/D** – Source is defined as left-most diffusion region and alternating regions to the right. Pins are not automatically permuted and can be switched using this parameter.
- **Bodytie Type** – None, Detached, or Integrated (butting source).
    - For Detached, user may select Left, Right, Top, and/or Bottom to specify the location of bodyties. Selecting all four creates a guardring.
    - For Detached, the user may specify Tap Extension (in microns) which sets the distance from the bodytie to the device. Maximum distance is 100 microns.
    - For Integrated, the user may select Left or Right for a device with an odd number of fingers (1, 3, 5, …). The user may select Left and Right for an even fingered device.
- **Drain diffusion area, etc** – Several simulation parameters are presented. The area and perimeter parameters are calculated and netlisted in accordance with the foundry models.

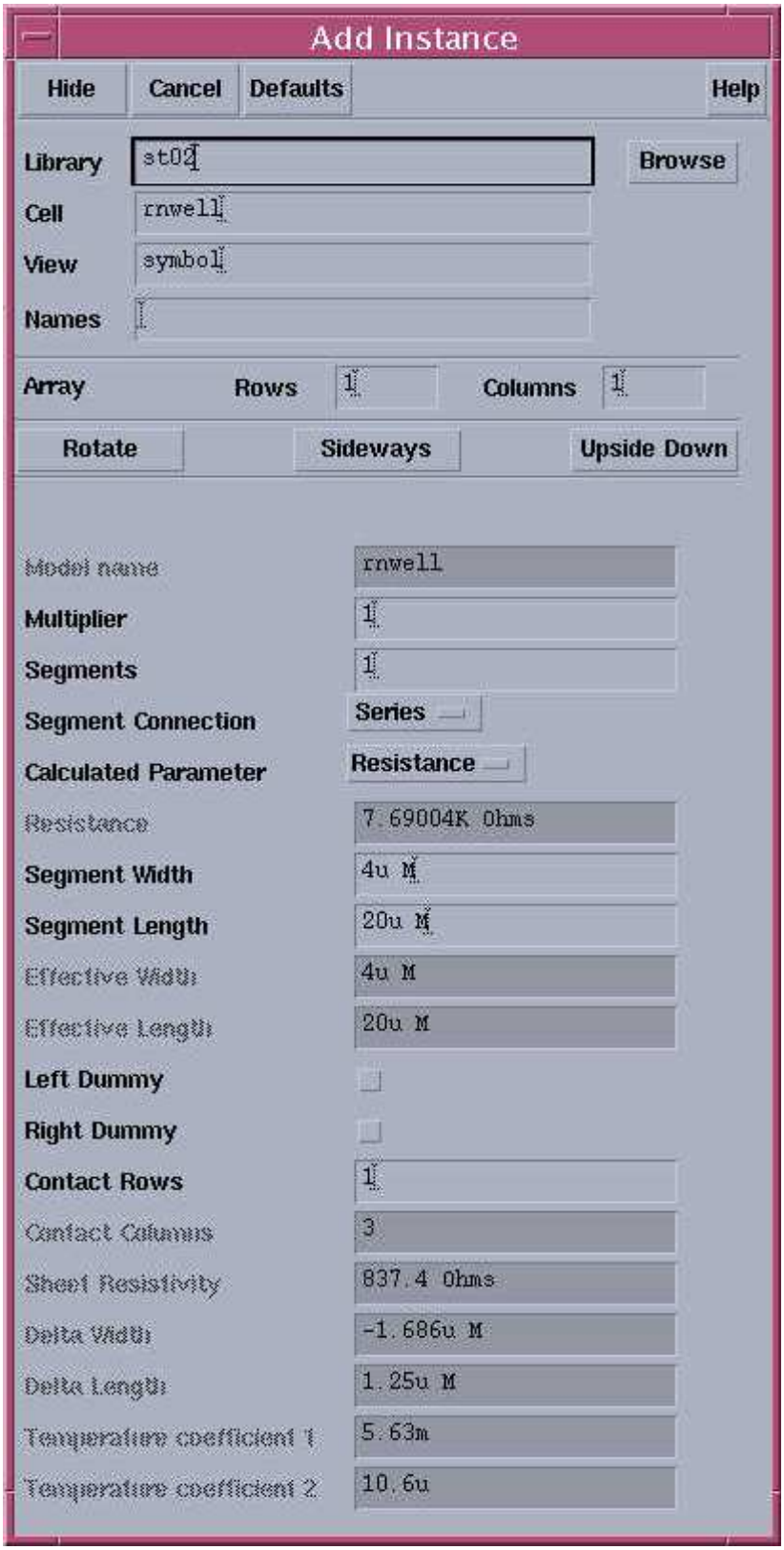
MOSFET ADD INSTANCE FORM



14.2 Resistors

- **Model name** – Spectre model name (non-editable)
- **Multiplier** - Number of parallel devices
- **Segments** – Number of resistor segments
- **Segment Connection** – Connection between segments (Parallel, Series)
- **Calculated Parameter** – Parameter to be calculated (Resistance, Length)
- **Resistance** – Entry or calculated value for resistance
- **Segment Width** – Entry value for segment width in meters
- **Segment Length** – Entry or calculated value for segment length in meters
- **Effective Width** – Calculated value based on number of segments, segment width, and segment connection (non-editable)
- **Effective Length** – Calculated value based on number of segments, segment length, and segment connection (non-editable)
- **Left Dummy** – Toggle for placement of dummy resistor segment on the left side
- **Right Dummy** – Toggle for placement of dummy resistor segment on the right side
- **Contact Rows** – Entry value for number of contact rows in each segment head
- **Contact Columns** – Calculated value for number of contact columns in each segment head (non-editable)

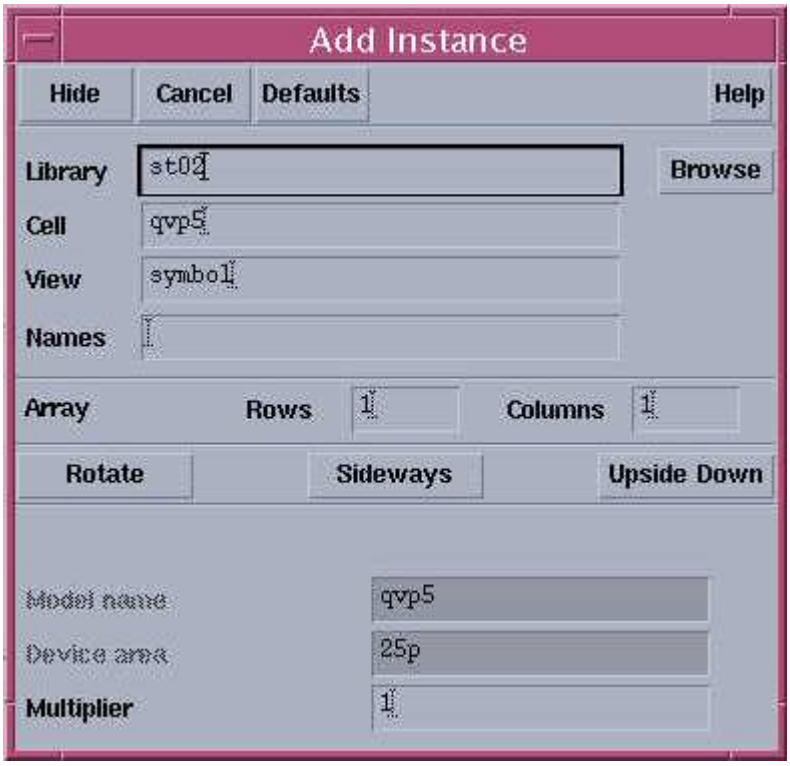
RESISTOR ADD INSTANCE FORM



14.3 Bipolar Junction Transistors

- **Model name** - Spectre model name (non-editable)
- **Device area** – Area of the emitter in meters squared (non-editable)
- **Multiplier** - Number of parallel devices

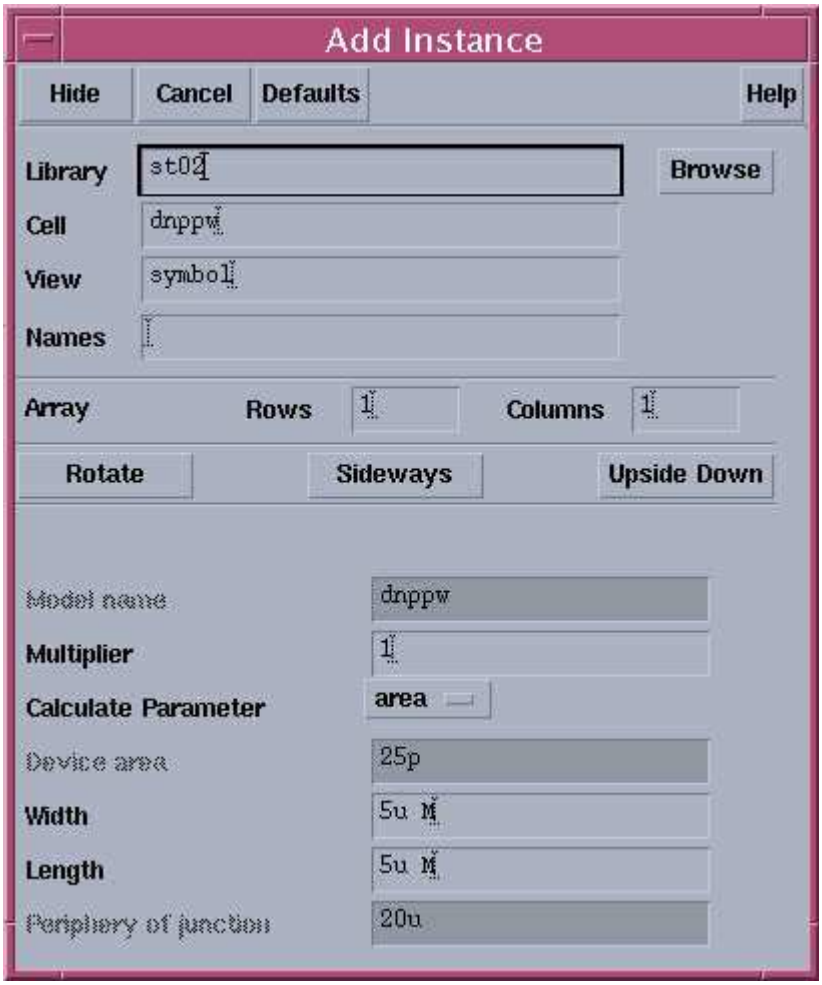
BIPOLAR ADD INSTANCE FORM



14.4 Diodes

- **Model name** - Spectre model name (non-editable)
- **Multiplier** - Number of parallel devices
- **Calculated Parameter** – Parameter to be calculated (area, width, length)
- **Device area** - Diode area in meters squared
- **Width** - Diode width in meters
- **Length** - Diode length in meters
- **Periphery of juction** - Diode perimeter in meters (non-editable)

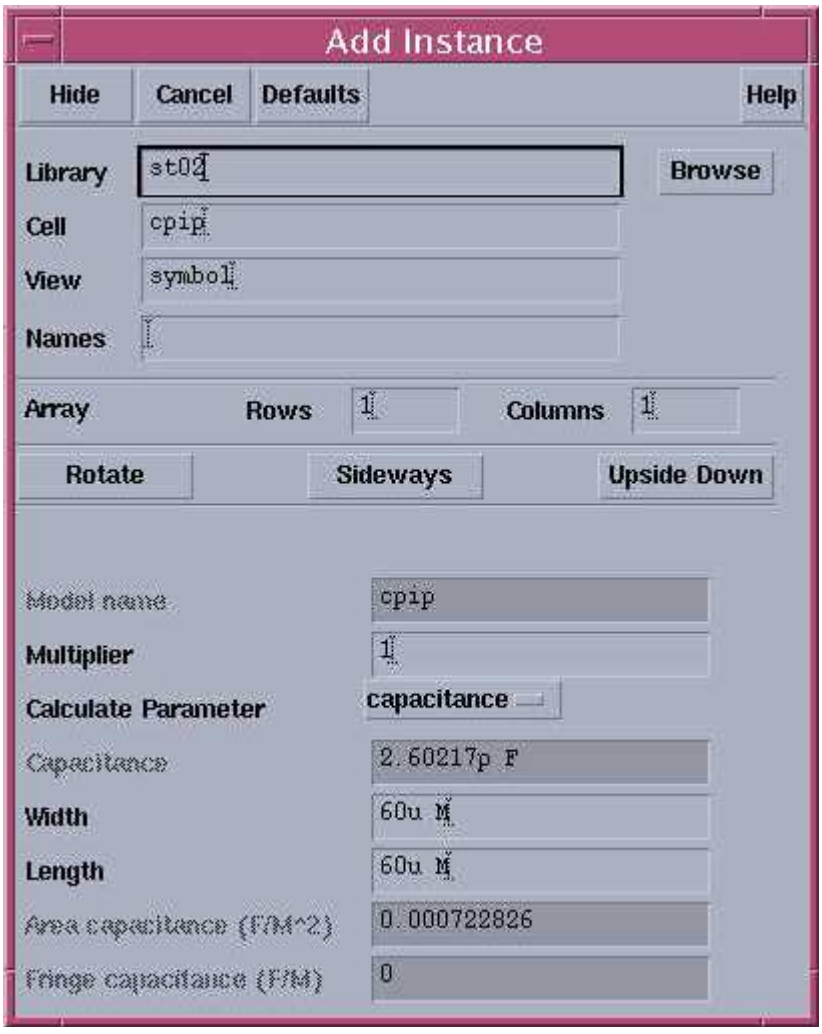
DIODE ADD INSTANCE FORM



14.5 Capacitors

- **Model name** – Spectre model name (non-editable)
- **Multiplier** - Number of parallel devices
- **Calculated Parameter** – Parameter to be calculated (capacitance, length, width)
- **Capacitance** – Capacitance corresponding to the length and width
- **Width** - Capacitor width in meters
- **Length** - Capacitor length in meters
- **Area capacitance** – Capacitance per unit area in F/M^2 (non-editable)
- **Fringe capacitance** – Capacitance per unit length in F/M (non-editable)

CAPACITOR ADD INSTANCE FORM



Component Label Defaults

14.6 MOSFETS

- component parameters: model, w, l, m
- operating point: id, vgs, vds, gm
- model: vto, kp, gamma
- instance name prefix: NM, PM

14.7 Resistors

- component parameters: r, segW, segL, segments, connection,m
- operating point: v i pwr
- model: tc1 tc2 coefs
- instance name prefix: R

14.8 Bipolar Junction Transistors

- component parameters: model, area
- operating point: betadc, ic, Vce
- model: bf, is, va
- instance name prefix: Q

14.9 Diodes

- component parameters: model, area, m
- operating point: id, vd, reg
- model: is, rs, n
- instance name prefix: D

14.10 Capacitors

- component parameters: model, c, w, l, m
- operating point: i
- model:
- instance name prefix: C

15 Techfile Layers

Techfile layers defined in the PDK are done in compliance with technology file supplied by CSMC. The compiled technology file with this PDK contains all layer/purpose as defined in the CSMC supplied techfile. Layer names and visibility /selectability may be altered from this technology file, if necessary.

16 Virtuoso XL

The standard Cadence Virtuoso XL design flow is implemented. This includes basic connectivity of connection layers, wells, and substrate, and symbolic contacts. The M factor is used for device instance multiplier - there is no conflict with the parameter used in cell operation. Names are displayed on the layout views to aid in schematic-layout instance correlation. Auto-abutment of MOSFET devices is supported. Pin permuting of MOSFET and Resistor device is also supported.

The users should follow the guidelines listed below for layout design:

The VirtuosoXL tool requires a separate license for operation.

Users obtain maximum leverage from the PDK by doing schematic driven layout in the Virtuoso XL environment. This flow will produce a correct design layout. The Virtuoso Custom Router (IC Craftsman) can be used to finish the interconnect in the layout.

Abutment is currently supported only for MOS transistors. Note, abutment will work only on schematic driven layouts.

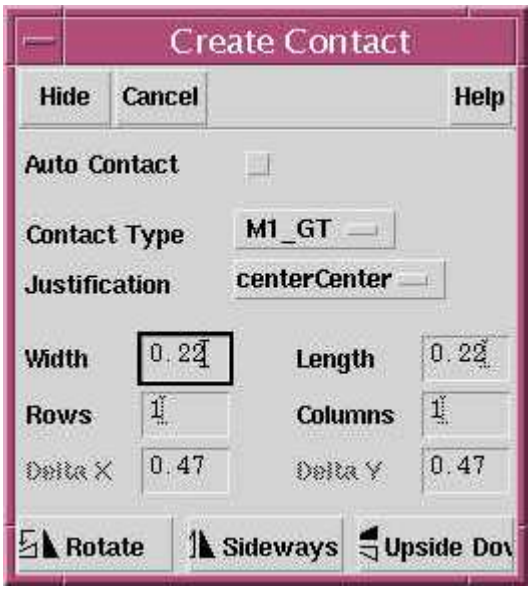
Schematic Driven Layout is recommended over Netlist Driven Layout.

NOTE: Skill pcell source code is not included in the PDK kit.

16.1 Symbolic Contacts

- NDIFF_M1 N+ Diff to Metal1 Contact
- PDIFF_M1 P+ Diff to Metal1 Contact
- POLY1_M1_LV Poly1 to Metal1 Contact for LV
- POLY1_M1_HV Poly1 to Metal1 Contact for HV
- POLY2_M1_cap Poly2 to Metal1 Contact for cap
- POLY2_M1_res Poly2 to Metal1 Contact for res
- M1_M2 Metal 1 to Metal 2 Via
- M2_M3 Metal 2 to Metal 3 Via

CREATE CONTACT FORM



17 Known Problems & Solutions

Note: There are two rhr poly2 resistors, rhr1k and rhr2k, that are exactly the same except for the marker layer. Both cannot be used in the same design, use only one.