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(54) METHOD OF MANUFACTURING THIN FILM TRANSISTOR

VERFAHREN FÜR HERSTELLUNG VON DÜNNFILMTRANSISTOR

PROCÉDÉ DE FABRICATION DE TRANSISTOR EN COUCHES MINCES

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Description

TECHNICAL FIELD

[0001] The present disclosure relates to the field of display device technology, and more particularly to a method for manufacturing a thin film transistor.

BACKGROUND

[0002] In a manufacturing process of a thin film transistor (TFT), as a material of an active layer in the TFT, a low temperature polysilicon (LTPS) thin film is commonly adopted.

[0003] Currently, during a preparation process of the TFT, an excimer laser annealing (ELA) approach is mainly adopted to form the LTPS thin film. The ELA approach mainly performs a laser beam irradiation on amorphous silicon thin film through an excimer laser having certain energy to transform the amorphous silicon into the LTPS at high temperatures using a laser beam energy. However, when the amorphous silicon is irradiated with the laser beam, all regions after irradiating is of a same temperature; therefore, a growth region of a polysilicon grain in the LTPS thin film after crystallization is random. This makes grains in the LTPS thin film be variable in size and of less uniformity, and causes a large amount of crystal boundaries in a TFT channel, which results in a large leakage current of the TFT, and further results in a unstable threshold voltage of the TFT, thus degrading a whole electrical performance of the TFT.

[0004] CN 102 610 520 A discloses a preparation method of a polycrystalline silicon thin film transistor. The polycrystalline silicon thin film transistor includes an active layer made of polycrystalline thin films with strip-shaped continuous crystalline domains.

[0005] US 2003/0211666 A1 discloses a thin-film transistor formed by a polycrystalline silicon film having a thin-film part and a thick-film part, the thin-film part minimally being used as a channel part.

[0006] US 2005/0224876 A1 discloses a LTPS-TFT structure including a cap layer, a polysilicon film and a gate. The cap layer is disposed over the substrate with a gap between the two.

[0007] US 2005/0037551 A1 discloses a high-quality isotropic polycrystalline silicon (poly-Si) and a method for fabricating high quality isotropic poly-Si film. The method includes forming a film of amorphous silicon (a-Si) and using a MISPC process to form poly-Si film in a first area of the a-Si film.

[0008] US 2015/0194310 A1 discloses a method for making low temperature poly-silicon thin film.

SUMMARY

[0009] The present disclosure provides in some embodiments a method for manufacturing a thin film transistor, so that the TFT may have a good electrical performance. The technical solutions are as follows.

[0010] In a first aspect, the present disclosure provides in some embodiments a method for manufacturing a thin film transistor, including: providing a substrate; forming a gate electrode, a gate insulating layer, an amorphous silicon material active layer and a cap layer on the substrate successively, wherein the cap layer is provided with a pattern on a side of the cap layer away from the amorphous silicon material active layer, and the pattern is composed of at least one groove along a length direction of the active layer and at least one groove along a width direction of the active layer; subjecting the amorphous silicon material active layer to laser annealing treatment to transform the amorphous silicon material active layer into a low temperature polycrystalline silicon material active layer; removing the cap layer.

[0011] In an implementation of embodiments of the present disclosure, the step of, forming the gate electrode, the gate insulating layer, the amorphous silicon material active layer and the cap layer on the substrate successively includes: forming the gate electrode on the substrate; forming the gate insulating layer on the gate electrode; forming an amorphous silicon material thin film and an oxide thin film on the gate insulating layer successively; and subjecting the amorphous silicon material thin film and the oxide thin film to patterning process treatment to obtain the amorphous silicon material active layer and the cap layer.

[0012] In another implementation of embodiments of the present disclosure, the step of, subjecting the amorphous silicon material thin film and the oxide thin film to patterning process treatment comprises: subjecting the amorphous silicon material thin film and the oxide thin film to patterning process treatment using a halftone mask.

[0013] In another implementation of embodiments of the present disclosure, the oxide thin film is a silicon dioxide thin film or an indium tin oxide thin film.

[0014] In another implementation of embodiments of the present disclosure, a projection of the pattern on the substrate in a perpendicular direction is located at a region corresponding to the gate electrode.

[0015] In another implementation of embodiments of the present disclosure, a center of the projection of the pattern on the substrate in the perpendicular direction coincides with a center of a projection of the gate electrode on the substrate in the perpendicular direction.

[0016] In another implementation of embodiments of the present disclosure, a thickness of a portion of the cap layer provided with the groove is in the range of 2~5 nanometers, and a thickness of a portion of the cap layer not provided with the groove is in the range of 10~30 nanometers.

[0017] In another implementation of embodiments of the present disclosure, the pattern includes at least two grooves along the length direction of the active layer and at least two grooves along the width direction of the active layer, and intersections of the grooves are distributed in

a matrix form.

[0018] In another implementation of embodiments of the present disclosure, a distance between any two grooves which are adjacent and parallel to each other is in the range of 2~5 micrometers.

[0019] In another implementation of embodiments of the present disclosure, the method further includes: before forming the gate electrode, forming a buffer layer on the substrate.

[0020] In a second aspect, not claimed, the present disclosure provides a thin film transistor, including a substrate, and a gate electrode, a gate insulating layer and a low temperature polycrystalline silicon material active layer covering the substrate successively. The low temperature polycrystalline silicon material active layer includes a first region and a second region. The first region is arranged right above the gate electrode in a direction perpendicular to the substrate. The first region is divided into a plurality of first sub-regions by crystal boundaries in the first region. The second region is divided into a plurality of second sub-regions by crystal boundaries in the second region. Each first sub-region is of an area larger than the second sub-region, and the plurality of first sub-regions are distributed in a matrix form.

[0021] In a third aspect, the present disclosure provides an array substrate, including the above thin film transistor.

[0022] In a fourth aspect, the present disclosure provides a display device, including the above array substrate.

[0023] The technical solutions provided by embodiments of the present disclosure have following beneficial effects.

[0024] In embodiments of the present disclosure, during the amorphous silicon is crystallized, since a thickness of the cap layer at a patterned portion is thinner, the amorphous silicon material thin film at a corresponding region enters into a fully melted state earlier when under a laser beam irradiation. As a result, a nucleation center is located below a center of a rectangular region formed by the pattern, and the growth direction of the grain is away from the nucleation center, whereupon a crystal boundary is formed below the groove in the pattern. By adopting the above manufacturing method, a number, a direction, a location of crystal boundaries in the polysilicon located below the cap layer in the LTPS thin film may be controlled, thus reducing the number of crystal boundaries in the TFT channel and the leakage current of the TFT, and improving the whole electrical performance of the TFT.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] In order to illustrate technical solutions in embodiments of the present disclosure, drawings to be used in the description of the embodiments will be described briefly hereinafter. Apparently, the drawings described hereinafter are only some embodiments of the present disclosure, and other drawings may be obtained by those skilled in the art according to those drawings without creative work.

Fig. 1 is a flow chart showing a method for manufacturing a thin film transistor according to some embodiments of the present disclosure;

Fig. 2 is a flow chart showing the method for manufacturing a thin film transistor according to some embodiments of the present disclosure;

Fig. 2a is a schematic diagram showing a thin film transistor during a manufacturing process according to some embodiments of the present disclosure;

Fig. 2b is a schematic diagram showing a thin film transistor during a manufacturing process according to some embodiments of the present disclosure;

Fig. 2c is a schematic diagram showing a thin film transistor during a manufacturing process according to some embodiments of the present disclosure;

Fig. 2d is a schematic diagram showing a thin film transistor during a manufacturing process according to some embodiments of the present disclosure;

Fig. 2e is a schematic diagram showing a thin film transistor during a manufacturing process according to some embodiments of the present disclosure;

Fig. 2f is a schematic diagram showing a thin film transistor during a manufacturing process according to some embodiments of the present disclosure;

Fig. 2g is a diagram showing a growth direction of a grain according to some embodiments of the present disclosure;

Fig. 2h is a schematic diagram showing a thin film transistor during a manufacturing process according to some embodiments of the present disclosure;

Fig. 3 is a schematic diagram showing a thin film transistor according to some embodiments of the present disclosure.

DETAILED DESCRIPTION

[0026] The invention is defined by the appended claims. In order to make the objects, the technical solutions and the advantages of the present disclosure more apparent, the present disclosure will be described hereinafter in a detailed manner in conjunction with the drawings. In drawings, a thickness and a shape of each layer of thin film do not reflect a true scale of the array substrate, which merely aims at exemplarily illustrating contents of the present disclosure.

[0027] Unless otherwise defined, any technical or scientific terms used herein shall have the common meaning understood by a person of ordinary skills. Such words as "first" and "second" used in the specification and claims are merely used to differentiate different components rather than to represent any order, number or importance. Similarly, such words as "one" or "one of' are merely used to represent the existence of at least one member, rather than to limit the number thereof. Such

words as "connect" or "connected to" may include electrical connection, direct or indirect, rather than being limited to physical or mechanical connection. Such words as "on/above", "under/below", "left" and "right" are merely used to represent relative position relationship, and when an absolute position of an object is changed, the relative position relationship will be changed too.

[0028] Fig. 1 is a flow chart showing a method for manufacturing a thin film transistor according to some embodiments of the present disclosure. Referring to Fig. 1, the method includes the following steps.

Step 101: Providing a substrate.

Step 102: Forming a gate electrode, a gate insulating layer, an amorphous silicon material active layer and a cap layer on the substrate successively. The cap layer is provided with a pattern on a side of the cap layer away from the amorphous silicon material active layer, and the pattern is composed of at least one groove along a length direction of the active layer and at least one groove along a width direction of the active layer.

Step 103: Subjecting the amorphous silicon material active layer to laser annealing treatment to transform the amorphous silicon material active layer into a low temperature polycrystalline silicon material active layer.

Step 104: Removing the cap layer.

[0029] In embodiments of the present disclosure, when the amorphous silicon is crystallized, since a thickness of the cap layer at a patterned portion is thinner, the amorphous silicon material thin film at a corresponding region enters into a fully melted state earlier when under a laser beam irradiation. As a result, a nucleation center is located below a center of a rectangular region formed by the pattern, and the growth direction of the grain is away from the nucleation center, whereupon a crystal boundary is formed below the groove in the pattern. By adopting the above manufacturing method, a number, a direction, a location of crystal boundaries in the polysilicon located below the cap layer in the LTPS thin film may be controlled, thus reducing the number of crystal boundaries in the TFT channel and the leakage current of the TFT, and improving the whole electrical performance of the TFT.

[0030] Fig. 2 is a flow chart showing method for manufacturing a thin film transistor according to some embodiments of the present disclosure. Referring to Fig. 2, the method includes the following steps.

[0031] Step 201: Providing a substrate.

[0032] The substrate may be a glass substrate, a transparent plastic substrate etc.

[0033] Step 202: Forming a gate electrode on the substrate.

[0034] As shown in Fig. 2a, a substrate 301 provided in the step 201 may be covered with a buffer layer 301A in advance, and then a gate electrode 302 is formed. Therefore, the method may further include: prior to forming the gate electrode, forming a buffer layer on the substrate. Specifically, the buffer layer may be a silicon nitride (e.g., SiN) layer or a silicon oxide (e.g., SiO_2) layer.

[0035] The gate electrode may be a metal gate electrode, and then the forming process of the gate electrode may include: forming a metal layer on the buffer layer first, and then subjecting the metal layer to patterning process treatment to form the above gate electrode.

[0036] Step 203: Forming a gate insulating layer on the gate electrode.

[0037] As shown in Fig. 2b, forming a gate insulating layer 303 on the gate electrode 302.

[0038] Specifically, the gate insulating layer may be a silicon nitride (e.g., SiN) layer or a silicon oxide (e.g., SiO_2) layer.

[0039] Step 204: Forming an amorphous silicon material thin film and an oxide thin film on the gate insulating layer successively.

[0040] As shown in Fig. 2c, covering the gate insulating layer 303 with an amorphous silicon material thin film 3041 and an oxide thin film 3051.

[0041] The oxide thin film is a silicon dioxide thin film, an indium tin oxide (ITO) thin film or other types of oxide thin film.

[0042] Step 205: Subjecting the amorphous silicon material thin film and the oxide thin film to patterning process treatment to obtain the amorphous silicon material active layer and the cap layer. The cap layer is provided with a pattern on a side of the cap layer away from the amorphous silicon material active layer, and the pattern is composed of at least one groove along a length direction of the active layer and at least one groove along a width direction of the active layer.

[0043] As shown in Fig. 2d, after subjecting the amorphous silicon material thin film 3041 and the oxide thin film 3051 to patterning process treatment, an amorphous silicon material active layer 3042 and a cap layer 305 are formed.

[0044] Fig. 2e is a stereo schematic diagram showing the structure shown in Fig. 2d. As shown in Fig. 2e, the pattern is composed of at least one groove a along a length direction of the channel of the active layer (i.e., the AA' direction in the figure) and at least one groove b along a width direction of the channel of the active layer (i.e., the BB' direction in the figure).

[0045] In embodiments of the present disclosure, the length direction of the active layer is identical to that of the channel of the TFT when it is turned on, and the width direction of the active layer is identical to that of the channel of the TFT when it is turned on. The length direction of the channel is a direction of current flow in the channel region, and the width direction of the channel is a direction perpendicular to the length direction of the channel in the channel region.

[0046] The patterning process in the step 205 may be realized using a mask photo-etching process, therefore the patterning of the cap layer and that of the active layer may be accomplished at one step without any additional

etching process. Specifically, the step 205 may include: subjecting the amorphous silicon material thin film and the oxide thin film to patterning process treatment using a halftone mask to obtain an amorphous silicon material active layer and a cap layer.

[0047] Specifically, a projection of the pattern on the substrate in a perpendicular direction is located at a region corresponding to the gate electrode. That is, the pattern is corresponding to the channel region. In embodiments of the present disclosure, the whole electrical performance of the TFT may be improved by improving the crystal boundaries in the polysilicon in the channel region of the active layer, and reducing the number of defect states.

[0048] Furthermore, a center of the projection of the pattern on the substrate in the perpendicular direction coincides with a center of a projection of the gate electrode on the substrate in the perpendicular direction.

[0049] A thickness of a portion of the cap layer provided with the groove is in the range of 2~5 nanometers, and a thickness of a portion of the cap layer not provided with the groove is in the range of 10~30 nanometers. In embodiments of the present disclosure, by setting of thickness of the above cap layer, a temperature difference between the patterned portion and non-patterned portion is assured, which plays a role of induction and guidance for a formation of crystal boundaries.

[0050] Specifically, the pattern includes at least two grooves along the length direction of the active layer and at least two grooves along the width direction of the active layer, and intersections of the grooves are distributed in a matrix form.

[0051] Furthermore, in embodiments of the present disclosure, the number of grooves in the pattern may be determined according to a width and a length of the channel of the TFT, the larger the width and length of the channel of the TFT, the greater number of grooves in the pattern. A distance between any two grooves which are adjacent and parallel to each other is in the range of 2-5 micrometers.

[0052] The distance between grooves in the pattern is configured to define the number and arrangement of the crystal boundaries in the active layer, and an arrangement of the above distance may ensure that the number of crystal boundaries in the channel of the active layer is small.

[0053] Step 206: Subjecting the amorphous silicon material active layer to a laser annealing treatment to transform the amorphous silicon material active layer into a low temperature polycrystalline silicon material active layer.

[0054] As shown in Fig. 2f, the amorphous silicon material active layer 3042 is melted under the laser beam irradiation and crystallized to form a low temperature polycrystalline silicon material active layer 304.

[0055] When the laser beam irradiates the cap layer, the amorphous silicon material is melted and crystallized in a length direction of the channel (the AA' direction in Fig. 2e). At an edge close to the gate electrode, since the amorphous silicon material is relatively thicker at the slope, the amorphous silicon material is partially melted down during ELA irritation. At this moment, a temperature gradient is formed in the AA' direction, therefore the grain growth is progressed towards to the melted portion from the partially melted portion to form a crystal boundary perpendicular to the channel.

[0056] Meanwhile, in the width direction of the channel (the BB' direction in Fig. 2e), a cooling speed at the edge of the channel is faster than that at the middle part, therefore there is also a temperature gradient along the BB' direction. As a result, the grain growth is progressed towards to the middle from the edge to form a crystal boundary parallel to the channel direction.

[0057] In another aspect, the crystal boundary above the gate electrode is formed under an impact of the pattern of the cap layer. Since the groove portion in the pattern is relatively thin, the amorphous silicon material at the corresponding region enters into a fully melted state first during the crystallization, whereupon the nucleation center is located a center of the region which is divided by the groove, and the growth direction of the grain is away from the nucleation center, therefore a crystal boundary is formed below the groove.

[0058] The growth direction of the grain is as shown in Fig. 2g, at the edge close to the gate electrode 302, the growth of grain 304A is progressed towards to the melted portion from the partially melted portion to form a crystal boundary 304B perpendicular to the channel. Moreover, the nucleation center is located in a center of the region divided by the groove b, and the growth direction of the grain 304A is away from the nucleation center, whereupon a crystal boundary 304B is formed below the groove b.

[0059] Step 207: Removing the cap layer.

[0060] As shown in Fig. 2h, removing the cap layer 305 on the low temperature polycrystalline silicon material active layer 304.

[0061] Specifically, in embodiments of the present disclosure, the cap layer may be removed using an etching process.

[0062] Furthermore, the method further includes: forming a source electrode and a drain electrode at two opposite sides of the active layer.

[0063] In embodiments of the present disclosure, when the amorphous silicon is crystallized, since a thickness of the cap layer at a patterned portion is thinner, the amorphous silicon material thin film at the corresponding region enters into a fully melted state earlier when under a laser beam irradiation. As a result, a nucleation center is located below a center of a rectangular region formed by the pattern, and the growth direction of the grain is away from the nucleation center, whereupon a crystal boundary is formed below the groove in the pattern. By adopting the above manufacturing method, the number, the direction, the location of crystal boundaries in the polysilicon located below the cap layer in the LTPS thin film may be

controlled, thus reducing the number of crystal boundaries in the TFT channel and the leakage current of the TFT, and improving the whole electrical performance of the TFT.

[0064] The present disclosure provides a thin film transistor, including a substrate, a gate electrode, a gate insulating layer and a low temperature polycrystalline silicon material active layer covering the substrate successively. The low temperature polycrystalline silicon material active layer includes a first region and a second region. The first region is arranged right above the gate electrode in a direction perpendicular to the substrate, the first region is divided into a plurality of first sub-regions by crystal boundaries in the first region. The second region is divided into a plurality of second sub-regions by crystal boundaries in the second region. Each first sub-region is of an area larger than the second sub-region, and the plurality of first sub-regions are distributed in a matrix form.

[0065] In embodiments of the present disclosure, the number of first sub-regions in the first region in the active layer is greater than that of the second sub-regions in the second region. Since both the first sub-regions and the second sub-region are divided by crystal boundaries, it can be seen that, crystal boundaries in the first region are less than that in the second region. Here, the first region is arranged right above the gate electrode, that is, the channel region. Therefore the number of crystal boundaries in the channel region in the above structure of the thin film transistor is small, which reduces the leakage current of the TFT, and improves the whole electrical performance of the TFT.

[0066] Fig. 3 is a schematic diagram showing a thin film transistor according to embodiments of the present disclosure. As shown in Fig. 3, the thin film transistor is formed using the method shown in Fig. 2, specifically including: a substrate 301, a buffer layer 301A arranged on substrate 301, a gate electrode 302 arranged on the buffer layer 301A, a gate insulating layer 303 arranged on the gate electrode 302, an active layer 304 arranged on the gate insulating layer 303, a source electrode 305 and a drain electrode 306 which are arranged at two opposite sides of the active layer 304 respectively and in contact with the active layer 304. The active layer 304 is a low temperature polycrystalline silicon material active layer. The low temperature polycrystalline silicon material active layer 304 includes a first region and a second region. The first region is arranged right above the gate electrode 302, the first region is divided into a plurality of first sub-regions by crystal boundaries in the first region. The second region is divided into a plurality of second sub-regions by crystal boundaries in the second region. Each first sub-region is of an area larger than the second sub-region, and the plurality of first sub-regions are distributed in a matrix form.

[0067] In embodiments of the present disclosure, the number of first sub-regions in the first region of the active layer is greater than that of the second sub-regions in the second region. Since both the first sub-regions and the second sub-region are divided by crystal boundaries, it can be seen that, crystal boundaries in the first region are less than that in the second region. Here, the first region is arranged right above the gate electrode, that is, the channel region. Therefore the number of crystal boundaries in the channel region in the above structure of the thin film transistor is small, which reduces the leakage current of the TFT, and improves the whole electrical performance of the TFT.

[0068] The present disclosure further provides an array substrate. The array substrate includes the thin film transistor according to any one of the above embodiments. Specifically, the array substrate further includes a gate line arranged on the substrate, a data line and a pixel electrode layer and the like. Here, a drain electrode of the thin film transistor is connected to the pixel electrode layer, a gate electrode of the thin film transistor is connected to the gate line, and a source electrode of the thin film transistor is connected to the data line.

[0069] The pixel electrode layer may be a transparent conductive metal oxide layer, such as an ITO layer, an indium zinc oxide (IZO) layer.

[0070] On the basis of the similar inventive concept, the present disclosure further provides a display device, including the array substrate according to above embodiments.

[0071] When specifically implementing, the display device according to embodiments of the present disclosure may be any product or component with display function, such as a mobile phone, a tablet PC, a TV set, a monitor, a notebook computer, a digital photo frame, a navigator.

[0072] The above are merely the preferred embodiments of the present disclosure and shall not be used to limit the scope of the present disclosure.

Claims

1. A method for manufacturing a thin film transistor, comprising:

providing a substrate (301);

forming a gate electrode (302), a gate insulating layer (303), an amorphous silicon material active layer (3042) and a cap layer (305) on the substrate (301) successively, wherein the cap layer (305) is provided with a pattern on a side of the cap layer (305) away from the amorphous silicon material active layer (3042), and the pattern is composed of at least one groove (a) along a length direction of the active layer and at least one groove (b) along a width direction of the active layer;

subjecting the amorphous silicon material active layer (3042) to laser annealing treatment to transform the amorphous silicon material active layer (3042) into a low temperature polycrystal-

line silicon material active layer; and
removing the cap layer (305).

2. The method according to claim 1, wherein the step of, forming the gate electrode (302), the gate insulating layer (303), the amorphous silicon material active layer (3042) and the cap layer (305) on the substrate (301) successively comprises:

forming the gate electrode (302) on the substrate (301);
forming the gate insulating layer (303) on the gate electrode (302);
forming an amorphous silicon material thin film (3041) and an oxide thin film (3051) on the gate insulating layer (303) successively; and
subjecting the amorphous silicon material thin film (3041) and the oxide thin film (3051) to patterning process treatment to obtain the amorphous silicon material active layer (3042) and the cap layer (305).

3. The method according to claim 2, wherein the step of, subjecting the amorphous silicon material thin film (3041) and the oxide thin film (3051) to patterning process treatment comprises:
subjecting the amorphous silicon material thin film (3041) and the oxide thin film (3051) to patterning process treatment using a halftone mask.

4. The method according to claim 2, wherein the oxide thin film (3051) is a silicon dioxide thin film or an indium tin oxide thin film.

5. The method according to any one of claims 1 to 4, wherein a projection of the pattern on the substrate (301) in a perpendicular direction is located at a region corresponding to the gate electrode (302).

6. The method according to claim 5, wherein a center of the projection of the pattern on the substrate (301) in the perpendicular direction coincides with a center of a projection of the gate electrode (302) on the substrate (301) in the perpendicular direction.

7. The method according to any one of claims 1 to 4, wherein a thickness of a portion of the cap layer (305) provided with the groove is in the range of 2-5 nanometers, and a thickness of a portion of the cap layer (305) not provided with the groove is in the range of 10-30 nanometers.

8. The method according to any one of claims 1 to 4, wherein the pattern comprises at least two grooves (a) along the length direction of the active layer and at least two grooves (b)along the width direction of the active layer, and intersections of the grooves are distributed in a matrix form.

9. The method according to claim 8, wherein a distance between any two grooves which are adjacent and parallel to each other is in the range of 2-5 micrometers.

10. The method according to any one of claims 1 to 4, further comprising:
before forming the gate electrode (302), forming a buffer layer (301A) on the substrate (301).

Patentansprüche

1. Verfahren zur Herstellung eines Dünnfilmtransistors, umfassend:

Bereitstellen eines Substrats (301);
Bilden einer Gate-Elektrode (302), einer Gate-Isolierschicht (303), einer Aktivschicht aus amorphen Siliciummaterial (3042) und einer Deckschicht (305) auf dem Substrat (301) nacheinander, wobei die Deckschicht (305) mit einer Struktur auf einer Seite der Deckschicht (305) ausgestattet ist, die von der Aktivschicht aus amorphem Siliciummaterial (3042) weg weist, und wobei die Struktur aus mindestens einer Rille (a) entlang einer Längsrichtung der Aktivschicht und mindestens einer Rille (b) entlang einer Breitenrichtung der Aktivschicht zusammengesetzt ist;
Unterziehen der Aktivschicht aus amorphem Siliciummaterial (3042) Lasertemperbehandlung, um die Aktivschicht aus amorphem Siliciummaterial (3042) in eine Aktivschicht aus bei tiefer Temperatur polykristallinem Siliciummaterial umzuwandeln; und
Entfernen der Deckschicht (305).

2. Verfahren nach Anspruch 1, wobei der Schritt des Bildens der Gate-Elektrode (302), der Gate-Isolierschicht (303), der Aktivschicht aus amorphem Siliciummaterial (3042) und der Deckschicht (305) auf dem Substrat (301) nacheinander umfasst:

Bilden der Gate-Elektrode (302) auf dem Substrat (301);
Bilden der Gate-Isolierschicht (303) auf der Gate-Elektrode (302);
Bilden eines Dünnfilms aus amorphem Siliciummaterial (3041) und eines Oxiddünnfilms (3051) auf der Gate-Isolierschicht (303) nacheinander; und
Unterziehen des Dünnfilms aus amorphem Siliciummaterial (3041) und des Oxiddünnfilm (3051) Strukturierungsprozessbehandlung, um die Aktivschicht aus amorphem Siliciummaterial (3042) und die Deckschicht (305) zu erhalten.

3. Verfahren nach Anspruch 2, wobei der Schritt des Unterziehens des Dünnfilms aus amorphem Siliciummaterial (3041) und des Oxiddünnfilms (3051) der Strukturierungsprozessbehandlung umfasst:
Unterziehen des Dünnfilms aus amorphem Siliciummaterial (3041) und des Oxiddünnfilms (3051) Strukturierungsprozessbehandlung unter Verwendung einer Halbtonmaske.

4. Verfahren nach Anspruch 2, wobei der Oxiddünnfilm (3051) ein Dünnfilm aus Siliciumdioxid oder ein Dünnfilm aus Indiumzinnoxid ist.

5. Verfahren nach einem der Ansprüche 1 bis 4, wobei eine Projektion der Struktur auf das Substrat (301) in einer senkrechten Richtung sich in einer Region befindet, die der Gate-Elektrode (302) entspricht.

6. Verfahren nach Anspruch 5, wobei ein Zentrum der Projektion der Struktur auf das Substrat (301) in der senkrechten Richtung mit einem Zentrum einer Projektion der Gate-Elektrode (302) auf das Substrat (301) in der senkrechten Richtung zusammenfällt.

7. Verfahren nach einem der Ansprüche 1 bis 4, wobei eine Dicke eines Anteils der Deckschicht (305), der mit der Rille ausgestattet ist, im Bereich von 2 bis 5 Nanometern liegt, und eine Dicke eines Anteils der Deckschicht (305), der nicht mit der Rille ausgestattet ist, im Bereich von 10 bis 30 Nanometern liegt.

8. Verfahren nach einem der Ansprüche 1 bis 4, wobei die Struktur mindestens zwei Rillen (a) entlang der Längsrichtung der Aktivschicht und mindestens zwei Rillen (b) entlang der Breitenrichtung der Aktivschicht umfasst, und wobei Schnittpunkte der Rillen in einer Matrixform verteilt sind.

9. Verfahren nach Anspruch 8, wobei ein Abstand zwischen beliebigen zwei Rillen, die benachbart und parallel zueinander sind, im Bereich von 2 bis 5 Mikrometern liegt.

10. Verfahren nach einem der Ansprüche 1 bis 4, das des Weiteren umfasst:
Bilden einer Pufferschicht (301A) auf dem Substrat (301) vor dem Bilden der Gate-Elektrode (302).

Revendications

1. Procédé de fabrication d'un transistor en couches minces, comprenant :

l'obtention d'un substrat (301) ;
la formation successive d'une électrode de grille (302), d'une couche d'isolation de grille (303), d'une couche active de matériau de silicium amorphe (3042) et d'une couche d'encapsulation (305) sur le substrat (301), la couche d'encapsulation (305) étant pourvue d'un motif sur un côté de la couche d'encapsulation (305) à l'écart de la couche active de matériau de silicium amorphe (3042), et le motif étant composé d'au moins une rainure (a) le long d'une direction de la longueur de la couche active et d'au moins une rainure (b) le long d'une direction de la largeur de la couche active ;
la soumission de la couche active de matériau de silicium amorphe (3042) à un traitement de recuit laser pour transformer la couche active de matériau de silicium amorphe (3042) en une couche active de matériau de silicium polycristallin à basse température ; et
le retrait de la couche d'encapsulation (305).

2. Procédé selon la revendication 1, dans lequel l'étape de formation de l'électrode de grille (302), de la couche d'isolation de grille (303), de la couche active de matériau de silicium amorphe (3042) et de la couche d'encapsulation (305) sur le substrat (301) comprend successivement :

la formation de l'électrode de grille (302) sur le substrat (301) ;
la formation de la couche d'isolation de grille (303) sur l'électrode de grille (302) ;
la formation successive d'un film mince de matériau de silicium amorphe (3041) et d'un film mince d'oxyde (3051) sur la couche d'isolation de grille (303) ; et
la soumission du film mince de matériau de silicium amorphe (3041) et du film mince d'oxyde (3051) à un traitement de gravure pour obtenir la couche active de matériau de silicium amorphe (3042) et la couche d'encapsulation (305).

3. Procédé selon la revendication 2, dans lequel l'étape de soumission du film mince de matériau de silicium amorphe (3041) et du film mince d'oxyde (3051) à un traitement de gravure comprend :
la soumission du film mince de matériau de silicium amorphe (3041) et du film mince d'oxyde (3051) à un traitement de gravure au moyen d'un masque tramé.

4. Procédé selon la revendication 2, dans lequel le film mince d'oxyde (3051) est un film mince de dioxyde de silicium ou un film mince d'oxyde d'indium et d'étain.

5. Procédé selon l'une quelconque des revendications 1 à 4, dans lequel une projection du motif sur le substrat (301) dans une direction perpendiculaire est située dans une région correspondant à l'électrode de grille (302).

6. Procédé selon la revendication 5, dans lequel un centre de la projection du motif sur le substrat (301) dans la direction perpendiculaire coïncide avec un centre d'une projection de l'électrode de grille (302) sur le substrat (301) dans la direction perpendiculaire.

7. Procédé selon l'une quelconque des revendications 1 à 4, dans lequel une épaisseur d'une partie de la couche d'encapsulation (305) pourvue de la rainure se situe dans la gamme de 2~5 nanomètres, et une épaisseur d'une partie de la couche d'encapsulation (305) dépourvue de la rainure se situe dans la gamme de 10~30 nanomètres.

8. Procédé selon l'une quelconque des revendications 1 à 4, dans lequel le motif comprend au moins deux rainures (a) le long de la direction de la longueur de la couche active et au moins deux rainures (b) le long de la direction de la largeur de la couche active, et des intersections des rainures sont réparties sous une forme matricielle.

9. Procédé selon la revendication 8, dans lequel une distance entre deux rainures quelconques qui sont adjacentes et parallèles l'une à l'autre se situe dans la gamme de 2~5 micromètres.

10. Procédé selon l'une quelconque des revendications 1 à 4, comprenant en outre :
avant la formation de l'électrode de grille (302), la formation d'une couche tampon (301A) sur le substrat (301) .

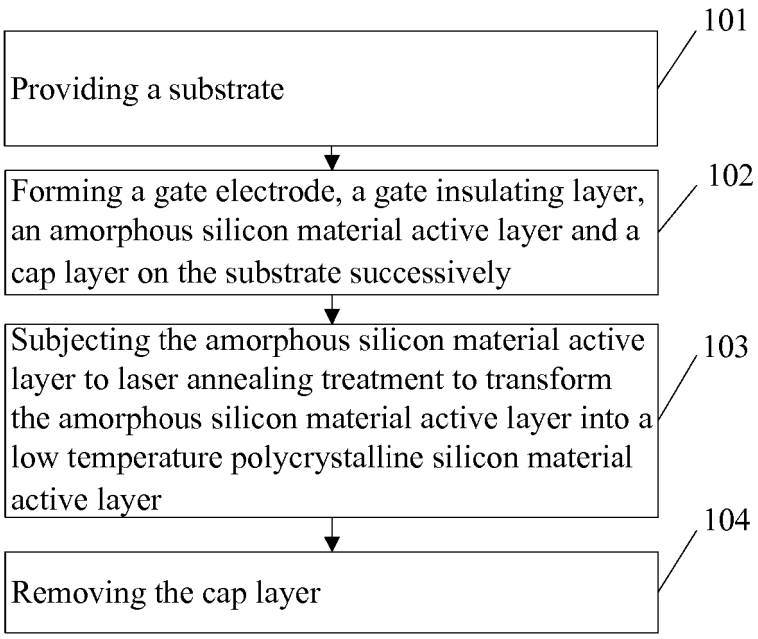
Providing a substrate
101
Forming a gate electrode, a gate insulating layer, an amorphous silicon material active layer and a cap layer on the substrate successively
102
Subjecting the amorphous silicon material active layer to laser annealing treatment to transform the amorphous silicon material active layer into a low temperature polycrystalline silicon material active layer
103
Removing the cap layer
104

Fig. 1

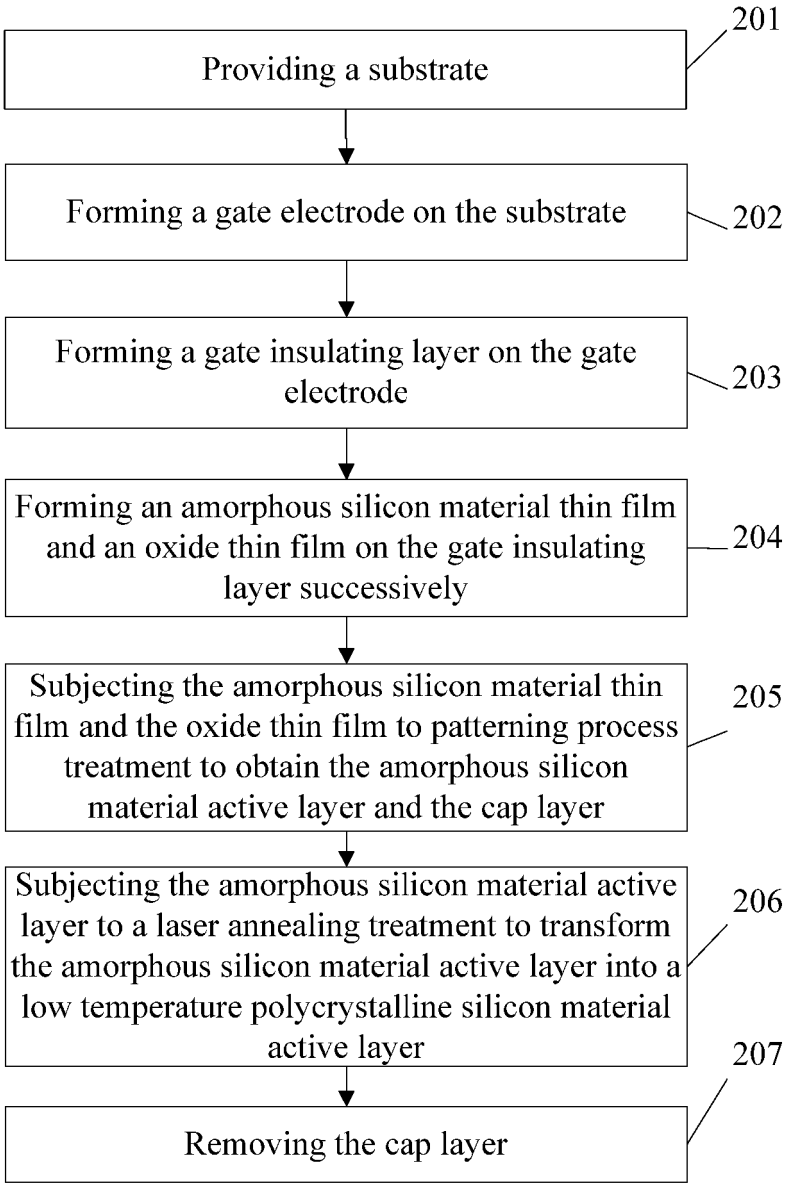
Providing a substrate
201
Forming a gate electrode on the substrate
202
Forming a gate insulating layer on the gate electrode
203
Forming an amorphous silicon material thin film and an oxide thin film on the gate insulating layer successively
204
Subjecting the amorphous silicon material thin film and the oxide thin film to patterning process treatment to obtain the amorphous silicon material active layer and the cap layer
205
Subjecting the amorphous silicon material active layer to a laser annealing treatment to transform the amorphous silicon material active layer into a low temperature polycrystalline silicon material active layer
206
Removing the cap layer
207

Fig. 2

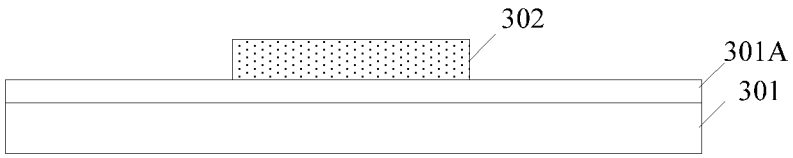
302
301A
301

Fig. 2a

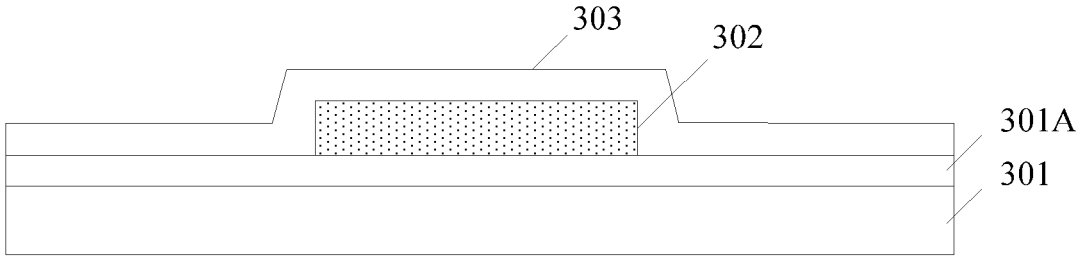

Fig. 2b

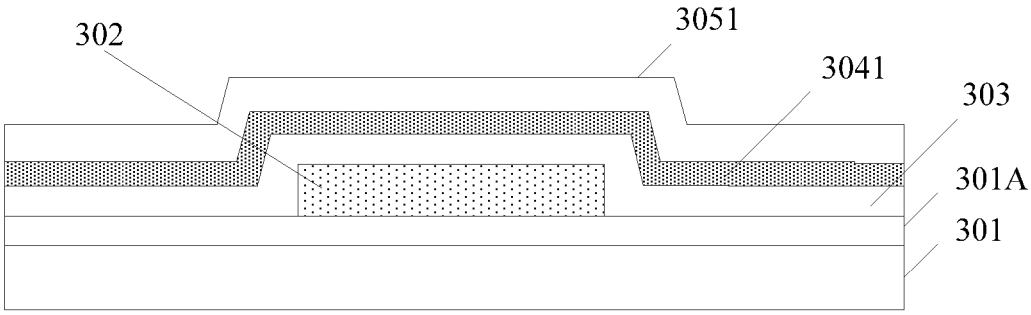

Fig. 2c

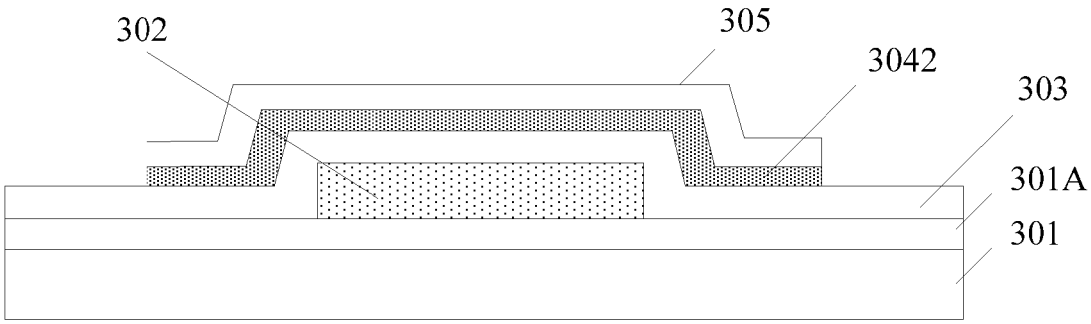

Fig. 2d

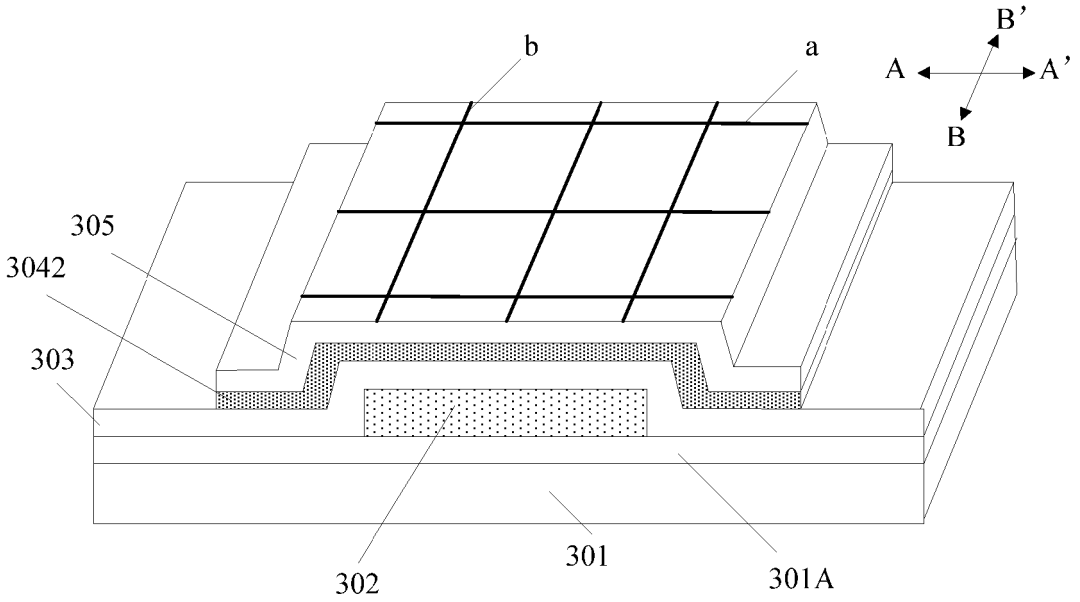

Fig. 2e

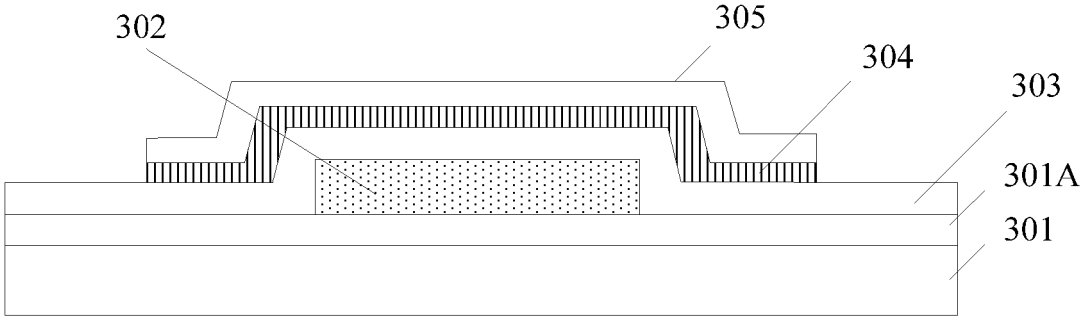

Fig. 2f

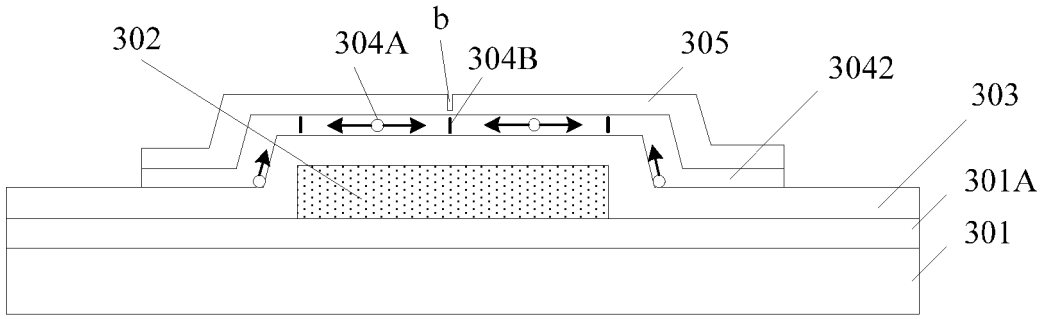

Fig. 2g

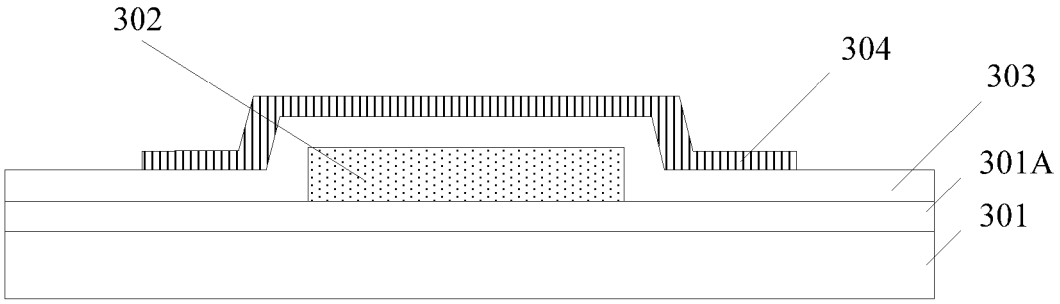

Fig. 2h

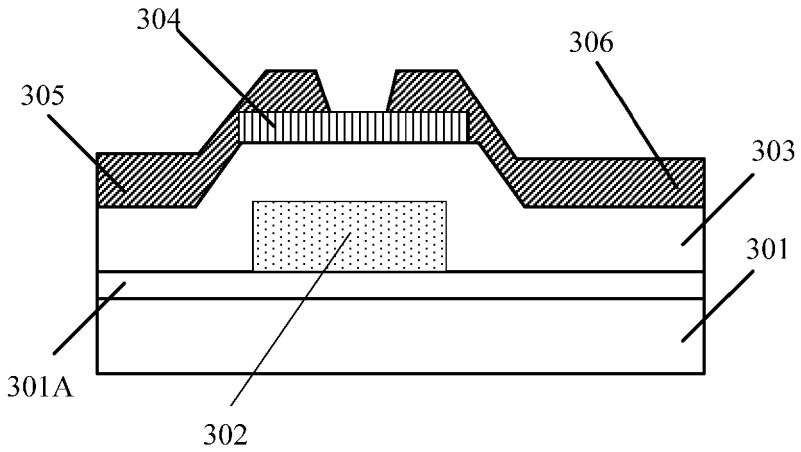

Fig. 3

REFERENCES CITED IN THE DESCRIPTION

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