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(54) **Micro domain partitioning in an active liquid crystal display**

Mikrodomänenaufteilung in einer aktiven Flüssigkristallanzeige

Partition aux micro-domaines pour un dispositif actif d'affichage à cristaux liquides

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**Description****BACKGROUND OF THE INVENTION****(a) Field of the Invention**

[0001] The present invention relates to a thin film transistor array panel for a liquid crystal display.

**(b) Description of the Related Art**

[0002] Generally, a liquid crystal display has two panels with electrodes, and a liquid crystal layer interposed between the two panels. Voltages are applied to the electrodes so that the liquid crystal molecules in the liquid crystal layer are re-oriented to thereby control the light transmission.

[0003] The liquid crystal display involves a critical shortcoming of a narrow viewing angle. In order to solve such a problem, various techniques of widening the viewing angle have been developed. For instance, it has been proposed that the liquid crystal molecules may be aligned perpendicular to the top and the bottom panels while forming a predetermined pattern of openings or protrusions at the pixel electrode and the common electrode.

[0004] In the case of formation of the opening pattern, the liquid crystal molecules are controlled in orientation by way of a fringe field due to the openings formed at the pixel electrodes and the common electrode.

[0005] In the case of formation of the protrusion pattern, protrusions are formed at the pixel electrode and the common electrode, and the liquid crystal molecules are controlled in orientation by way of an electric field deformed due to the protrusions.

[0006] Furthermore, it is possible that an opening pattern is formed at the pixel electrode of the bottom panel while forming a protrusion pattern at the common electrode of the top panel. The liquid crystal molecules are controlled in orientation by way of the fringe field due to the openings and the protrusions while forming a plurality of domains.

[0007] In such a multi-domain liquid crystal display, the viewing angle per the contrast ratio of 1:10 or the viewing angle defined as the limit angle of the inter-gray scale brightness inversion excellently reaches 80° or more in all directions. However, the lateral gamma curve is deviated from the front gamma curve so that visibility at the left and right sides is deteriorated, even compared to the twisted nematic (TN) mode liquid crystal display. For instance, in the patterned vertically aligned (PVA) mode where opening portions are formed for the domain partitioning, the screen becomes totally brighter as it comes to the lateral side, and the color becomes to be white. In a serious case, the difference in distance between the bright gray scales is removed while conglomerating the picture images. However, the trend is that visibility becomes important more and more as the monitor has been used for the multi-media purpose.

[0008] US 5608556 A discloses a liquid crystal display which provides a wide viewing angle and high display quality by controlling the orientation of liquid crystal directors.

[0009] KR 2000 0009518 A discloses a multi-domain vertical alignment liquid crystal display device having a very wide viewing angle.

**SUMMARY OF THE INVENTION**

[0010] It is an object of the present invention to provide a multi-domain liquid crystal display which involves excellent lateral side visibility.

[0011] This and other objects are achieved by a liquid crystal display as defined in claim 1. Preferred embodiments are claimed in the dependent claims.

[0012] In the following description, although numerous features are designated as optionally, e.g. by being introduced by "may" or "can", it is nevertheless acknowledged that all features comprised in each of the independent claims are not to be read as optional.

[0013] The electric field within the left and right domains is established to be weaker than that within the upper and lower domains.

[0014] According to one aspect, the liquid crystal display has a plurality of pixel regions. Each pixel region has a plurality of micro domains. The micro domains include a first directional domain and a second directional domain having different average inclination directions of liquid crystal molecules upon application of an electric field. The electric field within the first directional domain is weaker than the electric field within the second directional domain by a predetermined value.

[0015] When viewed from a front side, the liquid crystal molecules in the first directional domain are inclined left and right while the liquid crystal molecules in the second directional domain are inclined up and down. The predetermined value of difference in the electric field between the first directional domain and the second directional domain ranges from  $0.02/d$  (V/μm) to  $0.5/d$  (V/μm) where  $d$  is a cell gap.

**[0016]** According to another aspect, the liquid crystal display has a first insulating substrate, and a first signal line formed on the first insulating substrate in a first direction. A second signal line is formed on the first insulating substrate in a second direction while intersecting the first signal line in an insulating manner. A first thin film transistor is connected to the first and the second signal lines. A second thin film transistor is connected to the first and the second signal lines connected to the first thin film transistor. A first pixel electrode is connected to the first thin film transistor. A second pixel electrode is connected to the second thin film transistor. A second insulating substrate faces the first insulating substrate. A common electrode is formed on the second insulating substrate. A liquid crystal layer is interposed between the first and the second substrates. A domain partitioning member is formed on at least one of the first and the second insulating substrates while partitioning the first and the second pixel electrodes into a plurality of micro domains. The domain partitioning member partitions the first and the second pixel electrodes into first directional domains and second directional domains, and the first and the second pixel electrodes are capacitor-connected to each other.

**[0017]** The first and the second thin film transistors at the pixel of the  $n$ th pixel row on the  $m$ -th pixel column are connected to the  $m$ -th data line, and the first and the second thin film transistors at the pixel of the  $(n+1)$ -th pixel row on the  $m$ -th pixel column are connected to the  $(m+1)$ -th data line where  $n$  and  $m$  are integers. The second pixel electrode occupies the pixel region by 30-70%. The liquid crystal molecules in the liquid crystal layer are vertically aligned with respect to the first and the second insulating substrates in absence of an electric field.

**[0018]** A storage capacitor line is formed on (the first insulating substrate while being placed between the first pixel electrode and the second pixel electrode to thereby form a storage capacitor. When the liquid crystal capacitance formed between the second pixel electrode and the common electrode is indicated by  $C_{1cb}$ , the storage capacitance formed between the second pixel electrode and the storage capacitor line is indicated by  $C_{stb}$ , and the connection capacitance formed between the first and the second pixel electrodes is indicated by  $C_{pp}$ , the value of  $T$  defined by the equation  $T = (C_{1cb} + C_{stb} - C_{pp}) / (C_{1cb} + C_{stb} + C_{pp})$  is in the range of 0.65-0.95.

**[0019]** According to still another aspect, the liquid crystal display has a first insulating substrate, and a first signal line formed at the first insulating substrate in a first direction. A second signal line is formed at the first insulating substrate in a second direction while crossing the first signal line in an insulating manner. A thin film transistor is connected to the first and the second signal lines. A pixel electrode is connected to the thin film transistor while bearing a plurality of slits. A second insulating substrate faces the first insulating substrate. A common electrode is formed at the second insulating substrate. A liquid crystal layer is interposed between the first and the second substrates. A domain partitioning member is formed on at least one of the first and the second insulating substrates while partitioning the pixel electrode into a plurality of micro domains. The domain partitioning member partitions the pixel electrode into first directional domains and second directional domains, and the first directional domains are placed at the area of the slits.

**[0020]** The slit width of the pixel electrode is established to be 2-5  $\mu\text{m}$ , and the distance between the neighboring two slits is established to be 2-10  $\mu\text{m}$ .

**[0021]** According to still another aspect of the present invention, the liquid crystal display has a first insulating substrate, and a first signal line formed at the first insulating substrate in a first direction. A second signal line is formed at the first insulating substrate in a second direction while crossing the first signal line in an insulating manner. A thin film transistor is connected to the first and the second signal lines. A pixel electrode is connected to the thin film transistor. A second insulating substrate faces the first insulating substrate. A common electrode is formed at the second insulating substrate. A dielectric layer is formed on at least one of the pixel electrode and the common electrode. A liquid crystal layer is interposed between the first and the second substrates. A domain partitioning member is formed on at least one of the first and the second insulating substrates while partitioning the pixel electrode into a plurality of micro domains. The domain partitioning member partitions the pixel electrode into first directional domains and second directional domains, and the dielectric layer is placed at the area of the first directional domains.

**[0022]** The thickness of the dielectric layer is established to be 500Å-1.5  $\mu\text{m}$ . Opening portions are formed at the pixel electrode and the common electrode as the domain partitioning member.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

**[0023]** A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or the similar components, wherein:

Fig. 1 is a plan view of a liquid crystal display according to a first comparative example;

Fig. 2 is a cross sectional view of the liquid crystal display taken along the II-II' line of Fig. 1;

Fig. 3 is a graph illustrating the gamma curves at the front side of the test cell and the 60° side thereof;

Fig. 4 illustrates the VT curves when a single-domain vertically aligned liquid crystal cell is viewed from eight directions;

Fig. 5 illustrates the VT curve at the front side of a single-domain VA cell where the rubbing is vertically made in an

anti-parallel manner, the average VT curve at the left and right 60° sides thereof, the average VT curve at the top and bottom 60° sides thereof, and the curve of making the top and bottom average curve move by 0.3V;

Fig. 6 is a plan view of a liquid crystal display according to a second comparative example;

Fig. 7 is a cross sectional view of the liquid crystal display taken along the VII-VII' line of Fig. 6;

Fig. 8 is a cross sectional view of a liquid crystal display according to a third comparative example;

Fig. 9 is a plan view of a liquid crystal display according to a preferred embodiment of the present invention;

Figs. 10 and 11 are cross sectional views of the liquid crystal display taken along the XI-XI' line and the XII-XII' line of Fig. 9;

Fig. 12 is an equation circuit diagram of a liquid crystal display with the thin film transistor array panel shown in Fig. 9;

Fig. 13 is a plan view of a liquid crystal display according to a further comparative example; and

Fig. 14 is an equation circuit diagram of a liquid crystal display with the thin film transistor array panel shown in Fig. 13.

## **DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS**

**[0024]** Preferred embodiments of this invention will be explained with reference to the accompanying drawings.

**[0025]** Fig. 1 is a plan view of a liquid crystal display according to a first comparative example, and Fig. 2 is a cross sectional view of the liquid crystal display taken along the II-II' line of Fig. 1.

**[0026]** As shown in Figs. 1 and 2, gate lines 20 are formed on a transparent insulating substrate 10 such as glass while extending in the horizontal direction. Storage capacitor lines 30 extend parallel to the gate lines 20. Gate electrodes 21 protrude from the gate lines 20. First to fourth storage capacitor electrodes 31 to 34 and storage capacitor electrode connectors 35 and 36 are branched from the storage capacitor lines 30. The first storage capacitor electrode 31 is directly connected to the storage capacitor line 30 while extending in the vertical direction. The second and the third storage capacitor electrodes 32 and 33 are connected to the first storage capacitor electrode 31 while extending in the horizontal direction. The fourth storage capacitor electrode 34 is connected to the second and the third storage capacitor electrodes 32 and 33 while extending in the vertical direction. The storage capacitor electrode connectors 35 and 36 connect the fourth storage capacitor electrode 34 to the first storage capacitor electrode 31 at the pixel adjacent thereto. A gate insulating layer 40 is formed on the gate line assembly 20 and 21 and the storage capacitor line assembly 30 to 36, and a semiconductor layer 50 made of amorphous silicon is formed on the gate insulating layer 40 over the gate electrodes 21. An ohmic contact layer 61 and 62 made of amorphous silicon doped with n-type high concentration impurities such as phosphorous P is formed on the semiconductor layer 50. Source and drain electrodes 71 and 72 are formed on the ohmic contact layer 61 and 62, respectively. Data lines 70 are formed on the gate insulating layer 40 while extending in the vertical direction. The source electrodes 71 are connected to the data lines 70. A protective layer 80 is formed on the data lines assembly 70, 71 and 72 with contact holes 81 exposing the drain electrodes 72. A pixel electrode 90 is formed on the protective layer 80 at each pixel area while being connected to the drain electrode 72 through the contact hole 81. The pixel electrode 90 is formed with a transparent conductive material such as indium tin oxide (ITO) and indium zinc oxide (IZO). Each pixel area is defined by the two gate lines 20 and the two data lines 70 while being partitioned into upper and lower half parts.

**[0027]** The pixel electrode 90 is separated into first to third electrode portions 91 to 93, which are connected to each other by way of first to third connectors 94 to 96. The first electrode portion 91 is located at the lower half part of the pixel area, and has a rectangular shape where the four edges thereof are cut off. The first electrode portion 91 is directly connected to the drain electrode 72 through the contact hole 81. The second and the third electrode portions 92 and 93 are located at the upper half part of the pixel area, and have a rectangular shape with the four chamfered corners. The second electrode portion 92 is connected to the first electrode portion 91 by way of the first and the second connectors 94 and 96, and the third electrode portion 93 is connected to the second electrode portion 92 by way of the third connector 95.

**[0028]** A plurality of slits 99 are formed at the first electrode portion 91. The electric field generated between the first electrode portion 91 and the common electrode 400 due to the slits 99 is weaker than that generated between the common electrode 400 and the second electrode portion 92 or the third electrode portion 93.

**[0029]** Meanwhile, the second storage capacitor electrode 32 is placed between the first electrode portion 91 and the second electrode portion 92, and the third storage capacitor electrode 33 is placed between the second electrode portion 92 and the third electrode portion 93. The first storage capacitor electrode 31 and the fourth storage capacitor electrode 34 are placed between the pixel electrode 90 and the data line 70. The side of the first electrode portion 91 extending parallel to the data line is longer than the side thereof extending parallel to the gate line. The side of the second and the third electrode portions extending parallel to the data line is shorter than the side thereof extending parallel to the gate line. The second and the third electrode portions 92 and 93 overlap the first and the fourth storage capacitor electrodes 31 and 34, but the first electrode portion 91 does not overlap the first and the fourth storage capacitor electrodes 31 and 34. The storage capacitor line 30 is placed between the gate line 20 and the third electrode portion 93. The electric potential to be applied to the common electrode for the color filter panel is usually applied to the storage capacitor line

30, the storage capacitor electrodes 31 to 34, and the storage capacitor electrode connectors 35 and 36.

**[0030]** As described above, when the storage capacitor line or the storage capacitor electrode to be applied with the common electric potential is placed between the data line and the pixel electrode, or between the gate line and the pixel electrode, the affection of the data line electric potential and the gate line electric potential to the electric field of the pixel region is intercepted by the storage capacitor line and the storage capacitor electrode, thereby forming stable domains,

**[0031]** A color filter panel for the liquid crystal display will be now explained in detail.

**[0032]** A black matrix 200 is formed on a transparent glass substrate 100 with a double-layered structure while defining the pixel areas. The double-layered structure for the black matrix 200 is formed with chrome/chrome oxide. A color filter 300 is formed at each pixel area, and a common electrode 400 is formed on the entire surface of the substrate 100 having the color filters 400 with a transparent conductive material. The common electrode 400 is provided with an opening pattern at each pixel area. The opening pattern includes first to third opening portions 510, 520 and 530. The first opening portion 510 bisects the lower half part of the pixel region in the vertical direction, and the second and the third opening portions 520 and 530 trisect the upper half part of the pixel region in the horizontal direction. Both ends of the respective opening portions 510, 520 and 530 are gradually enlarged while forming the shape of an isosceles triangle. The opening portions 510, 520 and 530 are separated from each other.

**[0033]** Alternatively, the black matrix may be formed with an organic material, and the color filters may be formed at the thin film transistor array panel.

**[0034]** The thin film transistor array panel and the color filter panel are aligned, and assembled with each other. A liquid crystal material 900 is injected between the two panels such that the directors of the liquid crystal molecules are aligned perpendicular to the panels. Two polarizing plates 11 and 101 are attached to the outer surfaces of the substrates 10 and 100 such that the polarizing axes thereof extend perpendicular to each other.

**[0035]** The electrode portions 91, 92 and 93 of the pixel electrode 90 at the thin film transistor array panel, and the first to third opening portions 510, 520 and 530 of the common electrode 400 at the color filter panel overlap each other to thereby partition the pixel region into a plurality of micro-domains. The micro-domains partitioned by the first electrode portion 91 and the first opening portion 510 are referred to as the upper and lower domains (extending in the horizontal direction), and the micro-domains partitioned by the second and third electrode portions 92 and 93 and the second and third opening portions 520 and 530 are referred to as the left and right domains (extending in the vertical direction). This distinction is made depending upon the inclination directions of the liquid crystal molecules upon the application of the electric field. The respective electrode portions 91 to 93 includes two long sides and two short sides. The long side of the each electrode portion extends parallel to the data line 70 or the gate line 20, and makes an angle of  $45^\circ$  with respect to the polarizing axis of the polarizing plate (as shown in Fig. 3). In case the long side of the respective electrode portions 91 to 93 of the pixel electrode 90 is positioned close to the data line 70 or the gate line 20, the storage capacitor line 30 or the storage capacitor electrodes 31 to 34 are arranged between the data line 70 and the long side of the relevant electrode portion or the gate line 20 and the long side of the relevant electrode portion. Meanwhile, it is preferable that the storage capacitor line assembly 30 to 34 is not positioned close to the short side of the electrode portions 91 to 93 of the pixel electrode 90. In case the storage capacitor line assembly is positioned close to the latter, it is completely covered by the pixel electrode 90, or positioned distant from the pixel electrode 90 by  $3\ \mu\text{m}$  or more. The reason is that the electric potential of the data line 70 or the gate line 20 operates in the direction of hindering the domain formation at the area where the data line 70 or the gate line 20 is positioned close to the long side of the pixel electrode portions 91 to 93. On the contrary, the electric potential of the data line 70 or the gate line 20 operates in the direction of exerting the domain formation at the area where the data line 70 or the gate line 20 is positioned close to the short side of the pixel electrode portions 91 to 93.

**[0036]** Meanwhile, the electric field formed within the left and right domains due to the slit 99 at the first pixel electrode portions 91 is weaker than that formed within the upper and lower domains by a predetermined degree. With this structure, the visibility of the liquid crystal display at the left and the right sides can be improved. When the cell gap of the liquid crystal display is indicated by  $d$  (m), the electric field formed within the left and right domains preferably bears a value of from  $0.02/d$  (V/ $\mu\text{m}$ ) to  $0.5/d$  (V/ $\mu\text{m}$ ), which is weaker than the electric field formed within the upper and lower domains. That is, the voltage difference between the common electrode and the pixel electrode is established such that the voltage at the left and right domains is weaker than that at the upper and lower domains by 0.1-1V. For this purpose, the width of the slit 99 is preferably established to be 2-5 microns, and the distance between the neighboring two slits 99 is established to be 2-10 microns.

**[0037]** Fig. 3 is a graph illustrating the gamma curves at the front side of a test cell and at the  $60^\circ$ -lateral side thereof.

**[0038]** As shown in Fig. 3, the gamma curve at the front side of the test cell turns out to be higher than the gamma curve at the  $60^\circ$ -lateral side thereof. Particularly, as the width between the front side gamma curve and the lateral side gamma curve is significantly great, the brightness difference of two times to ten times is made depending upon whether the same gray scale is viewed from the front side or from the lateral side. As the gray scales of the red, green and blue pixels are varied separately, the deformation degree in the gamma curve at the lateral side is differentiated at the red, green and blue pixels. Therefore, when viewed from the lateral side, the pixels seem to bear an entirely different color

compared to the case where the same pixels are viewed from the front side. For instance, as shown in Fig. 5, assuming that the red, green and blue pixels express 56 gray scales, 48 gray scales and 24 gray scales, when viewed from the front side, the ratios of the red, green and blue colors are established to be as follows: R:G:B = 73:50:10 = 55%:37%:8%. By contrast, when viewed from the 60°-lateral side, the ratios of the red, green and blue colors are established to be as follows: R:G:B = 75:66:41 = 41 %:36%:23%. That is, in the latter case, the content of the blue color becomes heightened by three times or more so that the relevant pixel seems to bear an entirely different color.

[0039] In case the gamma curve is deformed as shown in Fig. 5, the low-proportioned color at the front side becomes increased in the proportion at the lateral side. By contrast, the high-proportioned color at the front side becomes decreased in the proportion at the lateral side. In this way, the ratios of the red, green and blue colors become to be approximated to each other. Consequently, the colors seemed to be different when viewed from the front side become reduced in the difference in the color sensation when viewed from the lateral side. The colors become totally light while being approximated to the white color, and this is called the "white-shift." As a result, the color representation property becomes deteriorated, and the picture Image appears to be cloudy. The most important cause of the white-shift is that the deformation of the gamma curve is serious at the lower gray scales. Even if the gamma deformation is made at the higher gray scales, it is extremely small. However, when the gamma deformation is made at the lower gray scales of 32 or less, the brightness difference is made by two times to ten times, and this makes the white-shift appear to a large scale.

[0040] Fig. 4 illustrates the VT curves when the single-domain vertically aligned liquid crystal cell is viewed from eight directions.

[0041] As shown in Fig. 4, the movement of the VT curve in the left direction with the lower gray scales is significantly made at the top side or at the bottom side. At the left and right sides, the curve at the lower gray scales is elevated with the same outline as that at the front side. At the left bottom side and the right bottom side, the gray scale inversion is made early, and the VT curve again moves in the right direction while being elevated. That is, the phenomenon where the gamma curve is deformed upward with the lower gray scales becomes serious when the direction of viewing the liquid crystal cell and the inclination direction of the liquid crystal molecules under the application of the electric field are the same (when viewed from the head or tail of the liquid crystal molecules), but becomes negligible when those directions are perpendicular to each other. Therefore, the gamma curve deformation at the left and right domains is important in viciously influencing the viewing angle based on the visibility at the left and right sides, and the gamma curve deformation at the upper and lower domains is important in viciously influencing the viewing angle based on the visibility at the top and bottom sides. From the viewpoint of the user, the viewing angle at the left and right sides is more important than the viewing angle at the top and bottom sides. In order to compensate the gamma curve deformation at the left and right domains that viciously influences the left and right side visibility, the strength in the electric field within the left and right domains becomes weaker compared to that within the upper and lower domains. This will be now explained in detail.

[0042] Fig. 5 illustrates the VT curve at the front side of a single-domain VA cell where the rubbing is vertically made in an anti-parallel manner (the liquid crystal molecules being inclined up and downward), the average VT curve at the left and right 60° sides thereof, the average VT curve at the top and bottom 60° sides thereof, and the curve of making the top and bottom average curve move by 0.3V.

[0043] As shown in Fig. 5, the VT curve at the left and right sides nearly agrees to the VT curve at the front side with the lower gray scales, but the VT curve at the top and bottom sides begins to elevate at lower voltages compared to the VT curve at the front side. That is, the threshold voltage  $V_{th}$  turns out to be lowered at the top and bottom sides, compared to that at the front side. However, when the VT curve at the top and bottom side moves by about 0.3V, it nearly agrees to the VT curve at the front side with the lower gray scales. The fact that the VT curve at the top and bottom sides agrees to the VT curve at the front side means that the visibility at the top and bottom sides is the same as the visibility at the front side. After all, in order that the visibility at the left and right sides be enhanced to the same degree as the visibility at the front side, the left and right side VT curves at the left and right domains may move by a predetermined voltage. The same effect as with the movement of the left and right side VT curve can be obtained in case the electric field within the left and right domains is established to be weaker than the electric field within the upper and lower domains.

[0044] Fig. 6 is a plan view of a thin film transistor array panel for a liquid crystal display according to a second comparative example, and Fig. 7 is a cross sectional view of the thin film transistor array panel taken along the VII-VII' line of Fig. 6.

[0045] As shown in Figs. 6 and 7, other components and structures of the liquid crystal display are the same as those related to the first comparative example except that a dielectric layer 600 is formed on the first pixel electrode portion 91 without forming any slit there.

[0046] The effect of forming the dielectric layer 600 on the first pixel electrode portion 91 is the same as that of forming slits at the first pixel electrode portion 91. That is, the electric field within the left and right domains is established to be weaker than that within the upper and lower domains. The thickness of the dielectric layer 600 is established to be in the range of 500Å-1.5 microns.

[0047] Fig. 8 is a sectional view of a liquid crystal display according to a third comparative example.

[0048] As shown in Fig. 8, other components and structures of the liquid crystal display are the same as those related

to the first comparative example except that a dielectric layer 600 is formed on the common electrode 400 while corresponding to the first pixel electrode portion 91 without forming any slit at the first pixel electrode portion 91.

**[0049]** The effect of forming the dielectric layer 600 on the common electrode 400 is the same as that of forming the slits at the first pixel electrode portion 91. That is, the electric field within the left and right domains is established to be weaker than that within the upper and lower domains.

**[0050]** Fig. 9 is a plan view of a thin film transistor array panel for a liquid crystal display according to a preferred embodiment of the present invention, Figs. 10 and 11 are cross sectional views of the thin film transistor array panel taken along the XI-XI' line and the XII-XII' line of Fig. 9, and Fig. 12 is an equivalent circuit diagram of a liquid crystal display with the thin film transistor array panel shown in Fig. 9.

**[0051]** A gate line assembly and storage capacitor lines 30 are formed at a transparent insulating substrate 10 such as glass.

**[0052]** The gate line assembly includes gate lines 20 extending in the horizontal direction, and gate electrodes 21 protruded from the gate lines 20 up and downward.

**[0053]** The storage capacitor line 30 extends parallel to the gate line 20. The storage capacitor line 30 may bear a branch line.

**[0054]** The gate line assembly and the storage capacitor line 30 are covered by a gate insulating layer 40, and a semiconductor layer 50 made of amorphous silicon is formed on the gate insulating layer 40. The semiconductor layer 50 overlaps the gate electrode 21 to thereby form a channel portion for the thin film transistor. An ohmic contact layer 61, 62 and 63 made of amorphous silicon doped with n-type high concentration impurities such as phosphorous are formed on the semiconductor layer 50.

**[0055]** A data line assembly and connection electrodes 74 are formed on the ohmic contact layer 61, 62 and 63 and the gate insulating layer 40. The data line assembly includes data lines 70 extending along the semiconductor layer 50, source electrodes 71 connected to the data lines 70, and first and second drain electrodes 72 and 73. The source electrodes 71 protrude from the data lines 70 while being placed over the gate electrodes 21. The first and the second drain electrodes 72 and 73 are placed at both sides of the source electrode 71, respectively. The first and the second drain electrodes 72 and 73 are extended into first and second pixel regions around the gate line 20. The connection electrode 74 partially overlaps the storage capacitor line 30 while electro-magnetically interconnecting the first and the second pixel electrodes 91 and 92 separated around the storage capacitor line 30. The ohmic contact layers 61, 62 and 63 are located only at the area where the semiconductor layer 50 overlaps the data line assembly.

**[0056]** A protective layer 80 is formed on the data line assembly. The protective layer 80 has first and second contact holes 81 and 82 exposing the one-sided ends of the first and second drain electrodes 72 and 73, and a third contact hole 83 exposing the one-sided end of the connection electrode 74.

**[0057]** First and second pixel electrodes 91 and 92 are formed on the protective layer 80 such that they are connected to the first and the second drain electrodes 72 and 73 through the first and the second contact holes 81 and 82. The second pixel electrode 92 is connected to the connection electrode 74 through the third contact hole 83. The first pixel electrode 91 is overlapped with the connection electrode 74 while making an electromagnetic combination (capacitor-combination). After all, the first and the second pixel electrodes 91 and 92 are capacitor-combined with each other by way of the connection electrode 74. The pixel electrodes 91 and 92 are made of a transparent conductive material such as indium tin oxide (ITO) and indium zinc oxide (IZO). Meanwhile, the first pixel electrode 91 is provided with a plurality of horizontal opening portions 95 extending in the horizontal direction. Vertical opening portions may be formed at the second pixel electrode 92. The occupation ratio of the first pixel electrode within one pixel region is preferably established to be 30-70%.

**[0058]** The electric potential of the common electrode counter to the pixel electrode 90 is usually applied to the storage capacitor line 30.

**[0059]** In the meantime, the color filter panel is provided with a black matrix, color filters and a common electrode. First to third opening portions 510, 520 and 530 are formed at the common electrode. The first opening portion 510 extends in the vertical direction such that it bisects the second pixel electrode 92 into left and right domains. The second and the third opening portions 520 and 530 trisect the first pixel electrode 91 up and downward. Consequently, the first pixel electrode 91 is vertically partitioned into four domains by way of the second and the third opening portions 520 and 530, and the horizontal opening portion 95.

**[0060]** The connection electrode 74 is formed on the same plane as the data line assembly. Alternatively, the connection electrode 74 may be formed on the same plane as the gate line assembly. In the latter case, the storage capacitor line 30 should not overlap the connection electrode 74.

**[0061]** The thin film transistor array panel is spaced apart from the color filter panel with a predetermined distance, and a liquid crystal material is injected between the two panels. The directors of the liquid crystal molecules are aligned vertical to the panels. A compensation film such as a biaxial film is attached to the color filter panel. Two polarizing plates are attached to the outer surfaces of the thin film transistor array panel and the color filter panel, respectively.

**[0062]** As described above, two thin film transistors and two pixel electrodes are formed at one pixel region, and the

two pixel electrodes at the pixel neighbors are capacitor-connected to each other by way of a connection electrode. In this structure, excellent visibility can be obtained even when viewed from the left and right sides. This is because the voltage of the second pixel electrode 92 for the left and right domains is kept to be lower than the voltage of the first pixel electrode 91 so that the electric field within the left and right domains is weaker than that within the upper and lower domains.

**[0063]** The reason that the voltage of the second pixel electrode 92 for the left and right domains is kept to be lower than that of the first pixel electrode 91 for the upper and lower domains will be now explained with reference to Fig. 12.

**[0064]** In the drawing, Clca indicates the liquid crystal capacitance formed between the a pixel electrode and the common electrode, Csta indicates the storage capacitance formed between the storage capacitor line and the a pixel electrode, Clcb indicates the liquid crystal capacitance formed between the b pixel electrode and the common electrode, Cstb indicates the storage capacitance formed between the storage capacitor line and the b pixel electrode, and Cpp indicates the connection capacitance between the a pixel electrode and the b pixel electrode.

**[0065]** As shown in Fig. 12, the first and the second thin film transistors are connected to the same gate and data lines, and the first and the second pixel electrodes are connected to the first and the second thin film transistors, respectively. The first and the second pixel electrodes make capacitor-connection (Cpp) with respect to each other while interposing the storage capacitor line 30 between them.

**[0066]** In relation to one data line 70, when the nth gate line 20 becomes to be on, two thin film transistor (TFT) channels become to be on so that voltage is applied to the first and the second pixel electrodes P(n)-a, and P(n)-b. As the P(n)-b is capacitor-connected to the P(n+1)-a, it is affected by the on-state of the latter. In this connection, the voltages of P(n)-a and P(n)-b may be given by way of mathematical formulas 1 and 2.

$$V[P(n)-a] = Vd(n) \quad (1)$$

$$V[P(n)-b] = Vd(n) + [Vd(n+1) - V'd(n+1)] Cpp / (Clcb + Cstb + Cpp) \quad (2)$$

**[0067]** In the mathematical formulas 1 and 2, Vd(n) indicates the voltage applied to the data line to drive the P(n) pixel, and Vd(n+1) indicates the voltage applied to the data line to drive the P(n+1) pixel. Furthermore, the V'd(n+1) indicates the voltage applied to the P(n+1) pixel at the previous frame.

**[0068]** As expressed in the mathematical formulas 1 and 2, the voltage applied to the P(n)-b pixel differs from the voltage applied to the P(n)-a pixel. Particularly, in case dot inversion driving or line inversion driving is made while the next pixel row expressing the same gray scale as with the previous pixel row (practically, most of the pixels being similar to this case), Vd(n) = Vd(n+1), and Vd(n) = -V'd(n) (assuming that the common electrode voltage is the earth voltage). Therefore, the mathematical formula 2 can be expressed by the following mathematical formula 3:

$$V[P(n)-b] = Vd(n) - 2Vd(n) Cpp / (Clcb + Cstb + Cpp) = [(Clcb + Cstb - Cpp) / (Clcb + Cstb + Cpp)] Vd(n) = TVd(n), \quad (3).$$

where  $T = (C1cb + Cstb - Cpp) / (C1cb + Cstb + Cpp)$ .

**[0069]** It can be known from the mathematical formula 3 that the voltage applied to the P(n)-b pixel is lower than that applied to the P(n)-a pixel. The value of T is preferably established to be 0.65-0.95.

**[0070]** Fig. 14 is a plan view of a thin film transistor array panel for a liquid crystal display according to a further comparative example, and Fig. 13 is an equivalent circuit diagram of a liquid crystal display with the thin film transistor array panel shown in Fig. 14.

**[0071]** In this comparative example, the thin film transistors and the pixel electrodes at one pixel column are alternately connected to two data lines. That is, the thin film transistor and the two pixel electrodes a and b at the P(n) pixel are connected to the m-th data line, and the thin film transistor and the two pixel electrodes a and b at the P(n+1) pixel are connected to the (m+1)-th data line. The detailed structure of each thin film transistor and pixel electrode is the same as that related to the third comparative example except that the opening portions 95, 510, 520 and 530 are varied in their positions. That is, in the preferred embodiment, the horizontal opening portion 95 is formed at the second pixel electrode 92. The first opening portion 510 is formed at the first pixel electrode 91 while bisecting the latter left and right, and the second and the third opening portions 520 and 530 are formed at the second pixel electrode 92 while trisecting the latter up and down. Consequently, the first pixel electrode 91 forms left and right domains, and the second pixel electrode 92 forms upper and lower domains.

**[0072]** In the above structure, when the dot inversion driving is made, the electric field within the left and right domains



is kept to be weaker than that within the upper and lower domains. That is, the electric potential of the first pixel electrode 91 is constantly kept to be lower than that of the second pixel electrode 92 so that the visibility at the left and right sides can be improved.

[0073] With the structure shown in Fig. 14, when the dot inversion driving is made, the voltage of the same polarity is applied to the pixel electrodes at the same pixel column so that the same effect as with the column inversion driving is resulted. Therefore, in case the next pixel row indicates the same gray scale as with the previous pixel row (practically, most of the pixels being similar to this case),  $V_d(n) = V_d(n+1)$ , and  $V_d(n) = -V'_d(n)$ . Therefore, the mathematical formula 2 can be expressed by the following mathematical formula 4:

$$V[P(n)-b] = \frac{V_d(n) + 2V_d(n)C_{pp}}{(C1cb + Cstb + Cpp)} = \frac{[(C1cb + Cstb + 3C_{pp}) / (C1cb + Cstb + Cpp)]V_d(n)}{1} = TV_d(n), \quad (4)$$

where  $T = (C1cb + Cstb + 3C_{pp}) / (C1cb + Cstb + Cpp)$ .

[0074] In the mathematical formula 4, the voltage of the b pixel is higher than that of the a pixel. Therefore, the electric field within the left and right domains is constantly kept to be weaker than that within the upper and lower domains.

[0075] As described above, the electric field at the left and right domains is constantly kept to be weaker than the upper and lower domains so that the visibility at the left and right sides can be enhanced.

[0076] While the present invention has been described in detail with reference to the preferred embodiment, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the scope of the present invention as set forth in the appended claims.

## Claims

### 1. A liquid crystal display, comprising:

- a first transparent insulating substrate (10);
- gate lines (20) formed on the first transparent insulating substrate (10) in a first direction;
- data lines (70) formed on the first transparent insulating substrate (10) in a second direction;
- the first direction being perpendicular to the second direction;
- a plurality of pixel regions arranged in rows in the first direction and in columns in the second direction;
- storage capacitor lines (30) in the first direction, one of each of the storage capacitor lines (30) extending parallel to and in between two adjacent gate lines (20); wherein each pixel region includes a first pixel electrode (91) and a second pixel electrode (92) on the first transparent insulating substrate (10), and wherein one of each of the storage capacitor lines (30) is positioned between the pixel region of the n-th pixel region row in the m-th pixel region column and the pixel region of the (n+1)-th pixel region row in the m-th pixel region column such that the storage capacitor line (30) is capacitively coupled with the second pixel electrode (92) of the pixel region in the n-th pixel region row and the m-th pixel region column and the first pixel electrode (91) of the pixel region in the (n+1)-th pixel region row and the m-th pixel region column by the partial overlap of said storage capacitor line (30) with said second pixel electrode (92) and said first pixel electrode (91) of said two adjacent pixel regions;
- a first thin film transistor and a second thin film transistor in each pixel region;
- a second transparent insulating substrate (100) facing the first transparent insulating substrate (10);
- a liquid crystal layer (900) interposed between the first and second transparent insulating substrates (10, 100);
- and
- wherein the liquid crystal layer on each of the first pixel electrodes and the second pixel electrodes is partitioned by a first directional domain partitioning member and a second directional domain partitioning member, respectively, for partitioning the liquid crystal layer (900) into a plurality of domains, wherein the first and second directional domain partitioning members are formed at a common electrode (400), the common electrode (400) being formed on the second transparent insulating substrate (100);
- wherein the directional partitioning members are comprising first to third opening portions (510, 520, 530) which are formed for partitioning the liquid crystal layer (900) into a plurality of domains;
- wherein the first opening portion (510) extends in the second direction bisecting the liquid crystal layer at the second pixel electrode (92) into domains, and
- wherein the second and the third opening portions (520, 530) extend in the first direction and trisect the liquid crystal layer at the first pixel electrode (91) into domains, and the first pixel electrode (91) is provided with a

fourth opening portion (95) extending in the first direction such that the liquid crystal layer at the first pixel electrode (91) is consequently partitioned in the second direction into four domains by the second and third opening portions (520, 530) and the fourth opening portion (95);

wherein in each pixel region the first pixel electrode (91) and the second pixel electrode (92) are electrically connected to one of the gate lines (20), being called the common gate line, formed on the first transparent insulating substrate (10) and one of the data lines (70), being called the common data line, formed on a gate insulating layer (40) via the first thin film transistor and the second thin film transistor, respectively;

wherein the second pixel electrode (92) of the n-th pixel region row and the first pixel electrode (91) of the (n+1)-th pixel region row in the same m-th pixel region column, are capacitor-connected to each other by one corresponding connection electrode (74), the connection electrode (74) being electrically connected to the second pixel electrode (92) of the n-th pixel region row and being overlapped with the first pixel electrode (91) of the (n+1)-th pixel region row such that the connection electrode (74) and the first pixel electrode (91) of the (n+1)-th pixel region row form a connection capacitance (C<sub>pp</sub>), such that, during the driving of the liquid crystal display, in each pixel region the voltage of the second pixel electrode (92) is lower than that of the first pixel electrode (91) with reference to the common electrode (400), where n and m are integers.

2. The liquid crystal display of claim 1, wherein in each pixel region the first pixel electrode (91) and the second pixel electrode (92), being connected to the corresponding common gate line (20) via the first thin film transistor and the second thin film transistor, are positioned at opposite sides of the common gate line (20).

3. The liquid crystal display of claim 1, wherein the liquid crystal molecules in the liquid crystal layer are aligned in the vertical direction with respect to the first transparent insulating substrate (10) in the absence of an electric field.

4. The liquid crystal display of claim 1, wherein each connection electrode (74) contacts the corresponding second pixel electrode (92) through a corresponding contact hole (83) formed in a protective layer (80).

5. The liquid crystal display of claim 4, wherein each connection electrode (74) overlaps the corresponding first pixel electrode (91), the protective layer (80) being between them.

6. The liquid crystal display of claim 5, wherein each connection electrode overlaps (74) one portion of the corresponding storage capacitor line (30) where the corresponding first pixel electrode (91) also is overlapping.

7. The liquid crystal display of claim 5, wherein the occupation ratio of the first pixel electrode (91) within one pixel region is 30-70%.

## Patentansprüche

1. Eine Flüssigkristallanzeige, die Folgendes umfasst:

ein erstes transparentes Isoliersubstrat (10); Gateleitungen (20), die in einer ersten Richtung auf dem ersten transparenten Isoliersubstrat (10) geformt sind; Datenleitungen (70), die in einer zweiten Richtung auf dem ersten transparenten Isoliersubstrat (10) geformt sind; wobei die erste Richtung senkrecht zur zweiten Richtung ist;

eine Vielzahl von Pixelbereichen, die in der ersten Richtung in Zeilen und in der zweiten Richtung in Spalten angeordnet sind;

Speicherkondensatorleitungen (30) in der ersten Richtung, wobei eine jeder Speicherkondensatorleitungen (30) sich parallel zu und zwischen zwei benachbarten Gateleitungen (20) erstreckt, wobei jeder Pixelbereich eine erste Pixelelektrode (91) und eine zweite Pixelelektrode (92) auf dem ersten transparenten Isoliersubstrat (10) einschließt, und wobei jede der Speicherkondensatorleitungen (30) zwischen dem Pixelbereich der n-th Pixelbereichszeile in der m-th Pixelbereichsspalte und dem Pixelbereich der (n+1)-th Pixelbereichszeile in der m-th Pixelbereichsspalte positioniert ist, so dass die Speicherkondensatorleitung (30) durch partielle Überlappung der Speicherkondensatorleitung (30) mit der zweiten Pixelelektrode (92) und der ersten Pixelelektrode (91) der zwei benachbarten Pixelbereiche kapazitiv mit der zweiten Pixelelektrode (92) des Pixelbereichs in der n-th Pixelbereichszeile und der m-th Pixelbereichsspalte und der ersten Pixelelektrode (91) des Pixelbereichs in der (n+1)-th Pixelbereichszeile und der m-th Pixelbereichsspalte gekoppelt ist;

einen ersten Dünnschichttransistor und einen zweiten Dünnschichttransistor in jedem Pixelbereich;

ein zweites transparentes Isoliersubstrat (100), das den ersten transparenten Isoliersubstrat (10) zugewandt ist;

eine Flüssigkristallschicht (900), die zwischen dem ersten und dem zweiten transparenten Isoliersubstrat (10, 100) angeordnet ist; und

wobei die Flüssigkristallschicht jeder der ersten Pixelelektroden und der zweiten Pixelelektroden durch ein erstes direktionales Domänen-Unterteilungsglied bzw. ein zweites direktionales Domänen-Unterteilungsglied unterteilt ist, um die Flüssigkristallschicht (900) in eine Vielzahl von Domänen zu unterteilen, wobei das erste und das zweite direktionale Domänen-Unterteilungsglied an einer gemeinsamen Elektrode (400) geformt sind, wobei die gemeinsame Elektrode (400) auf dem zweiten transparenten Isoliersubstrat (100) geformt ist; wobei die direktionalen Unterteilungsglieder erste bis dritte Öffnungsabschnitte (510, 520, 530) umfassen, die geformt sind, um die Flüssigkristallschicht (900) in eine Vielzahl von Domänen zu unterteilen; wobei der erste Öffnungsabschnitt (510) sich in die zweite Richtung erstreckt und die Flüssigkristallschicht an der zweiten Pixelelektrode (92) in zwei Domänen unterteilt, und

wobei der zweite und der dritte Öffnungsabschnitt (520, 530) sich in die erste Richtung erstrecken und die Flüssigkristallschicht an der ersten Pixelelektrode (91) in drei Domänen unterteilen und die erste Pixelelektrode (91) mit einem vierten Öffnungsabschnitt (95) versehen ist, der sich so in die erste Richtung erstreckt, dass die Flüssigkristallschicht an der ersten Pixelelektrode (91) in der zweiten Richtung durch den zweiten und den dritten Öffnungsabschnitt (520, 530) und den vierten Öffnungsabschnitt (95) in vier Domänen unterteilt ist; wobei in jedem Pixelbereich die erste Pixelelektrode (91) und die zweite Pixelelektrode (92) elektrisch mit einer der Gateleitungen (20) verbunden sind, die "gemeinsame Gateleitung" genannt wird und auf dem ersten transparenten Isoliersubstrat (10) geformt ist und eine der Datenleitungen (70) die "gemeinsame Datenleitungen" genannt wird durch den ersten Dünnschichttransistor bzw. den zweiten Dünnschichttransistor auf einer Gateisolierschicht (40) geformt ist,

wobei die zweite Pixelelektrode (92) der n-th Pixelbereichszeile und die erste Pixelelektrode (91) der (n+1)-th Pixelbereichszeile in derselben m-th Pixelbereichsspalte durch eine entsprechende Verbindungselektrode (74) kapazitiv miteinander verbunden sind, wobei die Verbindungselektrode (74) elektrisch mit der zweiten Pixelelektrode (92) der n-th Pixelbereichszeile verbunden ist und sich mit der ersten Pixelelektrode (91) der (n+1)-th Pixelbereichszeile so überlagert, dass die Verbindungselektrode (74) und die erste Pixelelektrode (91) der (n+1)-th Pixelbereichszeile eine Anschlusskapazität, connection capacitance-Cpp-, bilden, so dass während des Betriebes der Flüssigkristallanzeige in jedem Pixelbereich die Spannung der zweiten Pixelelektrode (92) mit Bezug auf die gemeinsame Elektrode (400) niedriger ist als diejenige der ersten Pixelelektrode (91), worin n und m ganze Zahlen sind.

2. Die Flüssigkristallanzeige gemäß Anspruch 1, wobei in jedem Pixelbereich die erste Pixelelektrode (91) und die zweite Pixelelektrode (92) die mit der entsprechenden gemeinsamen Gateleitung (20) über den ersten Dünnschichttransistor und den zweiten Dünnschichttransistor verbunden sind an gegenüberliegenden Seiten der gemeinsamen Gateleitung (20) positioniert sind.
3. Die Flüssigkristallanzeige gemäß Anspruch 1, wobei die Flüssigkristallmoleküle in der Flüssigkristallschicht in Abwesenheit eines elektrischen Feldes mit Bezug auf das erste transparente Isoliersubstrat (10) in die vertikale Richtung ausgerichtet sind.
4. Die Flüssigkristallanzeige gemäß Anspruch 1, wobei jede Verbindungselektrode (74) mit der entsprechenden zweiten Pixelelektrode (92) über ein entsprechendes Kontaktloch (83) in Kontakt steht, das in einer Schutzschicht (80) geformt ist.
5. Die Flüssigkristallanzeige gemäß Anspruch 4, wobei jede Verbindungselektrode (74) sich mit der entsprechenden ersten Pixelelektrode (91) überlagert, wobei sich die Schutzschicht (80) zwischen ihnen befindet.
6. Die Flüssigkristallanzeige gemäß Anspruch 5, wobei jede Verbindungselektrode (74) einen Abschnitt der entsprechenden Speicherkondensatorleitung (30) überlagert, wobei die entsprechende erste Pixelelektrode (91) ebenfalls überlagert.
7. Die Flüssigkristallanzeige gemäß Anspruch 5, wobei das Belegungsverhältnis der ersten Pixelelektrode (91) innerhalb eines Pixelbereichs 30-70% beträgt.

## Revendications

### 1. Affichage à cristaux liquides, comprenant :

un premier substrat isolant transparent (10) ;  
 des lignes de grille (20) formées sur le premier substrat isolant transparent (10) dans une première direction ;  
 des lignes de données (70) formées sur le premier substrat isolant transparent (10) dans une seconde direction ;  
 la première direction étant perpendiculaire à la seconde direction ;  
 une pluralité de régions de pixel agencées en rangées dans la première direction et en colonnes dans la seconde direction ;  
 des lignes de condensateurs de stockage (30) dans la première direction, une de chacune des lignes de condensateurs de stockage (30) s'étendant parallèle à et entre deux lignes de grille (20) adjacentes ;  
 dans lequel chaque région de pixel inclut une première électrode de pixel (91) et une seconde électrode de pixel (92) sur le premier substrat isolant transparent (10), et dans lequel une de chacune des lignes de condensateurs de stockage (30) est positionnée entre la région de pixel de la n-ième rangée de régions de pixel dans la m-ième colonne de régions de pixel et la région de pixel de la (n+1)-ième rangée de régions de pixel dans la m-ième colonne de régions de pixel de telle manière que la ligne de condensateurs de stockage (30) est couplée capacitivement avec la seconde électrode de pixel (92) de la région de pixel dans la n-ième rangée de régions de pixel et la m-ième colonne de régions de pixel et la première électrode de pixel (91) de la région de pixel dans la (n+1)-ième rangée de régions de pixel et la m-ième colonne de régions de pixel par la superposition partielle de ladite ligne de condensateurs de stockage (30) avec ladite seconde électrode de pixel (92) et ladite première électrode de pixel (91) desdites deux régions de pixel adjacentes ;  
 un premier transistor à film fin et un second transistor à film fin dans chaque région de pixel ;  
 un second substrat isolant transparent (100) faisant face au premier substrat isolant transparent (10) ;  
 une couche de cristaux liquides (900) intercalée entre les premier et second substrats isolants transparents (10, 100) ; et  
 dans lequel la couche de cristaux liquides sur chacune des premières électrodes de pixel et des secondes électrodes de pixel est partitionnée par un premier élément de partition en domaines directionnel et un second élément de partition en domaines directionnel, respectivement pour partitionner la couche de cristaux liquides (900) en une pluralité de domaines, dans lequel les premier et second éléments de partition en domaines directionnels sont formés au niveau d'une électrode commune (400), l'électrode commune (400) étant formée sur le second substrat isolant transparent (100) ;  
 dans lequel les éléments de partition directionnels comprennent des première à troisième parties d'ouverture (510, 520, 530) qui sont formées pour partitionner la couche de cristaux liquides (900) en une pluralité de domaines ;  
 dans lequel la première partie d'ouverture (510) s'étend dans la seconde direction coupant en deux la couche de cristaux liquides au niveau de la seconde électrode de pixel (92) en domaines, et  
 dans lequel les seconde et troisième parties d'ouverture (520, 530) s'étendent dans la première direction et coupent en trois la couche de cristaux liquides au niveau de la première électrode de pixel (91) en domaines, et la première électrode de pixel (91) est pourvue d'une quatrième partie d'ouverture (95) s'étendant dans la première direction de telle manière que la couche de cristaux liquides au niveau de la première électrode de pixel (91) est partitionnée de ce fait dans la seconde direction en quatre domaines par les seconde et troisième parties d'ouverture (520, 530) et la quatrième partie d'ouverture (95) ;  
 dans lequel dans chaque région de pixel la première électrode de pixel (91) et la seconde électrode de pixel (92) sont connectées électriquement à l'une des lignes de grille (20) étant appelée la ligne de grille commune, formée sur le premier substrat isolant transparent (10) et premier substrat isolant transparent (10) et l'une des lignes de données (70), étant appelée la ligne de données commune, formée sur une couche d'isolation de grille (40) via le premier transistor à film fin et le second transistor à film fin, respectivement ;  
 dans lequel la seconde électrode de pixel (92) de la n-ième rangée de régions de pixel et la première électrode de pixel (91) de la (n+1)-ième rangée de régions de pixel dans la même m-ième colonne de régions de pixel, sont connectées entre elles par des condensateurs, par une électrode de connexion (74) correspondante, l'électrode de connexion (74) étant connectée électriquement à la seconde électrode de pixel (92) de la n-ième rangée de régions de pixel et étant superposée avec la première électrode de pixel (91) de la (n+1)-ième rangée de régions de pixel de telle manière que l'électrode de connexion (74) et la première électrode de pixel (91) de la (n+1)-ième rangée de régions de pixel forment un condensateur de connexion (C<sub>pp</sub>), de telle manière que, pendant le pilotage de l'affichage à cristaux liquides, dans chaque région de pixel la tension de la seconde électrode de pixel (92) est inférieure à celle de la première électrode de pixel (91) en référence à l'électrode commune (400), où n et m sont des entiers.

2. Affichage à cristaux liquides selon la revendication 1, dans lequel dans chaque région de pixel la première électrode de pixel (91) et la seconde électrode de pixel (92), étant connectées à la ligne de grille commune (20) via le premier transistor à film fin et le second transistor à film fin, sont positionnées sur des cotés opposés de la ligne de grille commune (20).
3. Affichage à cristaux liquides selon la revendication 1, dans lequel les molécules de cristaux liquides dans la couche de cristaux liquides sont alignées dans la direction verticale par rapport au premier substrat isolant transparent (10) en l'absence d'un champ électrique.
4. Affichage à cristaux liquides selon la revendication 1, dans lequel chaque électrode de connexion (74) contacte la seconde électrode de pixel (92) correspondante par l'intermédiaire d'un trou de contact (83) correspondant formé dans une couche protectrice (80).
5. Affichage à cristaux liquides selon la revendication 4, dans lequel chaque électrode de connexion (74) est superposée à la première électrode de pixel (91) correspondante, la couche protectrice (80) étant entre elles.
6. Affichage à cristaux liquides selon la revendication 5, dans lequel chaque électrode de connexion (74) est superposée avec une partie de la ligne de condensateurs de stockage (30) correspondante où la première électrode de pixel (91) correspondante est aussi superposée.
7. Affichage à cristaux liquides selon la revendication 5, dans lequel le rapport d'occupation de la première électrode de pixel (91) dans la région de pixel est de 30-70%.

FIG.1

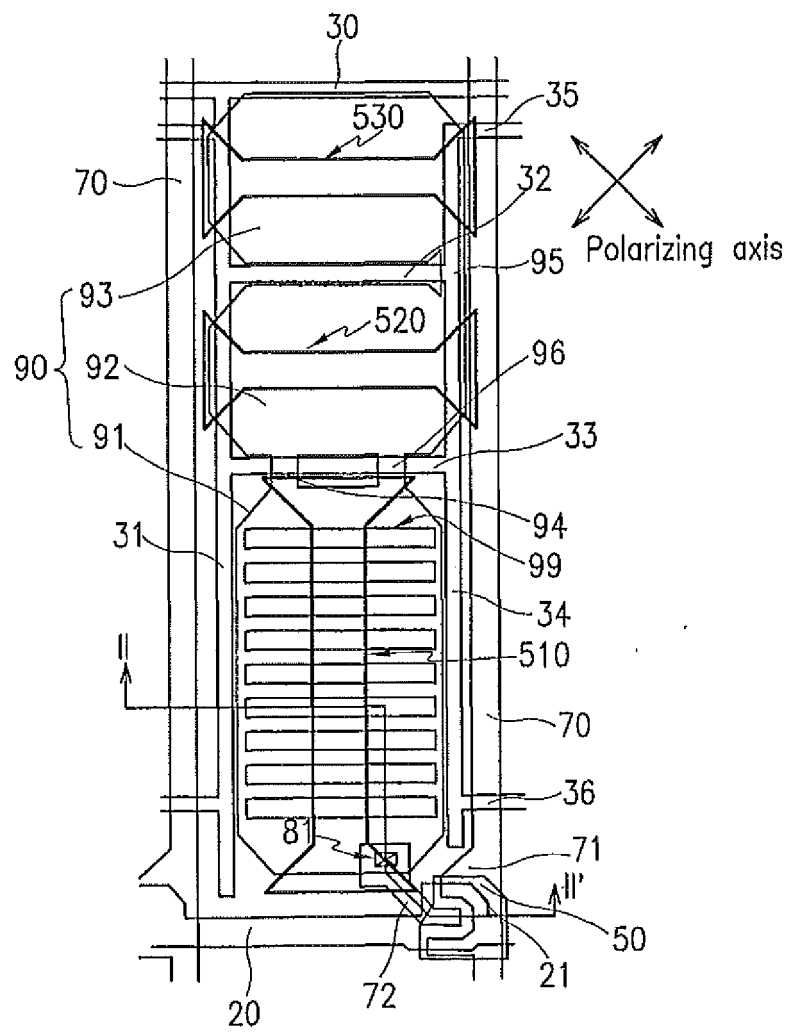


FIG.2

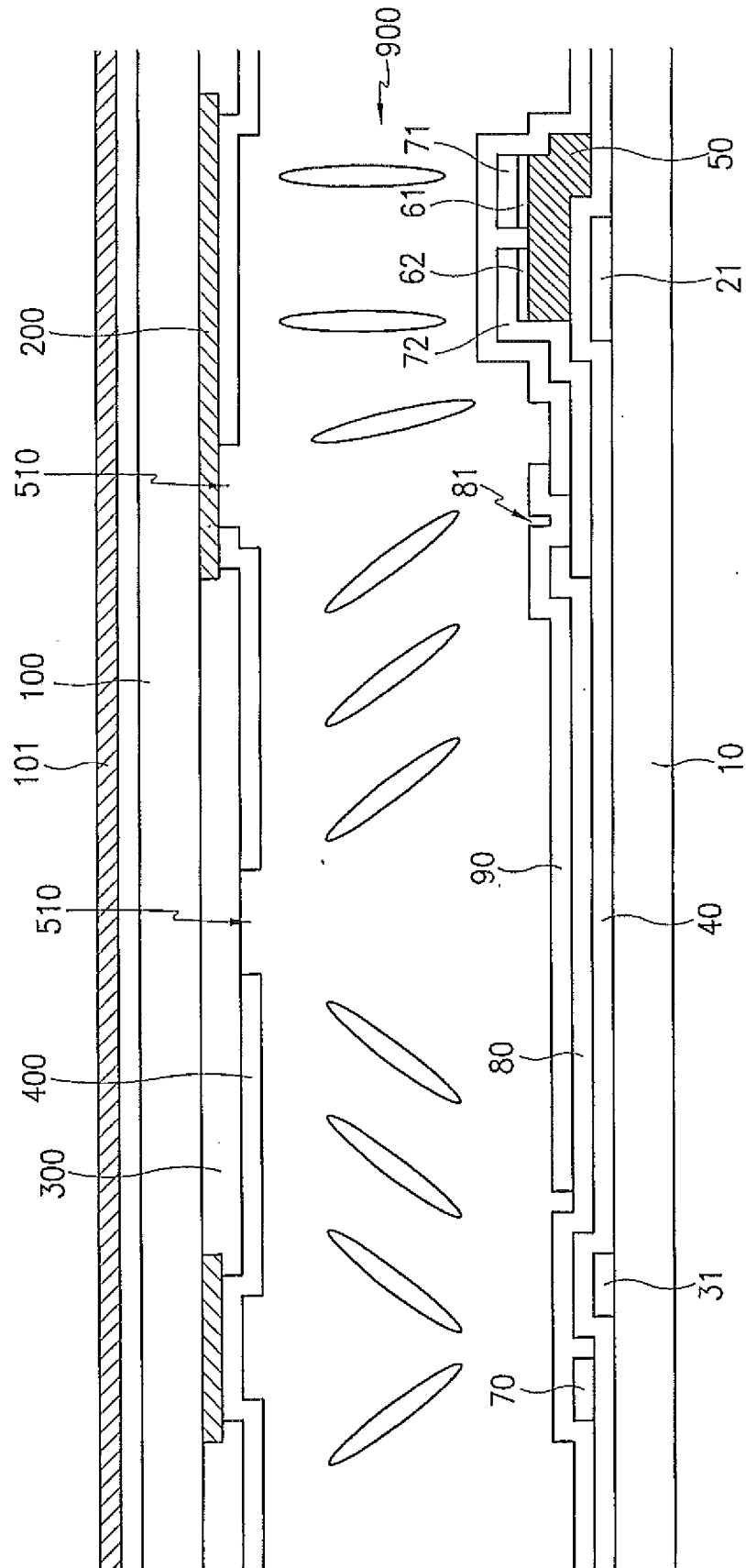


FIG.3

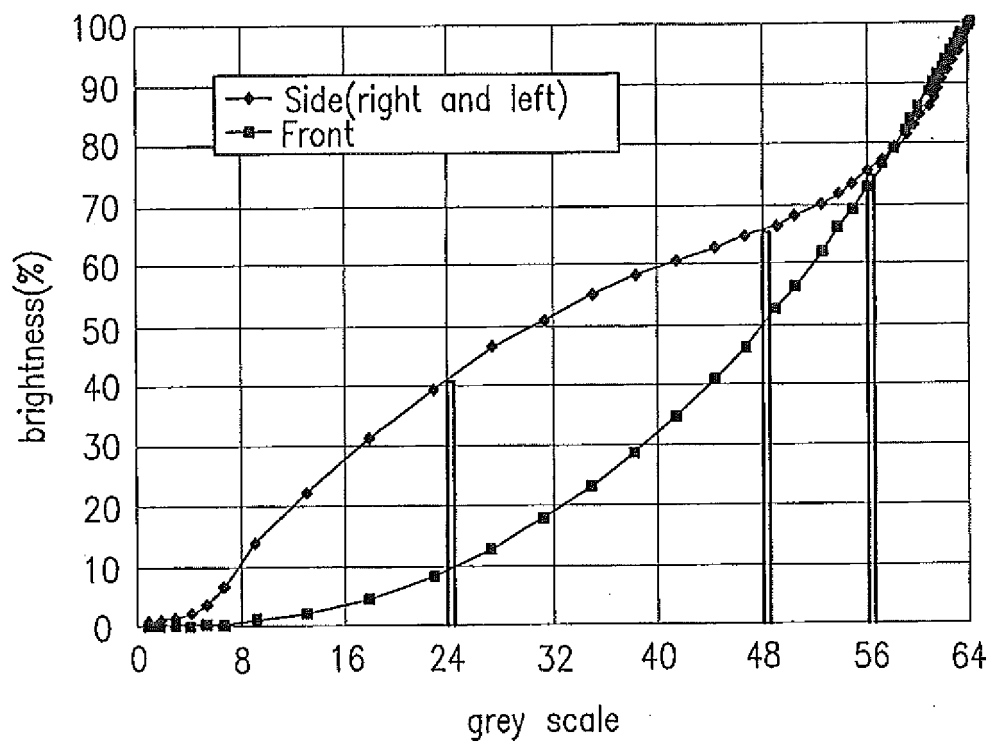




FIG.4

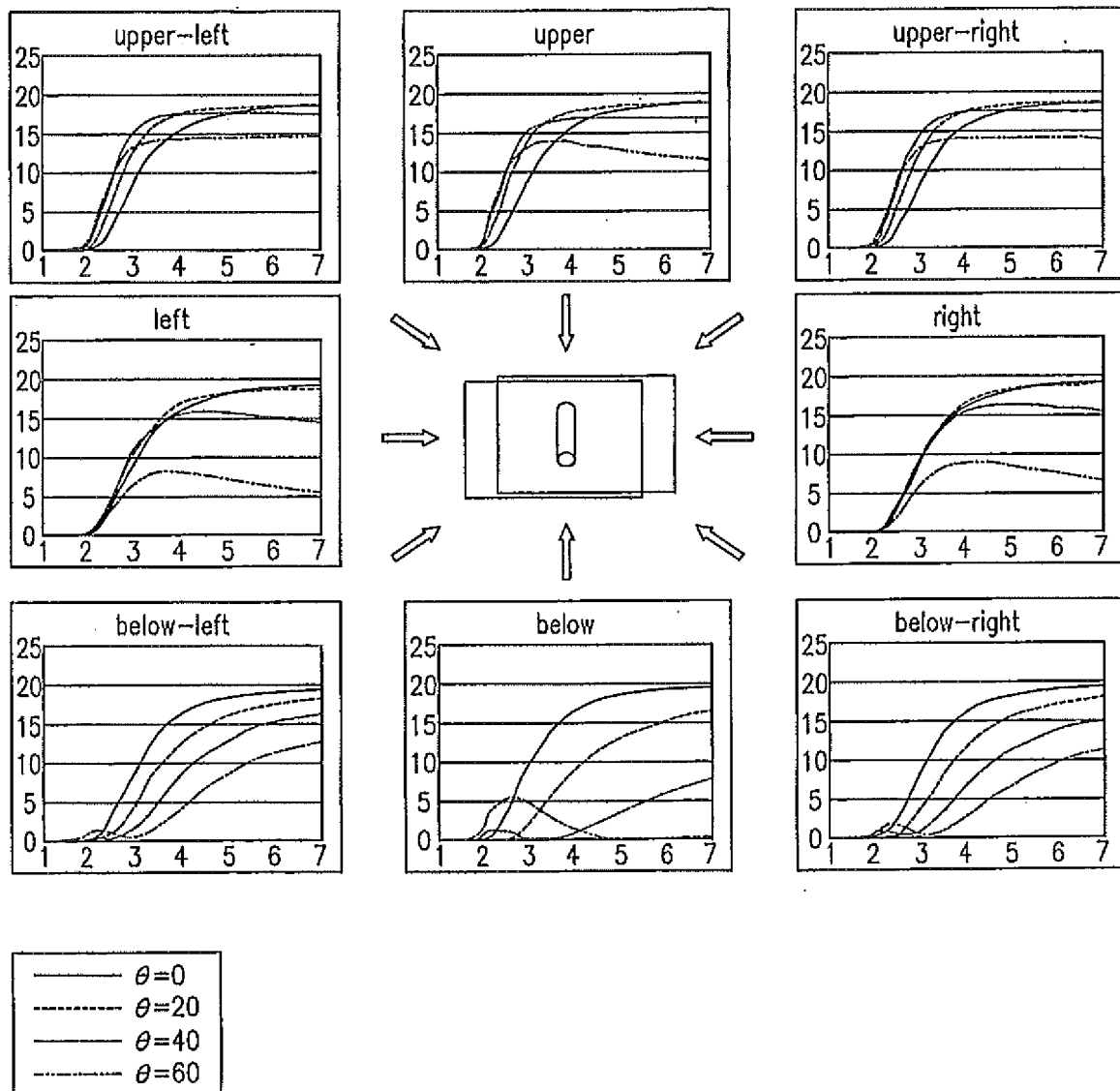


FIG.5

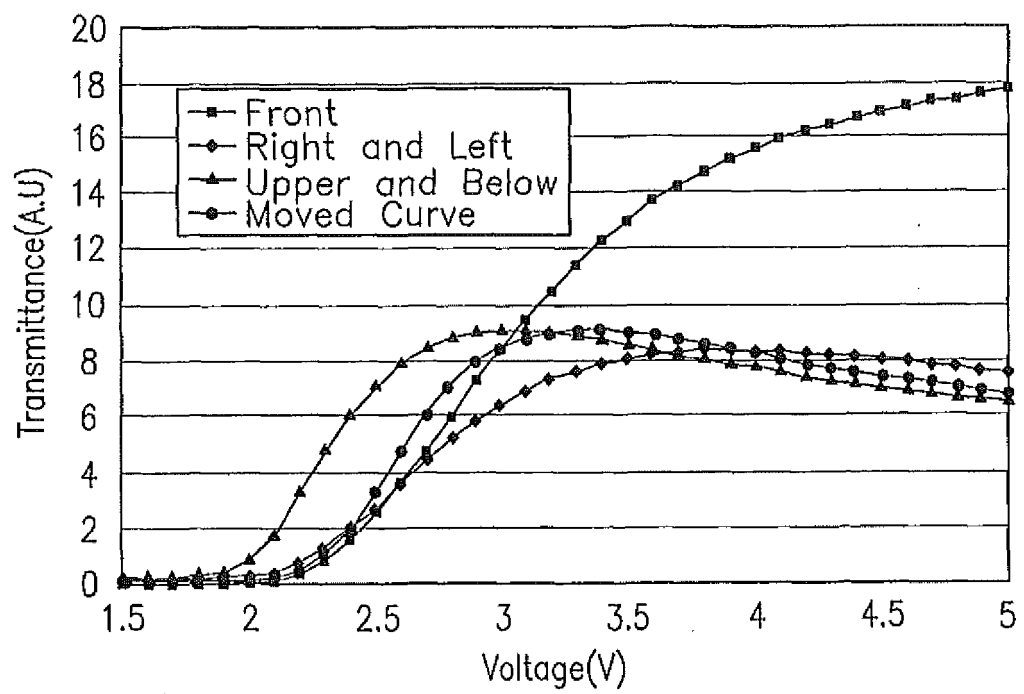


FIG.6

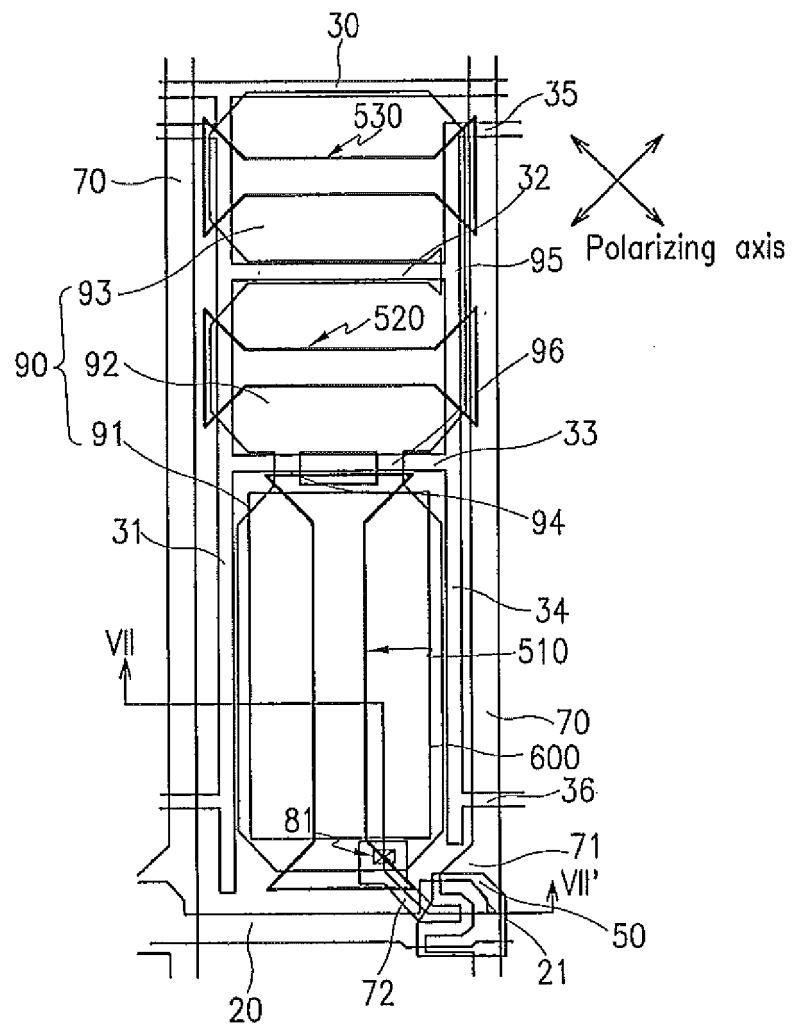
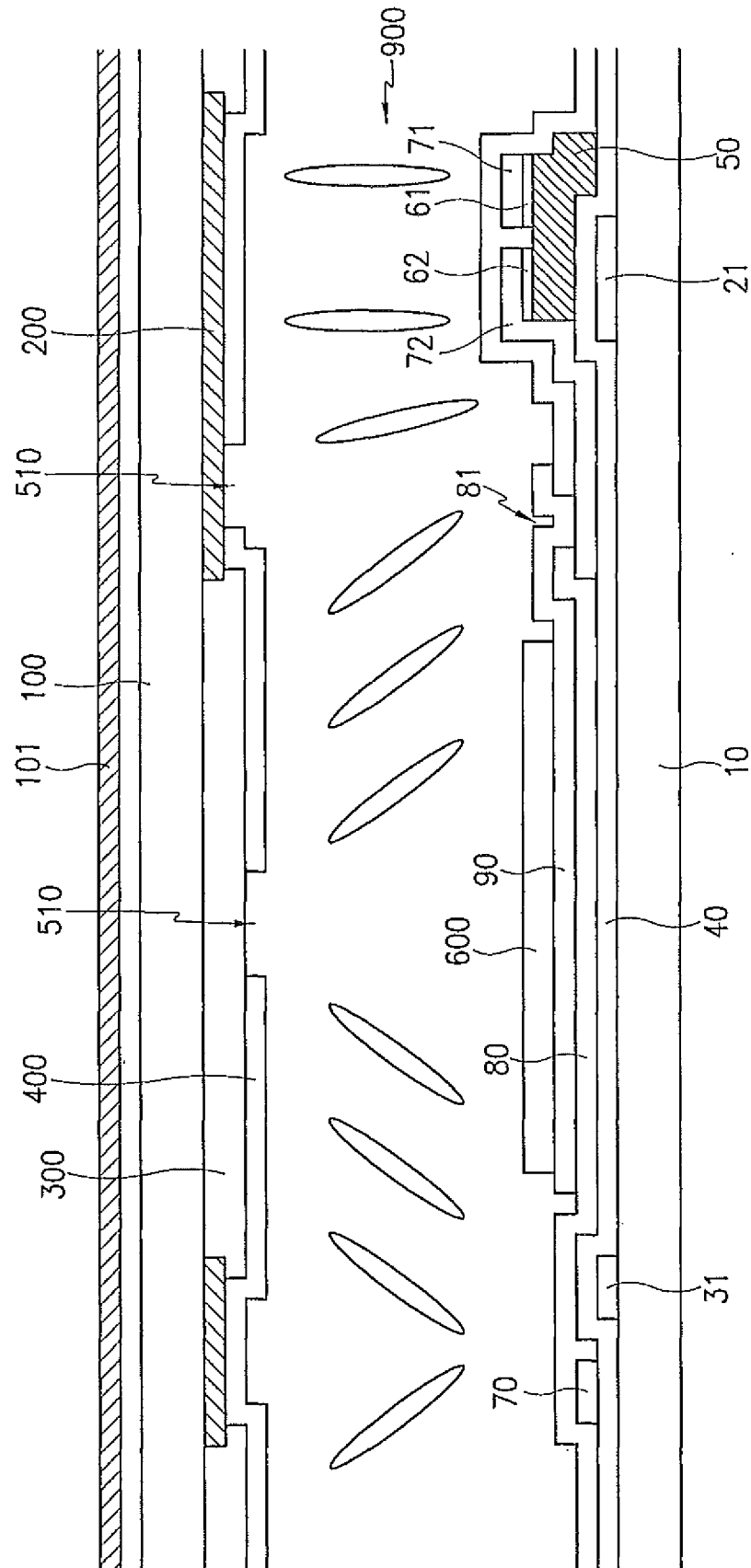


FIG. 7



8.  
G  
F

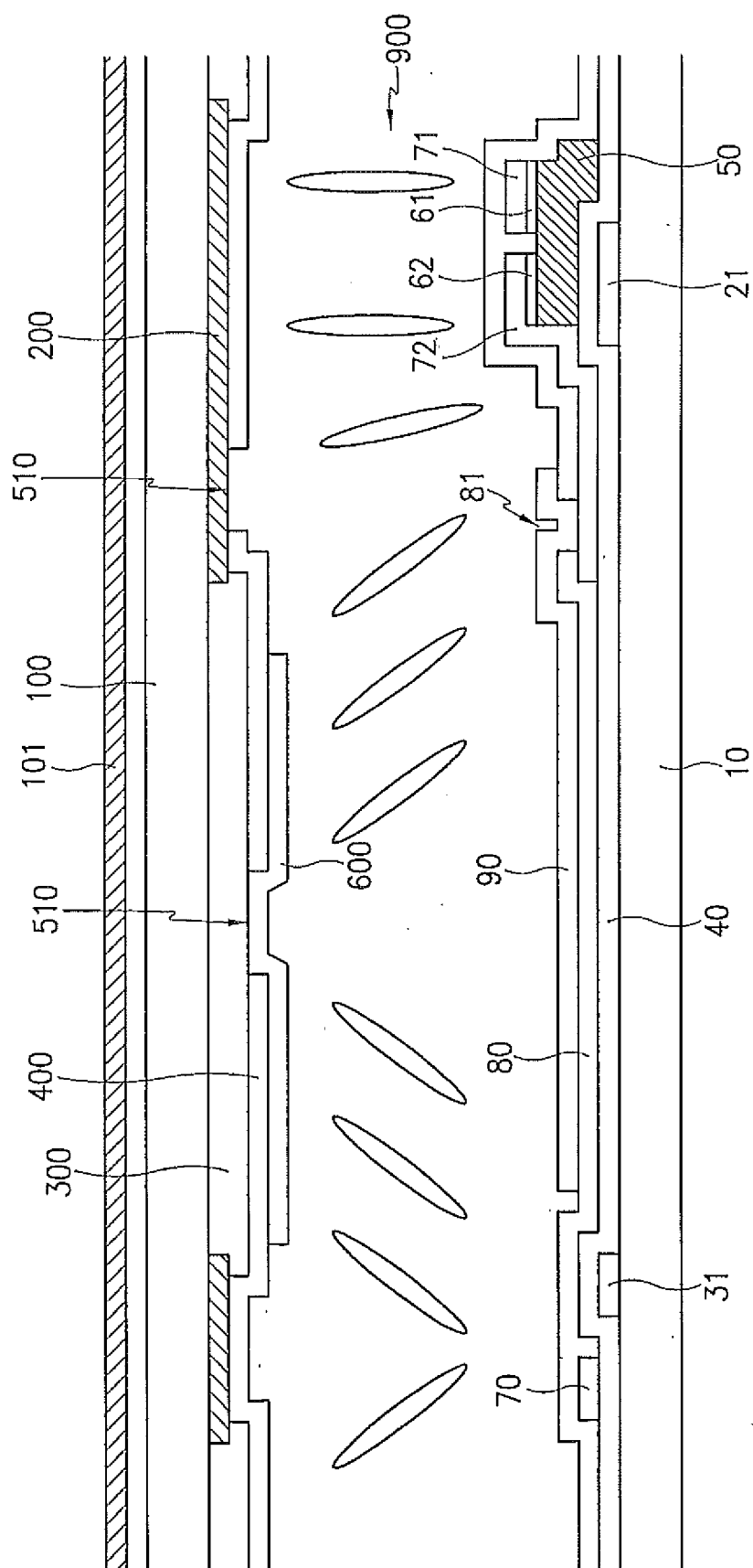


FIG.9

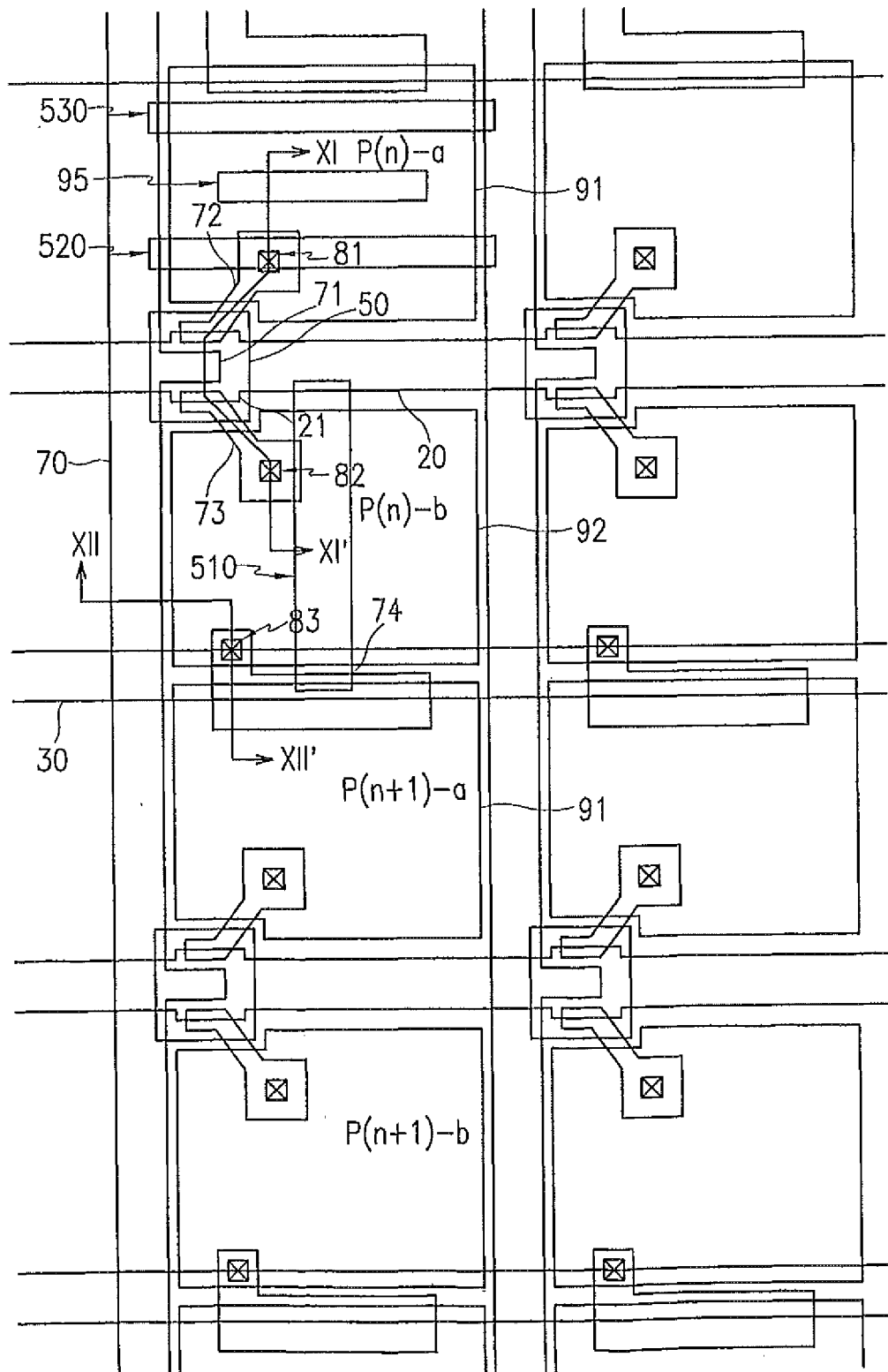


FIG.10

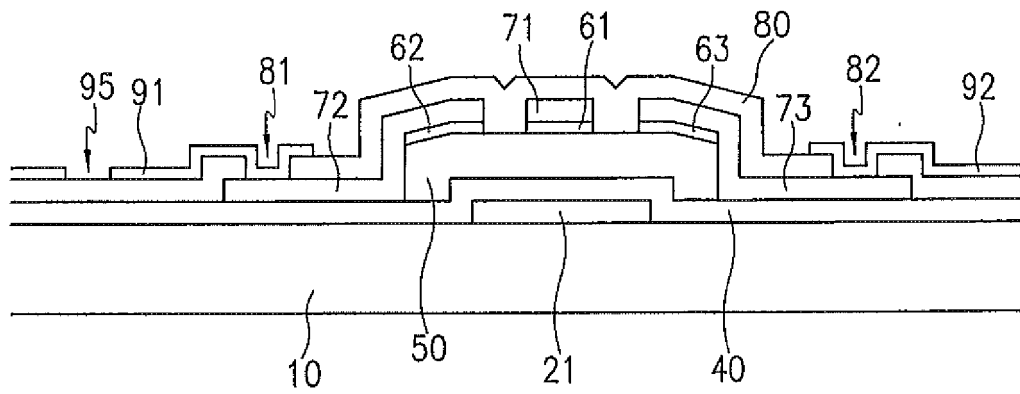


FIG.11

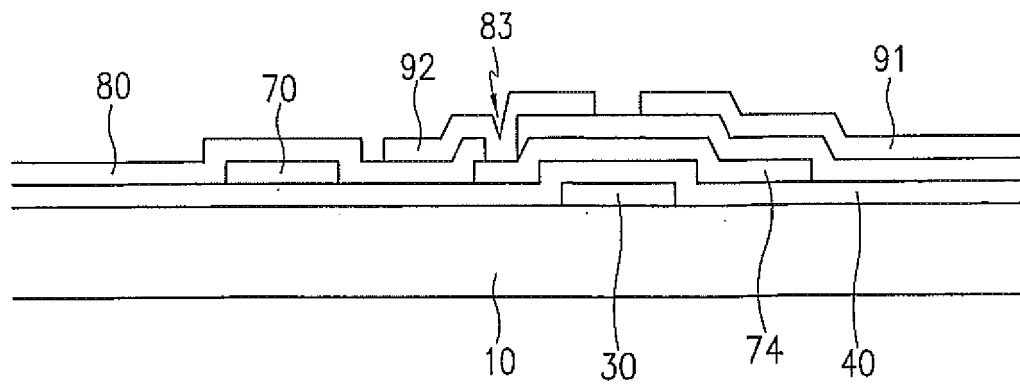


FIG.12

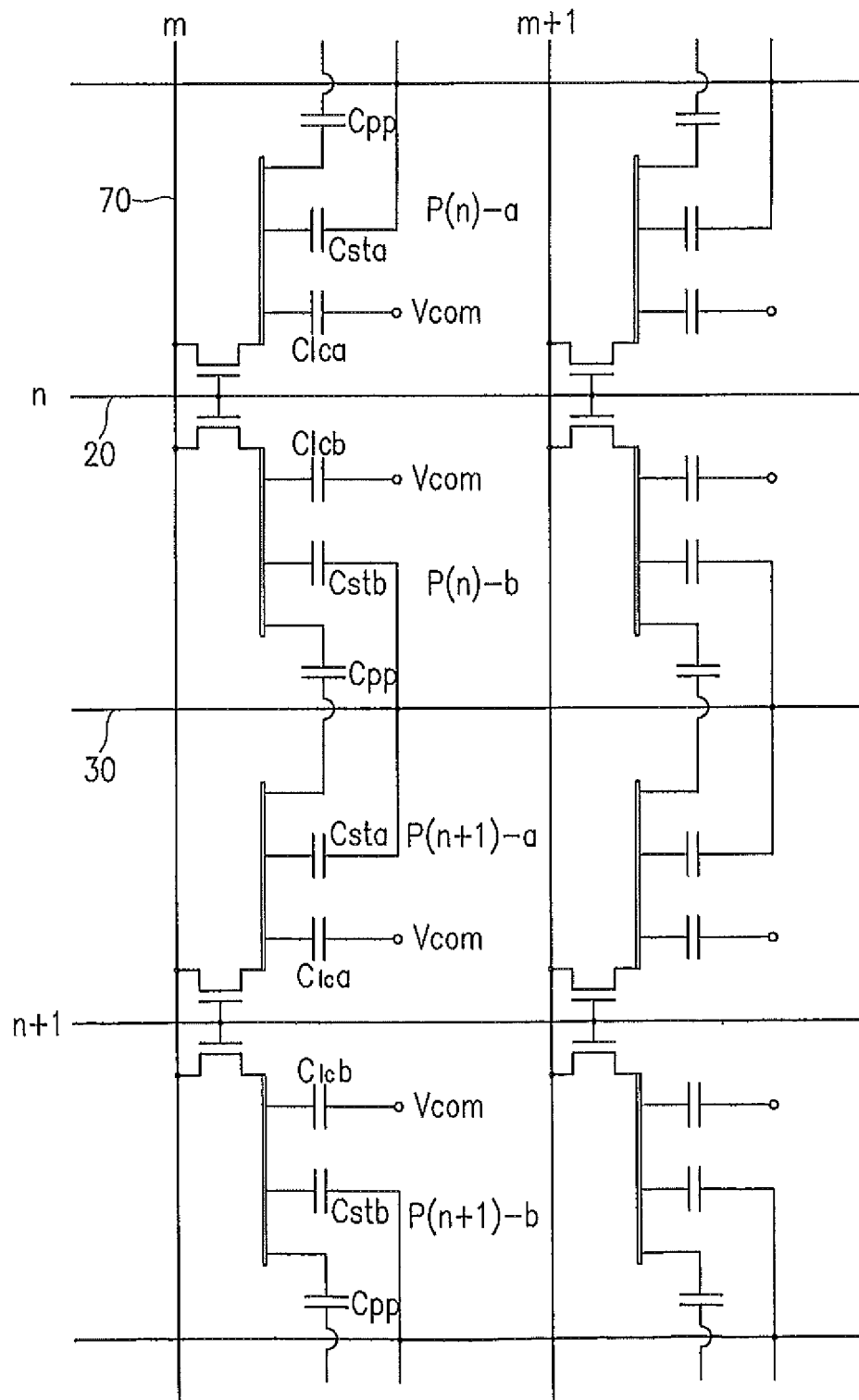




FIG.13

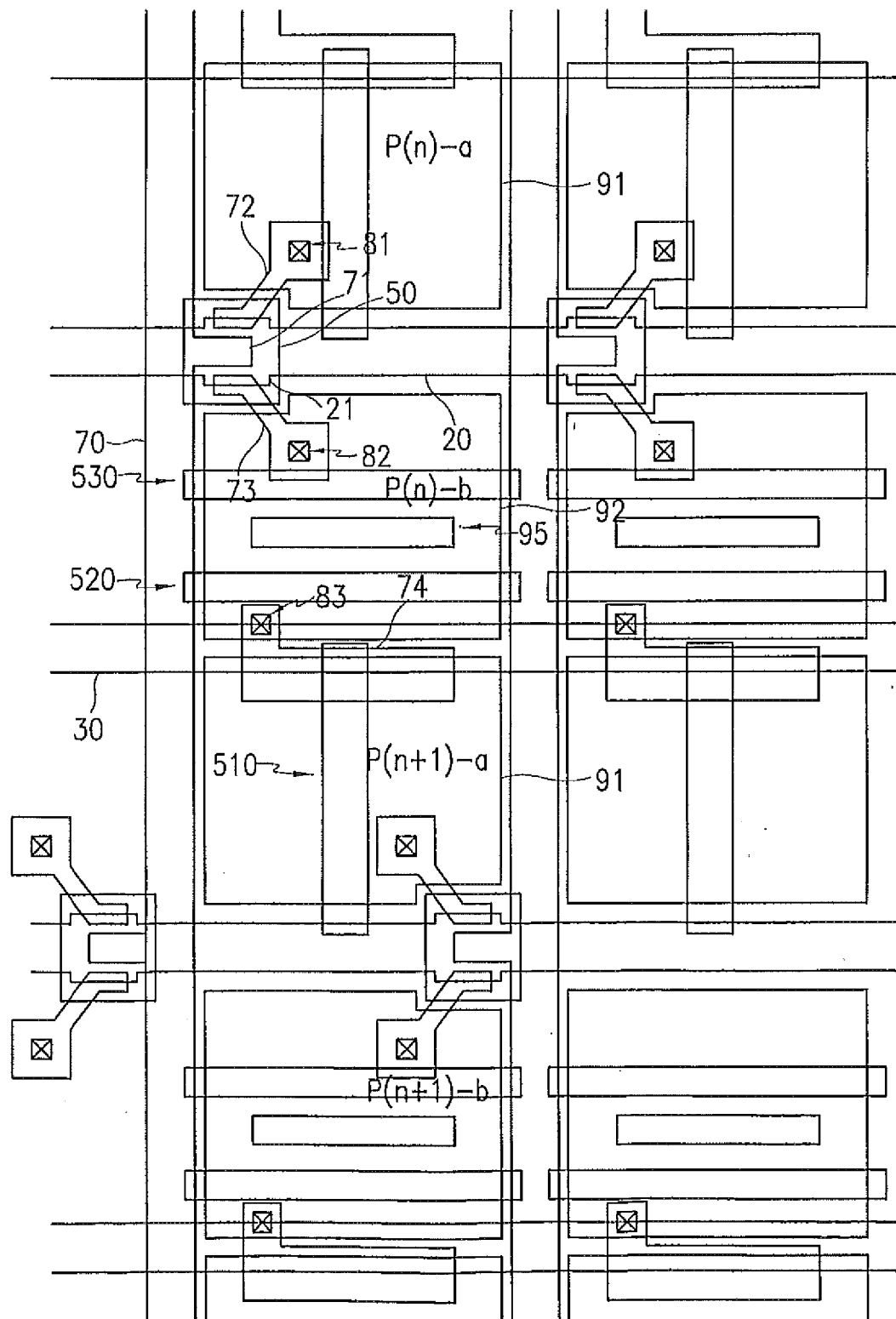
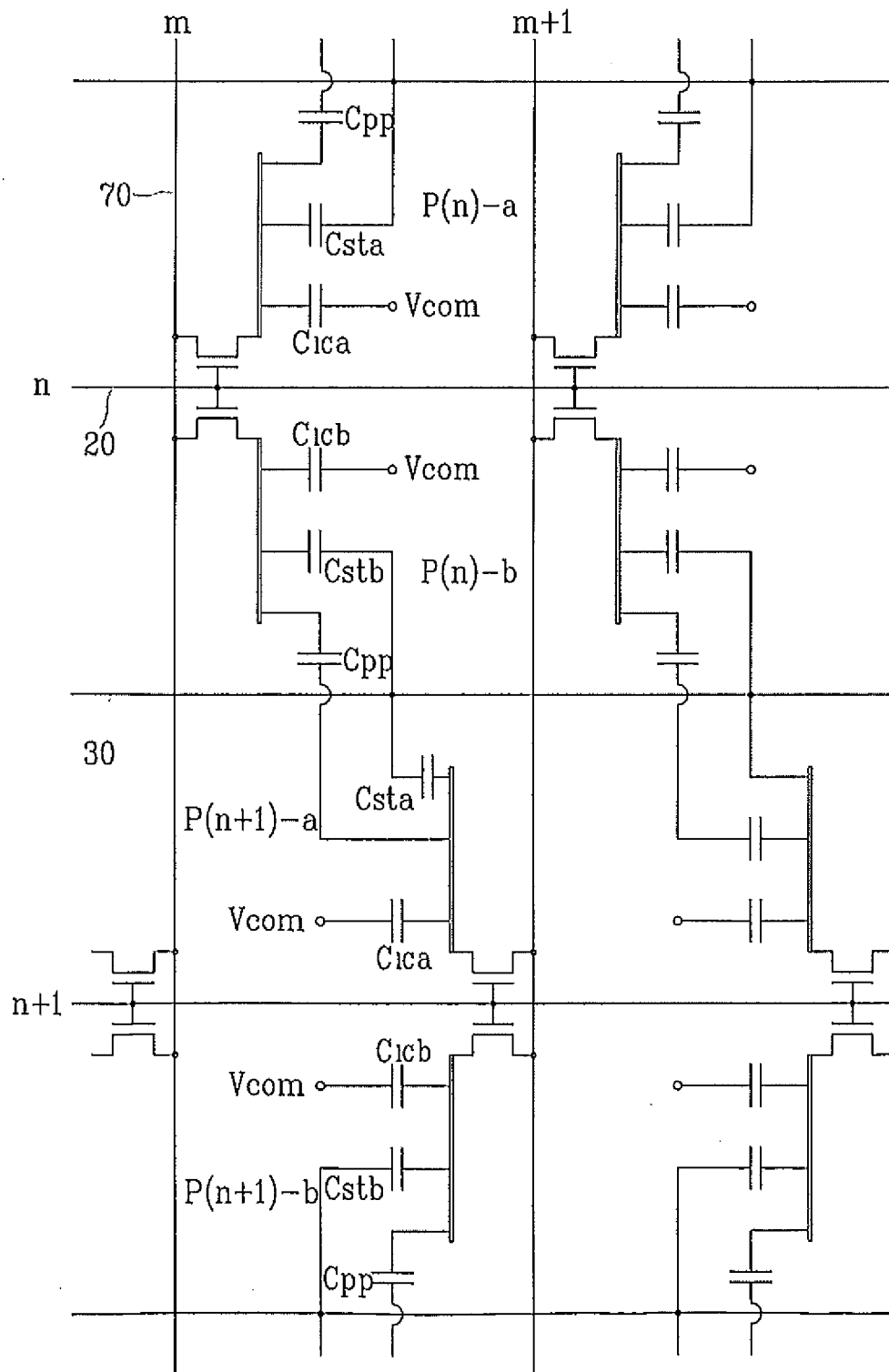


FIG.14



**REFERENCES CITED IN THE DESCRIPTION**

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**Patent documents cited in the description**

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