



(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
06.10.2021 Bulletin 2021/40

(51) Int Cl.:
B01J 19/00 (2006.01) G11C 13/00 (2006.01)

(21) Application number: **20167573.3**

(22) Date of filing: **01.04.2020**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME
Designated Validation States:
KH MA MD TN

(72) Inventors:
• **HENRY, Olivier**
3001 Leuven (BE)
• **FURNEMONT, Arnaud**
3001 Leuven (BE)
• **COSEMANS, Stefan**
3001 Leuven (BE)

(71) Applicant: **Imec VZW**
3001 Leuven (BE)

(74) Representative: **DenK iP bv**
Leuvensesteenweg 203
3190 Boortmeerbeek (BE)

(54) **ADDRESSING NANO-ELECTRODES IN A NANO-ELECTRODE ARRAY**

(57) In a first aspect, the present invention relates to a system for addressing nanoelectrodes (30-33) in a nanoelectrode array (20), the system comprising an array of electrode cells (60), each electrode cell (60) comprising: (i) an access transistor (70) having a gate resistively

coupled to a word line (71), a source resistively coupled to a bit line (72), and a drain; and (ii) a storage circuit (80) resistively coupled to the drain and comprising a nanoelectrode (30-33).

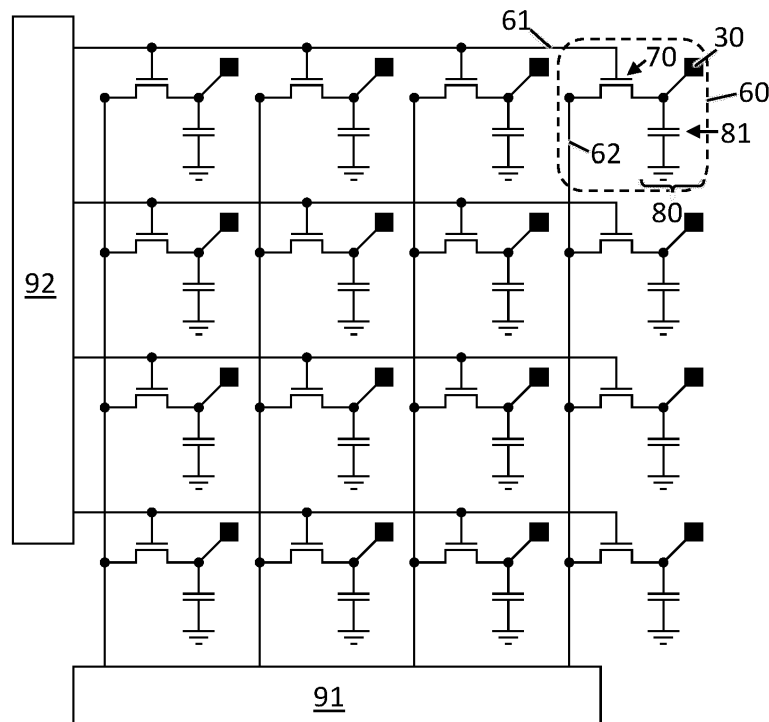


FIG 8

Description

Technical field of the invention

[0001] The present invention relates to nanoelectrode arrays for example for use in molecular synthesis and in particular to addressing the nanoelectrodes therein.

Background of the invention

[0002] The call for cheap and dense cold data storage increasingly raises interest in molecular data storage solutions such as DNA-based in which stable organic molecules are synthesized to map binary information. To make such molecular data storage practical, a high synthesis throughput is sought so that a reasonable 'write time' can be achieved. To that end, solutions have been explored in which multiple different molecules are parallelly synthesizing in an array of synthesis cells.

[0003] In order to form different molecules in the different synthesis cells, the synthesis must be made selective; i.e. the reaction needs to be enabled in a certain portion of the array and inhibited in the rest of the array. This challenge can be tackled in different ways, but the most promising approaches are based on electrodes. In such approaches, each synthesis cell typically has one or more electrodes associated therewith, with which the reaction conditions (e.g. pH) are locally controlled. US20160354751A1 for example describes a microarray of electrodes for oligonucleotide synthesis having in excess of 12,000 electrodes in a region of about 1 cm², with a circular electrode diameter of about 44 microns and an electrode distance-to-distance of about 75 microns.

[0004] However, in order to achieve writing speeds at which the molecular data storage can become commercially relevant, arrays of about one billion electrodes or more would be desired. With a factor in the order of 100,000 compared to US20160354751A1, this represents an aggressive change in scope that brings with it several complications which cannot be overcome in a trivial manner. There is thus still a need in the art for solutions which address at least some of these issues.

Summary of the invention

[0005] It is an object of the present invention to provide a good system for addressing nanoelectrodes in a nanoelectrode array. It is a further object of the present invention to provide good uses and methods associated with such a system. This objective is accomplished by systems, uses and methods in according to the present invention.

[0006] In particular, a convenient way is provided for realizing the aggressive change in scope that was described in the background section. First, at a density of 12,000 electrodes/cm², a straightforward extension of the microarray of US20160354751A1 would require an unwieldy array size of 8.3 m² to reach one billion elec-

trodes. Conversely, the required footprint is presently scaled down considerably through using nanoelectrodes (e.g. having a size of few hundred nanometre or less) rather than microelectrodes with a size of several tens of micrometre. Moreover, it was further realized that a mere size reduction is insufficient. Indeed, perhaps less immediately apparent but at least as important is the issue of how to address roughly one billion or more electrodes sufficiently simultaneously. After all, if the potential for each of these electrodes cannot be set within a relatively short time frame (e.g. compared to the required synthesis time), the synthesis in the synthesis cells will not be parallel and/or the required total write time will be unduly prolonged. This is true for the hypothetical 8.3 m² microarray but is even further exacerbated for an array of nanoelectrodes, where the requirements for the driving electronics (e.g. in terms of available/allowable space, current, power, heat production, etc.) are necessarily increasingly strict. Nevertheless, the present invention offers an elegant solution to this problem; as will be clarified further below.

[0007] It is an advantage of embodiments of the present invention that compact (i.e. densely packed) electrode arrays can be formed.

[0008] It is an advantage of embodiments of the present invention that a vast number of nanoelectrodes can be individually addressed. It is a further advantage of embodiments of the present invention that the nanoelectrodes can be set relatively simultaneously with respect to the typical time frame needed for a chemical reaction (e.g. the chemical reaction may occur on a time frame in the order of seconds, while all the nanoelectrodes may be set within a time frame in the order of tens of milliseconds). It is yet a further advantage of embodiments of the present invention that the potential for the nanoelectrodes can be quickly set, re-set and/or overwritten.

[0009] It is an advantage of embodiments of the present invention that addressing the nanoelectrodes can be performed at low power (e.g. in the order of up to 500 mW) and/or low voltage (e.g. about 0.5 to 1 V in addition to the voltage difference between the lowest and highest potential set for the nanoelectrodes, e.g. between an inactive and an active nanoelectrode or between a counteractive and an active nanoelectrode).

[0010] It is an advantage of embodiments of the present invention that the electrode cells have very long (e.g. almost infinite) endurance; i.e. they do not easily break down, even after extended use (e.g. the access transistor can be opened and the storage circuit charged about 10¹⁵ times or more before breaking down).

[0011] It is an advantage of embodiments of the present invention that the potential of the nanoelectrodes can be selected and set relatively freely (e.g. the potential is not limited to a discrete number of values). It is a further advantage of embodiments of the present invention that the potential of different nanoelectrodes in the nanoelectrode array can be individually selected and set.

[0012] It is an advantage of embodiments of the present invention that well-developed strategies and fabrication methods that have been developed for dynamic random-access memory (DRAM) can be optimally benefited from.

[0013] It is an advantage of embodiments of the present invention that the reaction conditions can be physically and/or electrochemically confined.

[0014] It is an advantage of embodiments of the present invention that a vast number of different molecules (e.g. DNA) can be synthesized in parallel. It is a further advantage of embodiments of the present invention that an effective DNA data storage can be realized.

[0015] It is an advantage of embodiments of the present invention that back end of line (BEOL) electrode cell access transistors can be used, thereby allowing to use the front end of line (FEOL) region entirely for peripheral circuits.

[0016] It is an advantage of embodiments of the present invention that in setting the potential of the nanoelectrodes also control over their current can be achieved. It is a further advantage of embodiments of the present invention that systems can be realized in which the nanoelectrodes can be operated potentiostatically, galvanostatically or potentiodynamically.

[0017] In a first aspect, the present invention relates to a system for addressing nanoelectrodes in a nanoelectrode array, the system comprising an array of electrode cells, each electrode cell comprising: (i) an access transistor having a gate resistively coupled to a word line, a source resistively coupled to a bit line, and a drain; and (ii) a storage circuit resistively coupled to the drain and comprising a nanoelectrode.

[0018] In a second aspect, the present invention relates to a use of a system as defined in any embodiment of the first aspect, for addressing nanoelectrodes in a nanoelectrode array.

[0019] In a third aspect, the present invention relates to a method for addressing nanoelectrodes in a system according to any embodiment of the first aspect, comprising: (a) selecting a potential for each nanoelectrode, and (b) setting the selected potentials by, for each electrode cell, opening the access transistor by asserting the word line and charging the storage circuit to the selected electrode potential by aptly biasing the bit line.

[0020] In a fourth aspect, the present invention relates to a method for synthesizing a molecule, comprising: (a) setting the potential of one or more nanoelectrodes using the method according to any embodiment of the third aspect, and (b) contacting one or more reagents to the nanoelectrodes; thereby locally forming an electrochemical environment for mediating the synthesis.

[0021] Particular and preferred aspects of the invention are set out in the accompanying independent and dependent claims. Features from the dependent claims may be combined with features of the independent claims and with features of other dependent claims as appropriate and not merely as explicitly set out in the claims.

[0022] Although there has been constant improvement, change and evolution of devices in this field, the present concepts are believed to represent substantial new and novel improvements, including departures from prior practices, resulting in the provision of more efficient, stable and reliable devices of this nature.

[0023] The above and other characteristics, features and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, which illustrate, by way of example, the principles of the invention. This description is given for the sake of example only, without limiting the scope of the invention. The reference figures quoted below refer to the attached drawings.

Brief description of the drawings

[0024]

FIG 1 and FIG 3 schematically show 3D views of an arrays for molecular synthesis in accordance with embodiments of the present invention.

FIG 2 and FIG 4 schematically shows more detailed vertical cross-sections of the arrays in FIG 1 and FIG 3.

FIG 5, FIG 6 and FIG 7 schematically show a top view of several nanoelectrodes, illustrating embodiments of the present invention in which the reaction conditions are electrochemically confined.

FIG 8 schematically depicts an array of electrode cells in accordance with embodiments of the present invention.

[0025] In the different figures, the same reference signs refer to the same or analogous elements.

Description of illustrative embodiments

[0026] The present invention will be described with respect to particular embodiments and with reference to certain drawings but the invention is not limited thereto but only by the claims. The drawings described are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes. The dimensions and the relative dimensions do not correspond to actual reductions to practice of the invention.

[0027] Furthermore, the terms first, second, third and the like in the description and in the claims, are used for distinguishing between similar elements and not necessarily for describing a sequence, either temporally, spatially, in ranking or in any other manner. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other sequences than described or illustrated herein.

[0028] Moreover, the terms top, bottom, over, under

and the like in the description and the claims are used for descriptive purposes and not necessarily for describing relative positions. It is to be understood that the terms so used are interchangeable with their antonyms under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other orientations than described or illustrated herein.

[0029] It is to be noticed that the term "comprising", used in the claims, should not be interpreted as being restricted to the means listed thereafter; it does not exclude other elements or steps. It is thus to be interpreted as specifying the presence of the stated features, integers, steps or components as referred to, but does not preclude the presence or addition of one or more other features, integers, steps or components, or groups thereof. The term "comprising" therefore covers the situation where only the stated features are present and the situation where these features and one or more other features are present. Thus, the scope of the expression "a device comprising means A and B" should not be interpreted as being limited to devices consisting only of components A and B. It means that with respect to the present invention, the only relevant components of the device are A and B.

[0030] Similarly, it is to be noticed that the term "coupled" should not be interpreted as being restricted to direct connections only. The terms "coupled" and "connected", along with their derivatives, may be used. It should be understood that these terms are not intended as synonyms for each other. Thus, the scope of the expression "an entity A coupled to an entity B" should not be limited to situations wherein an output of entity A is directly connected to an input of entity B. It means that there exists a path between an output of A and an input of B, which may be a path including other entities or means. "Coupled" may thus mean that two or more elements are either in direct contact (i.e. they may be connected), or that two or more elements are not in direct contact with each other but yet still co-operate or interact with each other.

[0031] Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment, but may. Furthermore, the particular features, structures or characteristics may be combined in any suitable manner, as would be apparent to one of ordinary skill in the art from this disclosure, in one or more embodiments.

[0032] Similarly, it should be appreciated that in the description of exemplary embodiments of the invention, various features of the invention are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however,

is not to be interpreted as reflecting an intention that the claimed invention requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims following the detailed description are hereby expressly incorporated into this detailed description, with each claim standing on its own as a separate embodiment of this invention.

[0033] Furthermore, while some embodiments described herein include some but not other features included in other embodiments, combinations of features of different embodiments are meant to be within the scope of the invention, and form different embodiments, as would be understood by those in the art. For example, in the following claims, any of the claimed embodiments can be used in any combination.

[0034] In the description provided herein, numerous specific details are set forth. However, it is understood that embodiments of the invention may be practised without these specific details. In other instances, well-known methods, structures and techniques have not been shown in detail in order not to obscure an understanding of this description.

[0035] Reference will be made to transistors. These are devices having a first main terminal (e.g. a source or collector), a second main terminal (e.g. a drain or emitter) and a control terminal (e.g. a gate or base) for controlling the flow of electrical charges between the first and second main terminals.

[0036] For a better qualitative understanding, an analogy with dynamic random-access memory (DRAM) and its operation will herein occasionally be made. It shall be clear however that the field of DRAM is hereto not a neighbouring field to nanoelectrode arrays and that they are concerned with different technical problems. As such, it shall be clear that this *ex post facto* analogy-which is given here only to aid the reader's understanding should not be abused to diminish the inventive step of the present invention. Indeed, the realization to our knowledge for the first time and without direction thereto in the prior art that circuits which are well known in DRAM can with the required adaptations-be repurposed to solve a technical problem faced in nanoelectrode arrays, forms an appreciable part of the inventive effort achieved by the present inventors.

[0037] In a first aspect, the present invention relates to a system for addressing nanoelectrodes in (e.g. arranged as) a nanoelectrode array, the system comprising an array of electrode cells, each electrode cell comprising: (i) an access transistor having a gate resistively coupled to a word line, a source resistively coupled to a bit line, and a drain; and (ii) a storage circuit resistively coupled to the drain and comprising a nanoelectrode.

[0038] It was surprisingly conceived within the present invention that addressing of nanoelectrodes in a nanoelectrode array can be realized in an effective manner by resistively coupling each nanoelectrode as part of a stor-

age circuit to the drain of an access transistor. Here, the analogy can be made with DRAM: the present electrode cell can be likened to a DRAM memory cell having a nanoelectrode coupled to the storage side thereof. Based on such an electrode cell, the potential of the nanoelectrodes can then be set using similar strategies (cf. *infra*) as have been developed to write to DRAM memory cells, including optionally periodically refreshing the set potentials.

[0039] In embodiments, the array of electrode cells may comprise one or more rows, the electrode cells in a row being linked by a common word line, and/or one or more columns, the electrode cells in a column being linked by a common bit line. In embodiments, the electrode cells may be arranged in a cubic packing, hexagonal packing or any other suitable arrangement.

[0040] In embodiments, the storage circuit may comprise the nanoelectrode and an electrical connection (e.g. wire) resistively coupling the nanoelectrode to the drain. In embodiments, the storage circuit may further comprise a capacitor. In embodiments, the capacitor may have a terminal resistively coupled to both the drain and the nanoelectrode (i.e. the same terminal may be coupled to both). In some embodiments, the capacitor may be a separate (i.e. distinct) capacitor; i.e. the capacitor may be an electrical component solely dedicated to that role. In other alternative or complementary embodiments, an electrical component may perform the role of capacitor and one or more further functions. For example, a capacitor may be formed about the electrical connection coupling the drain to the nanoelectrode, so that the ensemble simultaneously fulfils the role of the electrical connection and capacitor. Such a capacitor could for instance be achieved by wrapping the electrical connection with a dielectric and then wrapping a counter electrode about dielectric. In yet other alternative or complementary embodiments, through their inherent parasitic capacitance (e.g. wire capacitance), the storage circuit and/or the electrical connection as such may be regarded as a capacitor.

[0041] In embodiments, the storage circuit may have a capacitance of at least 0.01 fF, preferably at least 1 fF, more preferably at least 10 fF, yet more preferably at least 20 fF, such as at least 30, 50, 100, 200 or 500 fF. Especially in combination with a suitable refresh rate (e.g. 64 ms or more; cf. *infra*), such a capacitance in particular in the order of 10 fF (e.g. about 30 fF) or more should typically allow to store enough charge in order to drive an electrochemical reaction for a sufficient period of time (e.g. until the next refresh) to for instance enable or disable a synthesis reaction within a synthesis cell above the nanoelectrode. In embodiments, the capacitance of the storage circuit may be partially or entirely due to a parasitic capacitance (e.g. wire capacitance) of the storage circuit. In embodiments, the capacitor may have a capacitance of at least 0.01 fF, preferably at least 1 fF, more preferably at least 10 fF, yet more preferably at least 25 fF, most preferably at least 30 fF, such as at

least 30, 50, 100, 200 or 500 fF. Note that there is also a practical upper limit to the capacitance in that charging the storage circuit takes longer when the capacitance thereof is higher. As such, a favourable range for the capacitance may be from about 20 to about 500 fF when using a front-end-of-line (FEOL) access transistors, and from about 1 to 25 fF when using a back-end-of-line (BEOL; cf. *infra*) transistor.

[0042] In embodiments, the nanoelectrode may have a size (e.g. a width or diameter) of 1 μm or less, preferably 500 nm or less, more preferably 250 nm or less, yet more preferably 150 nm or less, such as 100 nm or less. In embodiments, the nanoelectrodes (e.g. the nanoelectrode array) may have a pitch (i.e. a centre-to-centre distance between adjacent nanoelectrodes) of 1 μm or less, preferably 500 nm or less, more preferably 250 nm or less, yet more preferably 150 nm or less, such as 100 nm or less. The currently most advanced DRAM nodes for example use a hexagonal lay-out (e.g. of the capacitors) with a pitch of about 30 nm, illustrating that the aforementioned dimensions are well within the current technological capabilities.

[0043] In embodiments, the access transistors and optionally the electrode cells as a whole may be formed on a semiconductor substrate (e.g. a Si, Ge, SiGe or semiconductor-on-insulator substrate). In embodiments, the access transistor may be a planar transistor (e.g. a planar field-effect transistor, planar FET) or a vertical transistor (e.g. a vertical FET, VFET). In embodiments, the access transistor may be a back end of line (BEOL) transistor; i.e. a transistor formed during the BEOL stage of semiconductor processing. The access transistor may for example be a thin film metal-oxide-semiconductor FET (MOSFET), such as based on an indium gallium zinc oxide (IGZO), polysilicon, 2D material (e.g. MoS_2 , MoSe_2 , MoTe_2 , WS_2 or WSe_2) thin film. The use of BEOL access transistors advantageously allows to dedicate the front end of line (FEOL) region below the electrode cell array for peripheral circuits (e.g. write drivers, refresh circuits and/or data transfers).

[0044] In embodiments, the array of electrode cells may count 30,000 electrode cells or more, preferably 100,000 or more, more preferably 250,000 or more, yet more preferably 1,000,000 or more, most preferably 10,000,000 or more, such as up to 16,000,000 or more. In embodiments, the array may have a size (e.g. a block size) in the order of 256 (e.g. along the wordline direction) by 128 (e.g. along the bitline direction) or more, preferably 1,024 by 256 or more, more preferably 16,384 by 1,024 or more. In embodiments, the system may comprise a plurality of electrode cell arrays. By having multiple electrode cell arrays which can be written simultaneously (i.e. akin to sub-banking in DRAM), the throughput at low energy can advantageously be improved. In embodiments, the system may count a total of 30,000 electrode cells or more, preferably 100,000 electrode cells or more, more preferably 1,000,000 or more, yet more preferably 10,000,000 or more, still yet more preferably

100,000,000 or more, most preferably 1,000,000,000 or more, such as up to 1,000,000,000,000 or more.

[0045] In embodiments, any feature of any embodiment of the first aspect may independently be as correspondingly described for any embodiment of any of the other aspects.

[0046] In a second aspect, the present invention relates to a use of a system as defined in any embodiment of the first aspect, for addressing nanoelectrodes in a nanoelectrode array.

[0047] In embodiments, the use may be for operating at least one of the nanoelectrodes potentiostatically, galvanostatically or galvanodynamically (cf. infra). In embodiments, the use may be for operating at least one of the nanoelectrodes potentiostatically, galvanostatically or galvanodynamically within a predetermined margin. Thus, the nanoelectrode may within the predetermined margin (i.e. plus or minus the margin) respectively be maintained at a constant potential, maintained at a constant current or its potential may be swept at a constant rate. The predetermined margin may be 30% or less, preferably 20% or less, more preferably 10%, yet more preferably 5% or less, most preferably 2% or less, such as 1% or less.

[0048] In embodiments, any feature of any embodiment of the second aspect may independently be as correspondingly described for any embodiment of any of the other aspects.

[0049] In a third aspect, the present invention relates to a method for addressing nanoelectrodes in a system according to any embodiment of the first aspect, comprising: (a) selecting a potential for each nanoelectrode, and (b) setting the selected potentials by, for each electrode cell, opening the access transistor by asserting the word line and charging the storage circuit to the selected electrode potential by aptly biasing the bit line.

[0050] In embodiments, step b may further comprise closing the access transistor after having charged the storage circuit. In embodiments, the access transistor may be closed before opening a further access transistor.

[0051] In embodiments, step b may comprise charging the storage circuit to the selected electrode potential by biasing the bit line to a potential (e.g. with respect to ground) of from -3 to 3 V, preferably from -2 to 2 V, such as from -1 to 1 V. In embodiments, the potential selected in step a and set in step b may differ for different nanoelectrode. The potential that can be selected and set is advantageously not limited to a discrete set of values (e.g. such as in a digital case), but can be essentially any of a continuous set of values (within the margins of experimental accuracy). This advantageously allows to select the potential based on the specific requirements for each nanoelectrode. For example, as a DNA strand is further expanded (cf. Example 4) away from the nanoelectrode, the generated H^+ concentration may need to rise in order to achieve the same deprotection efficiency on the further away protection group. As such, the degree to which the storage circuit is charged may need to be

raised in function of the length of the DNA strand. Moreover, different DNA strands across the array may have a different length, so that the optimal stored charge may differ from one storage circuit to the next. Moreover, the ideal potential for a nanoelectrode may depend on the state of the neighbouring cells. Such needs can advantageously be accommodated to within the present invention through changing the biasing potential and/or charging time used.

[0052] In embodiments, step b may comprise setting a plurality of the selected electrode potentials simultaneously by for a row of electrode cells linked by a common word line opening all access transistors by asserting the common word line and for each electrode cell in the row charging the storage circuit by aptly biasing the bit line. In embodiments, step b may further comprise closing all the access transistors in the row after having charged the storage circuits. In embodiments, the access transistors in the row may be closed before opening a further row of access transistors. Strategies akin to those that have been used to quickly write to a vast number of memory cells in DRAM can advantageously be used in the present invention to quickly (e.g. virtually simultaneously compared to the time frame of the chemical reactions that are being considered) address a large number of nanoelectrodes.

[0053] After having charged the storage circuit, the stored charge can be used to drive the nanoelectrode, e.g. to perform an electrochemical reaction. In doing so, the stored charge will typically be used over time. Moreover, even if not expended to drive an electrochemical reaction, the stored charge will typically (slowly; e.g. in the order of milliseconds) leak out of the storage circuit (e.g. through the reaction medium, transistor or capacitor) and thus anyway deplete overtime. Thus, after the storage circuit has been charged, the nanoelectrode will typically experience a potential profile which decays over time.

[0054] In embodiments, the method may comprise a further step c of: (c) refreshing the selected potentials by repeating step b. In embodiments, step c may comprise repeating step b periodically, such as periodically for a predetermined duration (e.g. for a duration needed to complete a chemical reaction). Refreshing the selected potentials advantageously allows to recover the decaying potential profile. In doing so, the experienced potential profile can be turned into a periodic function. Depending on the interplay between the characteristics of the storage circuit (e.g. its capacitance), the retention time/decay rate (as affected by actively using up the stored charge or through inevitable depletion) and the refresh rate (i.e. the duration between the start times of subsequent repetitions of step b) the amplitude of the periodic function can be made larger (e.g. corresponding to more pronounced potential pulses) or smaller (e.g. corresponding to an overall flatter potential profile). In embodiments, the refresh rate may from 5 to 500 ms, preferably from 20 to 250 ms, more preferably from 35 to 150

ms, yet more preferably from 40 to 100 ms, most preferably from 55 to 75 ms, such as 64 ms. The typical refresh rate for DRAM memory is for example 64 ms, so current refresh circuits are advantageously already adapted to such a refresh rate.

[0055] In step a, the potential for each nanoelectrode may typically be selected in function of the goal that is to be achieved for that nanoelectrode. This goal may for example include whether the nanoelectrode is to be set active, neutral or counteractive (cf. *infra*); but it can also include how the nanoelectrode is to be controlled, for example potentiostatically (i.e. aiming to maintain the nanoelectrode at a constant potential), galvanostatically (i.e. aiming to maintain the nanoelectrode at a constant current) or potentiodynamically (e.g. aiming to sweep the nanoelectrode's potential at a constant rate). Operating the nanoelectrode at a constant potential within a predetermined margin (cf. *supra*) can for example be achieved by refreshing the set potential before it has decayed (cf. *supra*) below this margin. Operating the nanoelectrode at a constant current again within a predetermined margin may be achieved using a comparable strategy, through an adaptive refresh. Here it may not suffice to simply set the potential back to the previously set value, but rather the storage circuit should be charged in function of the charge that has been expended since the previous set action; meaning that the potential to be set may need to be adapted for each refresh. This can for example be achieved by first reading out the remaining charge (remaining potential) through the bit line at the start of the refresh and determining therefrom the new potential that is to be set in order to maintain a (relatively) constant current. Another strategy to operate the nanoelectrode at a constant current within a predetermined margin is to make use of capacitive charge injection through the capacitor (if present), by connecting the capacitor's second terminal to an inject line. In that case, a linear voltage ramp on the inject line will for example result in a fixed charge influx into the storage circuit. For nanoelectrodes set to active (e.g. set to a high potential), depending on the specific parameters chosen a balance between incoming and outgoing charge can be achieved, resulting in a relatively constant current. For nanoelectrodes set to inactive (e.g. set to a low potential), the incoming charge will charge the storage circuit, but as long as the potential thereby developed is lower than needed to drive the reaction, this reaction will not be enabled. During a refresh, this built-up charge can then again be released through the word line, so that the inactive nanoelectrodes can be kept inactive by using a suitable refresh rate. In embodiments, these strategies for maintaining a (relatively) constant current can also advantageously be combined.

[0056] In embodiments, step b may comprise setting the nanoelectrode to be active, neutral or counteractive. 'Active', 'neutral' and 'counteractive' here refer to the electrochemical activity of the nanoelectrode: an active electrode has a suitable potential for bringing about a

particular electrochemical reaction, a counteractive electrode has a suitable potential for bringing about a different reaction (e.g. the opposite reaction, in so far as the electrochemical reaction is reversible) and an inactive electrode has an intermediate potential which is neither sufficient to bring about the particular electrochemical reaction nor its opposite. In embodiments, step a may comprise selecting more negative potentials for the nanoelectrodes which are to be active, and intermediate potentials for the nanoelectrodes which are to be inactive and/or more positive potentials for the nanoelectrodes which are to be counteractive. In other embodiments, step a may comprise selecting more positive potentials for the nanoelectrodes which are to be active, and intermediate potentials for the nanoelectrodes which are to be inactive and/or more negative potentials for the nanoelectrodes which are to be counteractive. In the above, rather than referring to absolute values, the potentials are expressed relative to one another. Indeed, the specific potential values will i.a. typically depend on the reference point that is selected (e.g. ground or a counter-electrode contacting the reaction medium). As such, a 'more negative' potential may in some instances still be positive, etc. Regardless of the reference point selected however, suitable potentials for setting a nanoelectrode to active, inactive or counteractive for a particular electrochemical reaction can typically be calculated (e.g. based theory and modelling) or can be derived by relatively simple and straightforward trial-and-error.

[0057] In embodiments, any feature of any embodiment of the third aspect may independently be as correspondingly described for any embodiment of any of the other aspects.

[0058] In a fourth aspect, the present invention relates to a method for synthesizing a molecule, comprising: (a) setting the potential of one or more nanoelectrodes using the method according to any embodiment of the third aspect, and (b) contacting one or more reagents to the nanoelectrodes; thereby locally generating reaction conditions for mediating the synthesis.

[0059] Synthesizing the molecule may typically be performed in a reaction medium; such as a fluid (e.g. a liquid or gas). In embodiments, the reaction medium may contact the nanoelectrodes. In embodiments, the reaction medium may comprise the one or more reagents. In embodiments, the method may further comprise contacting a counter-electrode to the reaction medium.

[0060] In embodiments, the molecule to be synthesized may be a molecule, such as a biomolecule; e.g. a biopolymer such as (synthetic) DNA. In embodiments, the method may be for forming a DNA data storage (i.e. a data storage system in which data is encoded in DNA) or for spatial transcriptomics, preferably DNA data storage.

[0061] In embodiments, the step b may be started before, together with or after starting step a. In embodiments, step a and step b may at least partially overlap in time. In other words, regardless of which step is per-

formed first, the nanoelectrodes are most commonly (still) at a certain potential when the reagents are (still) in contact with the nanoelectrodes.

[0062] In embodiments, mediating the synthesis may comprise locally enabling or disabling the synthesis. In embodiments, mediating the synthesis may comprise directly or indirectly mediating the synthesis. Most often, at least one of the contacted reagents may directly interact-undergo an electrochemical oxidation or reduction-with charges of an (active or counteractive) nanoelectrode, thereby yielding a change in reaction conditions (e.g. a change in the concentration of an active species, such as an electrochemical reagent or reaction product). Here, 'direct interaction with charges of the nanoelectrode' may comprise interaction at the nanoelectrode surface as such or away from said surface with charges having migrated through the reaction medium. Regardless, based on the altered reaction conditions, one or more further chemical reactions e.g. involving the reagents or reaction products of the first reaction and/or one or more further reagents may then be enabled or disabled. Such further reagents may be added together with the initial electrochemically active reagent or may added at a later stage. To name but one example of indirect mediation, the generated reaction conditions (e.g. a lowered pH) may lead to deprotection of a reagent (e.g. a DNA strand) by removal of a protective group and then in turn further enable a synthetic reaction between the deprotected reagent (e.g. DNA synthesis) and one or more further reagents (e.g. a nucleotide).

[0063] In embodiments, the generated reaction conditions in step b may comprise a change in pH (e.g. by generating protons through the oxidation of hydroquinone or consumption of protons through the reduction of benzoquinone), generation of free radicals (e.g. by an electrochemically produced from persulfates), the generation of Cu-ions (e.g. for click chemistry) or the generation of divalent cations (e.g. to control an enzymatic reaction).

[0064] In embodiments, the method may further comprise a step c of: (c) withdrawing (e.g. washing away) one or more of the reagents. In embodiments, the method may comprise repeating a sequence of steps a, b and optionally c. In embodiments, the sequence of steps may be repeated an arbitrary number of times (cf. Example 4).

[0065] In embodiments, any feature of any embodiment of the fourth aspect may independently be as correspondingly described for any embodiment of any of the other aspects.

[0066] The invention will now be described by a detailed description of several embodiments of the invention. It is clear that other embodiments of the invention can be configured according to the knowledge of the person skilled in the art without departing from the true technical teaching of the invention, the invention being limited only by the terms of the appended claims.

Example 1: Array with physical confinement of the reaction conditions

[0067] We now refer to FIG 1, depicting a 3D view of an array for molecular synthesis in which the reaction conditions are confined by physical means. To that end, the array comprises a nanoelectrode array (20) on a substrate (10) and a perforated cover layer (40) over the nanoelectrode array (20). The perforated cover layer (40) comprises cavities (51) which overlay and open up the nanoelectrodes (30) at the bottom thereof. As such, each cavity (51) forms a synthesis cell (50) in which the walls that define it hinder diffusion of the reaction medium from one synthesis cell (50) to the next, thereby locally confining the reaction medium and thus the reaction conditions. One or more counter electrodes (not depicted), for example arranged in a counter electrode array, are also typically present. These may for example be situated above the nanoelectrode array (20) (e.g. atop the perforated cover layer (40) or further above) in which case they may e.g. be parallel with nanoelectrodes (30) or coplanar with the electrode array (20). Each nanoelectrode (30) is then typically associated with a counter electrode although it is not excluded that one counter electrode may be associated with a plurality of nanoelectrodes (30) and the electric potential difference developed between both of these governs the electrochemical reaction in the synthesis cell (50).

[0068] This is also illustrated in FIG 2, where two active nanoelectrodes (31) are shown to electrochemically oxidize hydroquinone (HQ) to benzoquinone (BQ), thereby producing protons (H^+) and locally lowering the pH. Migration of the protons and other reaction products outside the synthesis cell (50) in which they are formed is however hindered by the walls of the perforated cover layer (40), so that they remain localized to the synthesis cell (50). Accordingly, a change in pH is not observed in the right-most synthesis cell (51), where the corresponding nanoelectrode (32) is inactive. This allows to control through setting the nanoelectrode (31, 32) the reaction conditions (e.g. pH) in each synthesis cell (50) individually, thereby across the array managing where a reaction is enabled and where it is disabled.

[0069] FIG 2 also shows more details of the electrode cells (60) with which the nanoelectrodes (31, 32) are addressed. Each electrode cell (60) comprises a storage circuit (80) with the corresponding nanoelectrode (31, 32) and an access transistor (70) with a gate, a source and a drain. Each nanoelectrode (31, 32) is then addressable through controlling the corresponding access transistor (70) in its electrode cell (60). More in particular, the potential of each nanoelectrode (31, 32) can be individually set by asserting the corresponding word line (71) to open the access transistor (70) and biasing the corresponding bit line (72) to charge the storage circuit (80). After disconnecting the access transistor (70), the charge stored the storage circuit (80) can then be ('slowly') used by the nanoelectrode (31, 32), e.g. to drive an electro-

chemical reaction. Moreover, even if not expended to drive an electrochemical reaction, slow e.g. in the order of (tens of) milliseconds depletion of the stored charge will typically occur; e.g. because of unavoidable leaks (cf. supra). Since the reaction time may typically be in the order of a fraction of a second to several seconds, the duration over which one may wish to maintain the potential will typically be longer than the retention/depletion time of the storage circuit (80). To remedy this, the nanoelectrodes (31, 32) can be periodically rewritten (i.e. re-set or recharged), thereby extending their duration (see also Example 3).

[0070] The storage circuit (80) depicted in FIG 2 comprises a capacitor (81) of which one terminal is resistively coupled to both the drain and the nanoelectrode (31, 32). However, a separate capacitor (81) isn't strictly required and a sufficient storage capacitance in the storage circuit (80) could be achieved based on parasitic capacitance (e.g. wire capacitance) of the storage circuit (80) as such and/or a capacitor (81) formed about the electrical connection coupling the drain to the nanoelectrode (31, 32).

Example 2: Array with electrochemical confinement of the reaction conditions

[0071] FIG 3 depicts a similar 3D view as FIG 1, but for an array in which confinement is achieved electrochemically. The array shown in FIG 3 differs from the one in FIG 1 in that it doesn't comprise the perforated cover layer (40). Instead, as illustrated in FIG 4, confinement is achieved by setting the nanoelectrodes (33) surrounding the active nanoelectrodes (31) to be counteractive, so that the opposite reaction occurs there. In the example shown in FIG 4, protons are generated by oxidizing hydroquinone to benzoquinone at the active nanoelectrode (31) and are consumed near the counteractive nanoelectrodes (33) in the reduction of benzoquinone back to hydroquinone. Thus, as the produced protons start to diffuse away from the active nanoelectrodes (31), they are consumed at the surrounding counteractive nanoelectrodes (33), thereby even in the absence of physical boundaries still confining the reaction conditions to the desired synthesis cells (50).

[0072] Surrounding of active nanoelectrodes (31) by counteractive nanoelectrodes (33) in a cubically packed array is also illustrated in the top views of FIG 5, FIG 6 and FIG 7. FIG 5 shows a single active nanoelectrode (31) surrounded by eight counteractive nanoelectrodes (33). However, as shown in FIG 6, it may in embodiments be sufficient to set only the four immediately closest nanoelectrodes (33) to counteractive and to have the further nanoelectrodes (32) kept inactive. FIG 7 illustrates a further situation in which two neighbouring nanoelectrodes (31) are set to be active, the nanoelectrodes (33) surrounding the active nanoelectrodes (31) are set to be counteractive and the nanoelectrode (32) which is not active and not next to an active nanoelectrode (31) are set to be inactive.

[0073] The above notwithstanding, it will be clear that the cubic packing shown here is only illustrative and that other arrangements (e.g. a hexagonal packing) of the array can likewise envisioned.

Example 3: Array of electrode cells

[0074] We now refer to FIG 8, which schematically depicts an array of electrode cells (60), each electrode cell (60) comprising a storage circuit (80) with a corresponding nanoelectrode (30) and an access transistor (70). The electrode cells (60) are arranged in rows and columns, wherein the electrode cells (60) in a row are linked by a common word line (71) and in a column by a common bit line (72). The word lines (71) are coupled to a row address selector (91), while the bit lines (72) are coupled to a column address selector (92). Note however that the electrode cell array is again not limited to a cubic packing and that other arrangements (e.g. hexagonal packing) can likewise envisioned.

[0075] Akin to the operation of DRAM memory, setting the potential of the nanoelectrodes (30) may be performed through opening all access transistors (70) in a row by asserting the common word line (71) and, for each electrode cell (60) in the row, charging the storage circuit (80) by correspondingly biasing the associated bit line (72).

[0076] In order to maintain the potential for an extended duration (e.g. several seconds), the nanoelectrodes (30) can be periodically rewritten (i.e. re-set or recharged); not unlike a periodic memory refresh in DRAM. Note however that in the present invention, the stored charge in the storage circuit (80) will typically be used up (e.g. in electrochemical reactions) or will otherwise dissipate (e.g. through the reaction medium) over time. As such, contrary to a DRAM refresh, it may not be possible to read the potential to be set back out prior to rewriting it and that information may need to be retrieved or maintained elsewhere (e.g. the selected potential for each nanoelectrode may need to be stored separately for as long as this information is still needed).

[0077] Likewise, other strategies used to improve the operation of DRAM memory can also be used in the context of the present invention. For example, the system may comprise multiple arrays in a sub-banked arrangement, so that the arrays can be (re)written at the same time, thereby improving the throughput at low energy.

Example 4: Using a system in accordance with the present invention in biological synthesis

[0078] An array such as for example described in Example 1 and Example 2, may for instance be used in the synthesis of (synthetic) DNA or another (bio)molecule. A method for expanding one or more protected DNA strands may for example start with providing the protected DNA strand(s) in the synthesis cells over the nanoelectrodes (e.g. one strand per synthesis cell). Next, one

or more reagents for in combination with an active nanoelectrode deprotecting the DNA strands may be provided in the reaction medium (e.g. a proton-generation agent, such hydroquinone, for the acid-based deprotection). A number of nanoelectrodes where a particular nucleotide is to be added can then be selected and the nanoelectrodes in the nanoelectrode array can be set accordingly (e.g. the corresponding nanoelectrodes can be activated and e.g. in an array such as described in Example 2 the surrounding nanoelectrodes can be set to be counteractive). By doing so, the deprotection reaction is locally enabled and specifically the selected DNA strands can be deprotected, while leaving the other DNA strands protected. A derivative of the nucleotide e.g. bearing a further protective group can then be brought into the reaction medium and be reacted with the deprotected strands, resulting in selectively expanded strands which again bear a protective group. After washing away the nucleotide derivative, the procedure can be restarted e.g. in order to add another nucleotide to the DNA strand(s) and it can be repeated an arbitrary number of times to yield DNA strands with an arbitrary sequence. Note in particular that, since the strands to be expanded can be selected in every instance of the procedure, the sequence of DNA strands need not be the same. Indeed, the DNA strand above each nanoelectrode may have a unique sequence. As such, the array can be used to make a DNA data storage.

[0079] It is to be understood that although preferred embodiments, specific constructions and configurations, as well as materials, have been discussed herein for devices according to the present invention, various changes or modifications in form and detail may be made without departing from the scope and technical teachings of this invention. For example, any formulas given above are merely representative of procedures that may be used. Functionality may be added or deleted from the block diagrams and operations may be interchanged among functional blocks. Steps may be added or deleted to methods described within the scope of the present invention.

Claims

1. A system for addressing nanoelectrodes (30-33) in a nanoelectrode array (20), the system comprising an array of electrode cells, each electrode cell (60) comprising:

i. an access transistor (70) having

- a gate resistively coupled to a word line (71),
- a source resistively coupled to a bit line (72), and
- a drain; and

ii. a storage circuit (80) resistively coupled to the drain and comprising a nanoelectrode (30-33).

2. The system according to claim 1, wherein the array of electrode cells (60) comprises

- one or more rows, the electrode cells (60) in a row being linked by a common word line (71), and/or
- one or more columns, the electrode cells (60) in a column being linked by a common bit line (72).

3. The system according to any of the previous claims, wherein the storage circuit (80) comprises the nanoelectrode (30-33) and an electrical connection resistively coupling the nanoelectrode (30-33) to the drain.

4. The system according to any of the previous claims, wherein the storage circuit (80) further comprises a capacitor (81).

5. The system according to claim 4, wherein the capacitor (81) has a terminal resistively coupled to both the drain and the nanoelectrode (30-33).

6. The system according to any of the previous claims, wherein the storage circuit (80) has a capacitance of at least 0.01 fF, preferably at least 1 fF, more preferably at least 10 fF, yet more preferably at least 25 fF.

7. The system according to any of the previous claims, wherein the array of electrode cells counts 30,000 electrode cells (60) or more, preferably 100,000 or more, more preferably 250,000 or more, yet more preferably 1,000,000 or more, most preferably 10,000,000 or more.

8. The system according to any of the previous claims, wherein the access transistor is a back end of line (BEOL) transistor.

9. Use of a system as defined in any of the previous claims, for addressing nanoelectrodes (30-33) in a nanoelectrode array (20).

10. The use according to claim 9, for operating at least one of the nanoelectrodes potentiostatically or galvanostatically.

11. A method for addressing nanoelectrodes (30-33) in a system as defined in any of claims 1 to 8, comprising:

- a. selecting a potential for each nanoelectrode (30-33), and

b. setting the selected potentials by, for each electrode cell (60),

- opening the access transistor (70) by asserting the word line (71) and 5
- charging the storage circuit (80) to the selected electrode potential by aptly biasing the bit line (72).

12. The method according to any of claim 11, wherein step b comprises setting a plurality of the selected electrode potentials simultaneously by, 10

- for a row of electrode cells (60) linked by a common word line (71), opening all access transistors (70) by asserting the common word line (71) and, 15
- for each electrode cell (60) in the row, charging the storage circuit (80) by aptly biasing the bit line (72). 20

13. The method according to any of claims 11 to 12, comprising a further step c of:
c. refreshing the selected potentials by repeating step b. 25

14. A method for synthesizing a molecule, comprising:

- a. setting the potential of one or more nanoelectrodes (30-33) using the method according to any of claims 11 to 13, and 30
- b. contacting one or more reagents to the nanoelectrodes (30-33);

thereby locally generating reaction conditions for mediating the synthesis. 35

15. The method according to claim 14, for forming a DNA data storage. 40

45

50

55

60

65

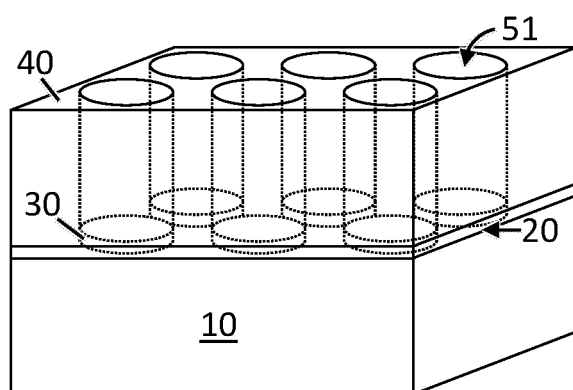


FIG 1

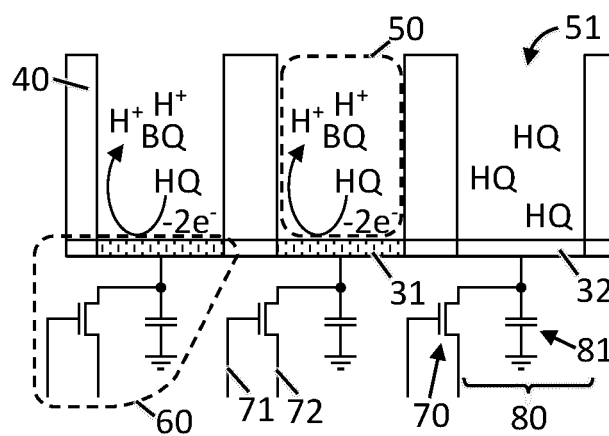


FIG 2

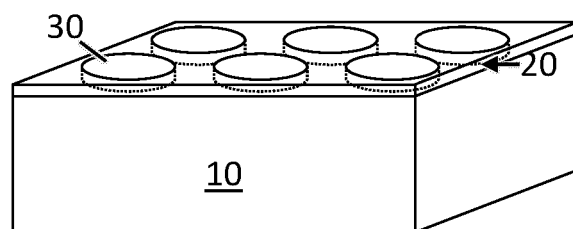


FIG 3

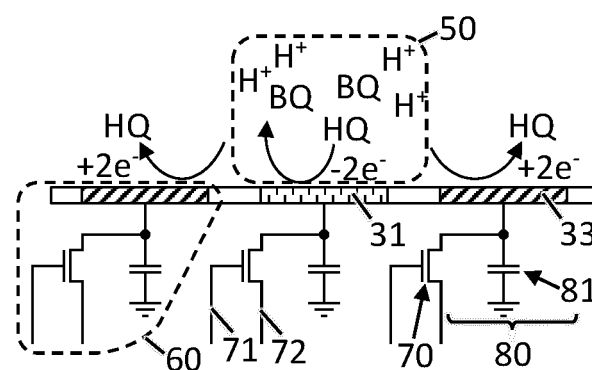


FIG 4

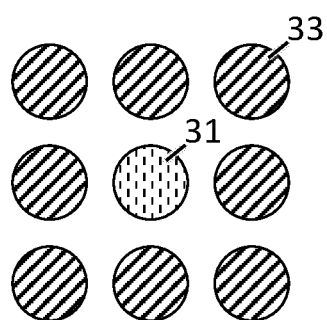


FIG 5

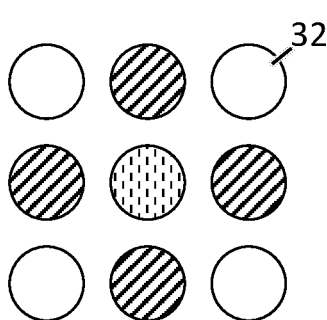


FIG 6

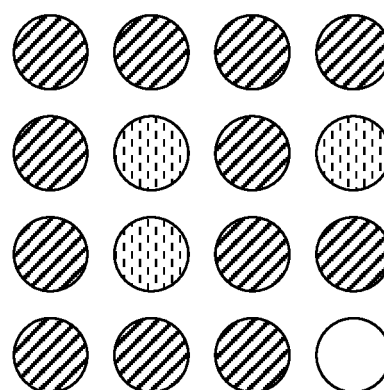


FIG 7

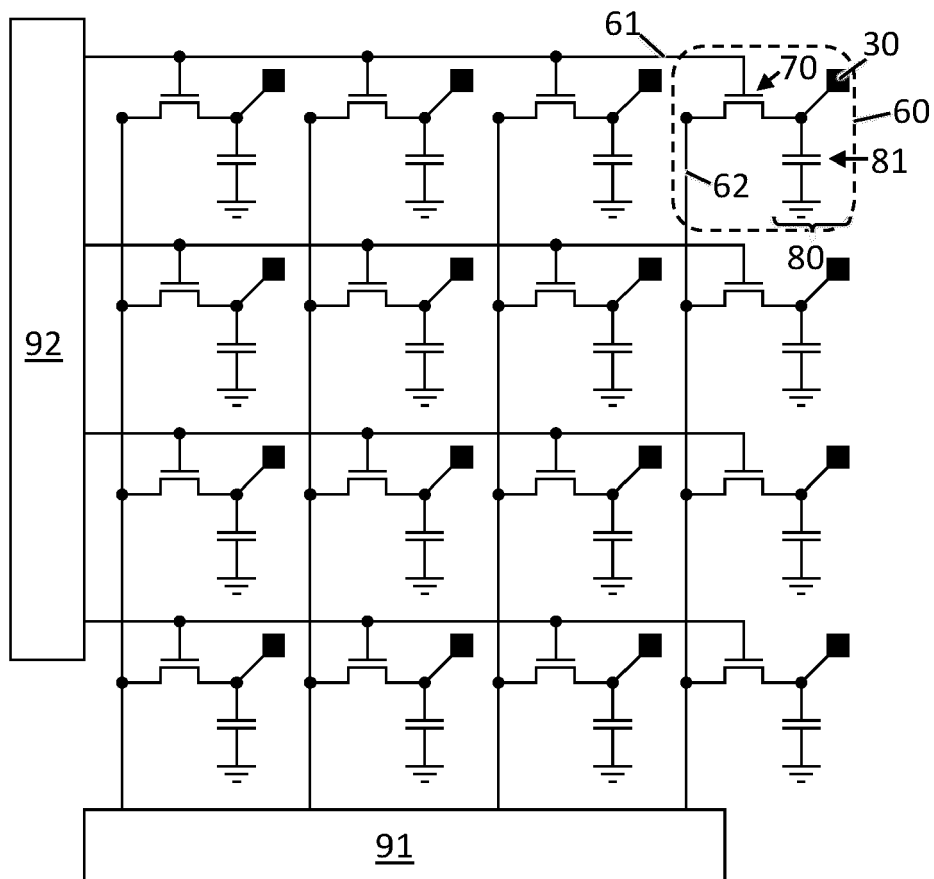


FIG 8



EUROPEAN SEARCH REPORT

Application Number
EP 20 16 7573

5

10

15

20

25

30

35

40

45

50

55

1

EPO FORM 1503 03.82 (P04C01)

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2010/052080 A1 (GARCIA TELLO PABLO [BE] ET AL) 4 March 2010 (2010-03-04) * paragraph [0030] - paragraph [0032] * * paragraph [0056] - paragraph [0061]; figure 1 * * paragraph [0072] - paragraph [0073]; figure 2 *	1,6,7, 9-13,15	INV. B01J19/00 G11C13/00
X	US 2002/029971 A1 (KOVACS GREGORY T A [US]) 14 March 2002 (2002-03-14) * paragraph [0002] - paragraph [0006] * * paragraph [0034]; figure 3 * * paragraph [0035]; figure 4a *	1-5,9, 11,14	
A,D	US 2006/231411 A1 (MAURER KARL [US] ET AL) 19 October 2006 (2006-10-19) * the whole document *	1-15	
			TECHNICAL FIELDS SEARCHED (IPC)
			B01J C40B G11C
The present search report has been drawn up for all claims			
Place of search The Hague		Date of completion of the search 30 September 2020	Examiner Knack, Steffen
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 20 16 7573

5 This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

30-09-2020

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010052080 A1	04-03-2010	CN 101669025 A	10-03-2010
		EP 2140256 A2	06-01-2010
		JP 5027296 B2	19-09-2012
		JP 2010525360 A	22-07-2010
		TW 200907337 A	16-02-2009
		US 2010052080 A1	04-03-2010
		WO 2008132656 A2	06-11-2008

US 2002029971 A1	14-03-2002	AU 722148 B2	20-07-2000
		BR 9710271 A	10-08-1999
		CA 2259406 A1	15-01-1998
		CN 1255197 A	31-05-2000
		EP 0920624 A1	09-06-1999
		JP 2001525921 A	11-12-2001
		KR 20000023659 A	25-04-2000
		NZ 333947 A	24-11-2000
		US 5965452 A	12-10-1999
		US 6258606 B1	10-07-2001
		US 2002029971 A1	14-03-2002
		US 2002127733 A1	12-09-2002
		US 2002131899 A1	19-09-2002
		US 2004149582 A1	05-08-2004
		US 2005155863 A1	21-07-2005
		US 2007095671 A1	03-05-2007
		WO 9801758 A1	15-01-1998

US 2006231411 A1	19-10-2006	AU 2006236516 A1	26-10-2006
		EP 1885914 A2	13-02-2008
		KR 20080007609 A	22-01-2008
		US 2006231411 A1	19-10-2006
		US 2016354751 A1	08-12-2016
		US 2020086290 A1	19-03-2020
WO 2006113554 A2	26-10-2006		

ORM P0459

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- US 20160354751 A1 [0003] [0004] [0006]