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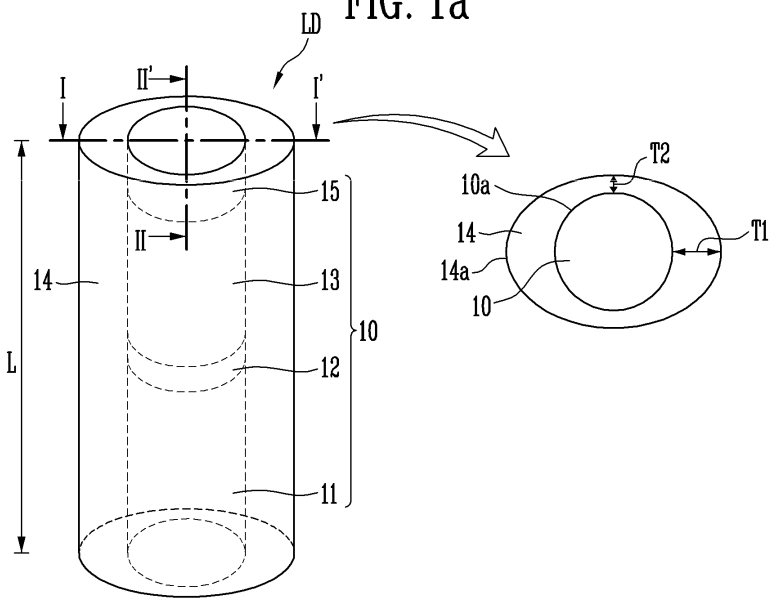
(54) LIGHT-EMITTING ELEMENT, MANUFACTURING METHOD THEREFOR, AND DISPLAY DEVICE HAVING LIGHT-EMITTING ELEMENT

(57) A light emitting element may include a rod-shaped emission stacked pattern including a first conductive semiconductor layer, an active layer disposed on the first conductive semiconductor layer, and a second conductive semiconductor layer disposed on the active layer; and an insulating film surrounding an outer surface of the emission stacked pattern, and having a non-uniform thickness.

FIG. 1a



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Description

Technical Field

[0001] Various embodiments of the present disclosure relate to a light emitting element, and more particularly, to a subminiature light emitting element, a method of manufacturing the light emitting element, and a display device including the light emitting element.

Background Art

[0002] A light emitting diode (LED) may have relatively satisfactory durability even under poor environmental conditions, and have excellent performances in terms of lifetime and luminance. Recently, research on the technology of applying such LEDs to various display devices has become appreciably more active.

[0003] As a part of such research, technologies of fabricating an LED having a small size corresponding to a size ranging from a nanometer scale to a micrometer scale using an inorganic crystalline structure, e.g., a structure obtained by growing a nitride-based semiconductor are being developed.

[0004] LEDs may be fabricated in a small size enough to form a pixel of a display panel, etc. After the LEDs are independently grown on a substrate, the grown LEDs may be separated and used to manufacture the display panel.

Disclosure

Technical Problem

[0005] Various embodiments of the present disclosure are directed to a light emitting element configured to prevent adjacent light emitting elements from being agglomerated, a method of manufacturing the light emitting element, and a display device including the light emitting element.

Technical Solution

[0006] According to an aspect of the present disclosure, a light emitting element may include a rod-shaped emission stacked pattern including a first conductive semiconductor layer, an active layer disposed on the first conductive semiconductor layer, and a second conductive semiconductor layer disposed on the active layer; and an insulating film configured to surround an outer surface of the emission stacked pattern, and having a non-uniform thickness.

[0007] The outer surface of the emission stacked pattern may be different in shape from an outer surface of the insulating film.

[0008] The emission stacked pattern may have a shape of a cylinder formed by sequentially stacking the first conductive semiconductor layer, the active layer, and the second conductive semiconductor layer in a first direction, and the outer surface of the insulating film may have an elliptical shape, a polygonal shape, and a shape in which the elliptical shape and the polygonal shape are mixed.

[0009] The outer surface of the insulating film may include at least one protrusion.

[0010] The outer surface of the emission stacked pattern may be equal in shape to an outer surface of the insulating film.

[0011] The outer surface of the emission stacked pattern and the outer surface of the insulating film each may have a polygonal shape.

[0012] According to an aspect of the present disclosure, a method of manufacturing a light emitting element may include providing a substrate; forming a rod-shaped emission stacked pattern on the substrate; forming an insulating film surrounding an outer surface of the emission stacked pattern and having a non-uniform thickness; and separating the emission stacked pattern, the emission stacked pattern being surrounded by the insulating film, from the substrate to form light emitting elements.

[0013] Forming the insulating film may include forming an insulating film pattern having an outer surface that has the same shape as the outer surface of the emission stacked pattern; and forming an insulating film having an outer surface that is different in shape from the outer surface of the emission stacked pattern by removing at least a portion of the insulating film pattern.

[0014] In forming the insulating film, the insulating film may be formed to have an outer surface having an elliptical shape, a polygonal shape or a shape in which the elliptical shape and the polygonal shape are mixed to surround a cylindrical outer surface of the emission stacked pattern.

[0015] In forming the insulating film, the outer surface of the insulating film may include at least one protrusion.

[0016] Forming the emission stacked pattern may include forming an emission stack on the substrate, the emission stack being formed by sequentially forming a first conductive semiconductor layer, an active layer, and a second conductive semiconductor layer; forming a plurality of first micro patterns on the emission stack; and forming a plurality of emission stacked patterns by etching the emission stack along the plurality of first micro patterns and removing the plurality of first micro patterns.

[0017] Forming the plurality of first micro patterns may include forming a plurality of first resins on the emission stack; providing the first resins to fill a plurality of first grooves of a first mold; and forming the plurality of first micro patterns on the emission stack, by removing the first mold.

[0018] Forming the insulating film may include forming a plurality of second micro patterns on the emission stacked pattern and the insulating film pattern; and forming the insulating film by etching the insulating film pattern along the plurality of second micro patterns.

[0019] Forming the plurality of second micro patterns

may include forming a plurality of second reins on the emission stacked pattern and the insulating film pattern that surrounds the outer surface of the emission stacked pattern; causing the second resins to fill a plurality of second grooves of a second mold; and forming a plurality of second micro patterns on the emission stacked pattern and the insulating film pattern that surrounds the outer surface of the emission stacked pattern, by removing the second mold.

[0020] A shape of the first groove of the first mold may be different from a shape of the second groove of the second mold.

[0021] In forming the insulating film, the insulating film may be formed to have the outer surface that is the same as the outer surface of the emission stacked pattern.

[0022] The outer surface of each of the emission stacked pattern and the insulating film may be formed to have a polygonal shape.

[0023] According to an aspect of the present disclosure, a display device may include a substrate including a display area and a non-display area; and a plurality of pixels provided in the display area of the substrate, and including a plurality of sub-pixels, respectively, wherein each of the sub-pixels may include a pixel circuit layer including at least one transistor, and a display element layer including an unit emission area that emits light, wherein the display element layer may include at least one light emitting element provided on the substrate and configured to emitt light, first electrode and second electrode spaced apart from each other by a predetermined distance with the light emitting element being interposed therebetween, a first contact electrode electrically coupling the first electrode and a first end of the light emitting element, and a second contact electrode electrically coupling the second electrode and a second end of the light emitting element, and wherein the light emitting element may include an emission stacked pattern including a first conductive semiconductor layer, an active layer disposed on the first conductive semiconductor layer, and a second conductive semiconductor layer disposed on the active layer; and an insulating film surrounding an outer surface of the emission stacked pattern, and having a non-uniform thickness.

[0024] The outer surface of the emission stacked pattern is different in shape from an outer surface of the insulating film.

Advantageous Effects

[0025] A light emitting element of the present disclosure includes an emission stacked pattern, and an insulating film which surrounds the outer surface of the emission stacked pattern and has a non-uniform thickness, thus preventing adjacent light emitting elements from being agglomerated.

[0026] Therefore, it is possible to prevent deterioration in light-emitting characteristics of a display device including the light emitting element of the present disclosure.

Description of Drawings

[0027]

FIG. 1a is a perspective view of a light emitting element in accordance with an embodiment of the present disclosure.

FIG. 1b is a sectional view taken along line I-I of FIG. 1a.

FIG. 1c is a sectional view taken along line II-II of FIG. 1a.

FIGS. 2a to 2d are perspective views of a light emitting element in accordance with another embodiment of the present disclosure.

FIGS. 3a to 3c are perspective views of a light emitting element in accordance with a further embodiment of the present disclosure.

FIGS. 4a to 4o are sectional views illustrating a method of manufacturing the light emitting element of FIG. 1a.

FIG. 5a is a perspective view of a first mold shown in FIG. 4d.

FIG. 5b is a plan view of the first mold of FIG. 5a when seen from below.

FIG. 6a is a perspective view of a second mold shown in FIG. 4k.

FIG. 6b is a plan view of the second mold of FIG. 6a when seen from below.

FIGS. 7a to 7g are diagrams illustrating various shapes of a second groove shown in FIG. 6b.

FIGS. 8a and 8b are perspective views of a light emitting element in accordance with another embodiment of the present disclosure.

FIG. 9 is a schematic plan view illustrating a display device in accordance with an embodiment of the present disclosure, in which the display device uses the light emitting element shown in FIG. 1a as a light emitting source.

FIGS. 10a to 10c are circuit diagrams illustrating various embodiments of a unit emission area of the display device of FIG. 9.

FIG. 11 is a plan view schematically illustrating first to third sub-pixels included in one pixel among pixels shown in FIG. 9.

FIG. 12a is a sectional view taken along line III-III of FIG. 11.

FIG. 12b is a sectional view taken along line IV-IV of FIG. 11.

FIGS. 13a and 13b are sectional views taken along line IV-IV of FIG. 11 including a light emitting element in accordance with another embodiment of the present disclosure.

Mode for Invention

[0028] Like components will be designated by like reference symbols. Furthermore, it should be noted that the drawings may be exaggerated in thickness, ratio, and

dimension of components for descriptive convenience and clarity only. The term "and/or" includes any and all combinations of one or more of the associated listed items.

[0029] It will be understood that, although the terms "first", "second", etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another element. For instance, a first element discussed below could be termed a second element without departing from the teachings of the present disclosure. Similarly, the second element could also be termed the first element. In the present disclosure, the singular forms are intended to include the plural forms as well, unless the context clearly indicates otherwise.

[0030] Also, the terms "under" , "below", "above", "upper", and the like are used herein for explaining relationship between one or more components illustrated in the drawings. These terms may be relative terms describing the positions of components in the drawings, but the positions of components are not limited thereto.

[0031] It will be further understood that the terms "comprise", "include", "have", etc. when used in this specification, specify the presence of stated features, integers, steps, operations, elements, components, and/or combinations of them but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or combinations thereof.

[0032] FIG. 1a is a perspective view of a light emitting element in accordance with an embodiment of the present disclosure when seen from above. FIG. 1b is a sectional view taken along line I-I of FIG. 1a, and FIG. 1c is a sectional view taken along line II-II of FIG. 1a.

[0033] As shown in FIGS. 1a, 1b, and 1c, the light emitting element LD in accordance with the embodiment of the present disclosure includes an emission stacked pattern 10, and an insulating film 14 which covers an outer surface 10a of the emission stacked pattern 10. Here, the emission stacked pattern 10 may be formed in a cylindrical shape, and the insulating film 14 is not uniform in thickness. To this end, the shape of the outer surface 10a of the emission stacked pattern 10 may be different from the shape of an outer surface 14a of the insulating film 14.

[0034] The emission stacked pattern 10 may include a first conductive semiconductor layer 11, an active layer 12, and a second conductive semiconductor layer 13. The emission stacked pattern 10 may include a stacked structure formed by successively stacking the first conductive semiconductor layer 11, the active layer 12, and the second conductive semiconductor layer 13 in a longitudinal direction L of the light emitting element LD. The light emitting element LD including the above-described emission stacked pattern 10 may be provided in the shape of a rod extending in one direction. The rod shape embraces a rod-like shape or a bar-like shape extending in the longitudinal direction L (i.e., to have an aspect ratio greater than 1).

[0035] The emission stacked pattern 10 may have a rod shape formed by successively stacking the first conductive semiconductor layer 11, the active layer 12, and the second conductive semiconductor layer 13 in the longitudinal direction L of the light emitting element LD, and may have a first end and a second end with respect to the active layer 12. One of the first conductive semiconductor layer 11 or the second conductive semiconductor layer 13 may be disposed on the first end of the emission stacked pattern 10, while the remaining one may be disposed on the second end of the emission stacked pattern 10.

[0036] The light emitting element LD may have a small size corresponding to a size ranging from a nanometer scale to a micrometer scale, for example, the diameter and/or length ranging from the nanometer scale to the micrometer scale. However, in the present disclosure, the size of the light emitting element LD is not limited thereto. For example, the size of the light emitting element LD may be changed in various ways depending on design conditions of various devices, e.g., a display device, which employs, as a light source, a light emitting device using the light emitting element LD.

[0037] The first conductive semiconductor layer 11 may include, for example, at least one n-type semiconductor layer. For instance, the first conductive semiconductor layer 11 may include an n-type semiconductor layer which includes any one semiconductor material of InAlGaN, GaN, AlGaN, InGaN, AlN, and InN, and is doped with a first conductive dopant such as Si, Ge, or Sn. However, the material forming the first conductive semiconductor layer 11 is not limited to this, and the first conductive semiconductor layer 11 may be formed of various other materials.

[0038] The active layer 12 may be formed in a single or multi quantum well structure. Although not shown in the drawings, a cladding layer (not shown) doped with the conductive dopant may be further formed on and/or under the active layer 12. For example, the cladding layer may be formed of an AlGaN layer or an InAlGaN layer. A material such as AlGaN or AlInGaN may be used to form the active layer 12, and various other materials may be used to form the active layer 12.

[0039] The second conductive semiconductor layer 13 may include a semiconductor layer of a type different from that of the first conductive semiconductor layer 11. For example, the second conductive semiconductor layer 13 may include at least one p-type semiconductor layer. For instance, the second conductive semiconductor layer 13 may include a p-type semiconductor layer which includes at least one semiconductor material of InAlGaN, GaN, AlGaN, InGaN, AlN, and InN, and is doped with a second conductive dopant such as Mg. However, the material forming the second conductive semiconductor layer 13 is not limited to this, and the second conductive semiconductor layer 13 may be formed of various other ma-

terials.

[0040] An electrode layer 15 may be further disposed on the first end of the emission stacked pattern 10. In the drawing, the electrode 15 is disposed on the second conductive semiconductor layer 13. In the following embodiment, a stacked structure including the first conductive semiconductor layer 11, the active layer 12, the second conductive layer 13, and the electrode layer 15 is referred to as the emission stacked pattern 10.

[0041] The electrode layer 15 may be an ohmic contact electrode electrically coupled to the second conductive semiconductor layer 13, but the present disclosure is not limited thereto. The electrode layer 15 may be made of a transparent or opaque material. To this end, the electrode layer 15 may use a metal material such as Cr, Ti, Al, Au, or Ni, or transparent conductive oxide such as ITO, IZO, or ITZO alone or in combination.

[0042] If a predetermined voltage is applied to both ends of the emission stacked pattern 10, the emission stacked pattern 10 emits light while electrons are combined with holes in the active layer 12. Using this principle, the emission stacked pattern 10 may be used as a light source of the display device.

[0043] Since the emission stacked pattern 10 has a cylindrical shape, the outer surface 10a of the emission stacked pattern 10 may be circular. In this case, the first conductive semiconductor layer 11, the active layer 12, the second conductive semiconductor layer 13, and the electrode layer 15 each have a cylindrical shape. Furthermore, although not shown in the drawings, the emission stacked pattern 10 may have the shape of an elliptical column or the shape of a polygonal column. In this case, the first conductive semiconductor layer 11, the active layer 12, the second conductive semiconductor layer 13, and the electrode layer 15 each may have the shape of an elliptical column or the shape of a polygonal column.

[0044] The emission stacked pattern 10 may be covered by the insulating film 14. The insulating film 14 prevents the active layer 12 from making contact with a conductive material except the first conductive semiconductor layer 11 and the second conductive semiconductor layer 13, and simultaneously minimizes the surface defects of the emission stacked pattern 10. The insulating film 14 may include various materials having insulating properties, for example, include one or more insulating materials selected from a group consisting of SiO_2, Si_3N_4, Al_2O_3, and TiO_2. However, the present disclosure is not limited thereto.

[0045] In the drawing, the insulating film 14 completely covers the outer surface 10a of the emission stacked pattern 10. However, the insulating film 14 may cover only a portion of the emission stacked pattern 10. In this case, the insulating film 14 may completely cover the active layer 12, and may expose portions of the first conductive semiconductor layer 11, the second conductive semiconductor layer 13, and the electrode layer 15.

[0046] As such, the light emitting element LD including the emission stacked pattern 10 and the insulating film 14 is a subminiature light emitting element LD having a very small size corresponding to a nanometer scale. In order to use the light emitting element LD as the light source of the display device, the light emitting elements LD may be arranged, respectively, in pixels of the display device. For example, a solution in which the light emitting elements LD are dispersed may be applied to each pixel area to use the light emitting elements LD as the light source of the display device.

[0047] However, since the light emitting elements LD are very small, they may be disposed to be adjacent to each other or agglomerated within the pixel. In this case, adjacent light emitting elements LD may come into contact with each other, so that insulating films 14 of the adjacent light emitting elements LD may come into contact with each other. Moreover, a portion of the insulating film 14 where the light emitting elements LD come into contact with each other may be removed, thereby causing a short-circuit.

[0048] Therefore, the light emitting element in accordance with the embodiment of the present disclosure includes the insulating layer 14 having the outer surface 14a that is different in shape from the outer surface 10a of the emission stacked pattern 10, so that the thickness of the insulating film 14 may not be uniform.

[0049] In detail, the cross-section of the cylindrical emission stacked pattern 10, i.e. the outer surface 10a of the emission stacked pattern 10 may be circular, but the outer surface 14a of the insulating film 14 may be elliptical. Therefore, the insulating film 14 is not uniform in thickness, and may include a first thickness T1 that is relatively thick and a second thickness T2 that is relatively thin.

[0050] On the other hand, in the light emitting element of the present disclosure, the thickness of the insulating film 14 is non-uniform. Thus, even if the light emitting elements LD are agglomerated or disposed adjacent to each other, the emission stacked patterns 10 of the light emitting elements LD which are adjacent to each other secure a sufficient distance therebetween through the insulating film 14 having the non-uniform thickness, thus preventing the adjacent light emitting elements LD from being agglomerated. Furthermore, even if a portion of the insulating film 14 is removed from a portion where the light emitting elements LD are adjacent to each other, the thickness of the insulating film 14 varies, thus preventing the emission stacked pattern 10 from being exposed to the outside.

[0051] Hereinafter, light emitting elements in accordance with another embodiment of the present disclosure will be described with reference to the accompanying drawings.

[0052] FIGS. 2a to 2d are perspective views of a light emitting element in accordance with another embodiment of the present disclosure.

[0053] As illustrated in FIGS. 2a, 2b, 2c, and 2d, the light emitting element in accordance with another em-

bodiment of the present disclosure may have a polygonal shape in which the outer surface 14a of the insulating film 14 surrounding the outer surface 10a of the emission stacked pattern 10 having a cylindrical shape is surrounded by three or more line segments. In this case, the insulating film 14 is not uniform in thickness, and may include a first thickness T1 that is relatively thick and a second thickness T2 that is relatively thin.

[0054] FIGS. 3a to 3c are perspective views of a light emitting element in accordance with a further embodiment of the present disclosure.

[0055] In the light emitting element in accordance with a further embodiment of the present disclosure, the outer surface 14a of the insulating film 14 may include at least one protrusion 14a_2. Therefore, even if the light emitting elements LD (FIG. 1a) are disposed adjacent to each other, a sufficient distance may be secured between adjacent light emitting elements LD (FIG.1a) through the protrusion 14a_2. Even if the protrusion 14a_2 is damaged in a portion where the light emitting elements LD (FIG. 1a) are adjacent to each other, it is possible to efficiently prevent the emission stacked pattern 10 from being exposed to the outside.

[0056] In detail, as illustrated in FIG. 3a, the outer surface 14a of the insulating film 14 may include the protrusion 14a_2, and the remaining area 14a_1 of the outer surface 14a of the insulating film 14 except for the protrusion 14a_2 may have the same shape as the outer surface 10a of the emission stacked pattern 10. In this case, the thickness of a portion of the insulating film 14 corresponding to the protrusion 14a_2 is the thickest. In other words, when the outer surface 14a of the insulating film 14 includes the protrusion 14a_2, a difference between the relatively thick first thickness T1 and the relatively thin second thickness T2 of the insulating film 14 is large, thus efficiently preventing adjacent light emitting elements LD from being agglomerated. Furthermore, as illustrated in FIG. 3b, the remaining area 14a_1 of the outer surface 14a of the insulating film 14 except for the protrusion 14a_2 may also be different from the outer surface 10a of the emission stacked pattern 10.

[0057] The protrusion 14a_2 serves to secure a sufficient distance between the emission stacked patterns 10 in the light emitting elements LD (FIG. 1a) adjacent to each other. When the outer surface 14a of the insulating film 14 includes at least two protrusions 14a_2, a distance may be stably secured between the light emitting elements LD (see FIG. 1a). For example, as illustrated in FIG. 3c, when the outer surface 14a of the insulating film 14 includes four protrusions 14a_2, it is possible to stably secure a distance between the light emitting elements LD (FIG. 1a). Here, the width or length of the protrusion 14a_2 may be easily changed.

[0058] Hereinafter, a method of manufacturing a light emitting element in accordance with an embodiment of the present disclosure will be described in detail with reference to the accompanying drawings.

[0059] FIGS. 4a to 4o are sectional views illustrating the method of manufacturing the light emitting element of FIG. 1a.

[0060] As illustrated in FIG. 4a, a substrate 1 is prepared, and a sacrificial layer 3 is formed on the substrate 1. The substrate 1 may be a GaAs, GaP, or InP substrate. The substrate 1 may be a wafer for epitaxial growth. For example, the substrate 1 may include a ZnO substrate having a GaAs layer on a surface. Furthermore, a Ge substrate having the GaAs layer on the surface and an Si substrate having the GaAs layer on an Si wafer with a buffer layer being interposed therebetween may also be applied.

[0061] A commercially available mono-crystal substrate manufactured by a known manufacturing method may be used as the substrate 1. When a selection ratio for manufacturing the light emitting element LD (FIG. 1a) is satisfied and the epitaxial growth is smoothly performed, the material of the substrate 1 is not limited thereto. In the following embodiment, the substrate 1 is described as being the GaAs substrate made of GaAs.

[0062] It is preferable that the surface of the substrate 1 to be epitaxially grown is flat. The size and diameter of the substrate 1 may vary depending on a product to which the substrate 1 is applied, and may be manufactured in a form capable of reducing bending caused by a stacked structure due to epitaxial growth. The shape of the substrate 1 is not limited to a circular shape, and may have a polygonal shape such as a rectangle.

[0063] The sacrificial layer 3 may be formed on the substrate 1 by an MOCVD method, an MBE method, a VPE method, an LPE method, or the like. The sacrificial layer 3 may be formed of GaAs, AlAs or AlGaAs. In the following embodiment, the sacrificial layer 3 is described as being made of GaAs.

[0064] The substrate 1 and the sacrificial layer 3 may be disposed to come into contact with each other. The sacrificial layer 3 may be positioned between the light emitting element LD and the substrate 1 in the process of manufacturing the light emitting element LD (FIG. 1a) to physically separate the light emitting element LD (FIG. 1a) from the substrate 1.

[0065] The sacrificial layer 3 may have various structures, i.e. a single layer structure or a multilayer structure. The sacrificial layer 3 may be a layer which is removed in a final manufacturing process of forming the light emitting element LD (FIG. 1a). When the sacrificial layer 3 is removed, interlayer separation may be performed above and under the sacrificial layer 3.

[0066] Referring to FIG. 4b, an emissive stack structrue 10' is formed on the sacrificial layer 3. The emissive stack structrue 10' may be formed through a step of forming the first conductive semiconductor layer 11 on the sacrificial layer 3, a step of forming the active layer 12 on the first conductive semiconductor layer 11, a step of forming the second conductive semiconductor layer 13 on the active layer 12, and a step of forming the electrode layer 15 on the second conductive semiconductor layer 13.

[0067] Similarly to the sacrificial layer 3, the first conductive semiconductor layer 11 may be formed through the epitaxial growth, and be formed by the MOCVD method, the MBE method, the VPE method, the LPE method or the like. In an embodiment, an additional semiconductor layer for improving crystallinity, such as a buffer layer and an undoped semiconductor layer, may be further formed between the first conductive semiconductor layer 11 and the sacrificial layer 3.

[0068] The first conductive semiconductor layer 11 may include a semiconductor material composed of III(Ga, Al, In)-V(P, As) groups, and may include a semiconductor layer doped with a first conductive dopant such as Si, Ge, or Sn. For example, the first conductive semiconductor layer 11 may include at least one semiconductor material among GaP, GaAs, GaInP, and AlGaInP doped with Si. In other words, the first conductive semiconductor layer 11 may include at least one n-type semiconductor layer. The material forming the first conductive semiconductor layer 11 is not limited to this, and the first conductive semiconductor layer 11 may be formed of various other materials.

[0069] The active layer 12 is an area in which electrons and holes are recombined. As the electrons and the holes are recombined, the active layer may be transferred to a low energy level and emit light having a wavelength corresponding thereto.

[0070] The active layer 12 may be formed on the first conductive semiconductor layer 11 and have a single or multiple quantum well structure. The location of the active layer 12 may be changed in various ways depending on the type of the light emitting element LD.

[0071] The active layer 12 may include at least one of GaInP, AlGaInP, GaAs, AlGaAs, InGaAs, InGaAsP, InP, and InAs. The active layer 12 may emit light having a wavelength of 400 nm to 900 nm. The active layer 12 may use a double heterostructure. In an embodiment, a cladding layer (not shown) doped with the conductive dopant may be further formed on an upper surface and/or a lower surface of the active layer 12.

[0072] The second conductive semiconductor layer 13 may include a semiconductor layer of a type different from that of the first conductive semiconductor layer 11. The second conductive semiconductor layer 13 may include semiconductor material composed of III(Ga, Al, In)-V(P, As) groups, and may include a semiconductor layer doped with a second conductive dopant such as Mg. For example, the second conductive semiconductor layer 13 may include at least one semiconductor material among GaP, GaAs, GaInP, and AlGaInP doped with Mg. In other words, the second conductive semiconductor layer 13 may include a p-type semiconductor layer. However, the material forming the second conductive semiconductor layer 13 is not limited thereto.

[0073] The electrode layer 15 is formed on the second conductive semiconductor layer 13. The electrode layer 15 may include metal or metal oxide. For example, the electrode layer 15 may use Cr, Ti, Al, Au, Ni, ITO, IZO, ITZO, oxide or alloy thereof alone or in combination. In an embodiment of the present disclosure, the electrode layer 15 may be made of transparent metal oxide such as indium tin oxide ITO so as to minimize the loss of light generated from the active layer 12 and emitted to the outside of the light emitting element LD (FIG. 1a) and improve current spreading effects to the second conductive semiconductor layer 13, without being limited thereto.

[0074] The first conductive semiconductor layer 11, the active layer 12, the second conductive semiconductor layer 13, and the electrode layer 15 which are sequentially stacked on the substrate 1 may form the emissive stack structrue 10'. However, the electrode layer 15 may not be formed. In this case, the first conductive semiconductor layer 11, the active layer 12, and the second conductive semiconductor layer 13 may form the emissive stack structrue 10'.

[0075] As illustrated in FIG. 4c, a first resin R1 is applied to the emissive stack structrue 10'. The first resin R1 may be applied to the emissive stack structrue 10' in the form of dots. The first resin R1 may include a photocuring material. As illustrated in FIG. 4d, a first mold M1 including a plurality of first grooves H1 is connected to the upper surface of the emissive stack structrue 10'. Here, the first mold M1is a soft mold, and a plurality of first grooves H1 of the first mold M1may be in close contact with the emissive stack structrue 10' using a roll laminating process. When the first mold M1includes a transparent material and then a process such as UV curing is performed to cure the first resin R1, the UV may pass through the transparent first mold M1to cure the first resin R1.

[0076] Hereinafter, the first mold will be described in detail with reference to the accompanying drawings.

[0077] FIG. 5a is a perspective view of a first mold M1 shown in FIG. 4d, and FIG. 5b is a plan view of the first mold M1of FIG. 5a when seen from below.

[0078] As illustrated in FIGS. 5a and 5b, the first mold M1includes a plurality of first grooves H1 formed on a surface thereof. Here, the first groove H1 is filled with the first resin R1 (FIG. 4c) formed on the emissive stack structrue 10' (FIG. 4d), thus forming the first resin R1 (FIG. 4c) in the shape of the first groove H1.

[0079] In an embodiment of the present disclosure, the first resin R1 (FIG. 4c) formed in the shape of the first groove H1 is used as a mask for patterning the emissive stack structrue 10' (FIG. 4d). As illustrated in FIG. 1a, in order to form the emission stacked pattern 10 (FIG. 1a) in a cylindrical shape, the first groove H1 may be circular. Here, the emission stacked pattern 10 (FIG. 1a) may be formed in a size from the nanometer scale to the micrometer scale by adjusting a width W1 of the first groove H1. Although not illustrated in the drawings, the first groove H1 may have a polygonal shape in order to form the emission stacked pattern 10 (FIG. 1a) in the shape of a polygonal column.

[0080] Turning back to FIG. 4d, if the first mold M1

comes into contact with the upper surface of the emissive stack structrue 10', the first resin R1 may fill the first grooves H1. Furthermore, the first resin R1 is cured using the UV or the like with the first resin R1 being filled in the first grooves H1. Meanwhile, when the first resin R1 contains a hot curing material, the first resin R1 may be cured through heat.

[0081] Furthermore, the first mold M1may be separated from the emissive stack structrue 10' as illustrated in FIG. 4e, and a plurality of first micro patterns MP1 may be formed on the emissive stack structrue 10' as illustrated in FIG. 4f. An edge of each first micro pattern MP1 is circular along the shape of the first groove H1, and each first micro pattern MP1 also has the same width W1 as the first groove H1.

[0082] Subsequently, as illustrated in FIG. 4g, the emissive stack structrue 10' (FIG. 4F) may be etched in a vertical direction using the first micro patterns MP1 as the mask to form a plurality of emission stacked patterns 10.

[0083] In detail, the electrode layer 15, the second conductive semiconductor layer 13, the active layer 12, and the first conductive semiconductor layer 11 in an area exposed by the first micro pattern MP1 may be etched to form the plurality of emission stacked patterns 10.

[0084] The primary etching may use a dry etching method such as RIE (reactive ion etching), RIBE (reactive ion beam etching), or ICP-RIE (inductively coupled plasma reactive ion etching, inductively coupled plasma reactive ion etching). Unlike a wet etching method, the dry etching method allows anisotropic etching to be suitable for forming the emission stacked patterns 10. However, the etching method may be changed in various ways without being limited thereto.

[0085] Subsequently, as illustrated in FIG. 4h, an insulating film pattern 14P surrounding the outer surface of the emission stacked pattern 10 including the first micro pattern MP1 is formed. In the drawing, the insulating film pattern 14P completely surrounds the outer surface of the emission stacked pattern 10. However, as described above, the insulating film pattern 14P may be formed to expose a portion of the emission stacked pattern 10. Here, the outer surface of the insulating film pattern 14P may also be circular to surround the circular outer surface of the cylindrical emission stacked pattern 10. In other words, the shape of the outer surface of the emission stacked pattern 10 is the same as that of the outer surface of the insulating film pattern 14P.

[0086] The insulating film pattern 14P may include various materials having insulating properties, for example, include one or more insulating materials selected from a group consisting of SiO_2, Si_3N_4, Al_2O_3, and TiO_2. However, the present disclosure is not limited thereto.

[0087] As illustrated in FIG. 4i, the electrode layer 15 of each emission stacked pattern 10 is exposed by removing the first micro pattern MP1 that remains on the upper surface of each emission stacked pattern 10.

[0088] Subsequently, as illustrated in FIG. 4j, a second resin R2 is applied to the emission stacked pattern 10. The second resin R2 may be applied to each emission stacked pattern 10 in the form of a dot. The second resin R2 may also include a photo-curing material as in the first resin R1 (FIG. 4k). Subsequently, as illustrated in FIG. 4k, the second mold M2 having a plurality of second grooves H2 comes into contact with the upper surfaces of the emission stacked patterns 10. Here, the second mold M2 is a soft mold, and a plurality of second grooves H2 of the second mold M2 may be in close contact with the emission stacked pattern 10 using a roll laminating process. Particularly, when the second mold M2 also includes a transparent material and then a process such as UV curing is performed to cure the second resin R2, the UV may pass through the transparent second mold M2 to cure the second resin R2.

[0089] Hereinafter, the second mold will be described in detail with reference to the accompanying drawings.

[0090] FIG. 6a is a perspective view of the second mold M2 shown in FIG. 4k, and FIG. 6b is a plan view of the second mold M2 of FIG. 6a when seen from below. Furthermore, FIGS. 7a to 7g are diagrams illustrating various shapes of a second groove shown in FIG. 6b.

[0091] As illustrated in FIGS. 6a and 6b, the second mold M2 includes a plurality of second grooves H2 formed on a surface thereof. Here, the second groove H2 is used to remove a portion of the insulating film pattern 14P (FIG. 4k) that surrounds the outer surface of the emission stacked pattern 10. Therefore, the width W2 of the second groove H2 is preferably greater than the width W1 of the first groove H1 of the first mold M1 of FIGS. 5a and 5b.

[0092] Furthermore, as illustrated in FIG. 1a, the second groove H2 may have an elliptical shape to form the outer surface of the insulating film 14 (FIG. 1a) in an elliptical shape. As illustrated in FIGS. 2a to 2d and FIGS. 3a to 3c, the second groove H2 may have various shapes of FIGS. 7a to 7g to form the insulating film 14 having various outer surfaces. Therefore, if the second mold M2 including the second groove H2 that has an elliptical shape, a polygonal shape, a mixed shape of an ellipse and a polygon, or a shape having a protrusion as illustrated in FIGS. 7a to 7g is employed, the second micro pattern MP2 having the same shape as the second groove H2 may be formed.

[0093] Turning back to FIG. 4k, if the second mold M2 is pressed against the upper surface of the emission stacked pattern 10, the second resin R2 may fill the second groove H2 of the second mold M2. Furthermore, the second resin R2 is cured using the UV or the like with the second resin R2 being filled in the second grooves H2.

[0094] Furthermore, as illustrated in FIG. 4l, the second mold M2 may be separated from the emission stacked patterns 10 to form a plurality of second micro patterns MP2 on the emission stacked patterns 10. Here, each of the second micro patterns MP2 has a width W2 that is greater than the width W1 of the first micro pattern

MP1 of FIG. 4f, so that the second micro pattern MP2 may be disposed on the insulating film pattern 14P surrounding the outer surface of the emission stacked pattern 10.

[0095] Subsequently, as illustrated in FIG. 4m, the insulating film pattern 14P surrounding the outer surface of each emission stacked pattern 10 may be vertically etched using the second micro pattern MP2 as the mask to form the insulating film 14. Therefore, the insulating film 14 has a structure in which at least a portion of the insulating film pattern 14P is removed, and the insulating film 14 may include an area having a thickness thinner than that of the insulating film pattern 14P.

[0096] In detail, as illustrated in FIG. 4l, the outer surface of the insulating film pattern 14P is circular as in the outer surface of the emission stacked pattern 10, and the outer surface 14a of the insulating film 14 is an elliptical outer surface 14a that is different from the outer surface 10a of the emission stacked pattern 10 of FIG. 1a.

[0097] Furthermore, as illustrated in FIG. 4n, the second micro pattern MP2 may be removed to form the light emitting element LD including the emission stacked pattern 10 surrounded by the insulating film 14.

[0098] Subsequently, as illustrated in FIG. 4o, the light emitting elements LD are separated from the substrate 1. For example, the light emitting elements LD may be separated from the substrate 1 using a chemical lift-off (CLO) method. For example, the sacrificial layer 3 may be removed to separate the light emitting elements LD from the substrate 1.

[0099] In other words, the method of manufacturing the light emitting element according to an embodiment of the present disclosure may form the emission stacked patterns 10 using the first micro pattern, and may form the insulating film 14 by selectively removing the insulating film pattern 14P that surrounds the outer surface of the emission stacked pattern 10 using the second micro pattern different from the first micro pattern.

[0100] Hereinafter, light emitting elements in accordance with another embodiment of the present disclosure will be described with reference to the accompanying drawings.

[0101] FIGS. 8a and 8b are perspective views of a light emitting element in accordance with another embodiment of the present disclosure.

[0102] As illustrated in FIGS. 8a and 8b, the light emitting element LD in accordance with another embodiment of the present disclosure may be configured such that the outer surface 10a of the emission stacked pattern 10 and the outer surface 14a of the insulating film 14 have the same shape, which may be selected from shapes other than a circular shape.

[0103] For example, as illustrated in FIGS. 8a and 8b, the outer surface of the emission stacked pattern 10 and the outer surface of the insulating film 14 may have the same polygonal shape. In the drawings, it is illustrated that both the outer surface of the emission stacked pattern 10 and the outer surface of the insulating film 14 have a triangular shape or a rectangular shape. In this case, the thickness of the insulating film 14 surrounding the outer surface of the emission stacked pattern 10 may no be uniform. In other words, the insulating film 14 may include a first thickness T1 that is relatively thick and a second thickness T2 that is relatively thin.

[0104] The light emitting element LD in accordance with another embodiment of the present disclosure may form the emission stacked pattern 10 having the outer surface of various shapes other than a circular shape using the second mold M2 of FIGS. 6b, 7a to 7g, and may form the insulating film 14 that surrounds the outer surface of the emission stacked pattern 10 and has the same outer surface as the outer surface of the emission stacked pattern 10.

[0105] Hereinafter, a display device including a light emitting element in accordance with an embodiment of the present disclosure will be described in detail with reference to the accompanying drawings.

[0106] FIG. 9 is a schematic plan view illustrating a display device in accordance with an embodiment of the present disclosure, in which the display device uses the light emitting element shown in FIG. 1a as a light emitting source.

[0107] For the sake of explanation, FIG. 9 schematically illustrates the structure of the display device, focused on a display area on which an image is displayed. In some embodiments, although not illustrated, at least one driving circuit (e.g., a scan driver and a data driver) and/or a plurality of signal lines may be further provided in the display device.

[0108] Referring to FIGS. 1a and 9, the display device in accordance with an embodiment of the present disclosure may include a substrate SUB, a plurality of pixels PXL provided on the substrate SUB and including at least one light emitting element LD (FIG. 1a), a driver (not shown) provided on the substrate SUB and driving the pixels PXL, and a line component (not shown) coupling the pixels PXL with the driver.

[0109] The display device may be classified into a passive-matrix type display device and an active-matrix type display device according to a method of driving the light emitting element LD (FIG. 1a). In the case where the display device is implemented as the active-matrix type, each of the pixels PXL may include a driving transistor configured to control the amount of current to be supplied to the light emitting element LD, and a switching transistor configured to transmit data signals to the driving transistor.

[0110] Recently, active-matrix type display devices capable of selectively turning on each pixel PXL taking into account the resolution, the contrast, and the working speed have been mainstreamed. However, the present disclosure is not limited thereto. For example, passive-matrix type display devices in which pixels PXL may be turned on by groups may also employ components (e.g., first and second electrodes) for driving the light emitting element LD (FIG. 1a).

[0111] The substrate SUB may include a display area DA and a non-display area NDA. The display area DA may be an area in which the pixels PXL for displaying an image are provided. The non-display area NDA may be an area in which the driver for driving the pixels PXL and a portion of the line component for coupling the pixels PXL to the driver are provided.

[0112] In the drawing, it is illustrated that the display area DA may be disposed in a central portion of the display device, and the non-display area NDA may be disposed in a perimeter portion of the display device in such a way as to enclose the display area DA. However, the present disclosure is not limited thereto, and the position may be changed.

[0113] The display area DA may have various shapes. For example, the display area DA may be provided in various forms such as a closed polygon including sides formed of linear lines, a circle, an ellipse or the like including a side formed of a curved line, and a semicircle, a semi-ellipse or the like including sides formed of a linear line and a curved line. The non-display area NDA may be provided on at least one side of the display area DA. In the drawing, it is illustrated that the non-display area NDA surrounds the display area DA, but the present disclosure is not limited thereto.

[0114] The substrate SUB may be a rigid or flexible substrate without being limited thereto. For example, the substrate SUB may be a rigid substrate made of glass or reinforced glass, or a flexible substrate formed of a thin film made of plastic or metal. Furthermore, the substrate SUB may be a transparent substrate, but it is not limited thereto. Furthermore, the substrate SUB may be a translucent substrate, an opaque substrate, or a reflective substrate.

[0115] The pixels PXL may be provided in the display area DA on the substrate SUB. Each of the pixels PXL refers to a minimum unit for displaying an image, and a plurality of pixels may be provided.

[0116] Each of the pixels PXL may include the light emitting element LD (FIG. 1a) configured to be driven in response to a scan signal and a data signal. The light emitting element LD (FIG. 1a) may have a small size in the range from the nanometer scale to the micrometer scale, and may be coupled in parallel to adjacent light emitting elements LD (FIG. 1a). The light emitting element LD (FIG. 1a) may form a light source of each pixel PXL.

[0117] Furthermore, each of the pixels PXL may include a plurality of sub-pixels. For example, each pixel PXL may include a first sub-pixel SP1, a second sub-pixel SP2, and a third sub-pixel SP3, which emit light of different colors. For instance, the first sub-pixel SP1 may be a red sub-pixel for emitting red light, the second sub-pixel SP2 may be a green sub-pixel for emitting green light, and the third sub-pixel SP3 may be a blue sub-pixel for emitting blue light. However, the color, type and/or number of the sub-pixels forming each pixel PXL are not limited thereto.

[0118] Furthermore, FIG 9 illustrates that the pixels PXL are arranged in the display area DA in a matrix form in a first direction DR1 and a second direction DR2 different from the first direction DR1. However, the arrangement of the pixels PXL is not limited thereto, but various arrangements are possible. Furthermore, the arrangement of the plurality of sub-pixels of each pixel PXL may also be changed in various ways.

[0119] The driver may provide a driving signal to each pixel PXL through the line component and thus control the operation of each pixel PXL. In FIG. 9, the line component is omitted for the sake of explanation.

[0120] The driver may include a scan driver configured to provide scan signals to the pixels PXL through scan lines, an emission driver configured to provide emission control signals to the pixels PXL through emission control lines, a data driver configured to provide data signals to the pixels PXL through data lines, and a timing controller. The timing controller may control the scan driver, the emission driver, and the data driver.

[0121] FIGS. 10a to 10c are circuit diagrams illustrating various embodiments of a unit emission area of the display device of FIG. 9.

[0122] In FIGS. 10a to 10c, each of the first to third sub-pixels may be configured as an active pixel. However, the type, structure and/or driving method of each of the first to third sub-pixels is not particularly limited. For example, each of the first to third sub-pixels may be configured as a pixel of a passive or active display device of various known structures.

[0123] In FIGS. 10a to 10c, the first to third sub-pixels may have substantially the same or similar structure. Hereinafter, for convenience, the first sub-pixel SP1 among the first to third sub-pixels will be described as a representative.

[0124] Referring to FIGS. 1a, 9, and 10a, the first sub-pixel SP1 may include an emission area EMA that generates light of a luminance corresponding to a data signal and a pixel driving circuit 144 that drives the emission area EMA.

[0125] In an embodiment, the emission area EMA may include a plurality of light emitting elements LD coupled in parallel between a first driving power supply VDD and a second driving power supply VSS. Here, the first driving power supply VDD and the second driving power supply VSS may have different potentials. For example, the first driving power supply VDD may be set as a high-potential power supply, and the second driving power supply VSS may be set as a low-potential power supply. A difference in potential between the first and second power supplies VDD and VSS may be set to a threshold voltage of the light emitting elements LD or more during a light emitting period of the first sub-pixel SP1.

[0126] A first electrode (e.g., an anode electrode) of each of the light emitting elements LD may be connected to a first driving power supply VDD via the pixel driving circuit 144, and a second electrode (e.g., a cathode electrode) of each of the light emitting elements LD may be

connected to a second driving power supply VSS. Therefore, each of the light emitting elements LD may emit light at a luminance corresponding to driving current which is controlled by the pixel driving circuit 144.

[0127] Although FIGS. 10a to 10c illustrate embodiments in which the light emitting elements LD are coupled in parallel to each other in the same direction (e.g. forward direction) between the first and second driving power supplies VDD and VSS, the present disclosure is not limited thereto. For example, in another embodiment, some of the light emitting elements LD may be coupled to each other in the forward direction between the first and second driving power supplies VDD and VSS, and the other light emitting elements LD may be coupled to each other in the reverse direction. One of the first and second driving power supplies VDD and VSS may be supplied in the form of AC voltage. In this case, the light emitting elements LD may alternately emit light by each group having the same coupling direction. Alternatively, in a further embodiment, the first sub-pixel SP1 may include only a single light emitting element LD.

[0128] The pixel driving circuit 144 may include a first transistor T1, a second transistor T2, and a storage capacitor Cst. However, the structure of the pixel driving circuit 144 is not limited to the embodiment illustrated in FIG. 10a.

[0129] A first electrode of the first transistor (switching transistor) T1 is connected to a data line Dj, and a second electrode thereof is connected to the first node N1. Here, the first electrode and the second electrode of the first transistor T1 may be different electrodes. For example, if the first electrode is a source electrode, the second electrode may be a drain electrode. A gate electrode of the first transistor T1 is connected to the scan line Si.

[0130] When a scan signal having a voltage (e.g., a low-level voltage) capable of turning on the first transistor T1 is supplied from the scan line Si, the first transistor is turned on to electrically couple the data line Dj with the first node N1. Here, a data signal of a corresponding frame is supplied to the data line Dj, whereby the data signal is transmitted to the first node N1. The data signal transmitted to the first node N1 is charged in the storage capacitor Cst.

[0131] The first electrode of the second transistor T2 (driving transistor) is connected to the first driving power supply VDD, and the second electrode is electrically connected to the first electrode of each of the light emitting elements LD. A gate electrode of the second transistor T2 is connected to a first node N1. As such, the second transistor T2 controls the amount of driving current to be supplied to the light emitting elements LD in response to the voltage of the first node N1.

[0132] One electrode of the storage capacitor Cst is connected to the first driving power supply VDD, and the other electrode thereof is connected to the first node N1. The storage capacitor Cst charges a voltage corresponding to the data signal supplied to the first node N1, and maintains the charged voltage until a data signal of a subsequent frame is supplied.

[0133] For the sake of explanation, FIG. 10a illustrates the pixel driving circuit 144 having a relatively simple structure including the first transistor T1 configured to transmit the data signal to the first sub-pixel SP1, the storage capacitor Cst configured to store the data signal, and the second transistor T2 configured to supply driving current corresponding to the data signal to the light emitting element LD.

[0134] However, the present disclosure is not limited thereto, and the structure of the pixel driving circuit 144 may be changed in various ways. For example, the pixel driving circuit 144 may further include at least one transistor element such as a transistor element configured to compensate for the threshold voltage of the second transistor T2, a transistor element configured to initialize the first node N1, and/or a transistor element configured to control the emission time of the light emitting elements LD, or other circuit elements such as a boosting capacitor for boosting the voltage of the first node N1.

[0135] Furthermore, although in FIG. 10a the transistors, e.g., the first and second transistors T1 and T2, included in the pixel driving circuit 144 have been illustrated as being formed of P-type transistors, the present disclosure is not limited to this. In other words, at least one of the first and second transistors T1 and T2 included in the pixel driving circuit 144 may be changed to an N-type transistor.

[0136] Next, referring to FIGS. 1a, 9, and 10b, the first and second transistors T1 and T2 in accordance with an embodiment of the present disclosure may be formed of N-type transistors. The configuration and operation of the pixel driving circuit 144 illustrated in FIG. 10b, other than a change in connection positions of some components due to a change in the type of transistor, are similar to those of the pixel driving circuit 144 of FIG. 10a. Therefore, detailed descriptions pertaining to this will be omitted.

[0137] In an embodiment of the present disclosure, the configuration of the pixel driving circuit 144 is not limited to the embodiments illustrated in FIGS. 10a and 10b. For example, the pixel driving circuit 144 may be configured in the same manner as that of an embodiment shown in FIG. 10c.

[0138] Referring to FIGS. 1a, 9, and 10c, the pixel driving circuit 144 may be coupled to the scan line Si and the data line Dj of the first sub-pixel SP1. For example, if the first sub-pixel SP1 is disposed on an i-th row and a j-th column of the display area DA, the pixel driving circuit 144 of the first sub-pixel SP1 may be coupled to an i-th scan line Si and a j-th data line Dj of the display area DA.

[0139] In an embodiment, the pixel driving circuit 144 may also be coupled to at least one different scan line. For example, the first sub-pixel SP1 disposed on the i-th row of the display area DA may also be coupled to an i-1-th scan line Si-1 and/or an i+1-th scan line Si+1.

[0140] In an embodiment, the pixel driving circuit 144

may be coupled not only to the first and second driving power supplies VDD and VSS but also to a third power supply. For example, the pixel driving circuit 144 may also be coupled to an initialization power supply Vint.

[0141] The pixel driving circuit 144 may include first to seventh transistors T1 to T7, and a storage capacitor Cst.

[0142] The first transistor (driving transistor) T1 may include a first electrode, e.g., a source electrode, connected to the first driving power supply VDD via the fifth transistor T5, and a second electrode, e.g., a drain electrode, connected to first ends of light emitting elements LD via the sixth transistor T6. A gate electrode of the first transistor T1 may be connected to a first node N1. The first transistor T1 controls driving current flowing between the first driving power supply VDD and the second driving power supply VSS via the light emitting elements LD in response to the voltage of the first node N1.

[0143] The second transistor (switching transistor) T2 is connected between the j-th data line Dj coupled to the first sub-pixel SP1 and the source electrode of the first transistor T1. A gate electrode of the second transistor T2 is connected to the i-th scan line Si coupled to the first sub-pixel SP1. When a scan signal having a gate-on voltage (e.g., a low-level voltage) is supplied from the i-th scan line Si, the second transistor T2 is turned on to electrically couple the j-th data line Dj to the source electrode of the first transistor T1. Hence, if the second transistor T2 is turned on, a data signal supplied from the j-th data line Dj is transmitted to the first transistor T1.

[0144] The third transistor T3 is connected between the drain electrode of the first transistor T1 and the first node N1. A gate electrode of the third transistor T3 is connected to the i-th scan line Si. When a scan signal having a gate-on voltage is supplied from the i-th scan line Si, the third transistor T3 is turned on to electrically couple the drain electrode of the first transistor T1 to the first node N1. Therefore, when the third transistor T3 is turned on, the first transistor T1 is connected in the form of a diode.

[0145] The fourth transistor T4 is connected between the first node N1 and the initialization power supply Vint. A gate electrode of the fourth transistor T4 is connected to a preceding scan line, e.g., an i-1-th scan line Si-1. When a scan signal of a gate-on voltage is supplied to the i-1-th scan line Si-1, the fourth transistor T4 is turned on so that the voltage of the initialization power supply Vint is transmitted to the first node N1. Here, the initialization power supply Vint may have a voltage equal to or less than the minimum voltage of the data signal.

[0146] The fifth transistor T5 is connected between the first driving power supply VDD and the first transistor T1. A gate electrode of the fifth transistor T5 is connected to a corresponding emission control line, e.g., an i-th emission control line Ei. The fifth transistor T5 is turned off when an emission control signal having a gate-off voltage is supplied to the i-th emission control line Ei, and is turned on in other cases.

[0147] The sixth transistor T6 is connected between the first transistor T1 and first ends of the light emitting elements LD. A gate electrode of the sixth transistor T6 is connected to the i-th emission control line Ei. The sixth transistor T6 is turned off when an emission control signal having a gate-off voltage is supplied to the i-th emission control line Ei, and is turned on in other cases.

[0148] The seventh transistor T7 is connected between the first ends of the light emitting elements LD and the initialization power supply Vint. A gate electrode of the seventh transistor T7 is connected to any one of scan lines of a subsequent stage, e.g., to the i+1-th scan line Si+1. When a scan signal having a gate-on voltage is supplied to the i+1-th scan line Si+1, the seventh transistor T7 is turned on so that the voltage of the initialization power supply Vint is supplied to the first ends of light emitting elements LD.

[0149] The storage capacitor Cst is connected between the first driving power supply VDD and the first node N1. The storage capacitor Cst stores a voltage corresponding both to the data signal supplied to the first node N1 during each frame period and to the threshold voltage of the first transistor T1.

[0150] For convenience, all of the first to seventh transistors T1 to T7 are illustrated in FIG. 10c as the P-type transistor, but the present disclosure is not limited thereto. For example, at least one of the first to seventh transistors T1 to T7 included in the pixel driving circuit 144 may be changed to the N-type transistor, or all of the first to seventh transistors T1 to T7 may be changed to the N-type transistor.

[0151] Hereinafter, the pixel of the display device of FIG. 9 will be described in detail with reference to the accompanying drawings.

[0152] FIG. 11 is a plan view schematically illustrating first to third sub-pixels included in one pixel among pixels shown in FIG. 9. FIG. 12a is a sectional view taken along line III-III of FIG. 11, and FIG. 12b is a sectional view taken along line IV-IV of FIG. 11.

[0153] For the sake of explanation, the transistor coupled to the light emitting elements LD and the signal lines coupled to the transistor are omitted in FIG. 11 In addition, it is illustrated in FIGS. 11, 12a and 12b that one pixel structure is simplified, for example, each electrode is only a single electrode layer, but the present disclosure is not limited thereto.

[0154] As illustrated in FIGS. 11, 12a, and 12b, one pixel PXL may include first to third sub-pixels SP1 to SP3. Each of the first to third sub-pixels SP1 to SP3 may include an emission area EMA that emits light, and a peripheral area PPA that is positioned around the emission area EMA.

[0155] Each of the first to third sub-pixels SP1 to SP3 may include a pixel circuit layer PCL disposed on the substrate SUB, and a display element layer DPL disposed on the pixel circuit layer PCL.

[0156] The pixel circuit layer PCL of each of the first to third sub-pixels SP1 to SP3 may include a buffer layer BFL disposed on the substrate SUB, first and second

transistors T1 and T2 disposed on the buffer layer BFL, a driving voltage line DVL, and a passivation layer PSV provided on the first and second transistors T1 and T2 and the driving voltage line DVL.

[0157] The substrate SUB may include an insulating material such as glass, an organic polymer, or crystal. Furthermore, the substrate SUB may be made of a material having flexibility so as to be bendable or foldable, and have a single-layer or multi-layer structure.

[0158] The buffer layer BFL may be provided on the substrate SUB and prevent impurities from diffusing into the first or second transistor T1 or T2. The buffer layer BFL may be omitted depending on the material of the substrate SUB or processing conditions.

[0159] The first transistor T1 may be a driving transistor that is electrically coupled to some of the light emitting elements LD provided on the display element layer DPL of a corresponding sub-pixel to drive the light emitting elements LD, and the second transistor T2 may be a switching transistor that switches the first transistor T1.

[0160] Each of the first and second transistors T1 and T2 may include a semiconductor layer SCL, a gate electrode GE, a source electrode SE, and a drain electrode DE.

[0161] The semiconductor layer SCL may be disposed on the buffer layer BFL. The semiconductor layer SCL may include a source area which comes into contact with the source electrode SE, and a drain area which comes into contact with the drain electrode DE. An area between the source area and the drain area may be a channel area.

[0162] The semiconductor layer SCL may be a semiconductor pattern formed of polysilicon, amorphous silicon, an oxide semiconductor, etc. The channel area may be an intrinsic semiconductor, which is a semiconductor pattern which is not doped with impurities. Each of the source area and the drain area may be a semiconductor pattern doped with impurities.

[0163] The gate electrode GE may be provided on the semiconductor layer SCL with a gate insulating layer GI interposed therebetween. Moreover, the source electrode SE and the drain electrode DE may respectively come into contact with the source area and the drain area of the semiconductor layer SCL through corresponding contact holes which pass through an interlayer insulating layer ILD and the gate insulating layer GI.

[0164] The driving voltage line DVL may be provided on the interlayer insulating layer ILD, but the present disclosure is not limited thereto. In an embodiment, the driving voltage line may be provided on any one of insulating layers included in the pixel circuit layer PCL. The second driving power supply VSS (FIG. 10a) may be applied to the driving voltage line DVL.

[0165] The passivation layer PSV may include a first contact hole CH1 that exposes a portion of the drain electrode DE of the first transistor T1, and a second contact hole CH2 that exposes a portion of the driving voltage line DVL.

[0166] The display element layer DPL of each of the first to third sub-pixels SP1 to SP3 may include a partition wall PW provided on the passivation layer PSV, first and second electrodes REL1 and REL2, first and second coupling lines CNL1 and CNL2, a plurality of light emitting elements LD, and first and second contact electrodes CNE1 and CNE2.

[0167] The partition wall PW may be provided on the passivation layer PSV in the emission area EMA of each of the first to third sub-pixels SP1 to SP3. Although not illustrated in the drawings, a pixel defining layer (or dam portion) made of the same material as the partition wall PW may be disposed in the peripheral area PPA between adjacent sub-pixels to define the emission area EMA of each sub-pixel.

[0168] The partition wall PW may be spaced apart from the adjacent partition wall PW on the passivation layer PSV by a predetermined distance. Two adjacent partition walls PW may be disposed on the passivation layer PSV to be spaced apart from each other by a length L (FIG. 1a) or more of one light emitting element LD. As illustrated in FIG. 12a, the partition wall PW may include a curved surface having a cross-section such as a semicircle or a semi-ellipse whose width is narrowed from one surface of the passivation layer PSV toward the top, but the present disclosure is not limited thereto. For example, the partition wall PW may have a cross-section of a trapezoid whose width is narrowed from one surface of the passivation layer PSV toward the top.

[0169] When viewed in a cross-section, the shape of the partition wall PW is not limited to the above-described embodiments, and may be variously changed within a range capable of improving the efficiency of light emitted from each of the light emitting elements LD. Two adjacent partition walls PW may be disposed on the same plane of the passivation layer PSV, and may have the same height.

[0170] The light emitting elements LD may be disposed in the emission area EMA of each of the first to third sub-pixels SP1 to SP3. In detail, the light emitting elements LD may be disposed on the first insulating layer INS1 disposed between the partition walls PW adjacent to each other.

[0171] Each of the light emitting elements LD may be a light emitting element LD of FIG. 1a which is made of material having an inorganic crystal structure and has a subminiature size, e.g., a size in the range from the nanometer scale to the micrometer scale.

[0172] Each of the light emitting elements LD may include an emission stacked pattern 10 formed by sequentially stacking a first conductive semiconductor layer 11, an active layer 12, a second conductive semiconductor layer 13, and an electrode layer 15 in the longitudinal direction L (FIG. 1a) of each light emitting element LD, and an insulating film 14 surrounding an outer surface 10a of the emission stacked pattern 10.

[0173] In the drawing, the insulating film 14 is disposed to completely surround the outer surface of the emission

stacked pattern 10. However, the insulating film 14 may be disposed to expose a portion of the outer surface 10a of the emission stacked pattern 10. In this case, the insulating film 14 may be disposed to completely surround the active layer 12, and may expose portions of the first conductive semiconductor layer 11, the second conductive semiconductor layer 13, and the electrode layer 15.

[0174] The thickness of the insulating film 14 may be non-uniform. To this end, the insulating film 14 may have an outer surface different from the outer surface of the emission stacked pattern 10. For example, when the outer surface 10a of the emission stacked pattern 10 has a circular shape, the outer surface 14a of the insulating film 14 may have an elliptical shape, a polygonal shape, or a shape in which an ellipse and a polygon are mixed. In the drawing, the outer surface 14a of the insulating film 14 has the elliptical shape.

[0175] The light emitting element LD may have a first end EP1 and a second end EP2 in the longitudinal direction L (FIG. 1a). For example, the first conductive semiconductor layer 11 may be disposed on the first end EP1 of each light emitting element LD, and the electrode layer 15 may be disposed on the second end EP2 thereof.

[0176] Furthermore, both ends EP1 and EP2 of each light emitting element LD may be electrically coupled to the first and second electrodes REL1 and REL2. To this end, the light emitting elements LD may be arranged in the first direction DR1 that is a horizontal direction so that both ends of each light emitting element are coupled to the first and second electrodes REL1 and REL2. Here, the light emitting elements LD may be disposed to be spaced apart from each other, or may be disposed to be partially adjacent to each other.

[0177] Each of the first and second electrodes REL1 and REL2 may be provided in the emission area EMA of each of the first to third sub-pixels SP1 to SP3, and may extend in a second direction DR2 crossing the first direction DR1. The first and second electrodes REL1 and REL2 may be provided on the same plane, and may be spaced apart from each other by a predetermined distance.

[0178] The first electrode REL1 may include a 1-1-th electrode REL1_1 and a 1-2-th electrode REL1_2 branched along the second direction DR2 from the first coupling line CNL1 extending in the first direction DR1. The 1-1-th electrode REL1_1, the 1-2-th electrode REL1_2, and the first coupling line CNL1 may be integrally provided to be electrically and/or physically coupled to each other. The 1-1-th electrode REL1_1 and the 1-2-th electrode REL1_2 may be electrically coupled to the 1-1-th contact electrode CNE1_1 and the 1-2-th contact electrode CNE1_2 through a 1-1-th encapsulation layer CPL1_1 and a 1_2-th encapsulation layer CPL1_2, respectively.

[0179] The second electrode REL2 may extend in the second direction DR2, and may be electrically coupled to the second coupling line CNL2. In an embodiment of the present disclosure, the second electrode REL2 may be branched from the second coupling line CNL2 along the second direction DR2. Thus, the second electrode REL2 and the second coupling line CNL2 may be integrally provided to be electrically and/or physically coupled to each other. Furthermore, the second electrode REL2 may also be electrically coupled to the second contact electrode CNE2 through a second encapsulation layer CPL2.

[0180] The 1-1-th encapsulation layer CPL1_1, the 1_2-th encapsulation layer CPL1_2, and the second encapsulation layer CPL2 prevent the first electrode REL1 and the second electrode REL2 from being damaged, in the process of manufacturing the display device. However, the 1-1-th electrode REL1_1 and the 1-2-th electrode REL1_2 may be electrically coupled to the 1-1-th contact electrode CNE1_1 and the 1-2-th contact electrode CNE1_2 without the 1-1-th encapsulation layer CPL1_1 and the1_2-th encapsulation layer CPL1_2. Furthermore, the second electrode REL2 may also be directly coupled to the second contact electrode CNE2.

[0181] Each of the first and second electrodes REL1 and REL2 may function as an alignment electrode for aligning the light emitting elements LD in the emission area EMA of each of the first to third sub-pixels SP1 to SP3, and may function as a driving electrode for driving the light emitting elements LD after the light emitting elements LD are aligned.

[0182] To be more specific, before the light emitting elements LD are aligned in the emission area EMA of each of the first to third sub-pixels SP1 to SP3, a first alignment voltage may be applied through the first coupling line CNL1 to the first electrode REL1, and a second alignment voltage may be applied through the second coupling line CNL2 to the second electrode REL2. The first alignment voltage and the second alignment voltage may have different voltage levels. As predetermined alignment voltages having different voltage levels are applied to the first electrode REL1 and the second electrode REL2, respectively, an electric field may be formed between the first electrode REL1 and the second electrode REL2. The light emitting elements LD may be aligned on the passivation layer PSV between the first electrode REL1 and the second electrode REL2 by the electric field.

[0183] When viewed on a plane, the second electrode REL2 may be provided between the 1-1-th electrode REL1_1 and the 1-2-th electrode REL1_2, and the second electrode REL2 may be spaced apart from the 1-1-th electrode REL1_1 and the 1-2-th electrode REL1_2 by a predetermined distance. The 1-1-th electrode REL1_1, the 1-2-th electrode REL1_2, and the second electrode REL2 may be alternately disposed on the passivation layer PSV.

[0184] The first and second electrodes REL1 and REL2 may be made of a material having a predetermined reflectivity to allow light emitted from both ends EP1 and EP2 of each of the light emitting elements LD to proceed in a direction (e.g. front direction) in which an image of the display device is displayed.

[0185] In an embodiment of the present disclosure, the first and second electrodes REL1 and REL2, the first coupling line CNL1, and the second coupling line CNL2 may be provided on the same layer, and may be made of the same material.

[0186] Each of the first and second electrodes REL1 and REL2, the first coupling line CNL1, and the second coupling line CNL2 may be made of a conductive material having a predetermined reflectivity. The conductive material may include metal such as Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, Ti, or an alloy of them, a conductive oxide such as an indium tin oxide (ITO), an indium zinc oxide (IZO), a zinc oxide (ZnO), or an indium tin zinc oxide (ITZO), and a conductive polymer such as PEDOT. The material of each of the first and second electrodes REL1 and REL2, the first coupling line CNL1, and the second coupling line CNL2 is not limited to the above-described materials.

[0187] Although each of the first and second electrodes REL1 and REL2, the first coupling line CNL1, and the second coupling line CNL2 may be formed of a single layer, but the present disclosure is not limited thereto. It may have a multi-layer structure formed by stacking two or more layers each including metal, an alloy, a conductive oxide, or a conductive polymer.

[0188] Each of the first and second electrodes REL1 and REL2, the first coupling line CNL1, and the second coupling line CNL2 may be formed of a multi-layer structure so as to minimize a voltage drop due to signal delay when a signal is transmitted to both ends EP1 and EP2 of each of the light emitting elements LD.

[0189] Since the first and second electrodes REL1 and REL2 have a shape corresponding to that of the partition wall PW, light emitted from both ends EP1 and EP2 of each of the light emitting elements LD may be reflected by the first and second electrodes REL1 and REL2 to further proceed to the front of the display device. Therefore, the efficiency of light emitted from each of the light emitting elements LD may be enhanced.

[0190] In an embodiment of the present disclosure, the partition wall PW and the first and second electrodes REL1 and REL2 may serve as a reflective member that causes light emitted from each of the light emitting elements LD to proceed to the front of the display device, thus improving the light emission efficiency of the light emitting elements LD.

[0191] Any one of the first and second electrodes REL1 and REL2 may be an anode electrode, and the other may be a cathode electrode. In an embodiment of the present disclosure, the first electrode REL1 may be an anode electrode, and the second electrode REL2 may be a cathode electrode.

[0192] In an embodiment of the present disclosure, the light emitting elements LD may be divided into a plurality of first light emitting elements LD1 aligned between the 1-1-th electrode REL1_1 and the second electrode REL2, and a plurality of second light emitting elements LD2 aligned between the second electrode REL2 and the 1-2-th electrode REL 1_2.

[0193] In an embodiment of the present disclosure, the first coupling line CNL1 may be electrically coupled to the drain electrode DE of the first transistor T1 through the first contact hole CH1 of the passivation layer PSV. Since the first coupling line CNL1 is provided integrally with the first electrode REL1, a signal of the first transistor T1 applied to the first coupling line CNL1 may be transmitted to the first electrode REL1.

[0194] The first electrode REL1 may be disposed adjacent to one of both ends EP1 and EP2 of each of the light emitting elements LD, and may be electrically coupled to each of the light emitting elements LD through the first contact electrode CNE1. Thus, the signal of the first transistor T1 applied to the first electrode REL1 may be transmitted to each of the light emitting elements LD through the first contact electrode CNE1.

[0195] In an embodiment of the present disclosure, the second coupling line CNL2 may be electrically coupled to the driving voltage line DVL through the second contact hole CH2 of the passivation layer PSV. Since the second coupling line CNL2 is provided integrally with the second electrode REL2, the second driving power supply VSS of the driving voltage line DVL applied to the second coupling line CNL2 may be transmitted to the second electrode REL2.

[0196] The second electrode REL2 may be disposed adjacent to a remaining one of both ends EP1 and EP2 of each of the light emitting elements LD, and may be electrically coupled to each of the light emitting elements LD through the second contact electrode CNE2. Thus, the second driving power supply VSS applied to the second electrode REL2 may be transmitted to each of the light emitting elements LD.

[0197] A first contact electrode CNE1 may be provided on the first electrode REL1 to stably electrically and/or physically couple the first electrode REL1 and one of both ends EP1 and EP2 of each of the light emitting elements LD. The first contact electrode CNE1 may be made of a transparent conductive material so that light emitted from each of the light emitting elements LD and reflected to the front of the display device by the first electrode REL1 may proceed to the front without loss.

[0198] When viewed on a plane, the first contact electrode CNE1 may cover the first electrode REL1 and overlap with the first electrode REL1. Furthermore, the first contact electrode CNE1 may partially overlap with one of both ends EP1 and EP2 of each of the light emitting elements LD.

[0199] In an embodiment of the present disclosure, the first contact electrode CNE1 may include a 1-1-th contact electrode CNE1_1 provided on the 1-1-th encapsulation layer CPL1_1, and a 1-2-th contact electrode CNE1_2 provided on the 1-2-th encapsulation layer CPL1_2.

[0200] A third insulating layer IN3 may be provided on the first contact electrode CNE1 to cover the first contact electrode CNE1. The third insulating layer IN3 may prevent the first contact electrode CNE1 from being exposed

to the outside, thus preventing the first contact electrode CNE1 from being corroded.

[0201] The third insulating layer INS3 may include an inorganic insulating layer made of inorganic material or an organic insulating layer made of organic material. Although the third insulating layer INS3 may be formed of a single layer as shown in the drawing, the present disclosure is not limited thereto. For example, the third insulating layer INS3 may be formed of a multi-layer structure. When the third insulating layer INS3 is formed of the multi-layer structure, the third insulating layer INS3 may have a structure formed by alternately stacking a plurality of inorganic insulating layers or a plurality of organic insulating layers. For example, the third insulating layer INS3 may have a structure formed by sequentially stacking the first inorganic insulating layer, the organic insulating layer, and the second inorganic insulating layer.

[0202] A second contact electrode CNE2 may be provided on the second electrode REL2. When seen in a plan view, the second contact electrode CNE2 may cover the second electrode REL2 and overlap with the second electrode REL2. Furthermore, the second contact electrode CNE2 may overlap with the second end EP2 of each of the first light emitting elements LD1 and the first end EP1 of each of the second light emitting elements LD2. The second contact electrode CNE2 may be made of the same material as that of the first contact electrode CNE1, but the present disclosure is not limited thereto.

[0203] A fourth insulating layer IN4 may be provided on the second contact electrode CNE2 to cover the second contact electrode CNE2. The fourth insulating layer IN4 may prevent the second contact electrode CNE2 from being exposed to the outside, thus preventing the second contact electrode CNE2 from being corroded. The fourth insulating layer INS4 may be formed of either of an inorganic insulating layer or an organic insulating layer.

[0204] An overcoat layer OC may be provided on the fourth insulating layer INS4. The overcoat layer OC may be a planarization layer that reduces steps generated by the partition wall PW disposed under the overcoat layer, the first and second electrodes REL1 and REL2, and the first and second contact electrodes CNE1 and CNE2. The overcoat layer OC may be an encapsulation layer to prevent oxygen and moisture from penetrating into the light emitting elements LD. In an embodiment, the overcoat layer OC may be omitted.

[0205] A predetermined voltage may be applied to both ends EP1 and EP2 of each of the light emitting elements LD through the first electrode REL1 and the second electrode REL2. Thus, each of the light emitting elements LD may emit light while electron-hole pairs are combined in the active layer 12 of each of the light emitting elements LD. Here, the active layer 12 may emit light having a wavelength range of 400 nm to 900 nm.

[0206] Meanwhile, when the light emitting element LD has a cylindrical shape, the cross-section of the light emitting element LD may have a circular shape. In other words, the outer surface 14a of the insulating film 14 may have a circular shape. In this case, due to the characteristics of the cylinder, the thickness of each of the first and second contact electrodes CNE1 and CNE2 connected to both ends EP1 and EP2 of the light emitting element LD while partially surrounding both ends of the light emitting element LD is not uniform. For example, in an area A where the light emitting element LD and the first insulating layer INS1 are in contact with each other, the thickness of each of the first and second contact electrodes CNE1 and CNE2 may be reduced or there may be portions that are not partially formed, due to the characteristic of the cylinder.

[0207] However, when the outer surface 10a of the emission stacked pattern 10 is different in shape from the outer surface 14a of the insulating film 14 as in the embodiment of the present disclosure, the thickness of each of the first and second contact electrodes CNE1 and CNE2 is not reduced even in an area where the light emitting element LD is in contact with the first insulating layer INS1. FIG. 12b illustrates a portion where the 1-1-th contact electrode CNE1_1 and the light emitting element LD come into contact with each other.

[0208] Moreover, when the outer surface 14a of the insulating film 14 has a polygonal structure, a reduction in thickness of each of the first and second contact electrodes CNE1 and CNE2 can be efficiently prevented in a portion A where the light emitting element LD and the first insulating layer INS1 come into contact with each other.

[0209] FIGS. 13a and 13b are sectional views taken along line IV-IV of FIG. 11 including a light emitting element in accordance with another embodiment of the present disclosure.

[0210] When the outer surface 14a of the insulating film 14 has a triangular shape as illustrated in FIG. 13a or has a rectangular shape as illustrated in FIG. 13b, the first insulating layer INS1 is sufficiently exposed even in the portion A where the light emitting element LD is in contact with the first insulating layer INS1. Therefore, the 1-1-th contact electrode CNE1_1 may be formed to have a sufficient thickness in the portion A where the light emitting element LD comes into contact with the first insulating layer INS1.

[0211] Although the embodiments of the present disclose have been disclosed, those skilled in the art will appreciate that the present disclose can be implemented as other concrete forms, without departing from the scope of the disclose as disclosed in the accompanying claims. Therefore, it should be understood that the exemplary embodiments are only for illustrative purposes and do not limit the bounds of the present invention.

Claims

1. A light emitting element, comprising:

a rod-shaped emission stacked pattern including a first conductive semiconductor layer, an active layer disposed on the first conductive semiconductor layer, and a second conductive semiconductor layer disposed on the active layer; and
an insulating film surrounding an outer surface of the emission stacked pattern, and having a non-uniform thickness.

2. The light emitting element according to claim 1, wherein the outer surface of the emission stacked pattern is different in shape from an outer surface of the insulating film.

3. The light emitting element according to claim 2, wherein the emission stacked pattern has a shape of a cylinder formed by sequentially stacking the first conductive semiconductor layer, the active layer, and the second conductive semiconductor layer in a first direction, and
wherein the outer surface of the insulating film has an elliptical shape, a polygonal shape, and a shape in which the elliptical shape and the polygonal shape are mixed.

4. The light emitting element according to claim 3, wherein the outer surface of the insulating film comprises at least one protrusion.

5. The light emitting element according to claim 1, wherein the outer surface of the emission stacked pattern is equal in shape to an outer surface of the insulating film.

6. The light emitting element according to claim 5, wherein the outer surface of the emission stacked pattern and the outer surface of the insulating film each have a polygonal shape.

7. A method of manufacturing a light emitting element, comprising:

providing a substrate;
forming a rod-shaped emission stacked pattern on the substrate;
forming an insulating film surrounding an outer surface of the emission stacked pattern and having a non-uniform thickness; and
separating the emission stacked pattern, the emission stacked pattern being surrounded by the insulating film, from the substrate to form light emitting elements.

8. The method according to claim 7, wherein forming the insulating film comprises:

forming an insulating film pattern having an outer surface that has the same shape as the outer surface of the emission stacked pattern; and
forming an insulating film having an outer surface that is different in shape from the outer surface of the emission stacked pattern by removing at least a portion of the insulating film pattern.

9. The method according to claim 7, wherein, in forming the insulating film, the insulating film is formed to have an outer surface having an elliptical shape, a polygonal shape or a shape in which the elliptical shape and the polygonal shape are mixed to surround a cylindrical outer surface of the emission stacked pattern.

10. The method according to claim 9, wherein, in forming the insulating film, the outer surface of the insulating film includes at least one protrusion.

11. The method according to claim 7, wherein forming the emission stacked pattern comprises:

forming an emission stack on the substrate, the emission stack being formed by sequentially forming a first conductive semiconductor layer, an active layer, and a second conductive semiconductor layer;
forming a plurality of first micro patterns on the emission stack; and
forming a plurality of emission stacked patterns by etching the emission stack along the plurality of first micro patterns and removing the plurality of first micro patterns.

12. The method according to claim 11,
wherein forming the plurality of first micro patterns comprises:

forming a plurality of first resins on the emission stack;
providing the first resins to fill a plurality of first grooves of a first mold; and
forming the plurality of first micro patterns on the emission stack, by removing the first mold.

13. The method according to claim 12, wherein forming the insulating film comprises:

forming a plurality of second micro patterns on the emission stacked pattern and the insulating film pattern; and
forming the insulating film by etching the insulating film pattern along the plurality of second micro patterns.

14. The method according to claim 13, wherein forming the plurality of second micro patterns comprises:

forming a plurality of second reins on the emission stacked pattern and the insulating film pattern that surrounds the outer surface of the emission stacked pattern;
causing the second resins to fill a plurality of second grooves of a second mold; and
forming a plurality of second micro patterns on the emission stacked pattern and the insulating film pattern that surrounds the outer surface of the emission stacked pattern, by removing the second mold.

15. The method according to claim 14, wherein a shape of the first groove of the first mold is different from a shape of the second groove of the second mold.

16. The method according to claim 7, wherein, in forming the insulating film, the insulating film is formed to have the outer surface that is the same as the outer surface of the emission stacked pattern.

17. The method according to claim 16, wherein the outer surface of each of the emission stacked pattern and the insulating film is formed to have a polygonal shape.

18. A display device, comprising:

a substrate including a display area and a non-display area; and
a plurality of pixels provided in the display area of the substrate, and including a plurality of sub-pixels, respectively,
wherein each of the sub-pixels comprises a pixel circuit layer including at least one transistor, and a display element layer including an unit emission area that emits light,
wherein the display element layer includes at least one light emitting element provided on the substrate and configured to emitt light, first electrode and second electrode spaced apart from each other by a predetermined distance with the light emitting element being interposed therebetween, a first contact electrode electrically coupling the first electrode and a first end of the light emitting element, and a second contact electrode electrically coupling the second electrode and a second end of the light emitting element, and
wherein the light emitting element comprises:

an emission stacked pattern including a first conductive semiconductor layer, an active layer disposed on the first conductive semiconductor layer, and a second conductive semiconductor layer disposed on the active layer; and
an insulating film surrounding an outer surface of the emission stacked pattern, and having a non-uniform thickness.

19. The display device according to claim 18, wherein the outer surface of the emission stacked pattern is different in shape from an outer surface of the insulating film.

FIG. 1a

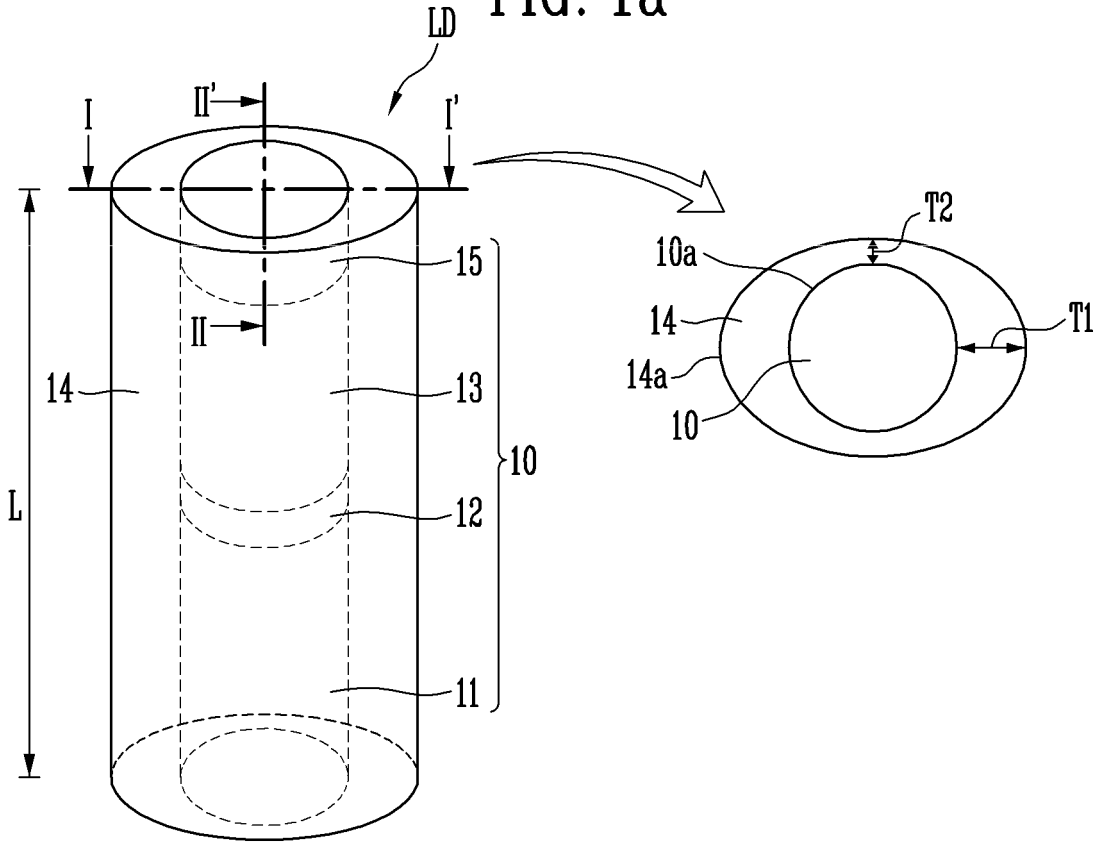


FIG. 1b

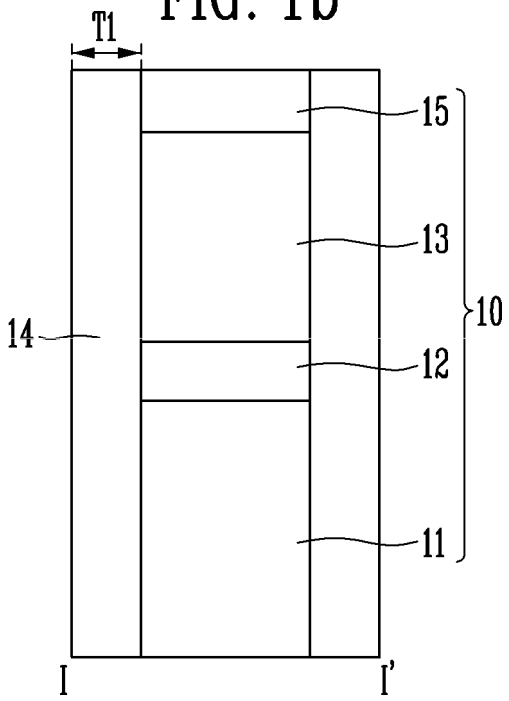


FIG. 1c

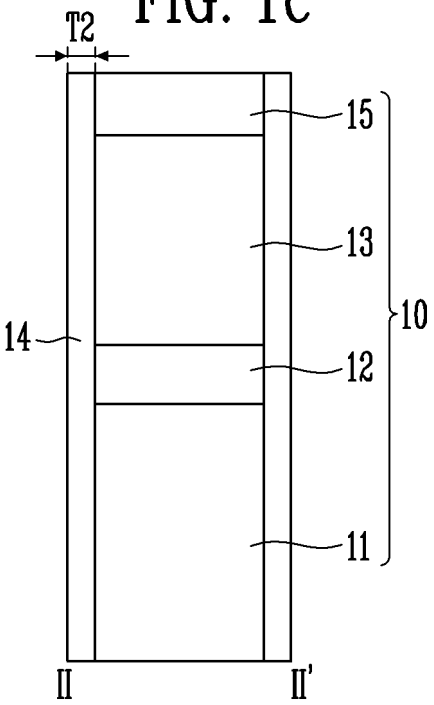


FIG. 2a

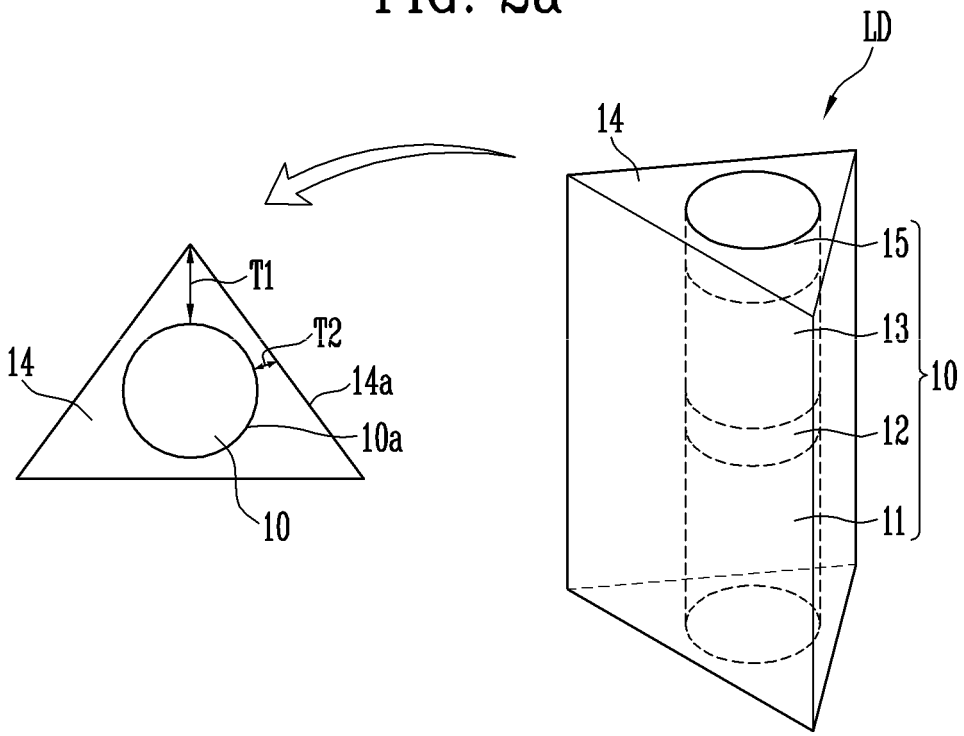


FIG. 2b

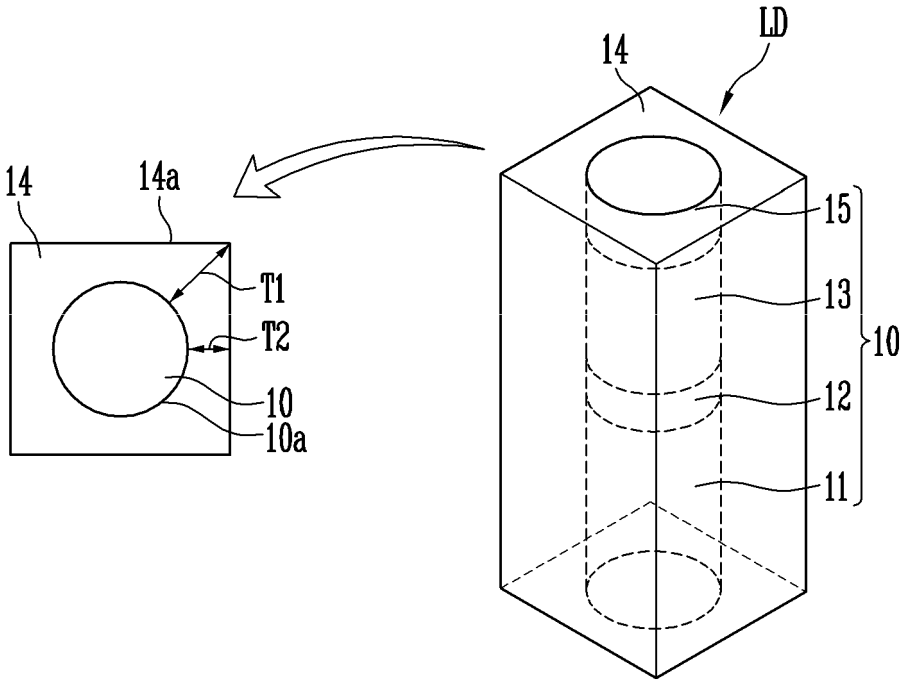


FIG. 2c

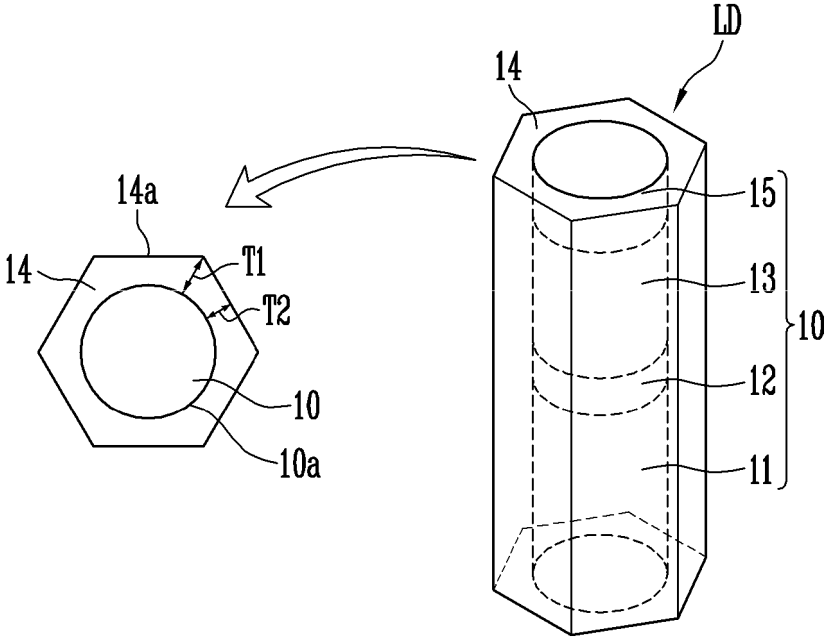


FIG. 2d

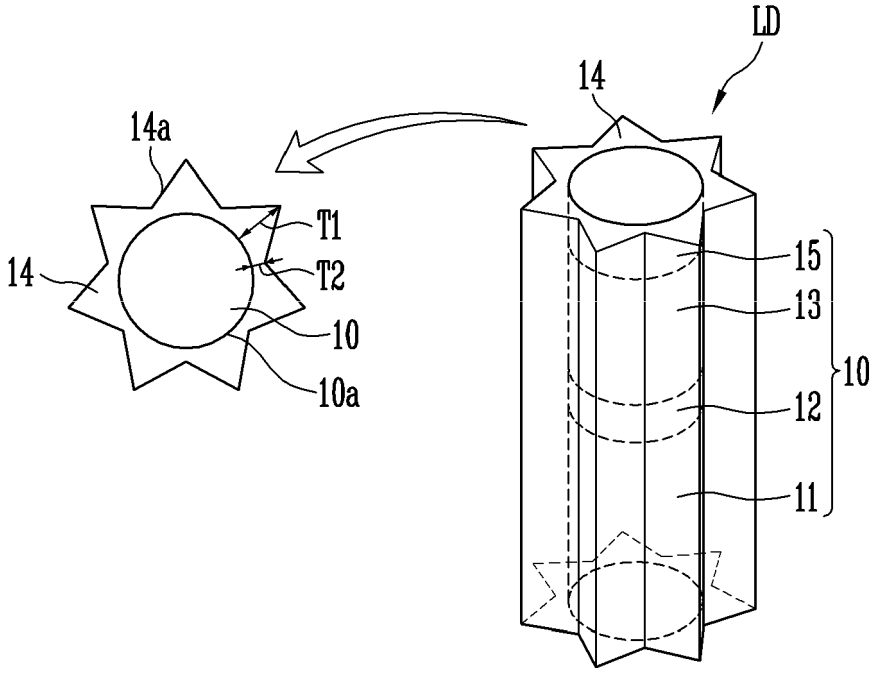


FIG. 3a

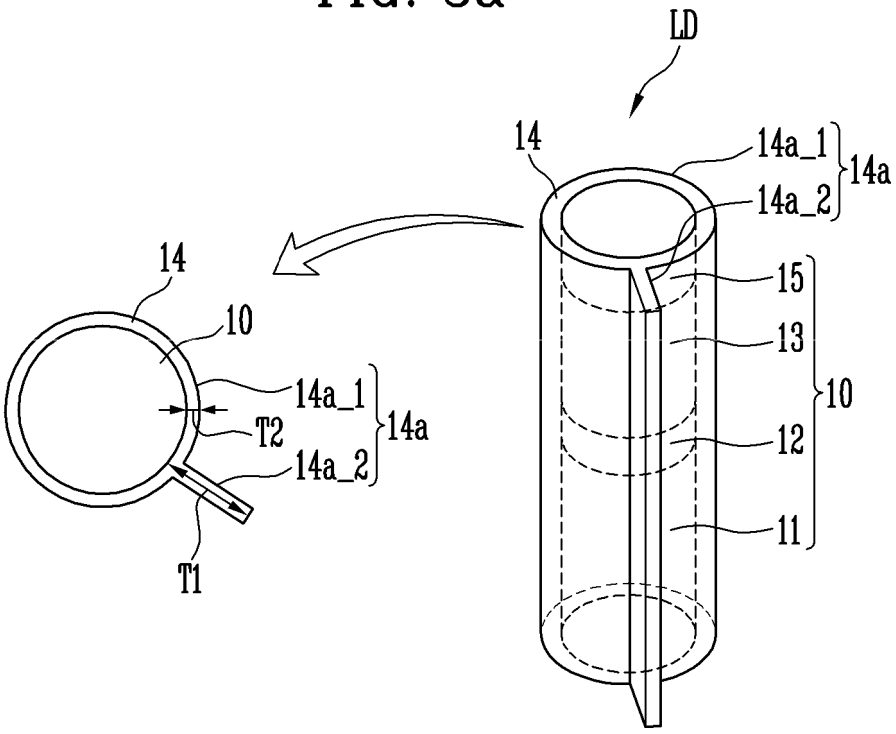


FIG. 3b

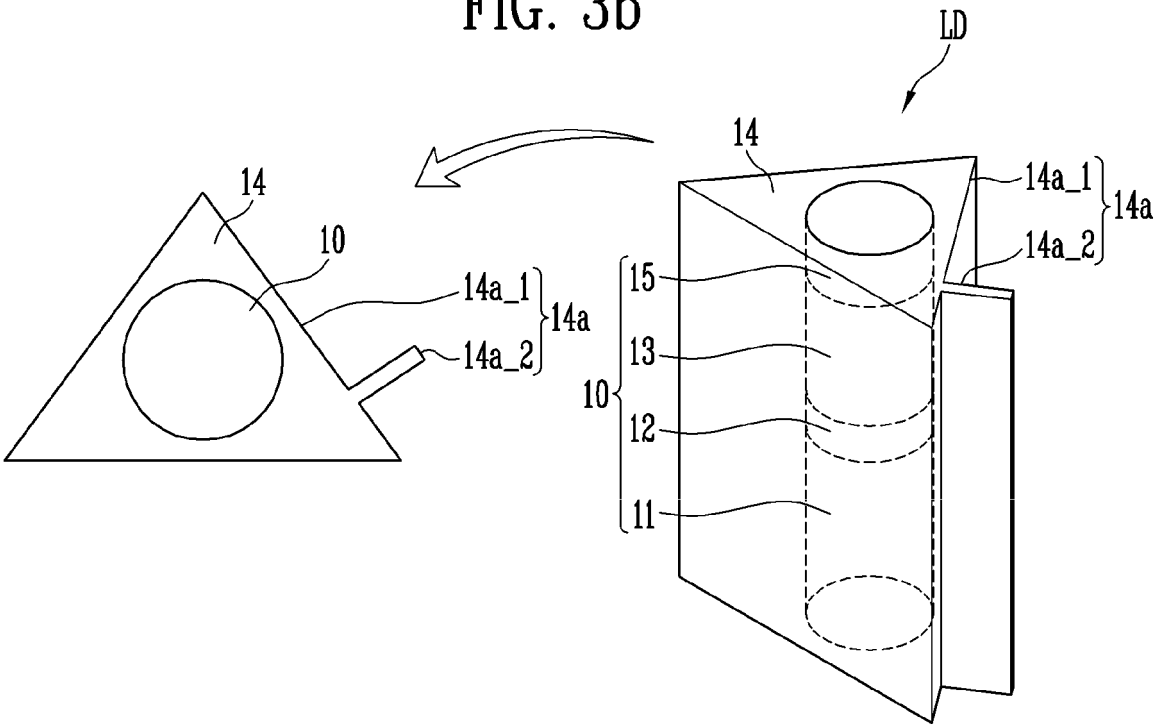


FIG. 3c

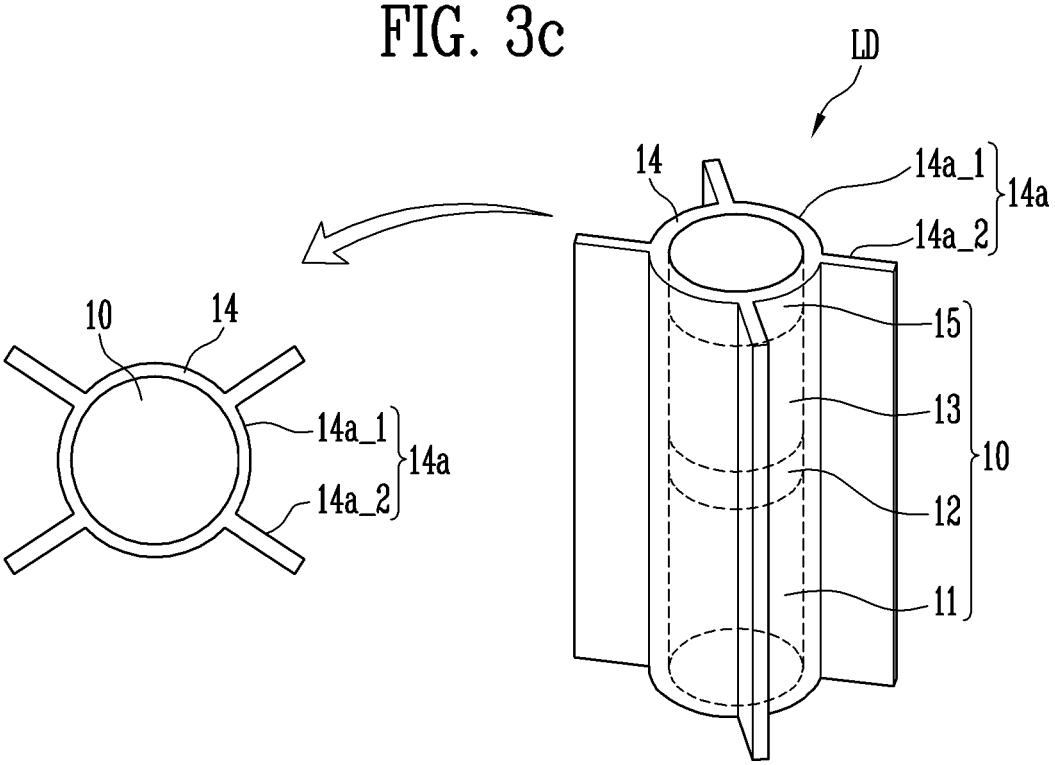


FIG. 4a

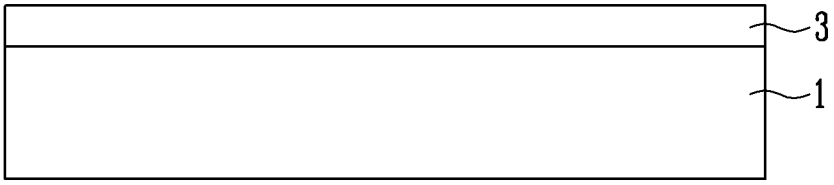


FIG. 4b

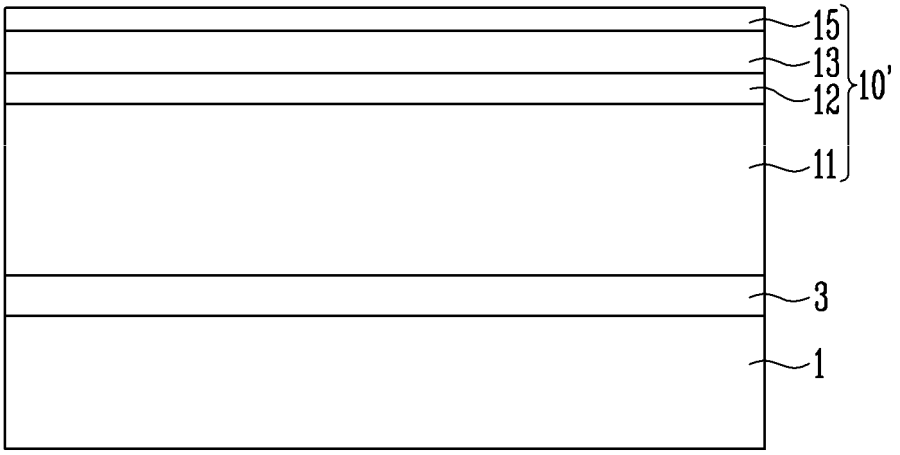


FIG. 4c

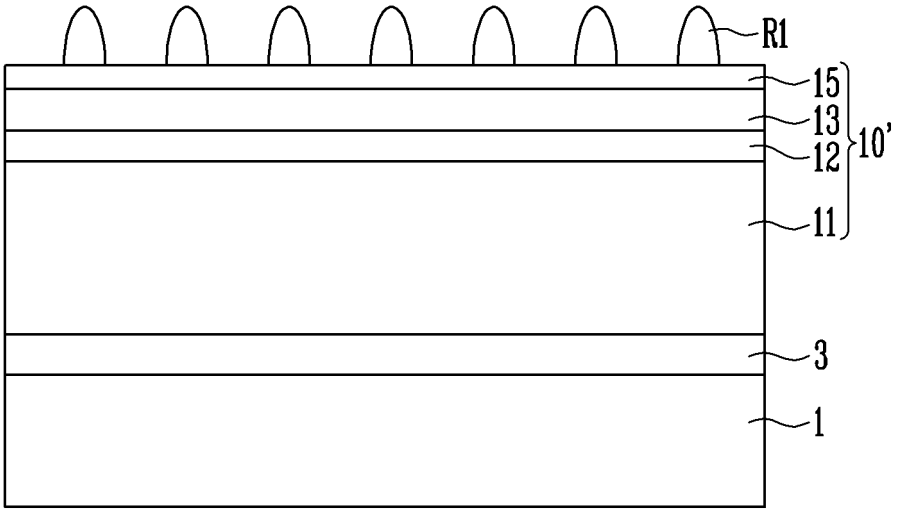


FIG. 4d

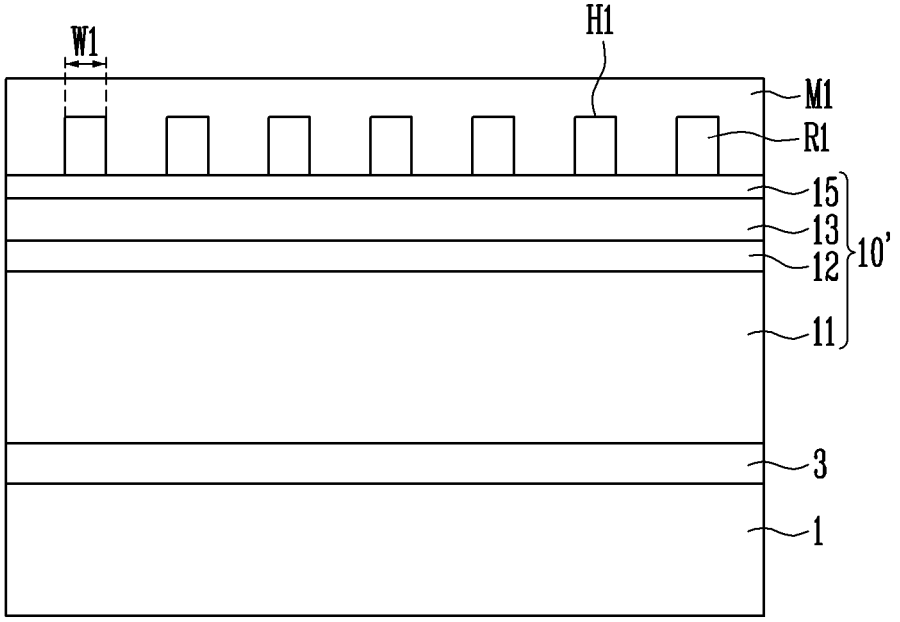


FIG. 4e

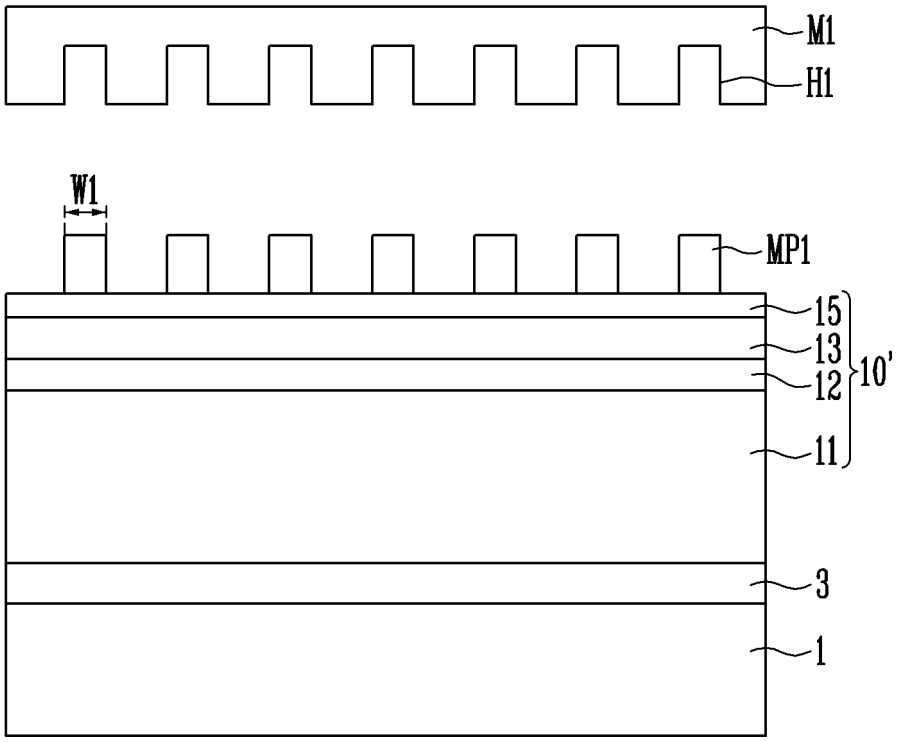


FIG. 4f

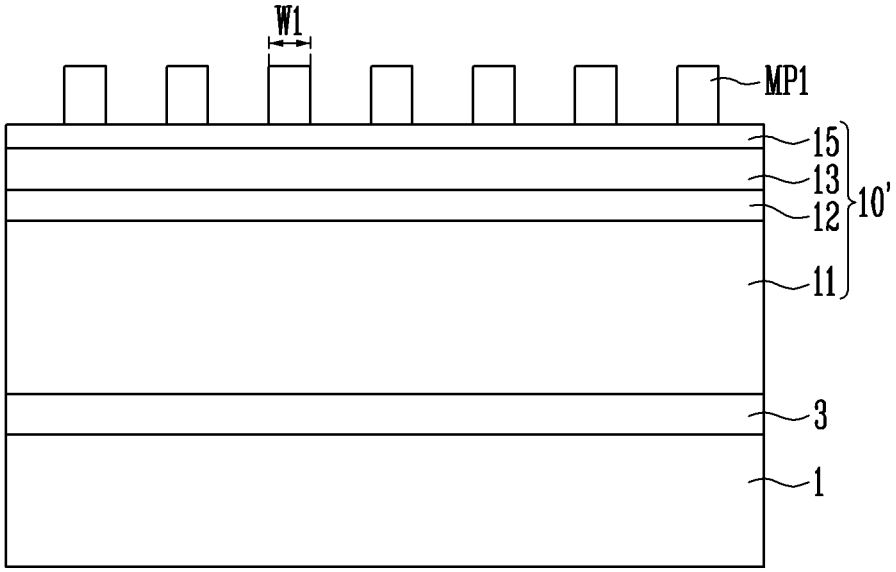


FIG. 4g

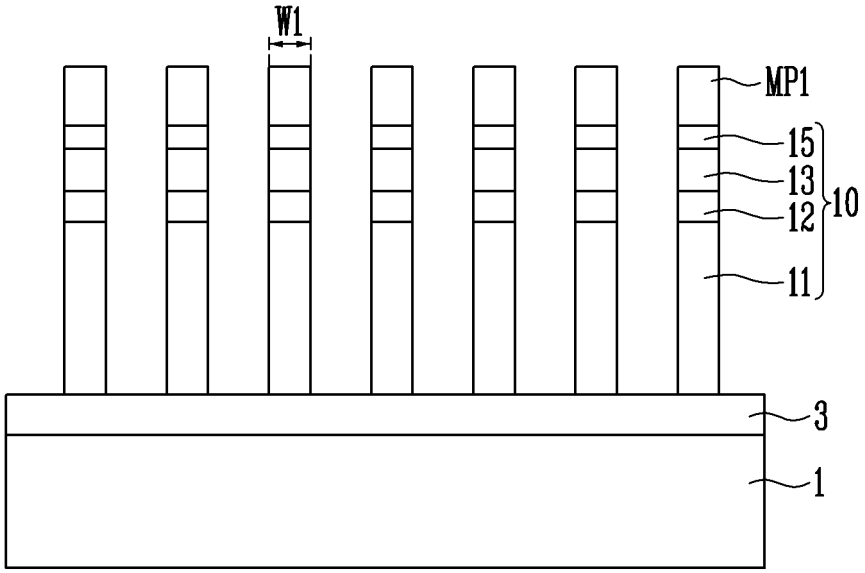


FIG. 4h

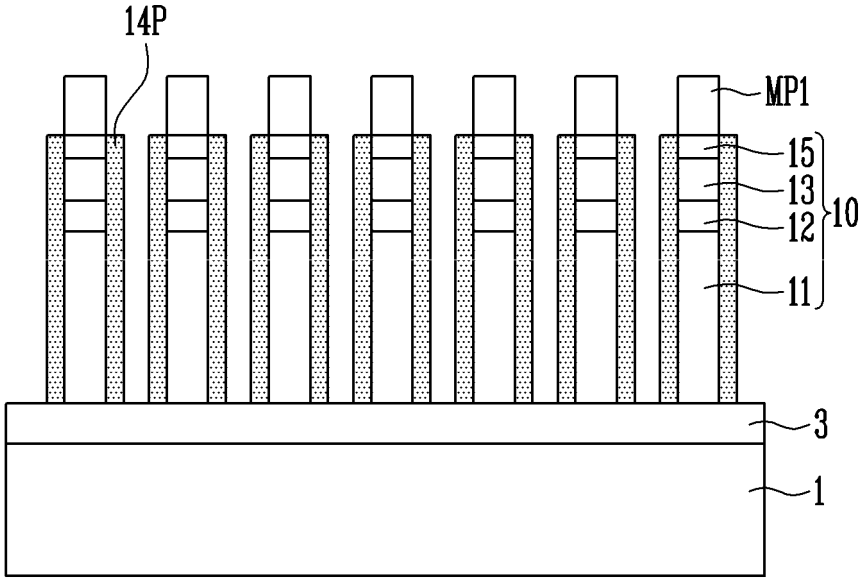


FIG. 4i

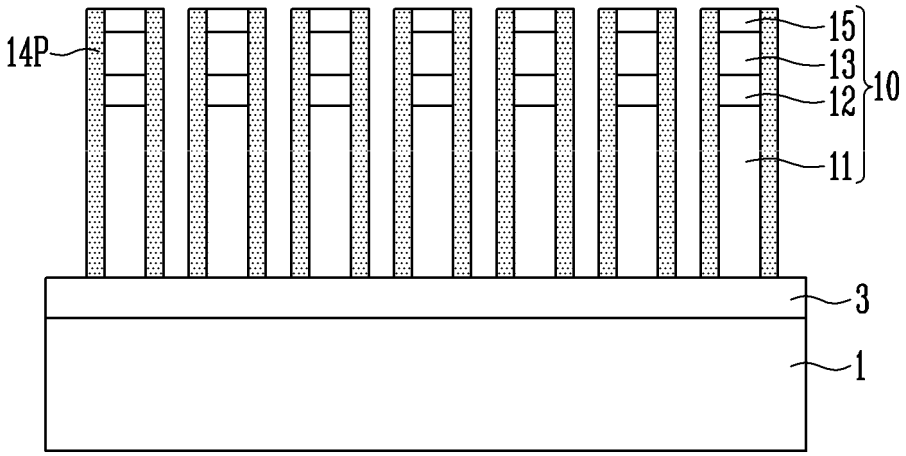


FIG. 4j

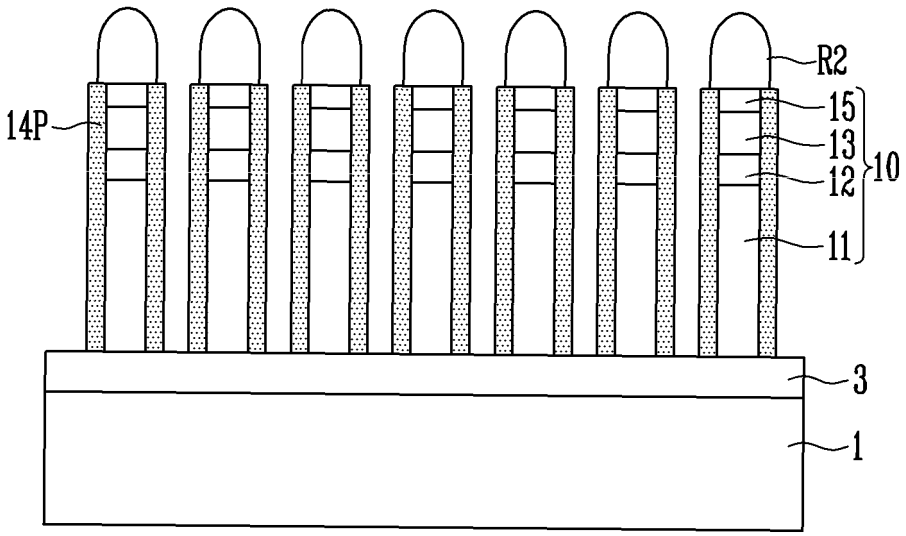


FIG. 4k

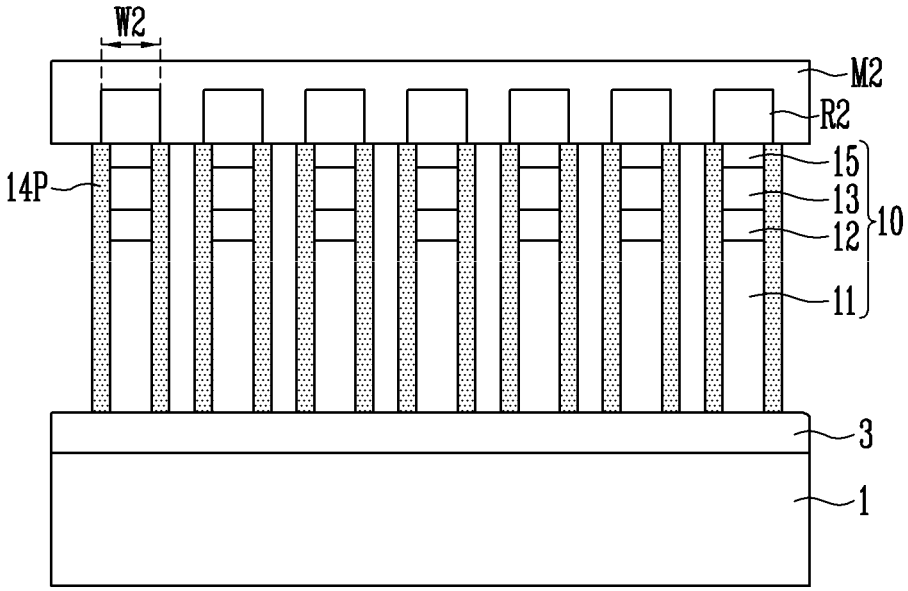


FIG. 41

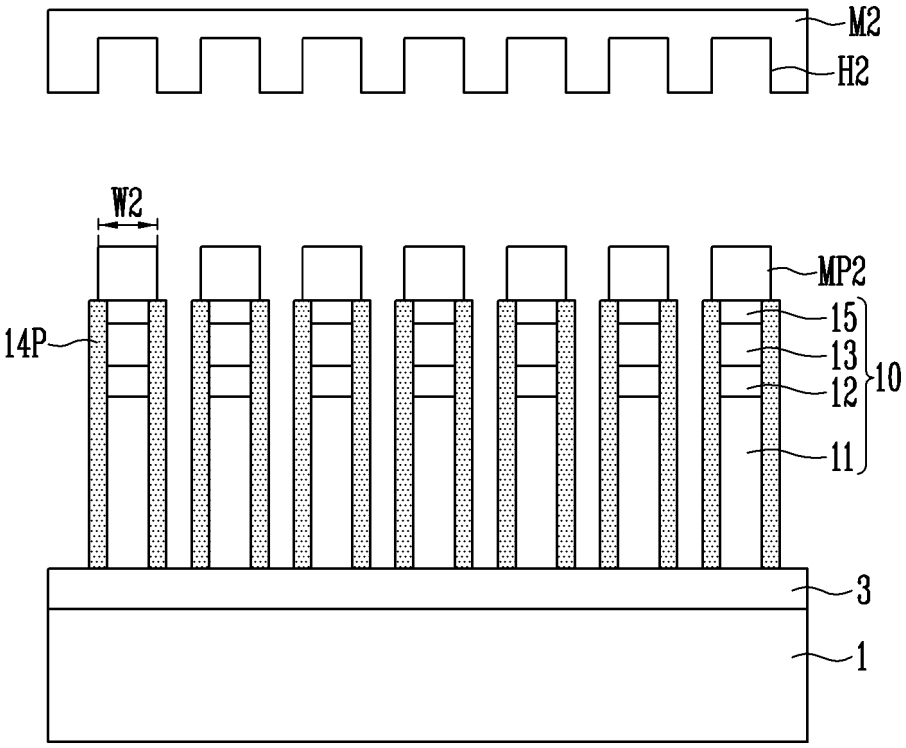


FIG. 4m

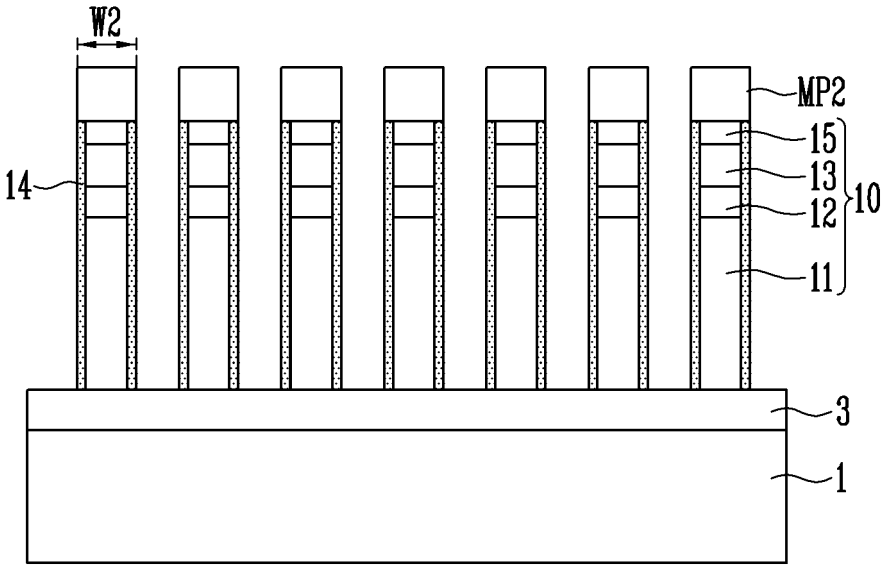


FIG. 4n

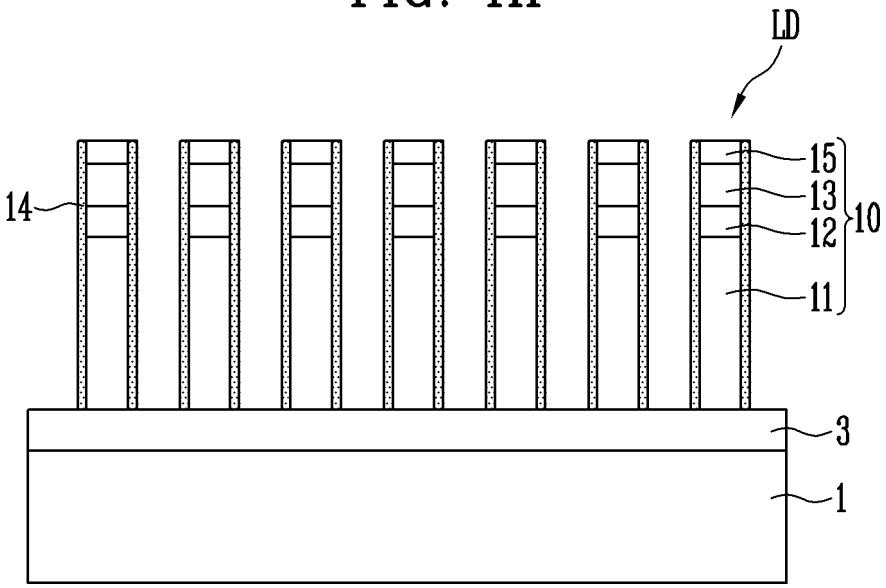


FIG. 4o

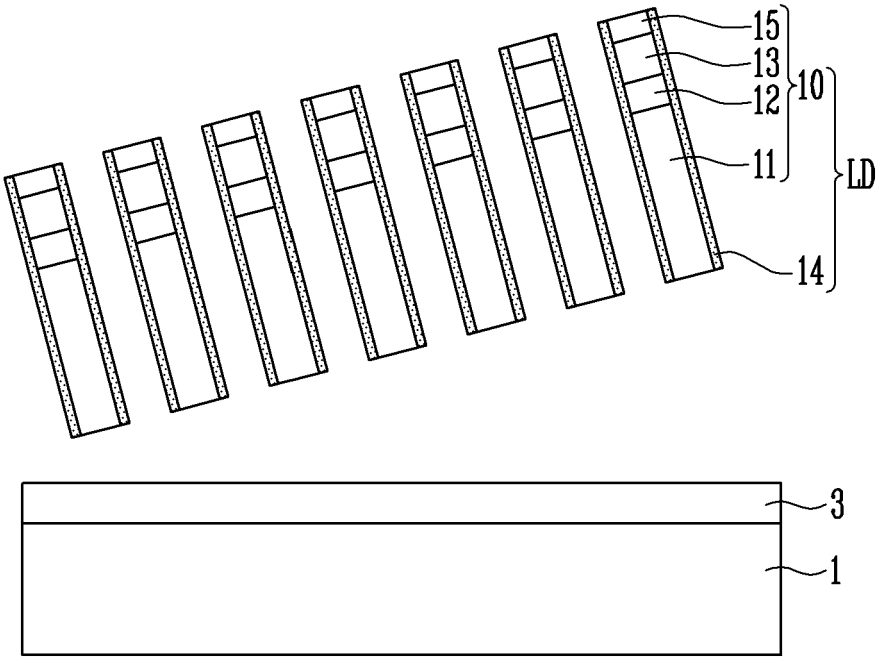


FIG. 5a

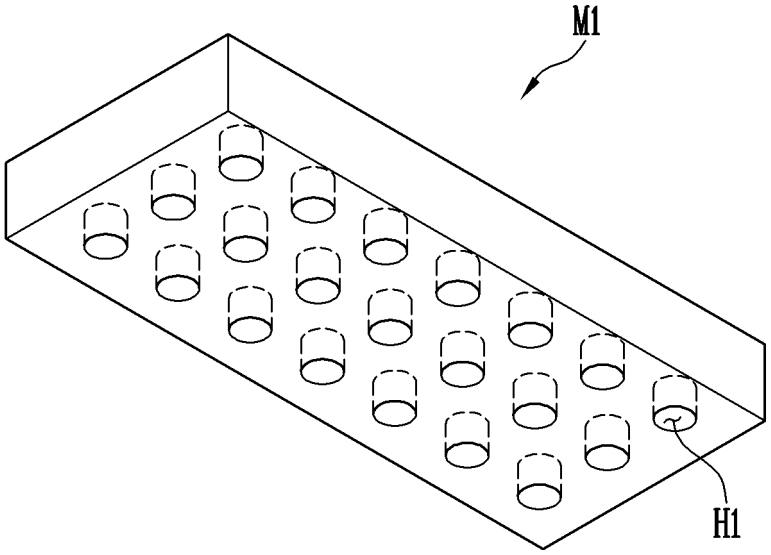


FIG. 5b

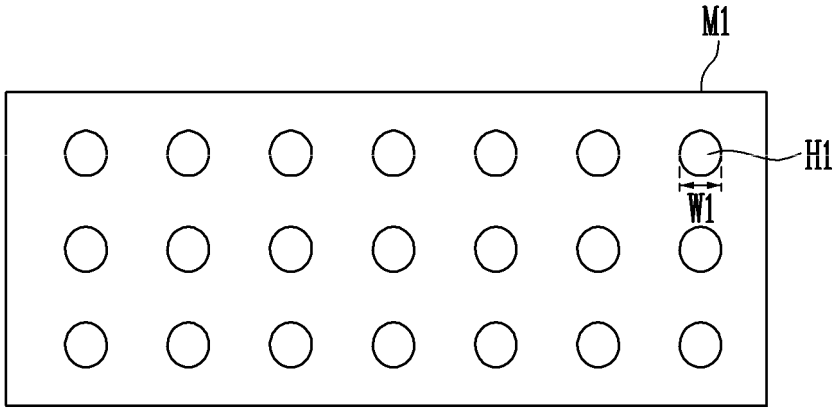


FIG. 6a

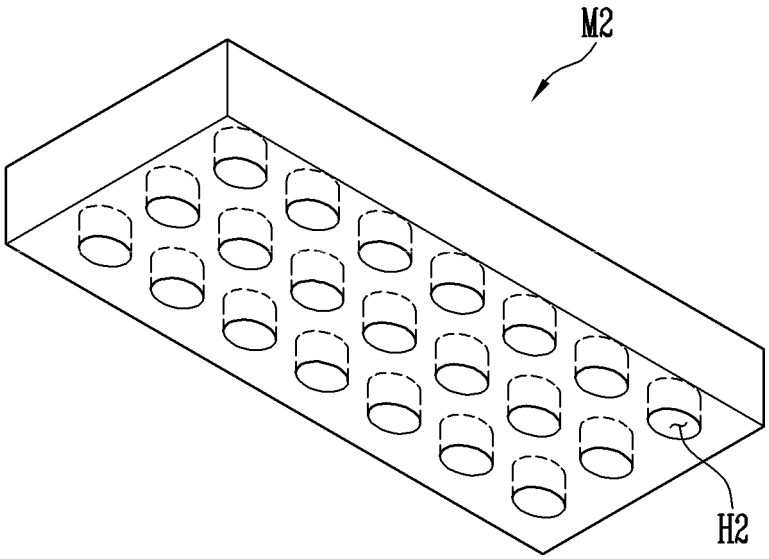


FIG. 6b

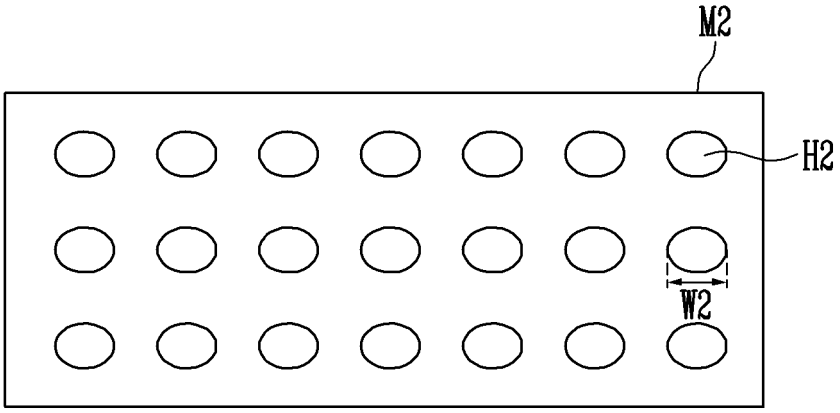


FIG. 7a

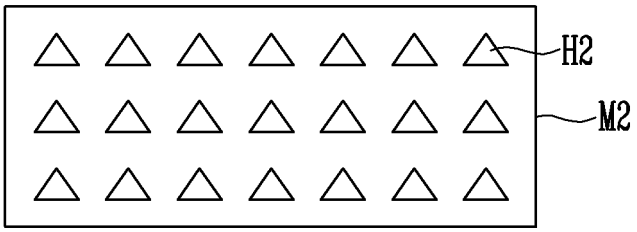


FIG. 7b

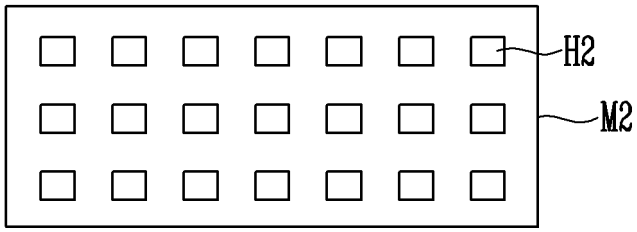


FIG. 7c

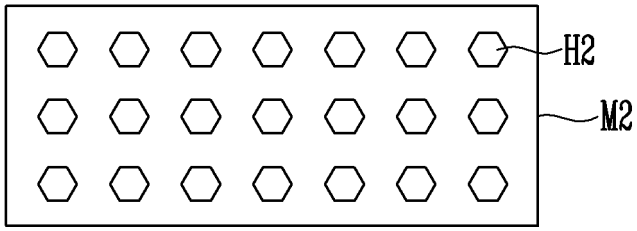


FIG. 7d

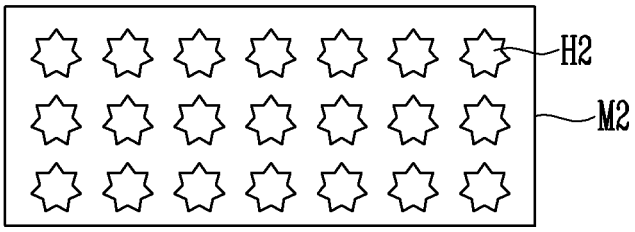


FIG. 7e

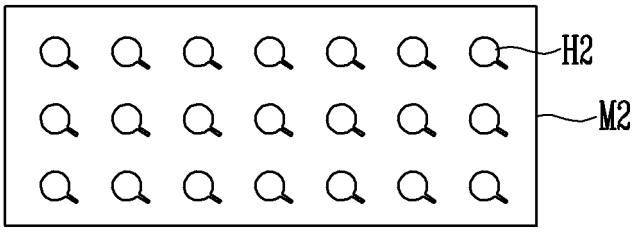


FIG. 7f

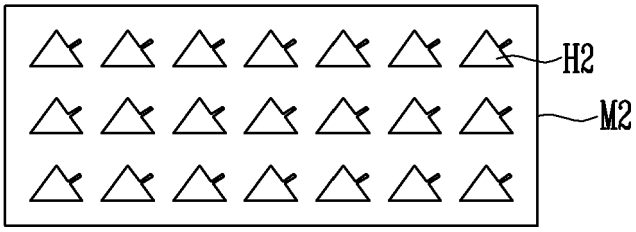


FIG. 7g

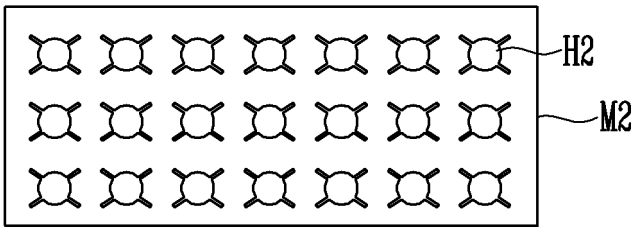


FIG. 8a

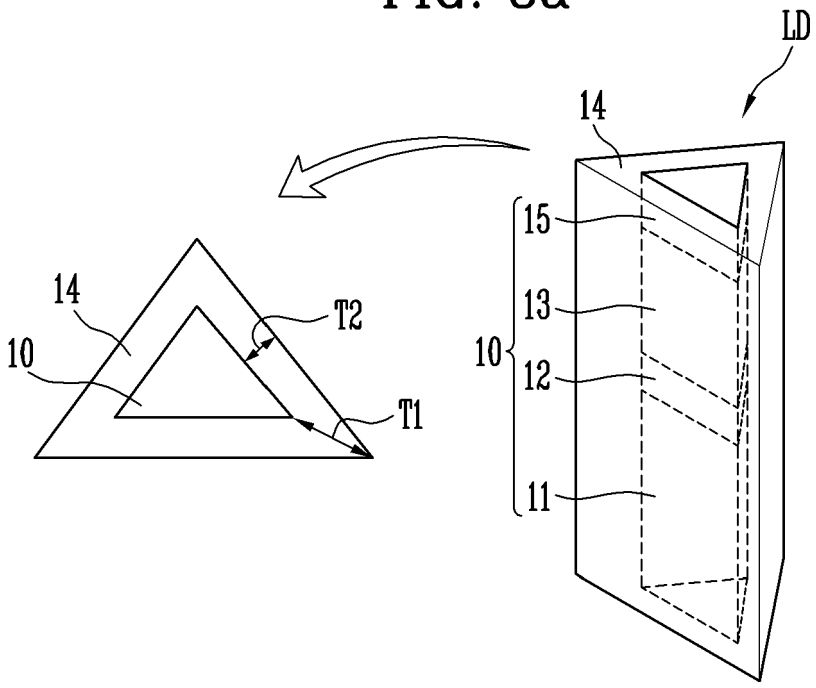


FIG. 8b

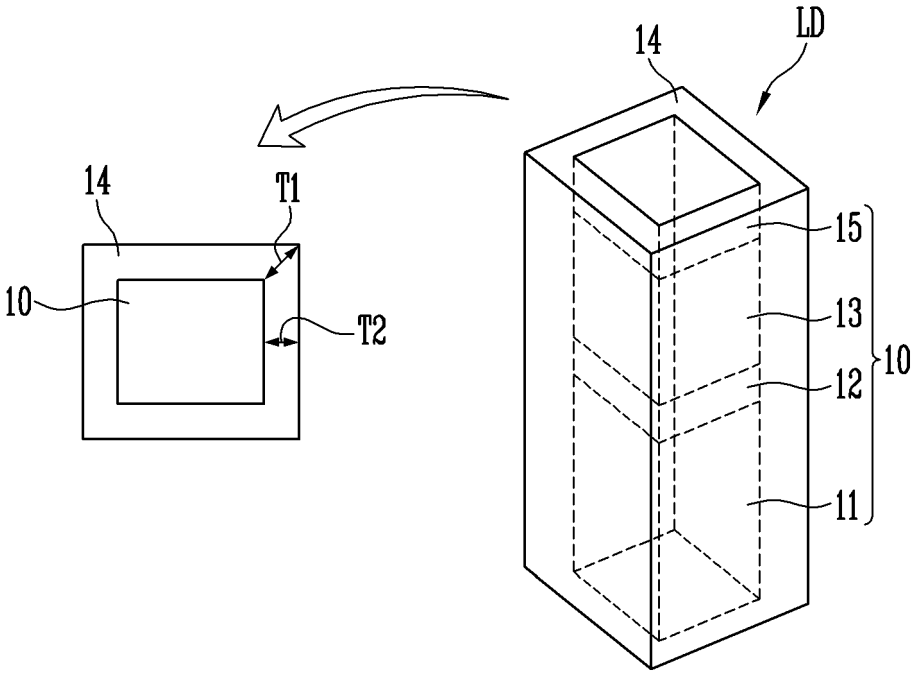


FIG. 9

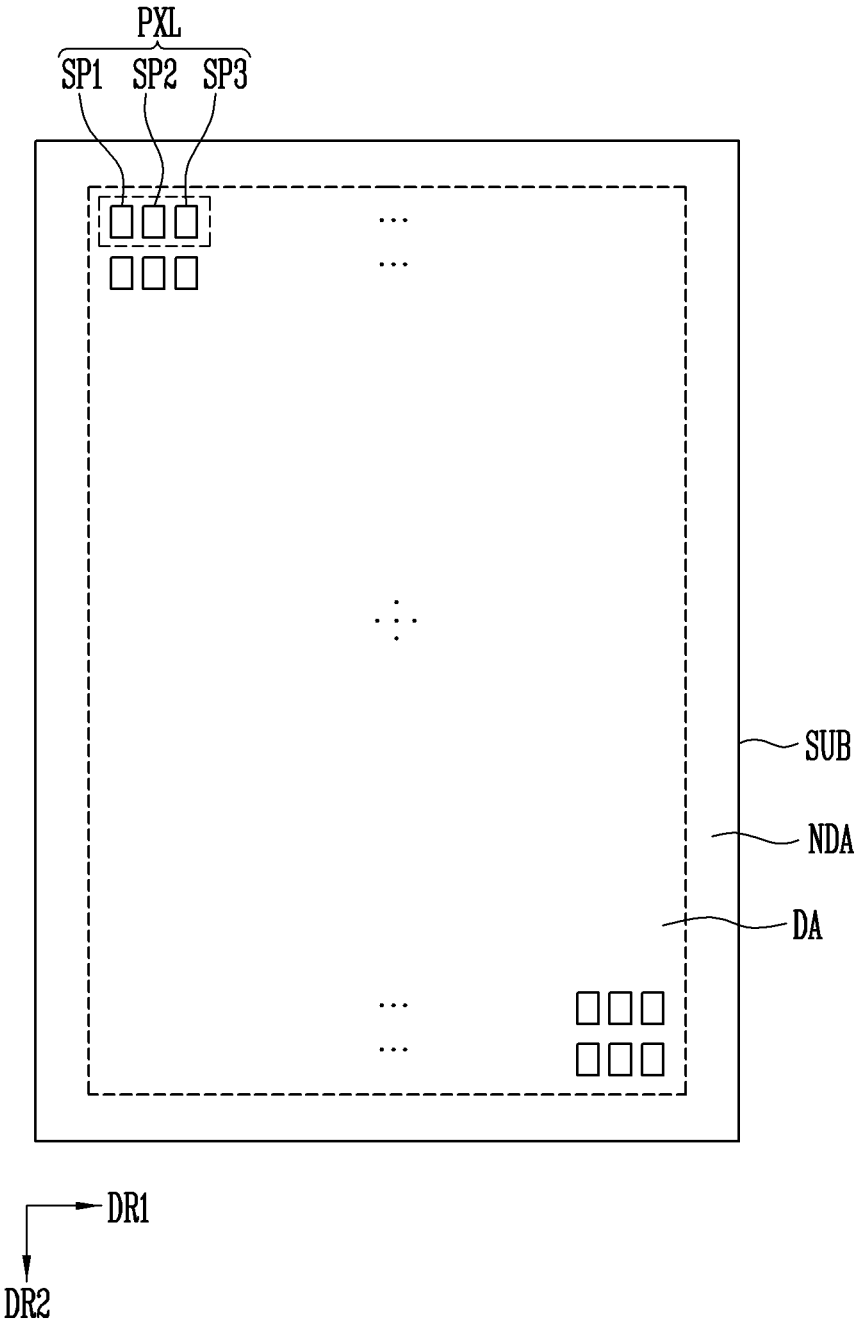


FIG. 10a

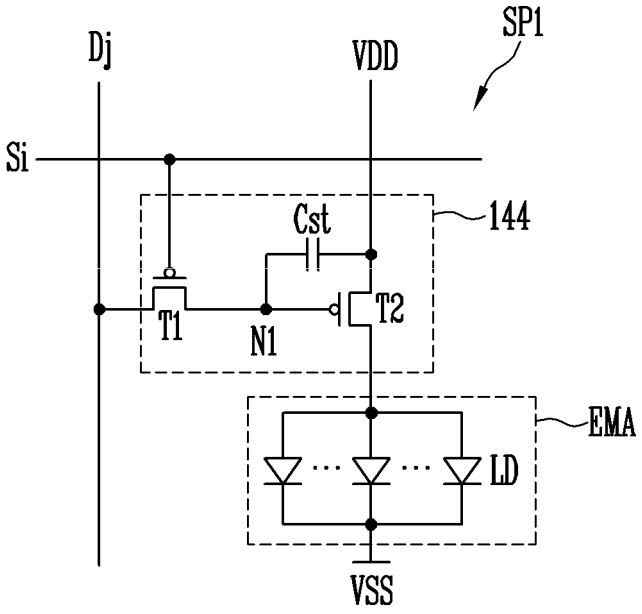


FIG. 10b

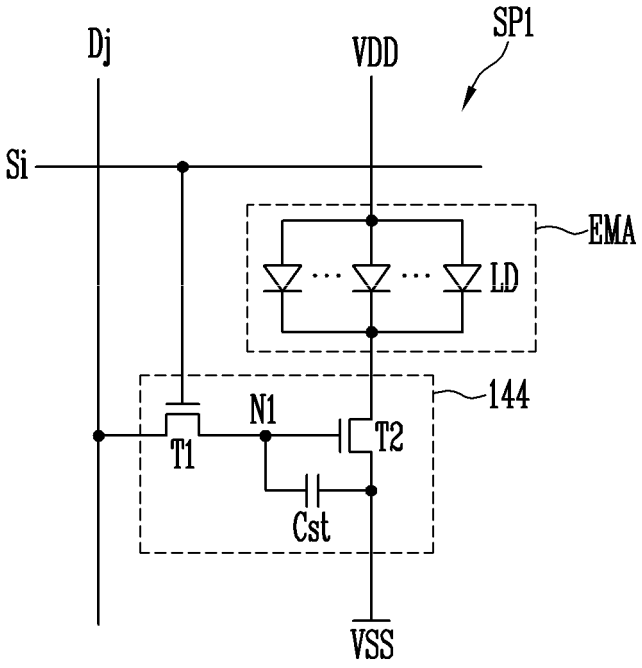
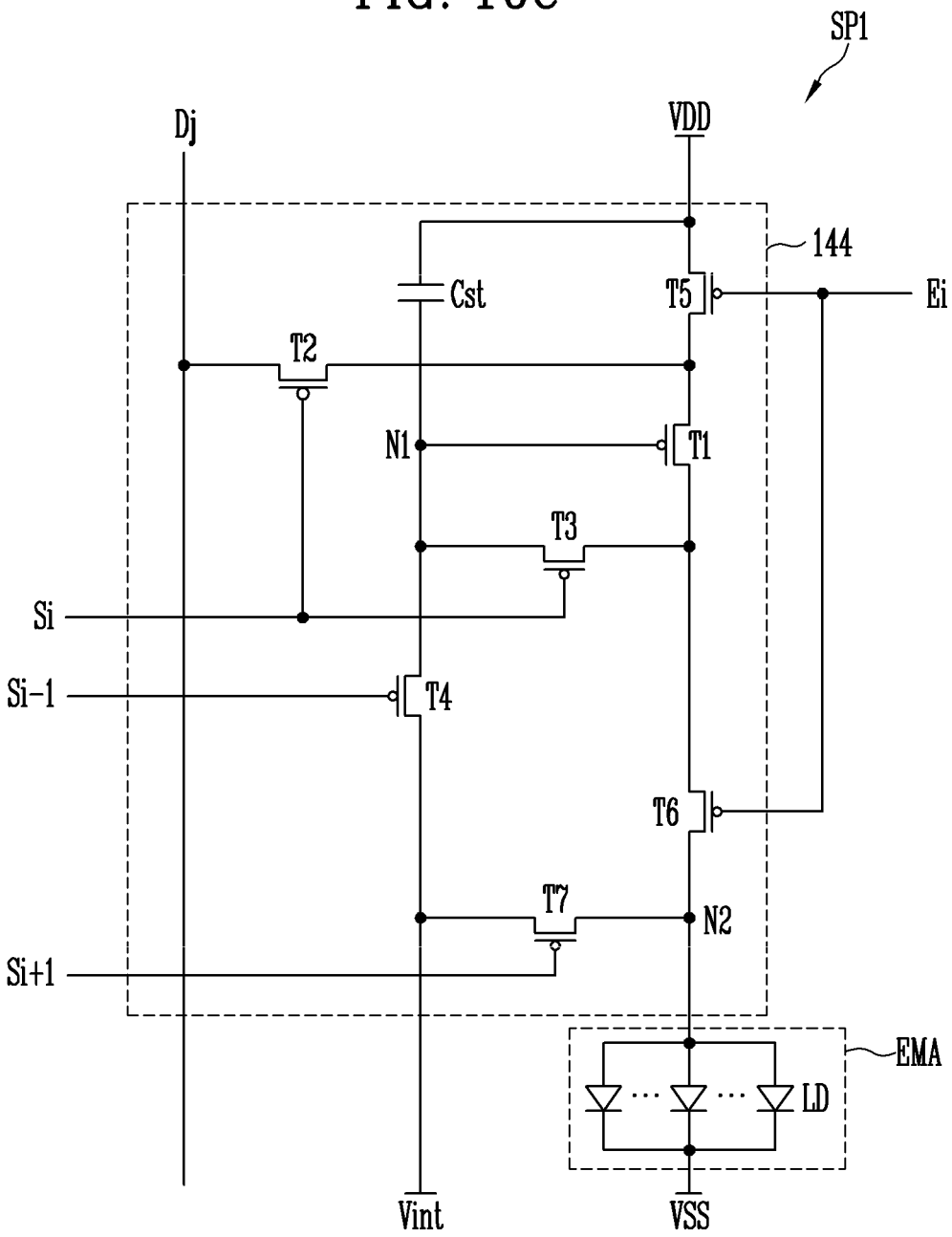


FIG. 10c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Ei
T2
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N2
Si+1
EMA
LD
Vint
VSS

FIG. 11

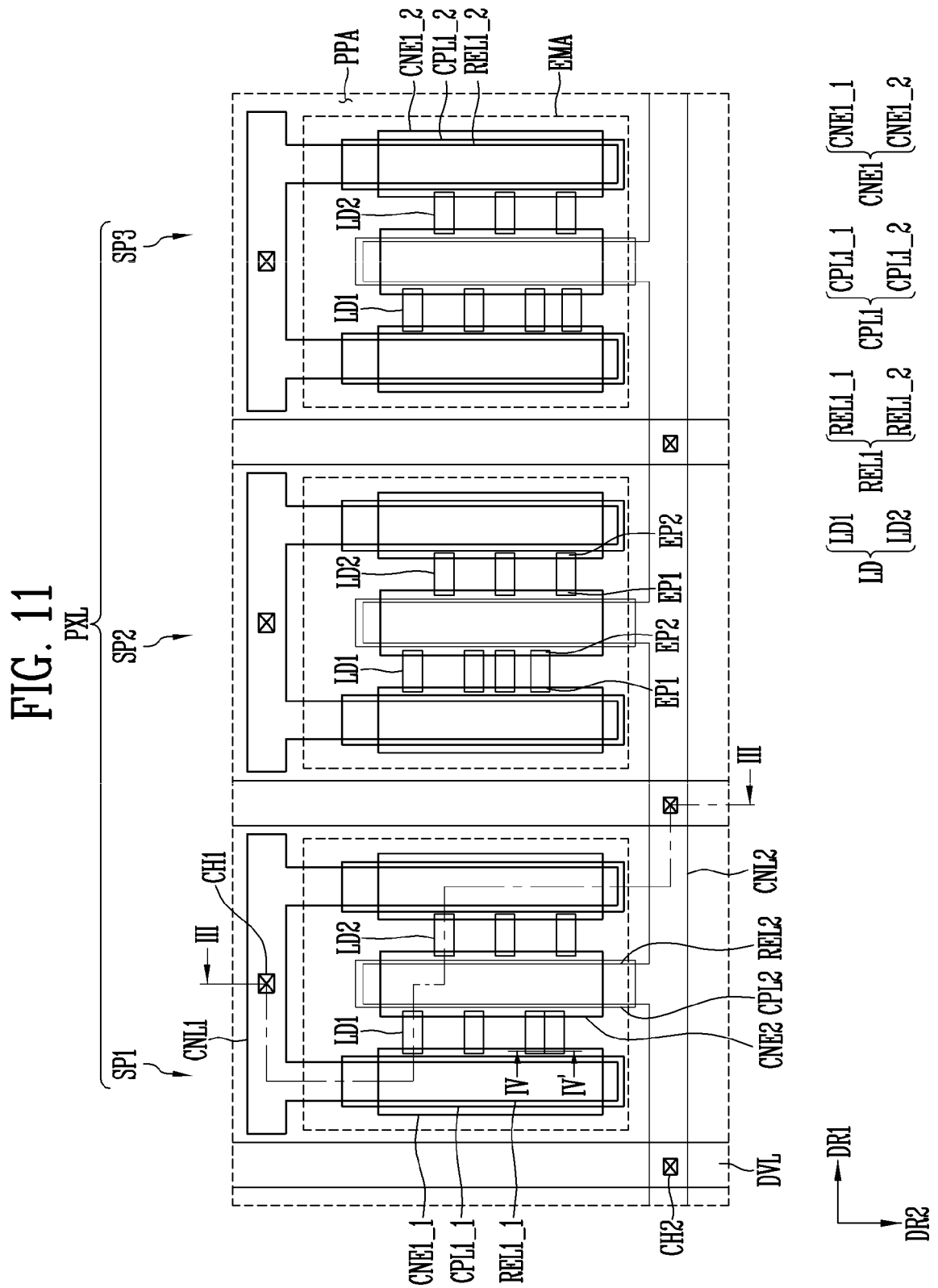
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FIG. 12a

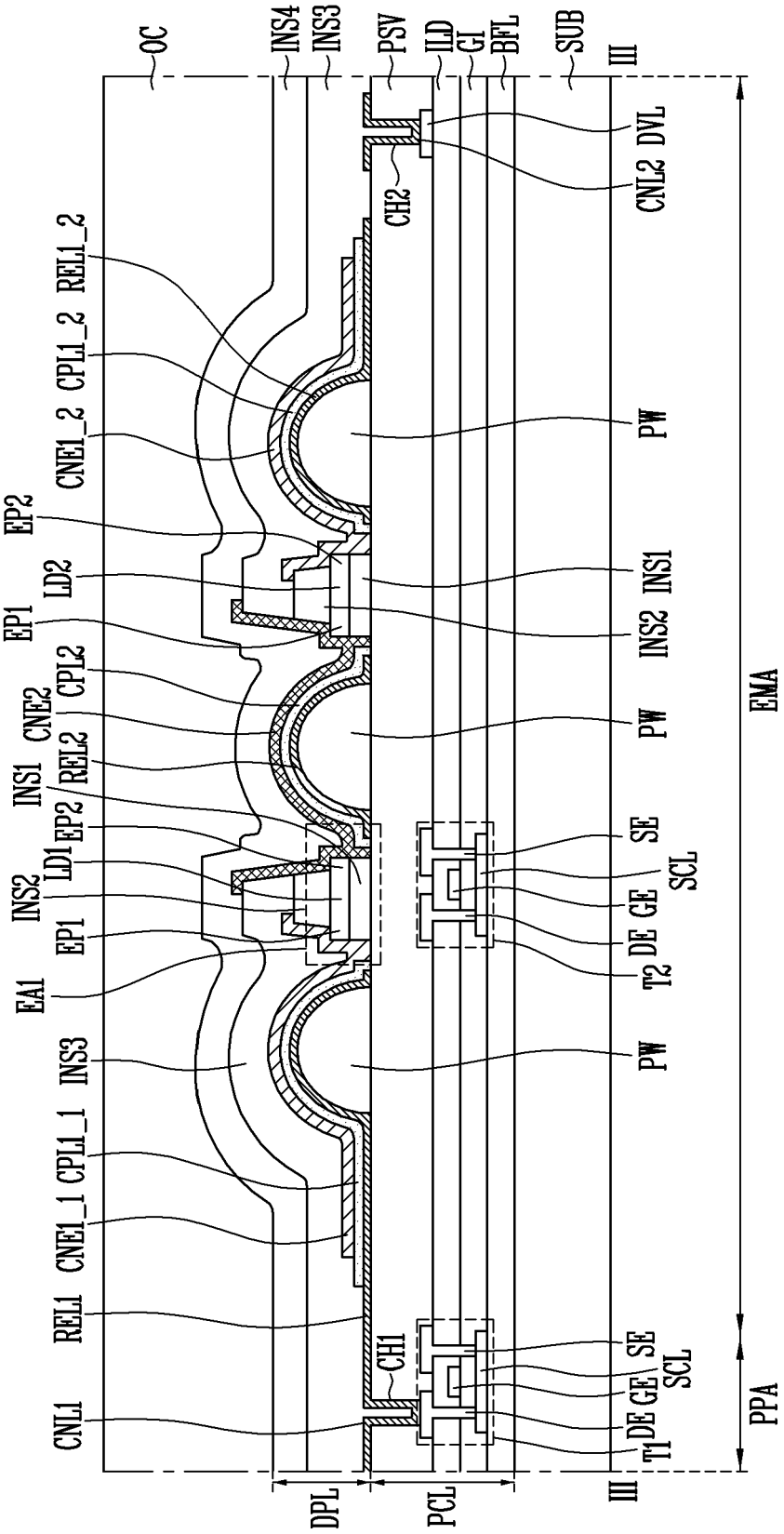
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FIG. 12b

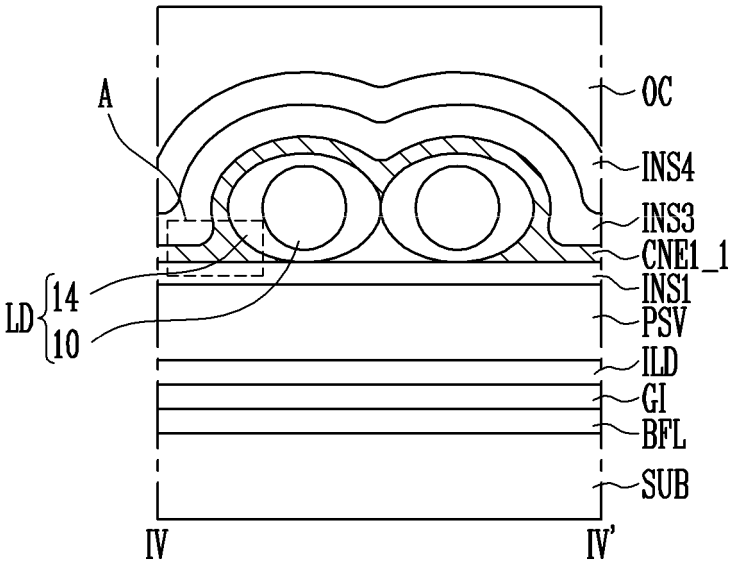


FIG. 13a

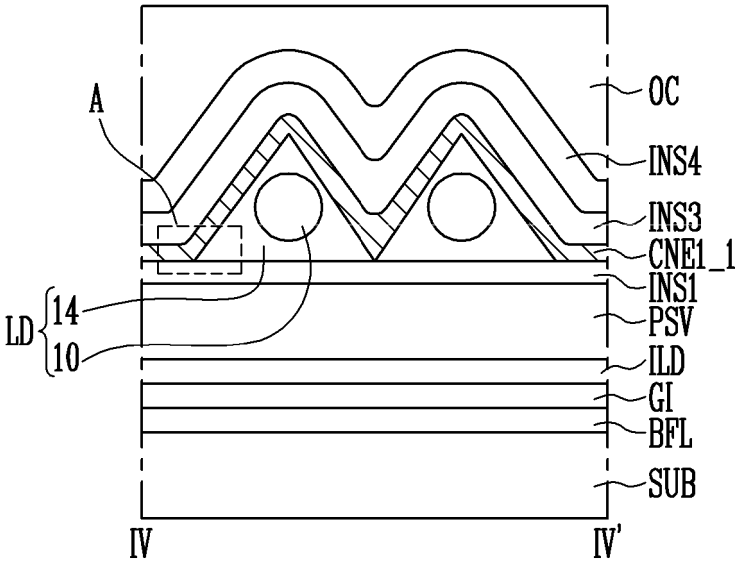
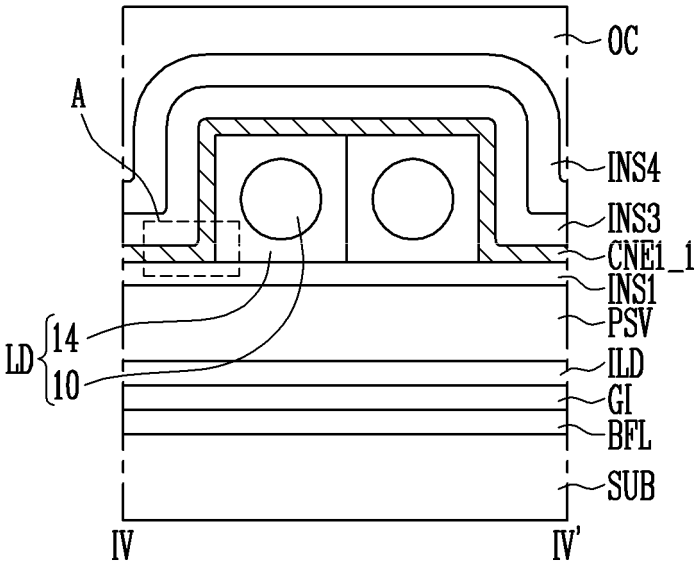


FIG. 13b



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2019/007465

A. CLASSIFICATION OF SUBJECT MATTER

H01L 33/24(2010.01)i, H01L 33/54(2010.01)i, H01L 33/00(2010.01)i, H01L 27/15(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 33/24; G02F 1/1333; G02F 1/1335; H01L 21/02; H01L 29/06; H01L 33/02; H01L 33/10; H01L 33/20; H01L 33/22; H01L 33/32; H01L 33/54; H01L 33/00; H01L 27/15

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models: IPC as above
Japanese utility models and applications for utility models: IPC as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS (KIPO internal) & Keywords: light emitting, pillar, thickness, shape, polygon, insulation

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	KR 10-2010-0054594 A (SAMSUNG LED CO., LTD.) 25 May 2010 See paragraphs [27]-[43], figures 2-10.	1-19
Y	KR 10-2017-0074296 A (KOREA ADVANCED NANO FAB CENTER) 30 June 2017 See paragraphs [61]-[76], claims 1-7, figures 1-2.	1-19
Y	KR 10-2018-0058910 A (LG DISPLAY CO., LTD.) 04 June 2018 See paragraphs [58]-[66], claims 1-10, figure 4.	18-19
A	WO 2011-162715 A1 (GLO AB.) 29 December 2011 See the entire document.	1-19
A	KR 10-2007-0060970 A (ELECTRONICS AND TELECOMMUNICATIONS RESEARCH INSTITUTE) 13 June 2007 See the entire document.	1-19

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
04 OCTOBER 2019 (04.10.2019)	**04 OCTOBER 2019 (04.10.2019)**
Name and mailing address of the ISA/KR Korean Intellectual Property Office Government Complex Daejeon Building 4, 189, Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea Facsimile No. +82-42-481-8578	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/KR2019/007465

Patent document cited in search report	Publication date	Patent family member	Publication date
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KR 10-2017-0074296 A	30/06/2017	KR 10-1837623 B1	13/03/2018
KR 10-2018-0058910 A	04/06/2018	None	
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		WO 2007-066854 A1	14/06/2007

Form PCT/ISA/210 (patent family annex) (January 2015)