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Week 2 Assignment Instructions and Files

There will be an application assignment in the next module. Please pay careful attention to these instructions, because the assignment requires you to do and record tasks as the module progresses. Following the steps in preparation for the assignment is open to all students in this course, while only paying learners will be able to access the final assignment in Week 2. Likewise, only paying learners will be able to access the instructions for and final assignment in Week 4.

You will install a number of FPGA development tools, and then create your own FPGA design using steps given in the videos. At each milestone you will record screenshots of your progress, so that we can verify that you have done the design work and help you by identifying mistakes at any particular point in the design process. You will create screenshots of the FGPA tool window by typing ALT- PrtSc and saving the result as a .jpg file or pasting this into a .pdf document.

In particular, you will be asked to submit these screenshots at the following points in the module:

- 1. The completed pipemult schematic after Video #6
- 2. The Compilation Report after Video #7 showing Fmax and % utilization
- 3. A high level RTL view after Video #8
- 4. The Compilation Report at the end of Video #10 showing Fmax and % utilization
- The ModelSim Simulation waveform window at the end of Video #11

Save these instructions so that you can refer to them throughout the module.

As you create your FPGA design following instructions in the videos, after each video you will reach a milestone. At this point, your results may look slightly different from the results we get. As you go forward to the next step, these differences may be confusing as the instructions may not match what you see. To keep everyone in sync, zipped up project files are made available so that you can start after each milestone with a known good solution. You should unzip these files to C:/ALteraPrj. These project files can be downloaded here: