

A two bit adder can be constructed from two one bit adders

From the table below, we can define a boolean expression

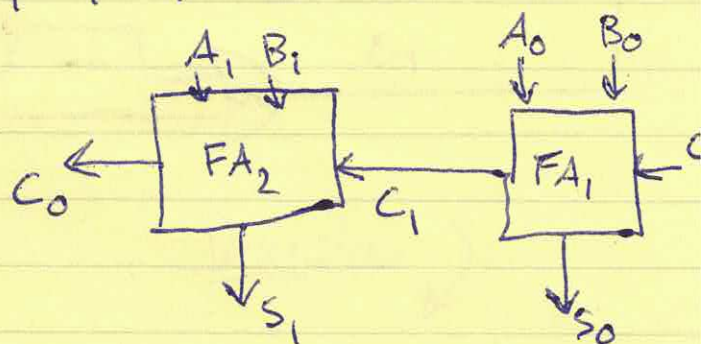
A_0	A_1	B_0	B_1	C_i	S_0	S_1	C_o
0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	0
0	0	1	0	0	1	0	0
0	0	1	0	1	0	1	0
0	1	0	0	0	1	1	0
0	1	0	0	1	0	1	0
0	1	1	0	0	0	1	1
0	1	1	0	1	1	0	1
1	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0
1	0	1	0	0	0	1	0
1	0	1	0	1	1	0	0
1	1	0	0	0	0	1	1
1	1	0	0	1	1	0	1
1	1	1	0	0	1	1	1
1	1	1	0	1	0	1	1

$$S_0 = A_0 \oplus B_0 \oplus C_i$$

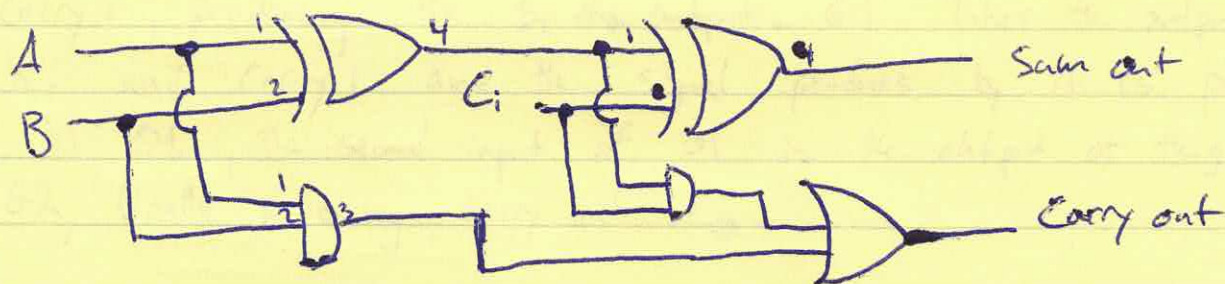
$$C_1 = A_0 B_0 + B_0 C_i + A_0 C_i$$

$$S_1 = A_1 \oplus B_1 \oplus C_1$$

$$C_o = A_1 B_1 + B_1 C_1 + A_1 C_1$$

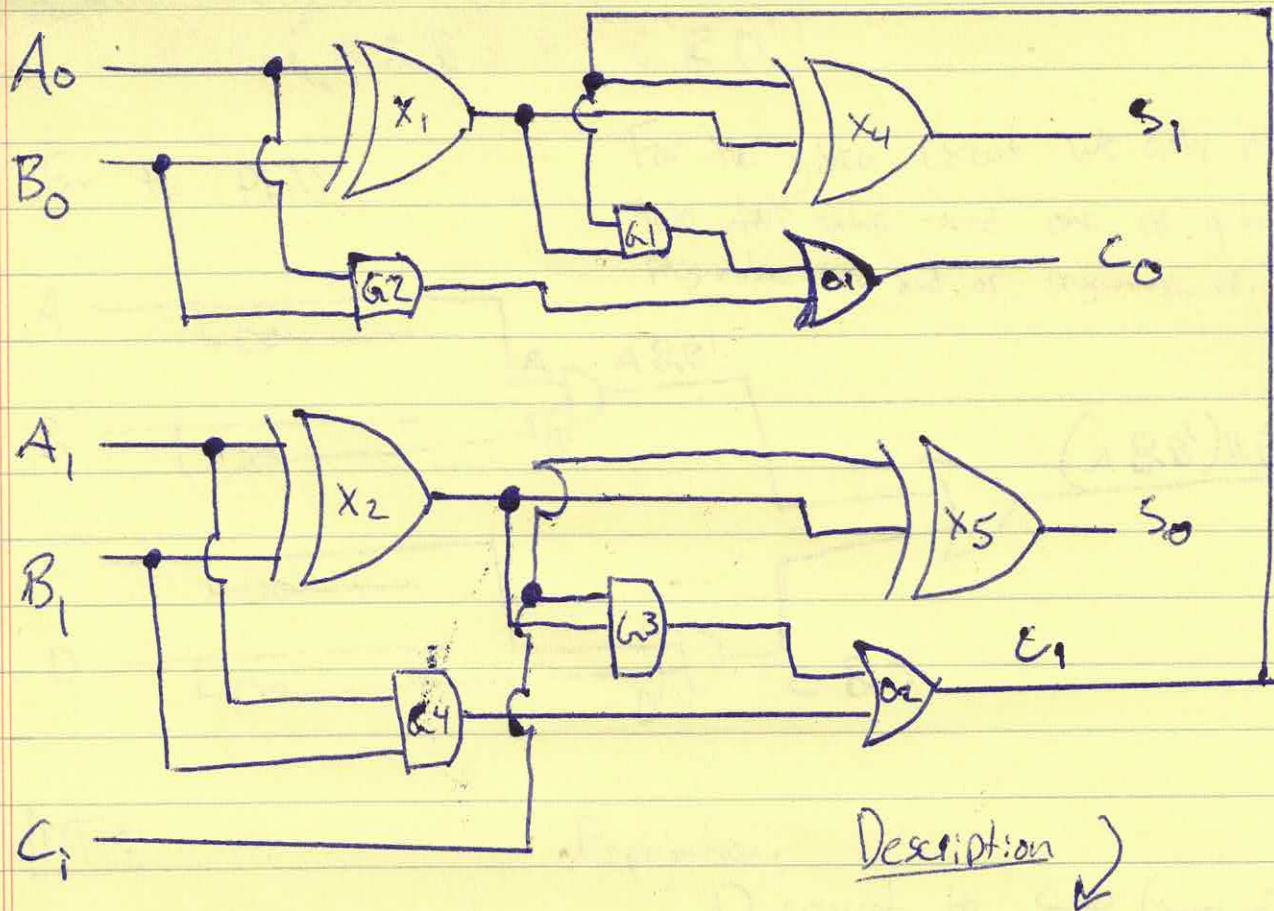


Full adder circuit



We have two inputs A and B and Carry in (C_i) which produces the output Sum and Carry out.

A two bit full adder will look like the following.



The Xor gate X_1 takes the input A_0 and B_0 and Xor gate X_2 takes the input A_1 and B_1 . The same for G_2 and G_4 respectively. X_4 takes the output of the X_1 and the output Carry 1, producing the S_1 output. G_1 Takes the output X_1 and Carry 1 and the signal produces by it is pass to O_1 , The second input of O_1 is the output of the gate G_2 , finally producing carry out C_0 .

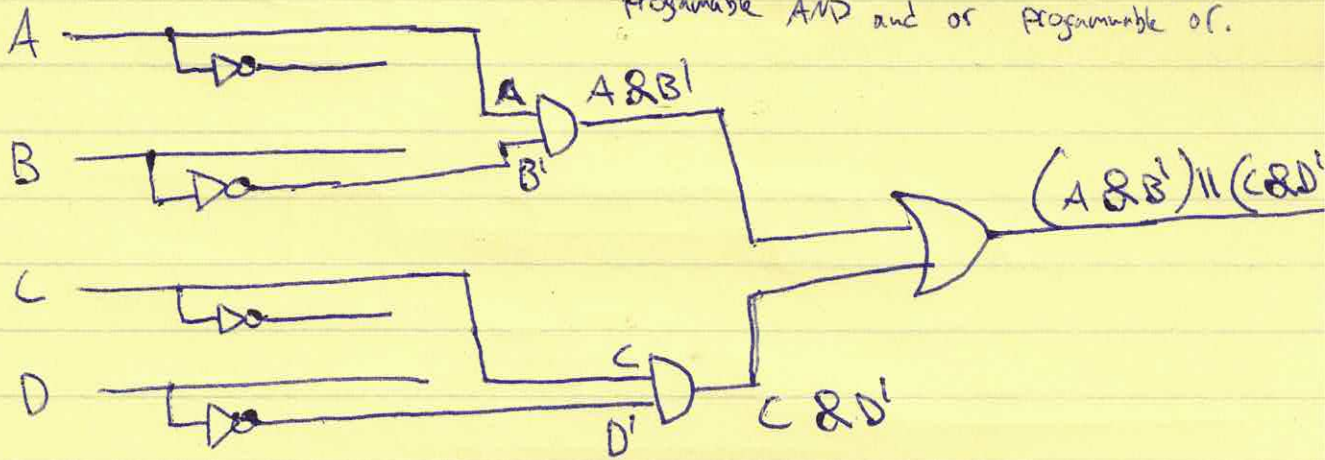
Gate X_5 takes the carry in and output of X_2 and produces the sum S_0 . ~~and~~ G_3 Takes carry in and output of X_2 and the output of this with G_4 is passed to the gate O_2 to produce the output Carry 1.

Q2

$$F = (A \& B') \parallel (C \& D')$$

For the PLA:

For the given circuit we only need two AND gates and one OR gate.
Programmable AND and OR Programmable OR.



Truth Table:

Explanation:

- 1) Convert to SOP (Sum of products)
- 2) Products implemented by AND
- 3) Sums are implemented by OR

	A	B	C	D	F
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1