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Extra Problem Homework

CSE 401

Extra problem - due anytime before the final:

Assume a 64 bit processor with instruction set similar to MIPS in that the only memory instructions are LOAD and STORE to/from register, and all other instructions are R-format (suitably extended for 64 bits). You have 64 registers and a 5 stage pipeline. L1 cache returns in 1 cycle, L2 cache takes 4 cycles for an L1 miss. Cache is write-through handled in hardware without CPU action, memory has a 20 cycle initial delay and after that supplies one word per cycle, and an L2 miss has a 40 cycle cost and loads 20 words into cache.

You are asked to design a 12 core chip where each core is as described, and will run at 2GHz. What memory bandwidth is required to support all 12 cores? Look up current memory bus speeds - are they sufficient to our requirements? State all assumptions.

(Note that:

1. You will need to make some assumption about the typical instruction mix.
2. You may need to make other assumptions.
3. Not all the given information is relevant to this problem.)

Extra Problem

- What memory bandwidth is required to support all 12 cores? Are they sufficient to our requirements?

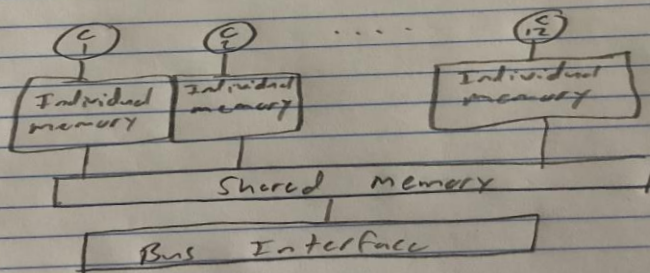
→ 64 bit mips (5 stage) processor

- The memory bandwidth requirement for a 12 core 64 bit @ 2GHz clock rate

$$\text{memory bandwidth} = 64 \text{ bits} \times 2 \text{ GHz} \times$$

$$= \frac{12 \text{ cores}}{1536 \text{ ccbits/sec}}$$

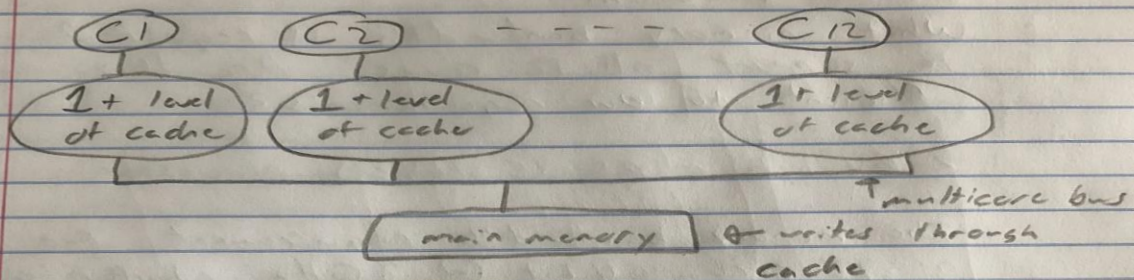
each core requires 128 ccb/s



Multicore chip → L1 is private, L2 is private in some and shared in others, memory is always shared.

| Core 1 | Core 2 |
|-----------------|--------|
| L1 | L1 |
| L2 cache memory | |

→ writes thru cache by CPU



With bus speeds of up over 3000MHz currently, with DDR4 RAM, yes the memory is sufficient to meet the requirements.