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Chapter 5 Homework

CSE 401

5.3

5.3.1 What is the cache block size (in words)?

Looking at the offset bits, 0-4. The block size would then become a 2^5bytes providing us 8 words in a block.

5.3.2 How many entries does the cache have?

Well assuming entries is related to block. The system would have 2^5 (index bits), giving us a 32 lines.

5.3.3 What is the ratio between total bits required for such a cache implementation over the data storage bits?

The ratio would become a total bits / total data bits = [32 * (32*8 + 20 + 1)] / [32 * (32*8)] = 277/256.

5.3.4 How many blocks are replaced?

There are 2 blocks that are replaced.

5.3.5 What is the hit ratio?

The hit ratio is simply 3/10 or a 0.30 ratio.

5.3.6 List the final state of the cache, with each valid entry represented as a record of .

Address	Block address	Cache Index	Hit or Miss
0	0	0	Miss
4	0	0	Hit
16	0	0	Hit
132	4	4	Miss
232	7	7	Miss
160	5	5	Miss
1024	128	0	Miss
30	0	0	Miss
140	0	0	Miss
3100	4	4	Miss
180	0	0	Hit
2180	96	96	Miss

5.5.6 For constant miss latency, what is the optimal block size?

For the constant miss latency, block size with the lowest miss rate is the optimal choice, therefore the 128 byte with a 1% is the best choice.