

California State University, Northridge
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ECE 442L
Digital Electronics Laboratory

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CMOS INVERTERS AND THEIR VOLTAGE TRANSFER CHARACTERISTICS DESIGN, SIMULATION AND EXPERIMENTAL TEST AS WELL AS ANALYSIS

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I.I. ABSTRACT

Creating a CMOS inverter by incorporating PMOS and NMOS in parallel using PSPICE, and subsequently conducting experimental analysis. Assessing the propagation delay of the CMOS under various frequencies and making adjustments accordingly.

I.II. KEY WORDS

NMOS, PMOS, CMOS, Ramp, High & Low Margins and Propagation Delay, Capacitor

I.III. INTRODUCTION

The CMOS inverter holds significance within digital circuits, utilizing the fundamental logic of an inverter. Illustrated in Figure 1b, this circuit consists of two complementary MOSFETs, comprising a PMOS at the top and an NMOS at the bottom.

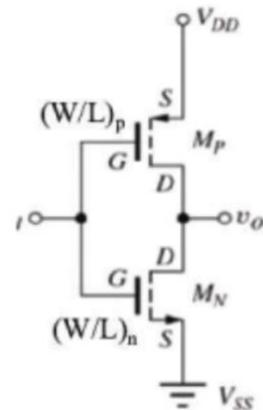


Figure 1.1 CMOS Diagram

The core principle of CMOS operation is straightforward: when the input registers 5V, the output drops to 0V; conversely, when the input is at 0V, the output flips to 5V, effectively inverting the signal. This behavior is clearly illustrated in the table below.

	Channel OFF	Channel ON
PMOS	$V_{gsp} > V_{T_p}$ or $V_{in} > V_T + V_{DD}$	$V_{gs} < V_T$ or $V_{in} < V_T + V_{DD}$
NMOS	$V_{gsn} < V_{T_n}$ or $V_{in} < V_{T_n}$	$V_{gs} > V_T$ or $V_{in} > V_{T_n}$

Table 1.1 Table of NMOS and PMOS Characteristics

The information about the CMOS inverter can be shown in Figure 1.2, which specifies

the transistor modes for different operational regions.

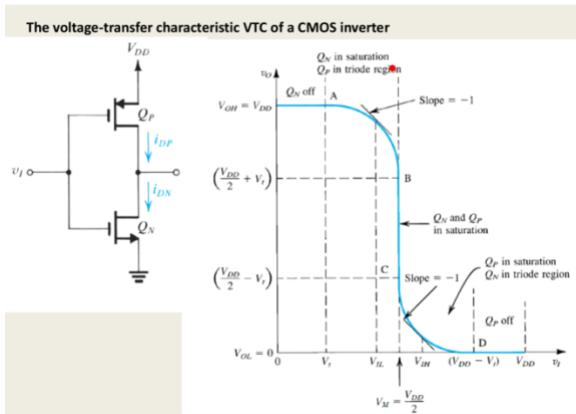


Figure 1.2: Voltage Transfer Characteristic

This report will discuss the simulations conducted for the CMOS inverter, along with the associated equations. The simulations will encompass parameters such as propagation delay, switching threshold, and high and low noise margins. The switching threshold marks the point where the input voltage equals the output voltage. The high and low noise margins represent the excess amounts by which a signal surpasses the minimum requirement for proper operation. They are calculated using the following formulas: $NML = VIL - VOL$ for low noise margin, and $NMH = VOH - VIH$ for high noise margin. Additionally, the laboratory experiment will utilize the CD4007 CMOS chip, and its pin layout is depicted in Figure 1.3.

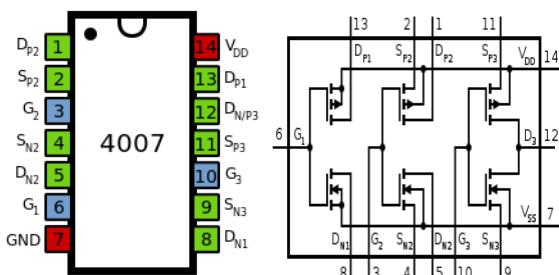


Figure 1.3: CMOS Chip Pin Layout

I.IV. EXPERIMENTAL AND SIMULATION SETUPS

The experiment comprises several scenarios featuring varied frequency ranges, all employing the same circuit configuration as depicted in Fig. 1b. The frequency ranges for each case are as follows: 100kHz to 200kHz for the first case, 300kHz to 500kHz for the second case, 600kHz to 800kHz for the third case, and a range of 900kHz to 1.2MHz for the final case. In each instance, a 5V square wave input is utilized.

I.V. EXPERIMENTAL AND SIMULATION DATA AND RESULTS

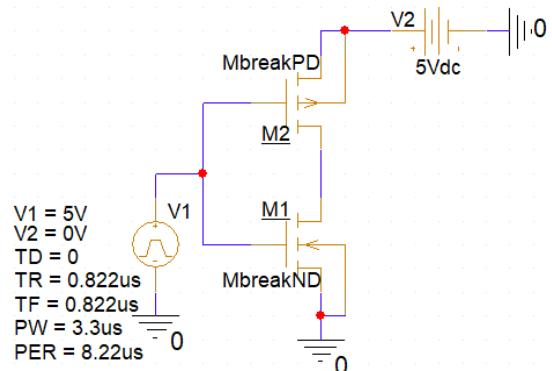


Figure 1.4: CMOS Inverter circuit with 5V square wave input and $f = 124$ kHz

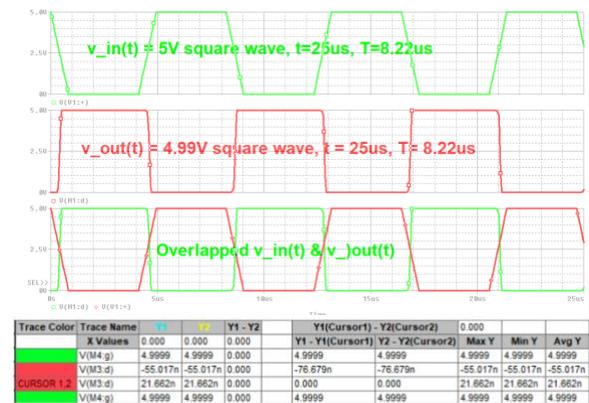


Figure 1.5: I/p – O/p Waveform of the CMOS Inverter circuit with 5V square wave input and $f = 124$ kHz



Figure 1.6: Zoomed I/p-O/p Waveform for CMOS Inverter to measure the Propagation Delay High-to-Low (tau_{HL}) for Rectangular Input Case 1 for $f = 124$ kHz

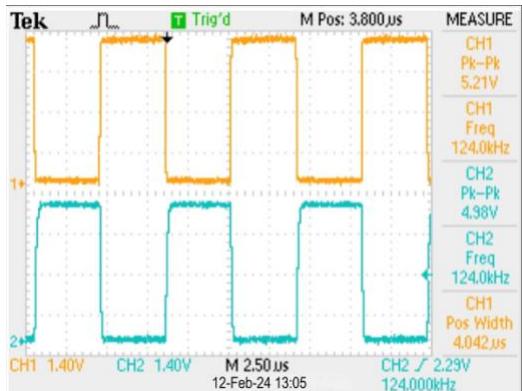


Figure 1.7: I/p – O/p Waveform of the CMOS Inverter circuit with 5V square wave input and $f = 124$ kHz

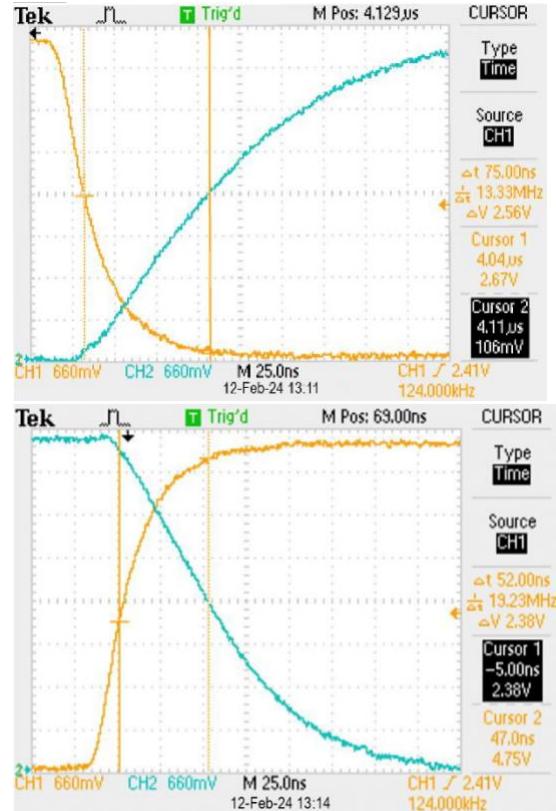


Figure 1.8: A close-up view of the input-output waveform is captured for a CMOS inverter to assess the low-to-high propagation delay (tau_{LH}) under the rectangular input condition of Case 1, with a frequency of 124 kHz. The calculated average propagation delay is determined to be 63.5 ns.

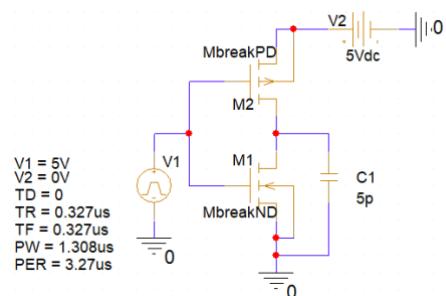


Figure 1.9: CMOS Inverter circuit with 5V square wave input and $f = 320$ kHz

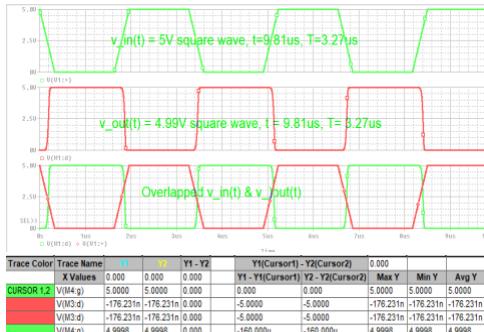


Figure 1.10: I/p – O/p Waveform of the CMOS Inverter circuit with 5V square wave input and f = 320 kHz

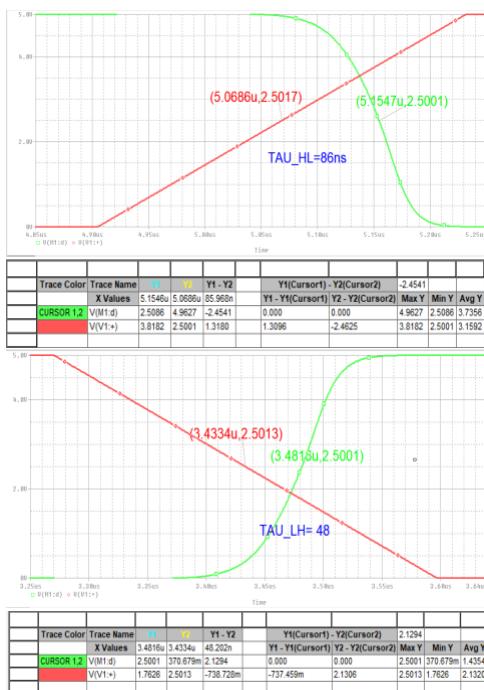


Figure 1.11 displays a magnified input-output waveform of a CMOS inverter, illustrating the measurement of the high-to-low propagation delay (tau_{HL}) under the rectangular input condition of Case 1, with a frequency of 320 kHz.

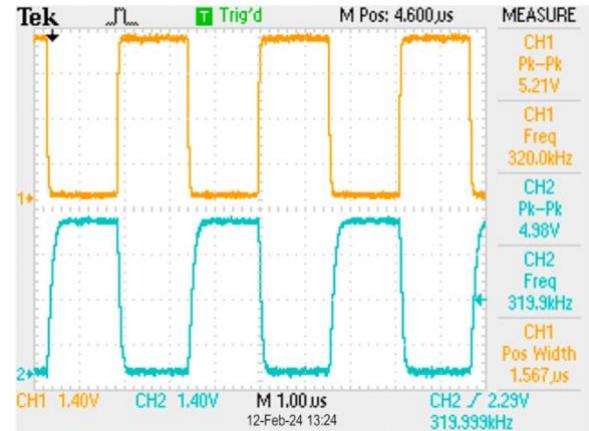


Figure 1.12: I/p – O/p Waveform of the CMOS Inverter circuit with 5V square wave input and f = 320 kHz

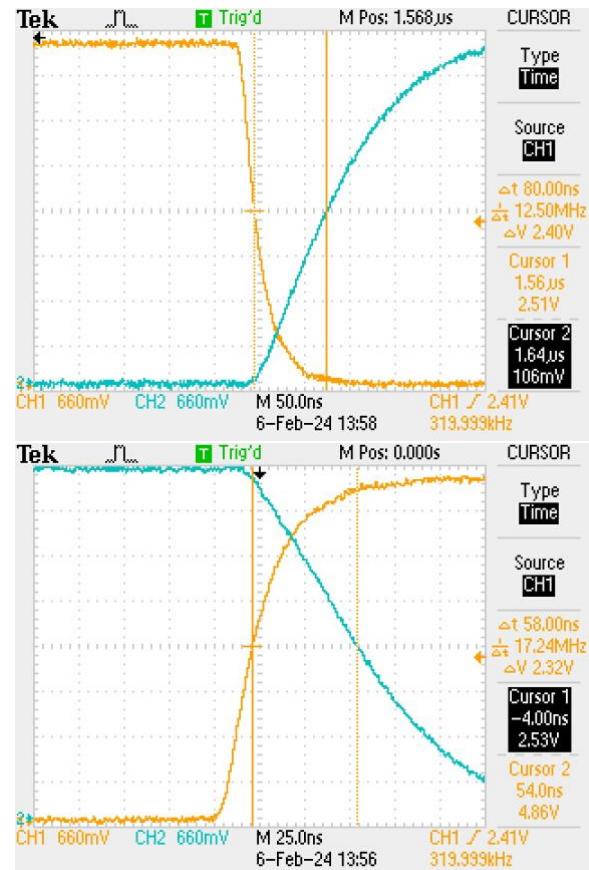


Figure 1.13 illustrates a magnified input-output waveform of a CMOS inverter used to assess the low-to-high propagation delay (tau_{LH}) for Rectangular Input Case 1 at a frequency of 320 kHz. The average propagation delay is determined to be 69 ns.

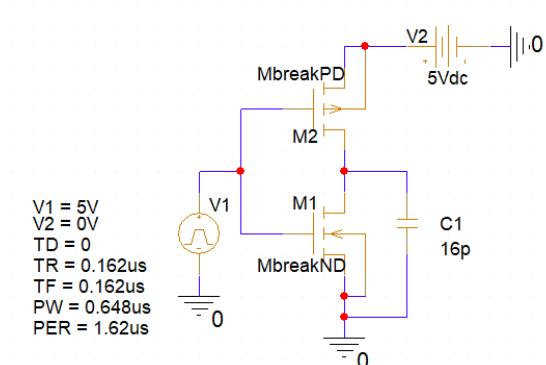


Figure 1.14: CMOS Inverter circuit with 5V square wave input and $f = 635$ kHz

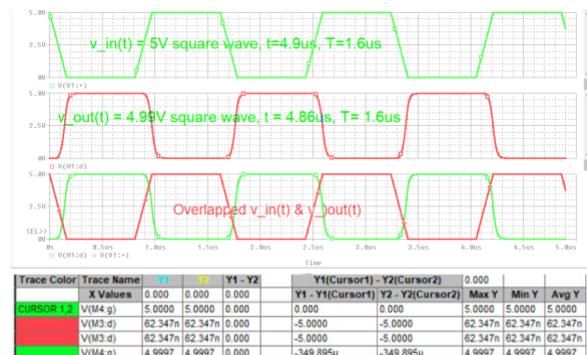
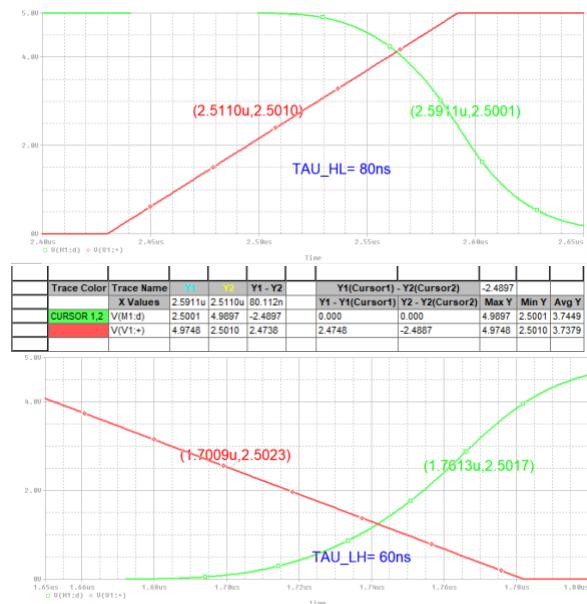


Figure 1.15: I/p – O/p Waveform of the CMOS Inverter circuit with 5V square wave input and $f = 635$ kHz



Trace Color	Trace Name	X	Y	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)	Max Y	Min Y	Avg Y
	X Values	1.7613u	1.7009u	60.336n	Y1 - Y1(Cursor1) Y2 - Y2(Cursor2)	2.4022	2.5017	99.567m
CURSOR 1,2	V(M1-d)	2.5017	99.567m	2.4022	0.000	0.000	2.5017	99.567m
CURSOR 1,2	V(V1+)	640.108m	2.5023	-1.8622	-1.8616	2.4028	2.5023	640.108m

Figure 1.16 presents an enlarged input-output waveform of a CMOS inverter used for evaluating the high-to-low propagation delay (τ_{HL}) in Rectangular Input Case 1 at a frequency of 635 kHz.

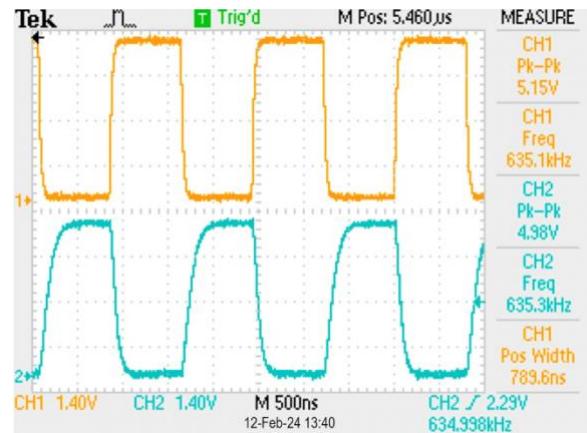


Figure 1.17: CMOS Inverter circuit with 5V square wave input and $f = 635$ kHz

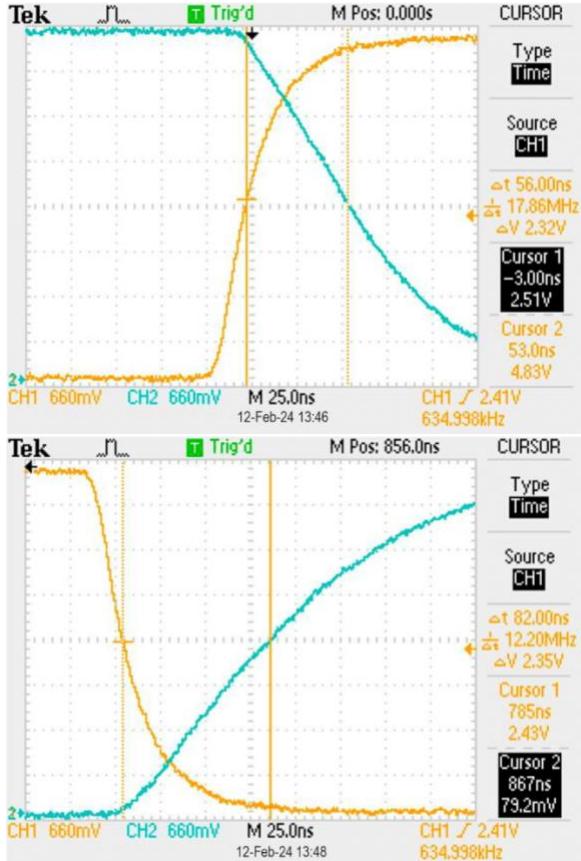


Figure 1.18 displays an amplified input-output waveform of a CMOS inverter employed to assess the low-to-high propagation delay (τ_{LH}) in Rectangular Input Case 1 at a frequency of 635 kHz. The calculated average propagation delay is 69 ns.

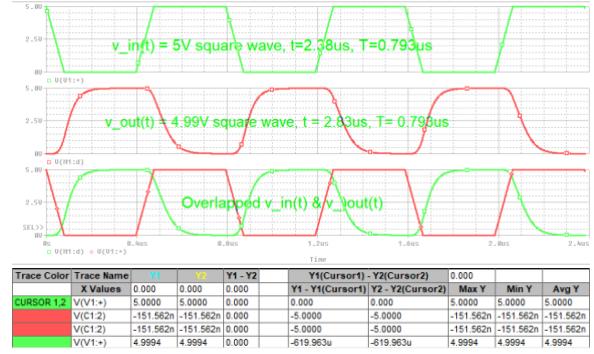
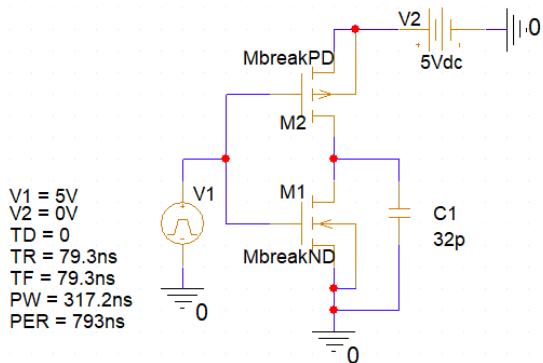


Figure 1.20: I/p – O/p Waveform of the CMOS Inverter circuit with 5V square wave input and $f = 1.24$ MHz

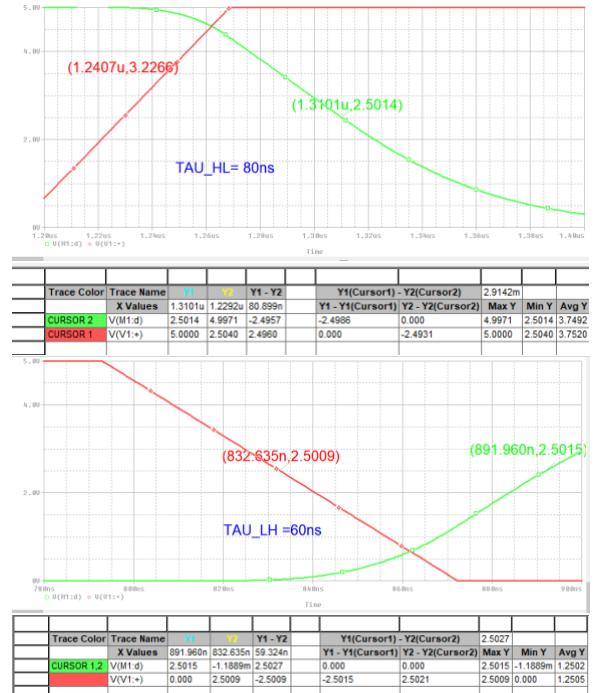


Figure 1.21 exhibits an enlarged input-output waveform of a CMOS inverter utilized for measuring the high-to-low propagation delay (τ_{HL}) in Rectangular Input Case 1 at a frequency of 1.24 MHz.

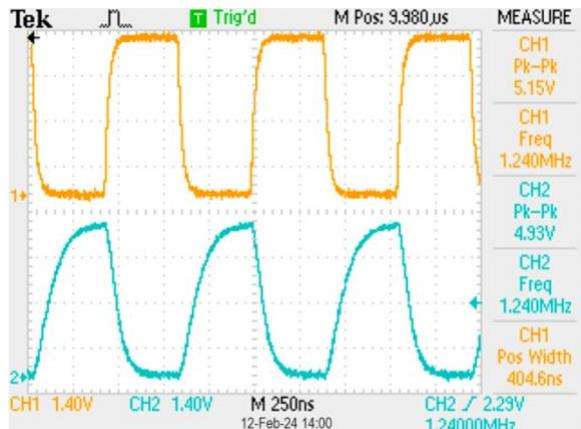


Figure 1.22: CMOS Inverter circuit with 5V square wave input and $f = 1.24$ MHz

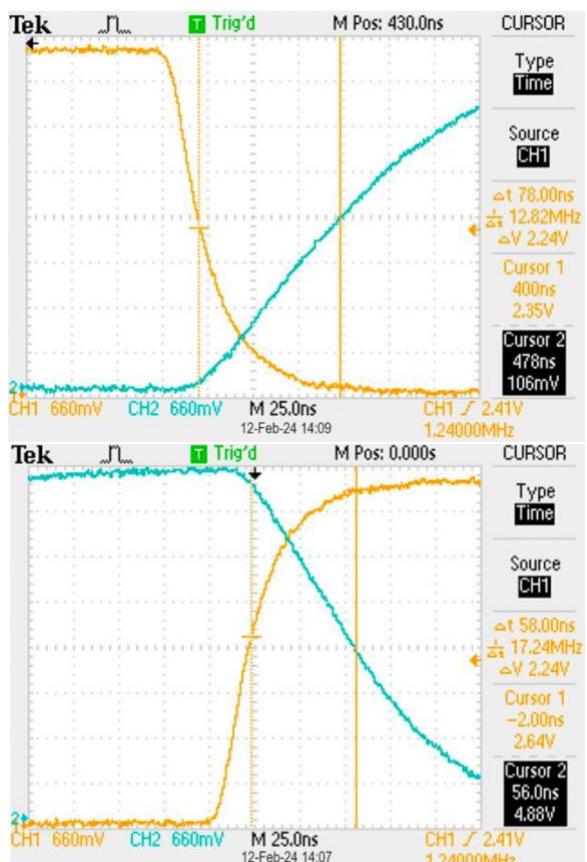


Figure 1.23 depicts an enlarged input-output waveform of a CMOS inverter used to determine the low-to-high propagation delay (τ_{LH}) in Rectangular Input Case 1 at a frequency of 1.24 MHz. The average propagation delay is calculated to be 68 ns.

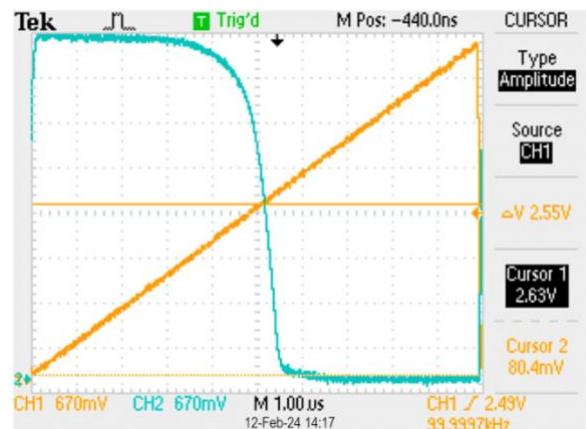


Figure 1.24: CMOS Inverter I/p-O/p Voltage Transfer Characteristics Curve for 5V Ramp Case 1, $f = 100$ kHz with normal sizing of NMOS = $(W/L) = (30 \text{ } \mu\text{m}/10 \text{ } \mu\text{m})$

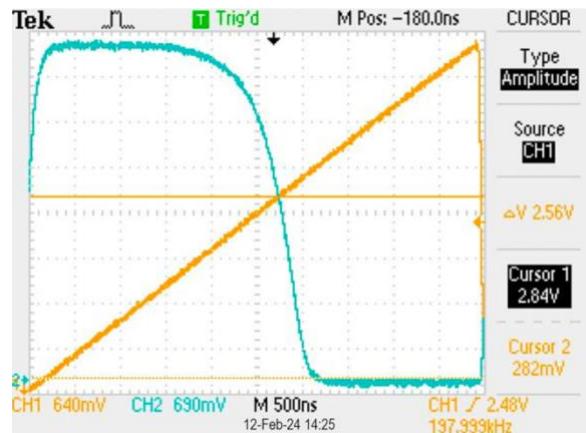


Figure 1.25: CMOS Inverter I/p-O/p Voltage Transfer Characteristics Curve for 5V Ramp Case 1, $f = 198$ kHz with normal sizing of NMOS = $(W/L) = (30 \text{ } \mu\text{m}/10 \text{ } \mu\text{m})$.

I.VI. DISCUSSION AND CONCLUSION

We managed to construct the CMOS inverter; however, we encountered challenges due to poor chip quality, resulting in significant noise even with short cables and high-quality scope probes. Particularly problematic was the high-frequency case at 1.24 MHz, as our scope couldn't accurately probe at that rate, leading to compromised results.

Nevertheless, we reconstructed the circuit with guidance from Professor Berhe, enabling us to conduct all test cases and achieve a propagation delay of approximately 70 ns once we appropriately sized the transistors.

I.VII. REFERENCES

- [1] ECE442 Lab Report
- [2] Jaeger, R. C., Blalock, T. N., & Blalock, B. J. (2023). *Microelectronic Circuit Design*. McGraw Hill LLC.
- [3] Supporting Slides on CMOS Transition Theory – Sequare Daniel-Berhe, Ph.D.

CMOS TWO-INPUT NAND GATE DESIGN, SIMULATION AND EXPERIMENTAL TEST AS WELL AS ANALYSIS

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I.I. ABSTRACT

Create a fixed 2-Input CMOS NAND gate utilizing the CMOS inverter as a basis. Grasp the approach to transistor sizing to meet the design requirements effectively.

I.II. KEY WORDS

NMOS, PMOS, CMOS, NAND

I.III. INTRODUCTION

The CMOS NAND gate holds significance within digital circuits, utilizing the Boolean logic of a NAND gate, which serves as a fundamental building block for various other gates. The foundational circuit is depicted in Figure 1b.

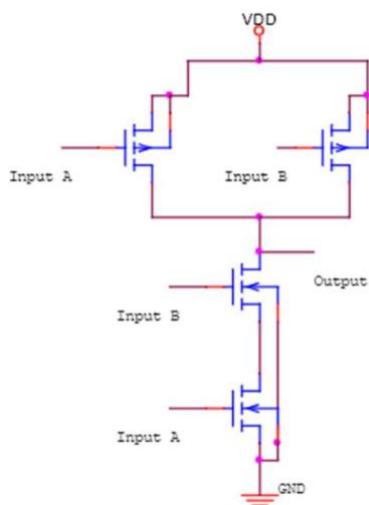


Figure 1b

This report will discuss the simulations conducted for the CMOS NAND gate, along with the relevant equations. The simulations will involve examining V_{in} and V_{out} across different frequencies. Additionally, the laboratory experiment will utilize the CD4007 CMOS chip. The pin configuration for this chip is illustrated in Figure 1.3.

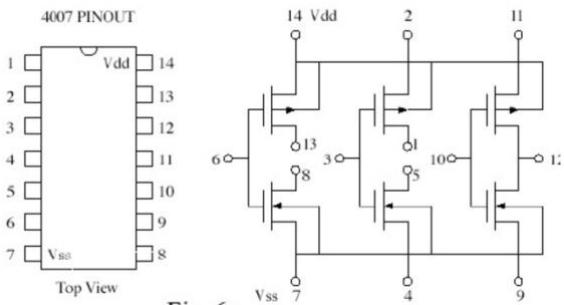


Figure 1.3

I.IV. EXPERIMENTAL AND SIMULATION SETUPS

The experiment involves various scenarios encompassing different frequency ranges while utilizing the same circuit configuration. Once more, this circuit is illustrated in Fig. 1b. The first scenario spans frequencies from 100kHz to 200kHz. The second scenario ranges from 300kHz to 500kHz. The third scenario covers frequencies from 600kHz to 800kHz. Lastly, there is a scenario with frequencies ranging from 900kHz to 1.2MHz. In all the

aforementioned scenarios, a 5V square wave serves as the input signal.

I.V. EXPERIMENTAL AND SIMULATION DATA AND RESULTS

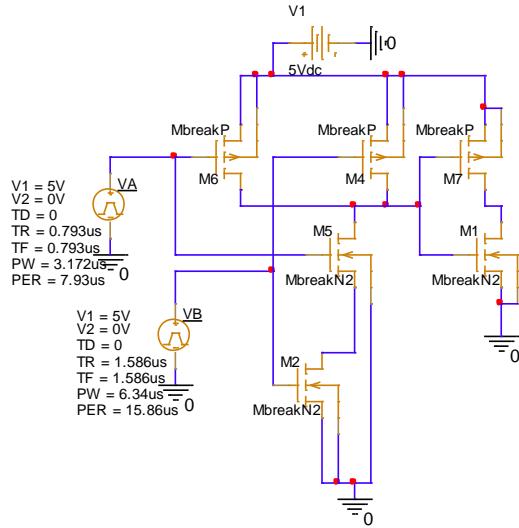


Figure 1.4: CMOS Inverter circuit with two 5V square wave inputs and $f = 126$ kHz



Figure 1.5: I/p – O/p Waveform of the CMOS Inverter circuit with 5V square wave inputs and $f = 126$ kHz

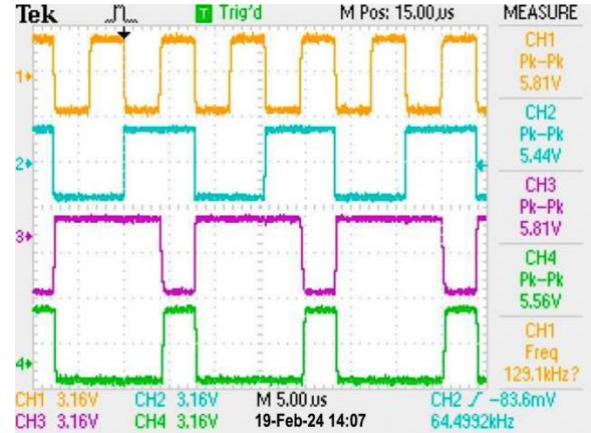


Figure 1.7: I/p – O/p Waveform of the CMOS Inverter circuit with 5V square wave input and f = 124 kHz

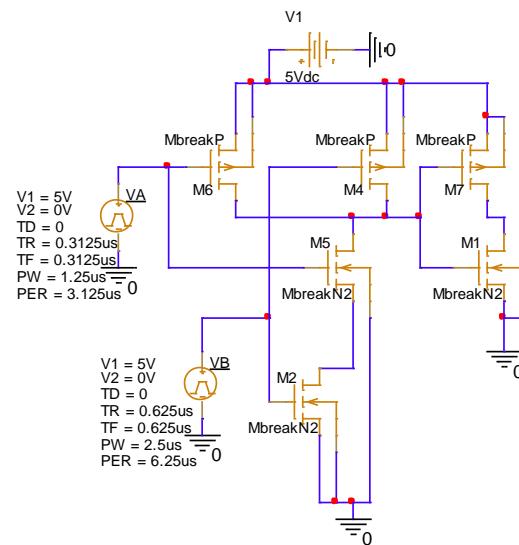


Figure 1.9: CMOS Inverter circuit with 5V square wave inputs and $f = 320$ kHz

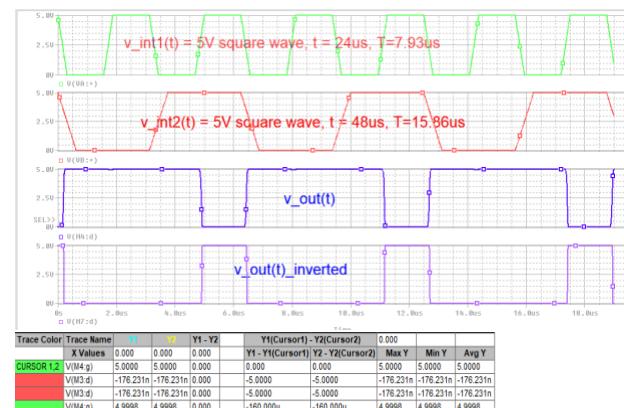


Figure 1.10: I/p – O/p Waveform of the CMOS Inverter circuit with 5V square wave inputs and f = 320 kHz

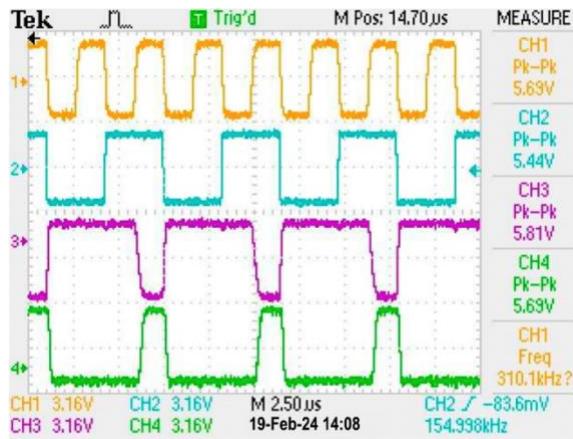


Figure 1.12: I/p – O/p Waveform of the CMOS Inverter circuit with 5V square wave input and f = 320 kHz

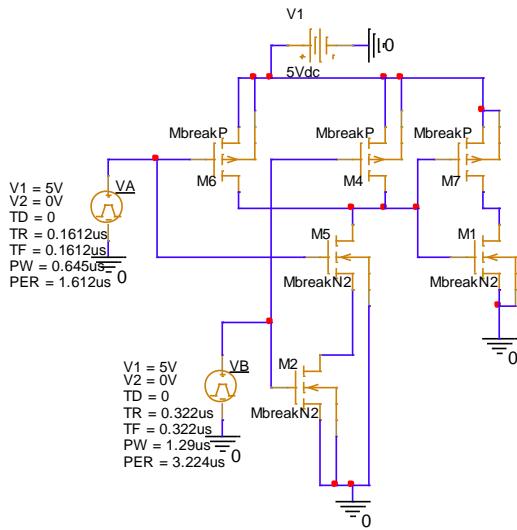
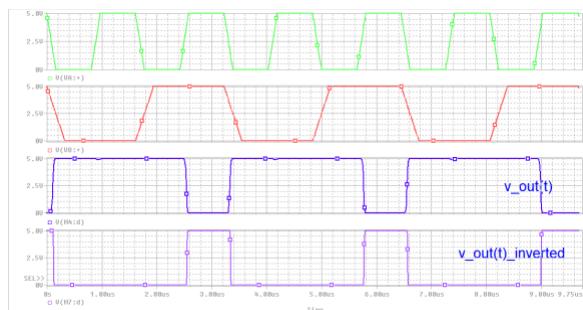


Figure 1.14: CMOS Inverter circuit with 5V square wave inputs and f = 620 kHz



Trace Color	Trace Name	X	Y	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	X Values	0.000	0.000	0.000	0.000	5.0000	5.0000	5.0000
CURSOR 1,2	V(M4_g)	5.0000	5.0000	0.000	0.000	5.0000	5.0000	5.0000
CURSOR 1,2	V(M3_d)	62.347n	62.347n	0.000	-5.0000	62.347n	62.347n	62.347n
CURSOR 1,2	V(M3_d)	62.347n	62.347n	0.000	-5.0000	62.347n	62.347n	62.347n
CURSOR 1,2	V(M4_g)	4.9997	4.9997	0.000	-349.895u	-349.895u	4.9997	4.9997

Figure 1.15: I/p – O/p Waveform of the CMOS Inverter circuit with 5V square wave inputs and f = 620 kHz

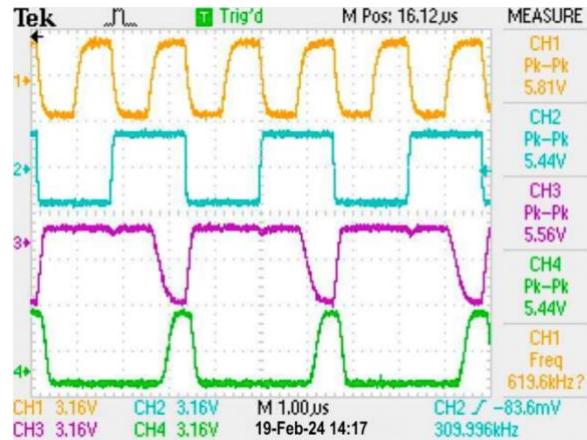


Figure 1.17: CMOS Inverter circuit with 5V square wave input and f = 635 kHz

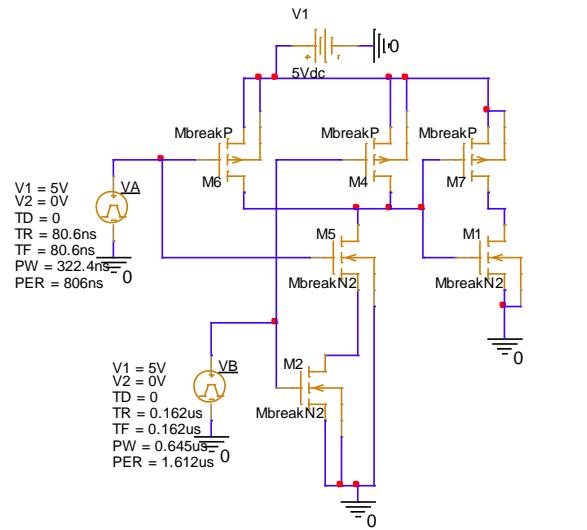


Figure 1.20: I/p – O/p Waveform of the CMOS Inverter circuit with 5V square wave inputs and $f = 1.24$ MHz

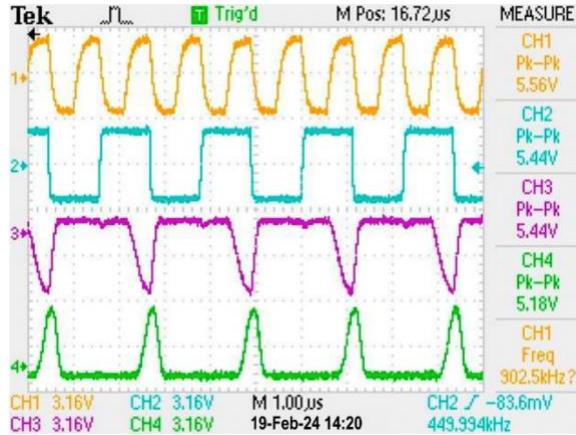


Figure 1.22: CMOS Inverter circuit with 5V square wave input and $f = 1.24$ MHz

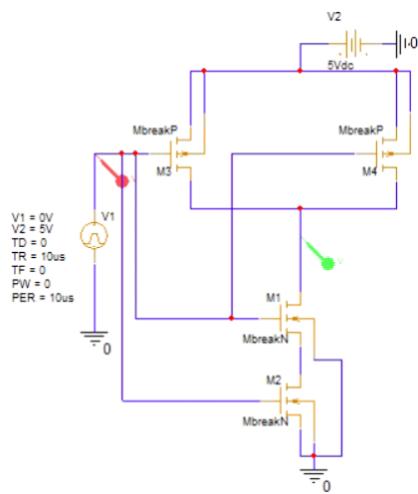


Figure 1.23: 5V ramp case at 80 kHz

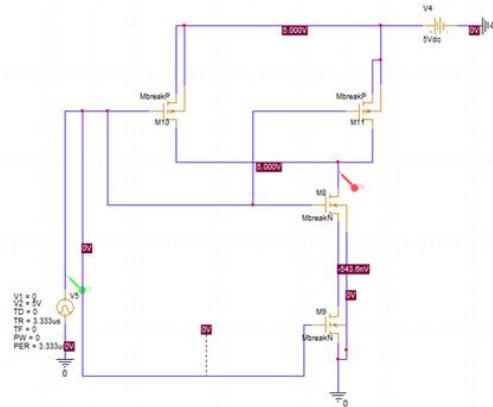
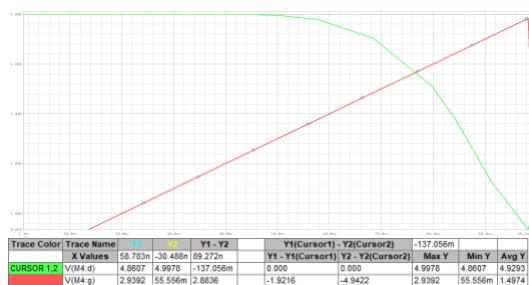


Figure 1.24: 5V ramp case at 180 kHz

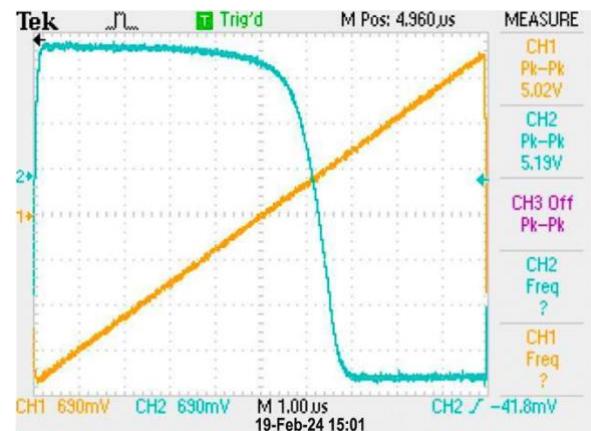
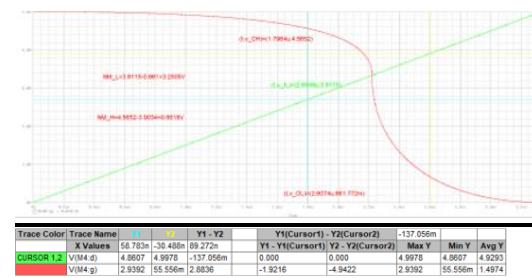


Figure 1.24: CMOS Inverter I/p-O/p Voltage Transfer Characteristics Curve for 5V Ramp Case 1, $f = 100$ kHz with normal sizing of NMOS = $(W/L) = (30 \text{ um}/10 \text{ um})$

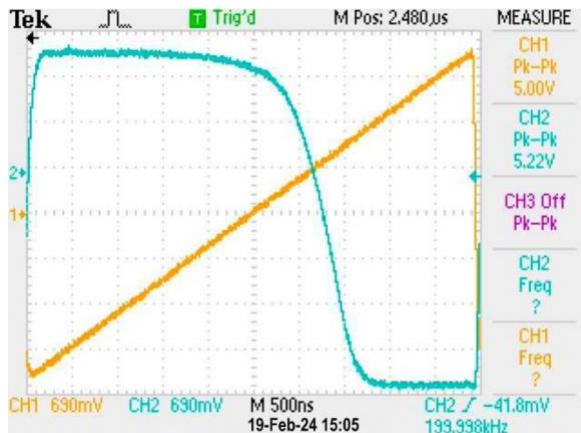


Figure 1.25: CMOS Inverter I/p-O/p Voltage Transfer Characteristics Curve for 5V Ramp Case 2, $f = 185$ kHz with normal sizing of NMOS = (W/L) = (30 um/10 um).

I.VI. DISCUSSION AND CONCLUSION

We managed to complete this lab relatively smoothly since we used the same chips as in lab 1. We connected them accordingly and, after some initial problem-solving, successfully obtained the correct inverted and non-inverted outputs. However, challenges arose in the high-frequency scenario due to HF distortion induced by the chips, and our probes lacked the necessary resolution to accurately capture the signal at 1MHz. Moreover, in PSpice, our circuits failed to converge despite our efforts, leading us to transfer our circuit to a different computer with a functioning simulation tool. We then utilized the settings from that simulation run to generate our graphs.

I.VII. REFERENCES

- [1] ECE442 Lab Report

[2] Jaeger, R. C., Blalock, T. N., & Blalock, B. J. (2023). *Microelectronic Circuit Design*. McGraw Hill LLC.

[3] Supporting Slides on CMOS Transition Theory – Sequare Daniel-Berhe, Ph.D.

CMOS RING OSCILLATION AND CLOCK GENERATION DESIGN, SIMULATION AND EXPERIMENTAL TEST AS WELL AS ANALYSIS

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I.I. ABSTRACT

Creating a cascading CMOS inverter (combining PMOS and NMOS in parallel) through PSPICE simulation and practical experimentation. Evaluating the propagation delay of the Ring Oscillator across various frequencies and making necessary adjustments.

I.II. KEY WORDS

NMOS, PMOS, CMOS, Ramp, High & Low Noise Margins and Propagation Delay, Capacitors, Inverter

I.III. INTRODUCTION

The CMOS inverter holds significance within digital circuits, operating based on the Boolean logic of inversion. However, exploring the implications when multiple CMOS inverters are arranged in series or cascaded is crucial, particularly in its role as a fundamental component of clock signal generation.

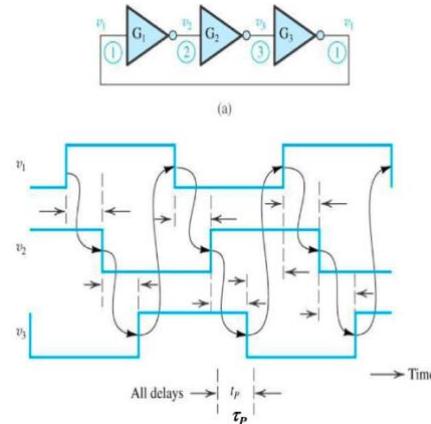
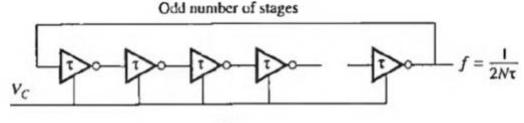


Figure 3.1 CMOS Inverted Ring Oscillator and Gate Operations

Figure 1a shows a basic setup with CMOS inverters connected in a series. In Figure 1b, it's specified that there must be an odd number of these inverters in the circuit. If you follow the paths of the gates, you'll notice that a rising edge starts at gate 1, moves through the other gates, and returns back to the initial rising clock. A ring oscillator, which has an odd number of inverter stages, produces oscillating signals at each step. The time it takes for one complete oscillation depends on the delay in each stage and the total number of stages, which is $3t_p$ in this case. However, the resulting clock signal might vary and be unstable due to differences in manufacturing processes.



$$\tau_{PHL} \cong 2R_{onN}C \left\{ \ln \left[4 \left(\frac{V_{DD} - V_{TN}}{V_{DD} + V_L} \right) - 1 \right] + \frac{1}{2} \right\}$$

$$\tau_{PLH} \cong 2R_{onP}C \left\{ \ln \left[4 \left(\frac{V_{DD} + V_{TP}}{V_H} \right) - 1 \right] + \frac{1}{2} \right\}$$

$$f_{osc} = \frac{1}{n(\tau_{PHL} + \tau_{PLH})} = \frac{1}{2n\tau_p} \quad \& \quad \tau_p = \frac{1}{2n f_{osc}}$$

Figure 3.2 Formulas for Path delay and Frequency of Oscillation of the Ring Oscillator

This report will discuss the simulations conducted on the cascading CMOS inverter and the corresponding equations. The simulations will involve analyzing propagation delay and oscillation frequency, which can be calculated by determining the delays at each signal, as illustrated in Figure 3.

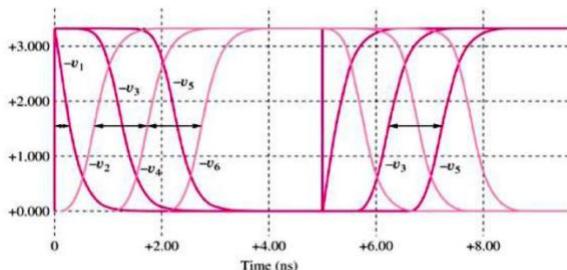


Figure 3.3 Oscillating Frequency Output

In addition, this lab experiment will utilize the CD4007 CMOS chip, with each NMOS and PMOS arranged in series and in an odd number of stages. The layout of the circuit is depicted in Figure 4.

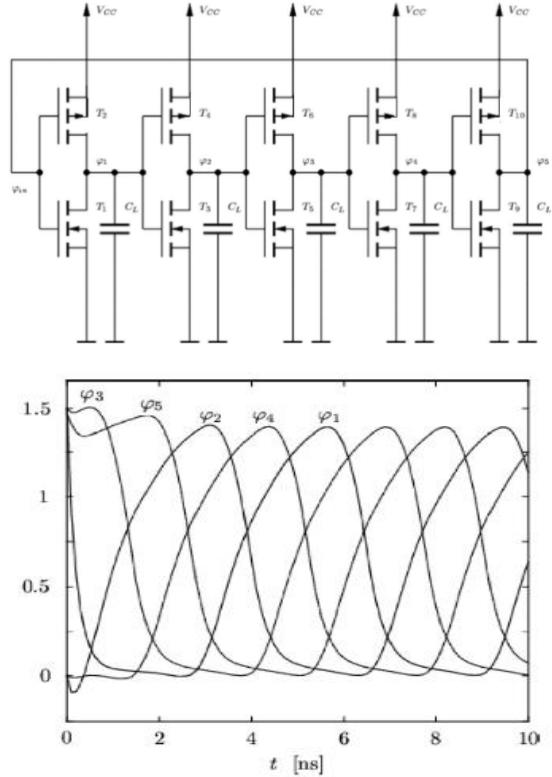


Figure 3.4 Ring Oscillator Circuit and Output

I.IV. EXPERIMENTAL AND SIMULATION SETUPS

The experiment comprises various scenarios involving different quantities of gates employed in the circuit. Once more, the circuit layout can be observed in Figure 4. The initial scenario entails a three-ring oscillator, followed by a five-ring oscillator for the second scenario, a seven-ring oscillator for the third scenario, and finally, a nine-ring oscillator for the fourth scenario.

I.V. EXPERIMENTAL AND SIMULATION DATA AND RESULTS

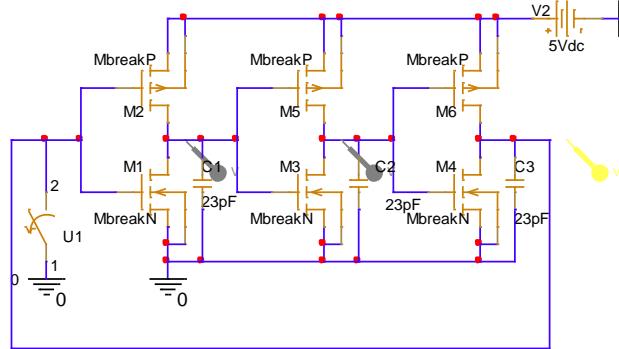


Figure 3.5 Ring Oscillator circuit with 3 inverters in series

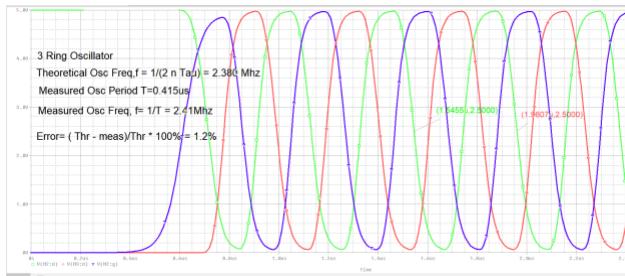


Figure 3.6 I/p – O/p Waveform of the Ring Oscillator circuit with 3 inverters

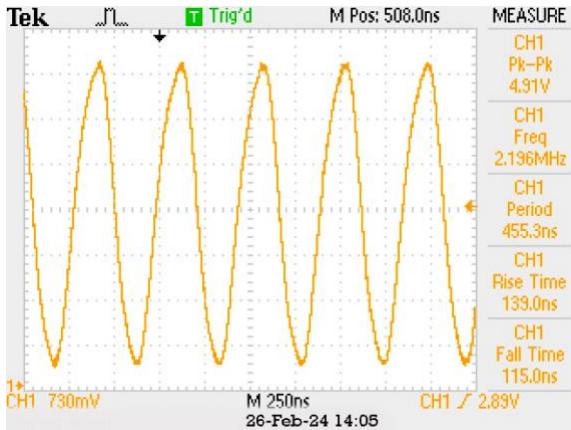


Figure 3.7 O/p Waveform of the first CMOS Inverter in the Oscillator

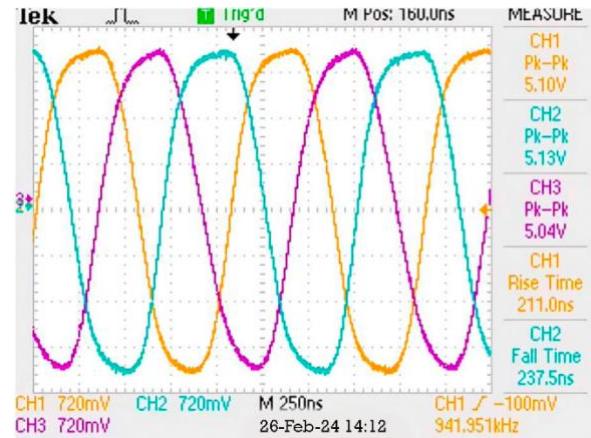


Figure 3.8 I/p – O/p Waveform of the Ring Oscillator circuit with 3 inverters

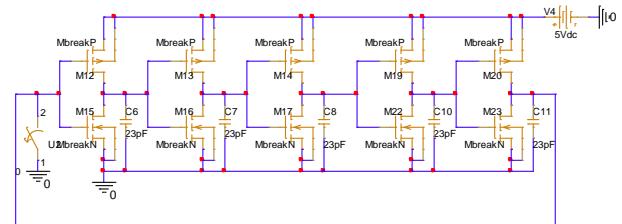


Figure 3.9 Ring Oscillator circuit with 5 inverters in series

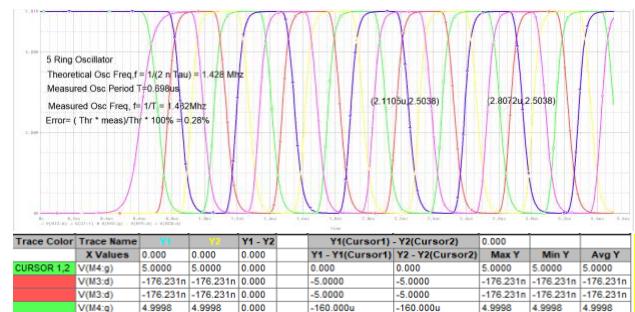


Figure 3.10 I/p – O/p Waveform of the Ring Oscillator circuit with 5 inverters

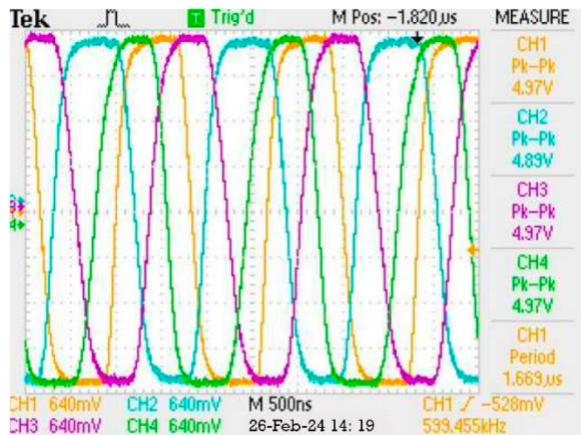


Figure 3.11 I/p – O/p Waveform of the Ring Oscillator circuit with 5 inverters

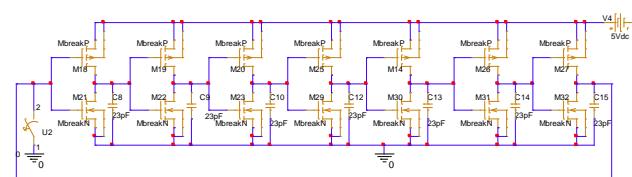


Figure 3.12 Ring Oscillator circuit with 7 inverters in series

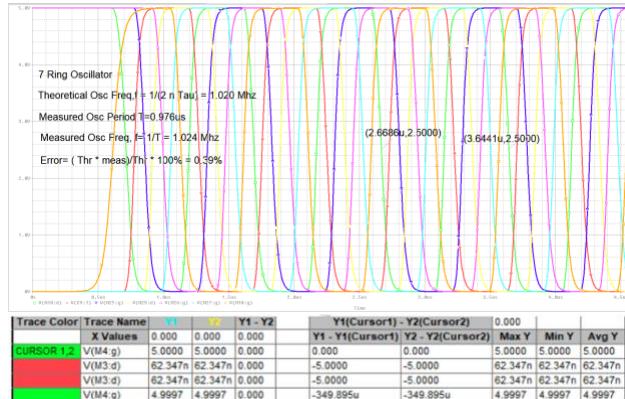


Figure 3.13 I/p – O/p Waveform of the Ring Oscillator circuit with 7 inverters

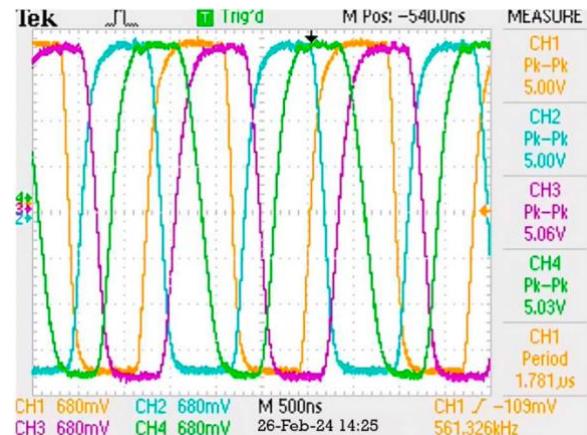


Figure 3.14 I/p – O/p Waveform of the Ring Oscillator circuit with 7 inverters

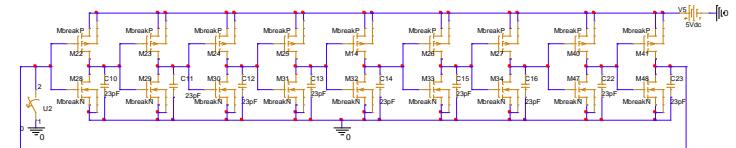


Figure 3.15 Ring Oscillator circuit with 9 inverters in series

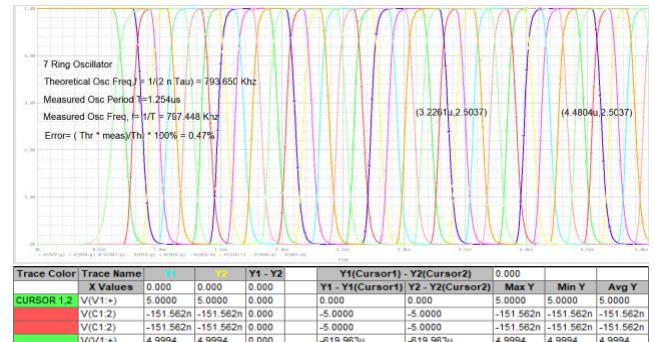


Figure 3.16 Ring Oscillator circuit with 9 inverters in series

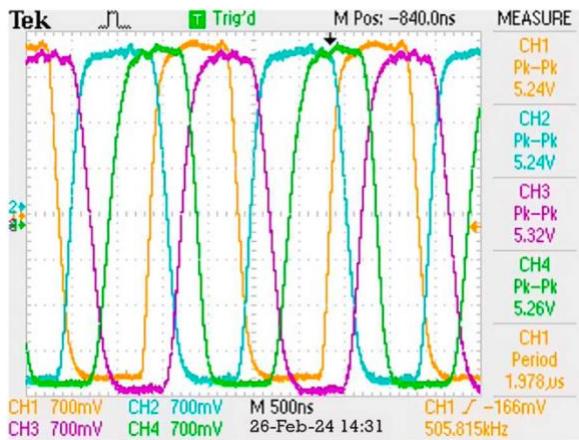


Figure 3.17 I/p – O/p Waveform of the Ring Oscillator circuit with 9 inverters

I.VI. DISCUSSION AND CONCLUSION

During this experiment, we encountered significant challenges as we increased the number of rings. With each additional ring, we required more connections to additional chips, resulting in heightened complexity and noise levels. Consequently, errors became more prevalent, although we managed to mitigate them by employing a new chip and reducing distortion. Eventually, we achieved a seven-ring oscillator with an error margin below 1%, albeit the process was notably smoother in PSpice compared to the lab setting.

Another obstacle involved ensuring that all chips were properly grounded, as we encountered issues related to misplaced or floating grounds. Once all connections were established and the circuit was operational, we observed that with each additional ring, the frequency decreased. This phenomenon arises because "N" acts as the divisor, leading to an inversely proportional relationship where frequency diminishes as "N" increases.

I.VII. REFERENCES

- [1] ECE442 Lab Report
- [2] Jaeger, R. C., Blalock, T. N., & Blalock, B. J. (2023). *Microelectronic Circuit Design*. McGraw Hill LLC.
- [3] Supporting Slides on CMOS Transition Theory – Sequare Daniel-Berhe, Ph.D.

CMOS TRANSMISSION GATE DESIGN, SIMULATION AND EXPERIMENTAL TEST AS WELL AS ANALYSIS

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I.I. ABSTRACT

In this lab, we'll study a CMOS transmission gate design, which is really handy for both analog and digital tasks. It works like a switch, turning on and off between Vdd and Vss. This gate uses NMOS and PMOS transistors to do its job.

I.II. KEY WORDS

Transmission Gate NMOS, PMOS, CMOS, Clock Frequency, Sine Wave, Sine Input, Sampling, Clock Input Frequency

I.III. INTRODUCTION

The CMOS transmission gate establishes a two-way resistive link between the input and output terminals. When the gate is conducting, these terminals are connected via the combined resistance of the two transistors. It's important to note that the equivalent resistance varies with the input voltage, as illustrated in Figure 1.

$$R_{EQ} = \frac{R_{onp} R_{onn}}{R_{onp} + R_{onn}}$$

Figure 4.1 The maximum value of Req is approximately 4 k Ohm. The transmission gate is the basis for D-Latch and/or D Flip-

flop which are very important to circuit design for holding data.

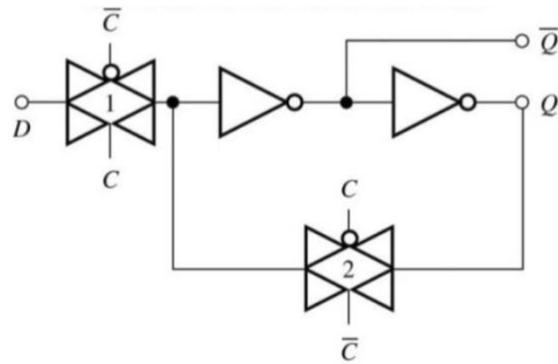


Figure 4.2 Schematic of a Transmission Gate

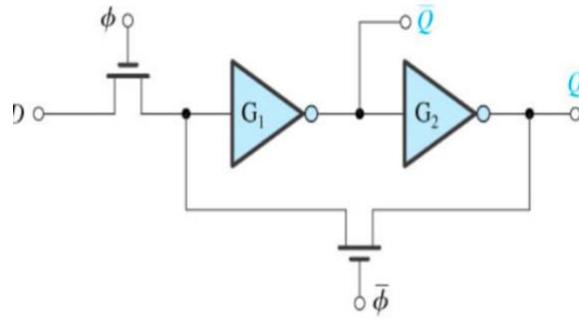


Figure 4.3 A Simple D Flip-flop Implementation

I.IV. EXPERIMENTAL AND SIMULATION SETUPS

The experiment has multiple cases with different ranges of frequencies and input

voltages, but the exact circuit is used. Once again this circuit can be seen in Fig. 1b. The case ranges are as follows:

1)v_{in(t)} Sine wave in the range 50mV \leq 200mV

Sine input frequency in the range 5 kHz \leq f_{v_in} \leq 10 kHz clock input frequency (f_{clk} = 20 x f_{v_in}) in the range 100 kHz \leq f_{clk} \leq 200 kHz

2)

v_{in(t)} Sine wave in the range 300mV \leq 500mV

Sine input frequency in the range 15 kHz \leq f_{v_in} \leq 20 kHz clock input frequency (f_{clk} = 20 x f_{v_in}) in the range 300 kHz \leq f_{clk} \leq 400 kHz

3)

v_{in(t)} Sine wave in the range 600mV \leq 1V
Sine input frequency in the range 30 kHz \leq f_{v_in} \leq 40 kHz clock input frequency (f_{clk} = 20 x f_{v_in}) in the range 600 kHz \leq f_{clk} \leq 800 kHz

4)

v_{in(t)} Triangular waveform with same as [Case #1] specification

5)

v_{in(t)} Ramp waveform with same as [Case #2] specification.

6) v_{in(t)} Triangular waveform with same as [Case #3] specification.

I.V. EXPERIMENTAL AND SIMULATION DATA AND RESULTS

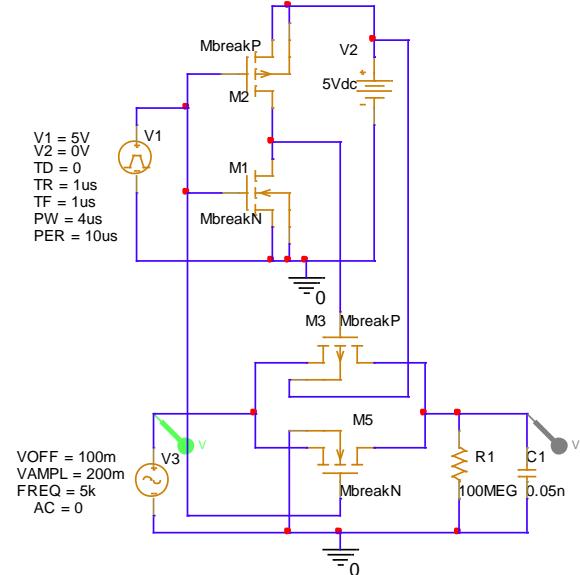


Figure 4.4: CMOS Transition Gate with 5 kHz sine wave frequency and 200mV peak schematic

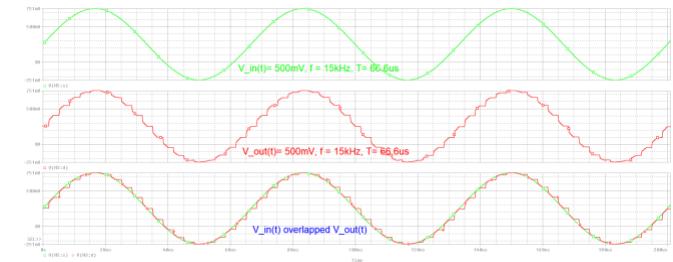


Figure 4.5: CMOS Transition Gate with 5 kHz sine wave frequency and 200mV peak output waveforms

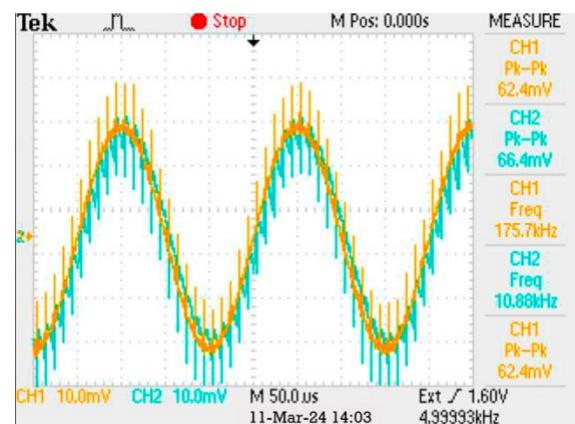


Figure 4.6: CMOS Transition Gate with 5 kHz sine wave frequency and 200mV peak output waveforms

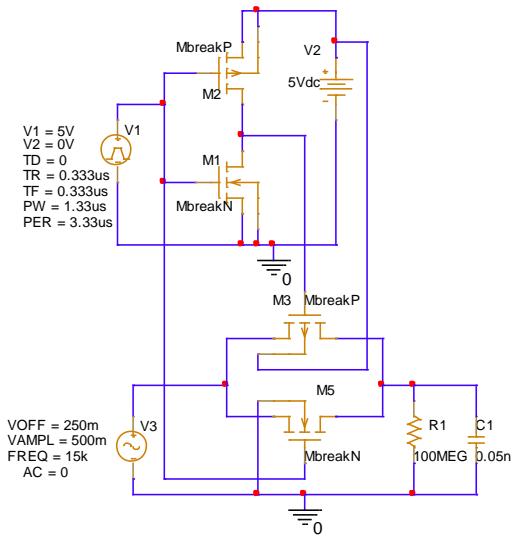


Figure 4.7: CMOS Transition Gate with 15 kHz sine wave frequency and 500mV peak schematic

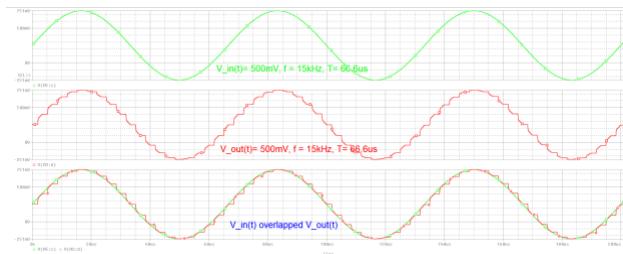


Figure 4.8: CMOS Transition Gate with 15 kHz sine wave frequency and 500mV peak schematic output waveforms

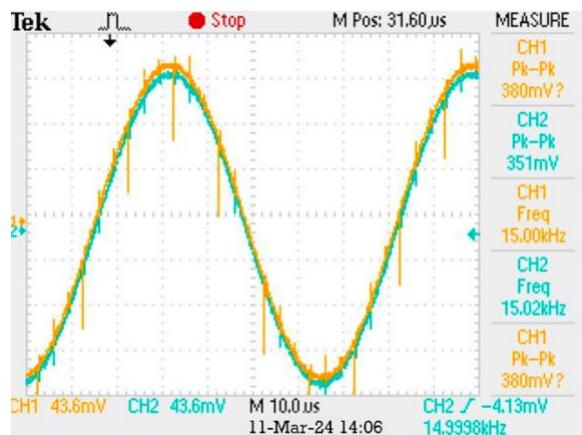


Figure 4.9 CMOS Transition Gate with 15 kHz sine wave frequency and 500mV peak schematic output waveforms

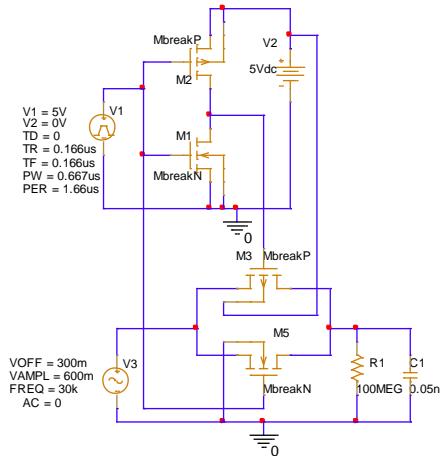


Figure 4.10 CMOS Transition Gate with 30 kHz sine wave frequency and 600mV peak schematic

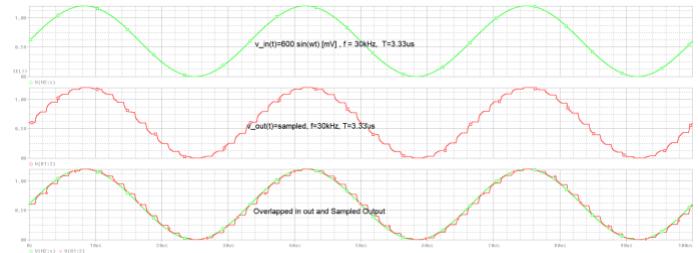


Figure 4.11: CMOS Transition Gate with 30 kHz sine wave frequency and 600mV peak output waveforms

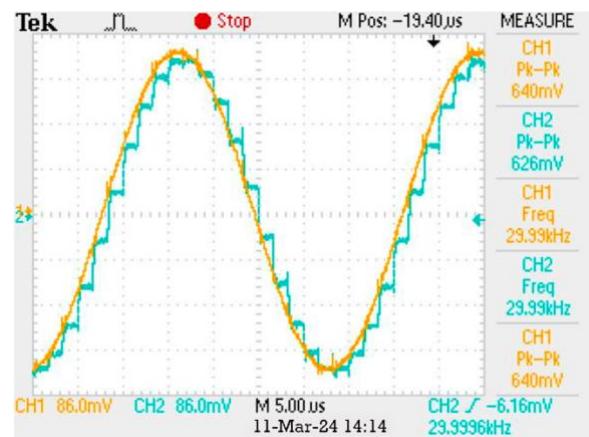


Figure 4.12: CMOS Transition Gate with 30 kHz sine wave frequency and 600mV peak output waveforms

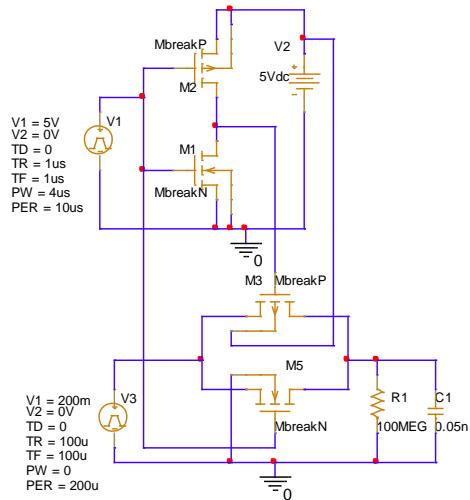


Figure 4.13: CMOS Transition Gate Triangular input wave with case 1 values schematic

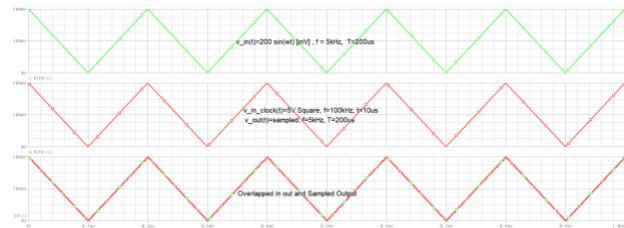


Figure 4.14: CMOS Transition Gate Triangular input wave with case 1 values output waveforms

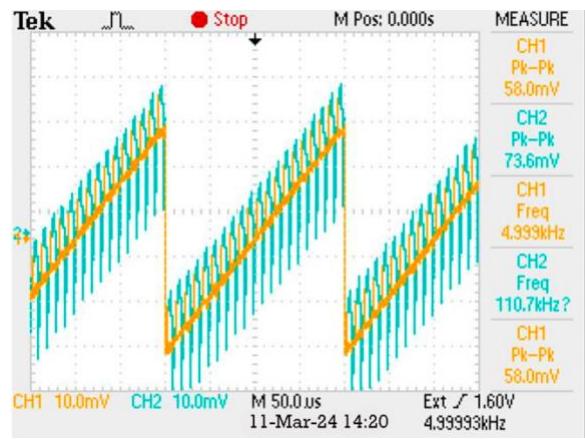


Figure 4.15: CMOS Transition Gate Triangular input wave with case 1 values output waveforms

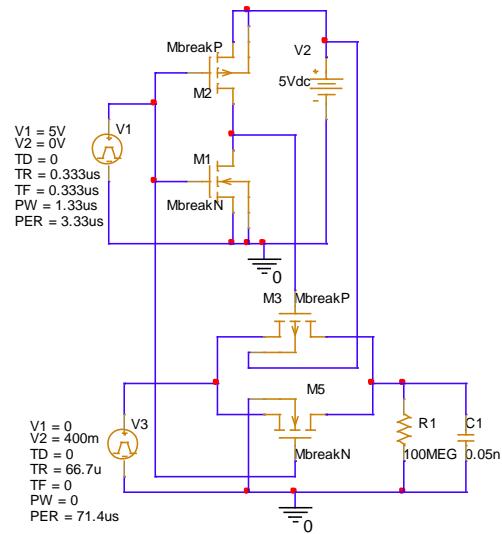


Figure 4.16: CMOS Transition Gate Ramp input wave with case 2 values schematic

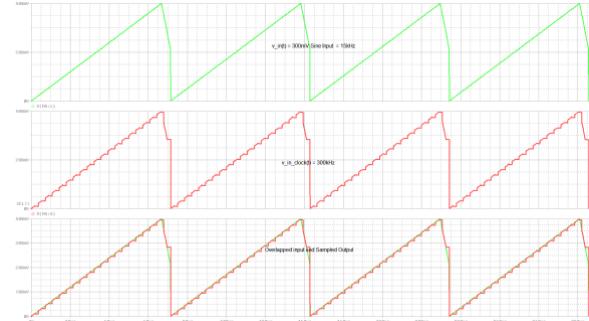


Figure 4.17: CMOS Transition Gate Ramp input wave with case 2 values output waveforms

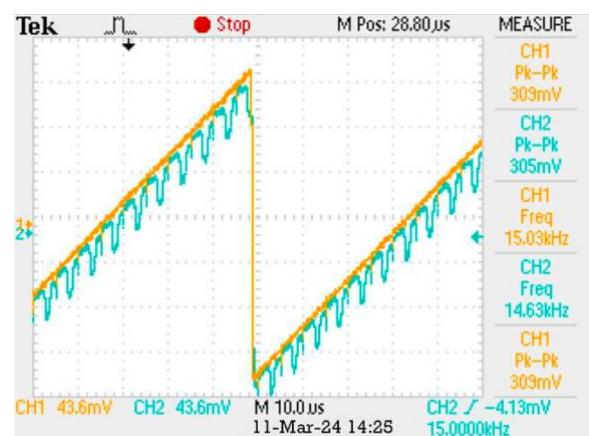


Figure 4.18: CMOS Transition Gate Ramp input wave with case 2 values output waveforms

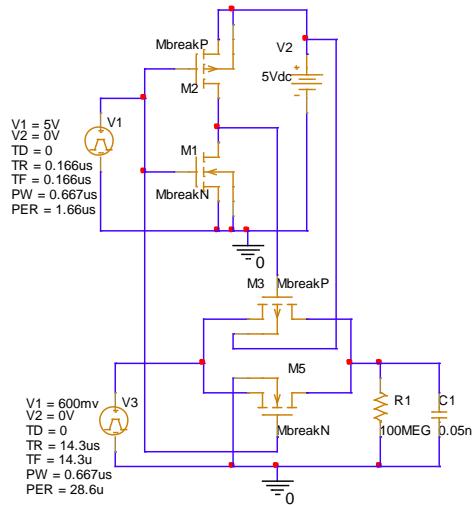


Figure 4.19: CMOS Transition Gate Triangular input wave with case 3 values schematic

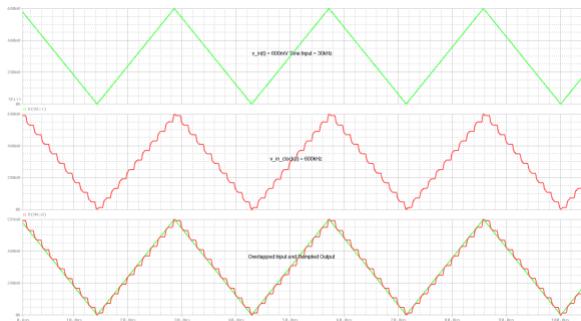


Figure 4.20: CMOS Transition Gate Triangular input wave with case 3 values output waveforms

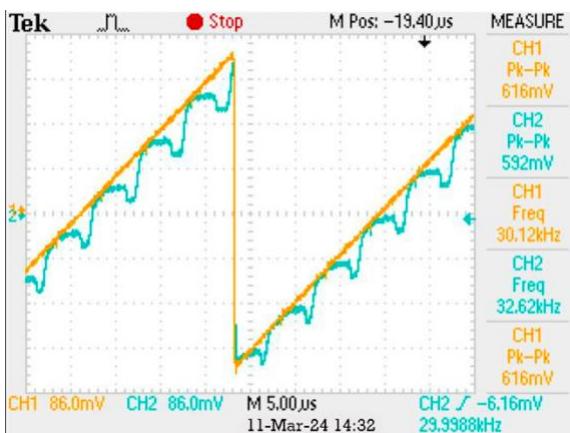


Figure 4.21: CMOS Transition Gate Triangular input wave with case 3 values output waveforms

I.VI. DISCUSSION AND CONCLUSION

This laboratory session proved to be quite frustrating during the circuit construction phase. Unfortunately, there wasn't much guidance available, which led to numerous avoidable errors that could have been prevented if theoretical aspects were emphasized or illustrated.

One issue encountered in this lab was the presence of noise on the oscilloscope display. This problem was resolved by replacing the probes and adjusting the capacitor. Ultimately, we successfully achieved the desired pausing and holding functionality for a specific duration. The clock played a crucial role in maintaining the output while the CMOS transmission gate facilitated transitions between Vdd and Vss voltages.

I.VII. REFERENCES

- [1] ECE442 Lab Report
- [2] Jaeger, R. C., Blalock, T. N., & Blalock, B. J. (2023). *Microelectronic Circuit Design*. McGraw Hill LLC.
- [3] Supporting Slides on CMOS Transition Theory – Sequare Daniel-Berhe, Ph.D.

CMOS D-LATCH DESIGN, SIMULATION AND EXPERIMENTAL TEST AS WELL AS ANALYSIS

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I.I. ABSTRACT

Create a CMOS D-latch switch using PSPICE and conduct experimental analysis. Evaluate the utilization of the 7474 Flip Flop as a frequency divider.

I.II. KEY WORDS

CMOS, NMOS, PMOS, D-latch, Flip-flop, frequency divider, Q & Q_bar, CMOS DATA

I.III. INTRODUCTION

The D flip-flop and D-latch are among the most commonly employed circuits in CMOS design. Outputs of sequential circuits are influenced by both past and present input states. These circuits incorporate memory elements like the D-latch to retain data. These memory elements serve to ensure proper sequencing. In the absence of sequencing, subsequent elements may overtake previous ones, resulting in corruption of both. Consequently, a Sequencing Delay is introduced into these circuits to postpone elements that arrive prematurely.

Enable	D	Q+	Q'+
1	1	1	0
1	0	0	1
0	1	Q	Q'
0	0	Q	Q'

Figure 5.1 D-Latch Truth Table

You can observe this behavior in the table provided. When the clock signal is at a low level, the flip-flop remains in its memory or reset state. Changes in the D input signal during this time do not affect the state of the flip-flop. When the clock signal transitions to a high level, the flip-flop captures the logic level present on the D input just before the rising edge of the clock. This type of flip-flop is known as edge-triggered.

Below is the design of the D-latch, featuring two transmission gates. Each transmission gate consists of an NMOS and PMOS transistor connected source to source and drain to drain. The gates of these transistors are connected to the clock and its complement (clock-bar), where the clock signal is inverted by the "driver." The

inverters depicted in the diagram below are simply CMOS inverters.

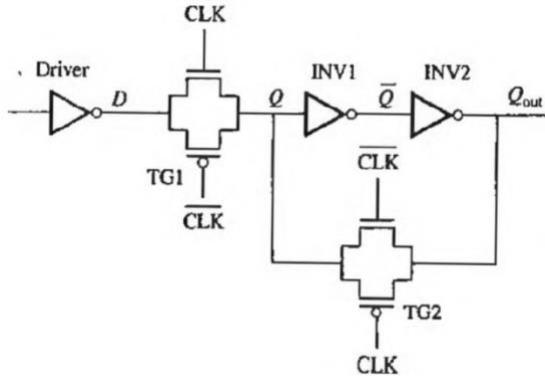


Figure 5.2: D-Latch Diagram

A crucial aspect of this experiment involves frequency division achieved through the utilization of the 7474 chip, as depicted in Figure 3, which provides fundamental details about the division process. In this scenario, the output frequency is circulated within the 7474 chips to attain the desired frequency division.

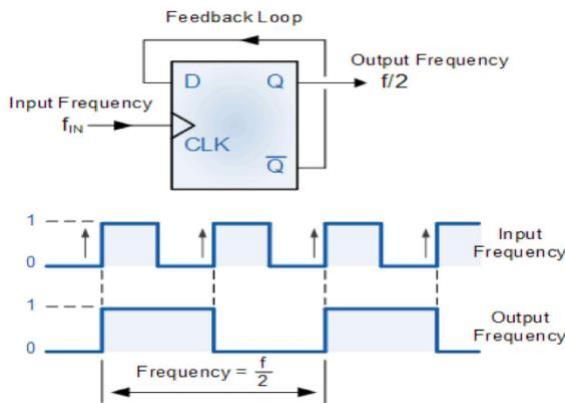


Figure 5.3: Frequency Division

I.IV. EXPERIMENTAL AND SIMULATION SETUPS

The experiment involves various scenarios with different frequency ranges, all divided by the 7474 chip, while maintaining the same circuit layout, which is illustrated in Fig. 1b.

The first scenario entails a 5V square wave input clock with a frequency of 100kHz divided by 2. The second scenario involves the same input clock, but divided by 4. The third scenario deals with the input clock divided by 8, while the fourth scenario divides the input clock by 16, all operating at 5V.

I.V. EXPERIMENTAL AND SIMULATION DATA AND RESULTS

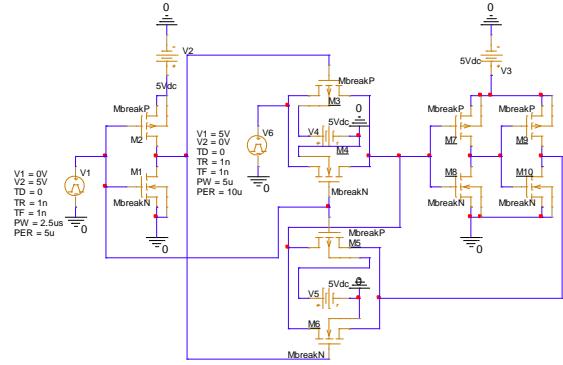


Figure 5.4: CMOS D-Latch Design applying a 5V rectangular waveform input with a frequency 100kHz and Clock divided by 2

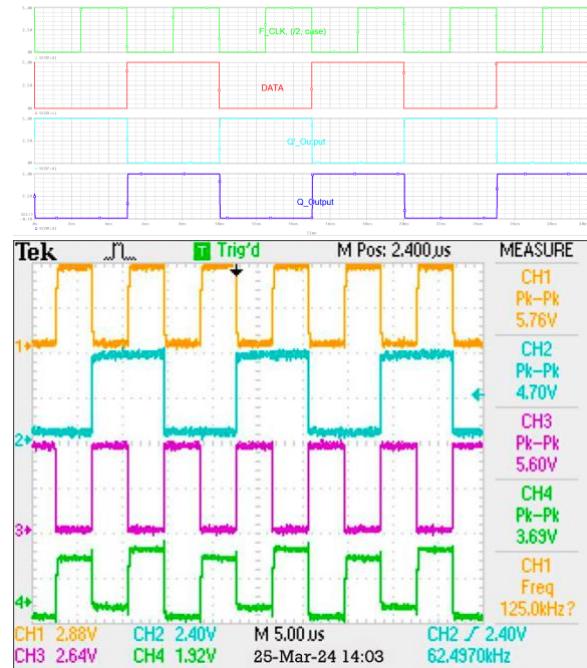


Figure 5.5: Simulation and Experimental I/p – O/p CMOS D-Latch Design applying a 5V rectangular waveform input with a frequency 100kHz and Clock divided by 2

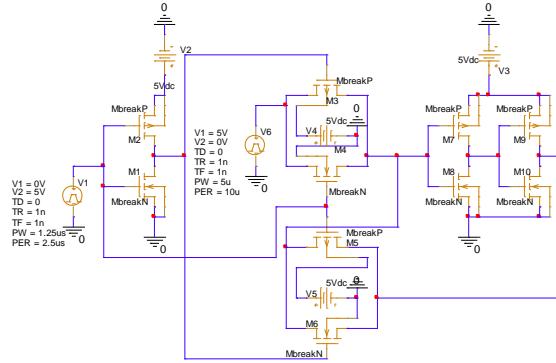


Figure 5.6: CMOS D-Latch Design applying a 5V rectangular waveform input with a frequency 100kHz and Clock divided by 4

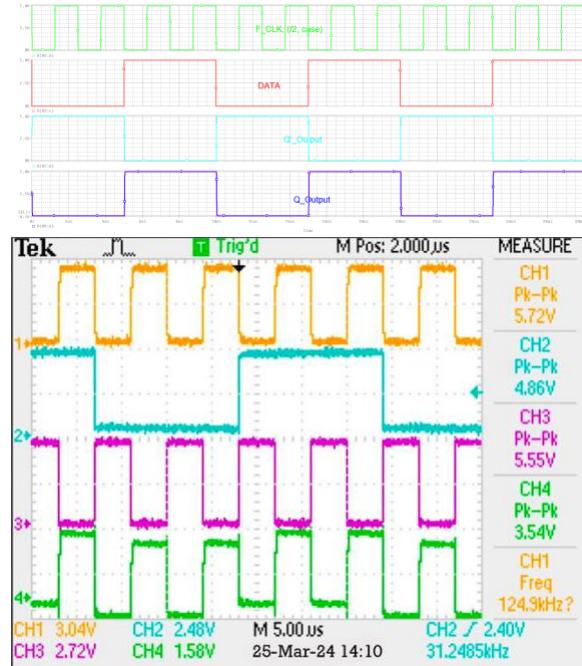


Figure 5.7: Simulation and Experimental I/p – O/p CMOS D-Latch Design applying a 5V rectangular waveform input with a frequency 100kHz and Clock divided by 4

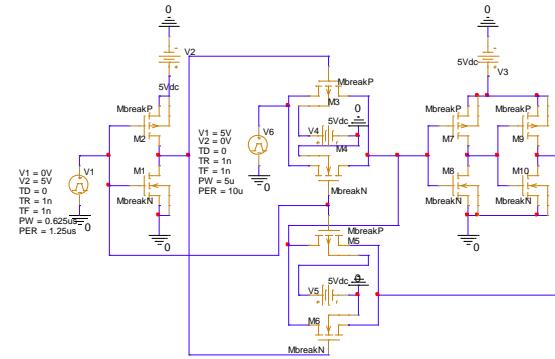


Figure 5.8: CMOS D-Latch Design applying a 5V rectangular waveform input with a frequency 100kHz and Clock divided by 8

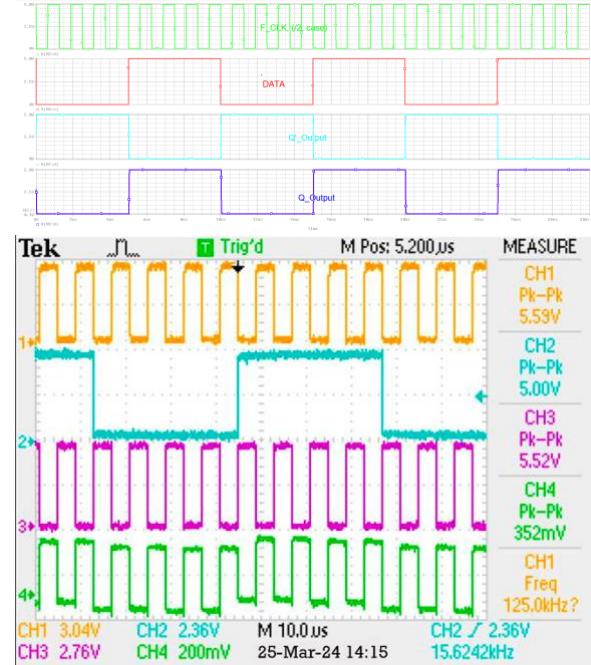


Figure 5.9: Simulation and Experimental I/p – O/p CMOS D-Latch Design applying a 5V rectangular waveform input with a frequency 100kHz and Clock divided by 8

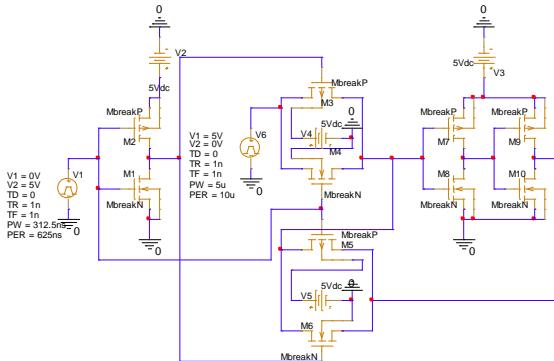


Figure 5.10: Simulation and Experimental I/p – O/p CMOS D-Latch Design applying a 5V rectangular waveform input with a frequency 100kHz and Clock divided by 16

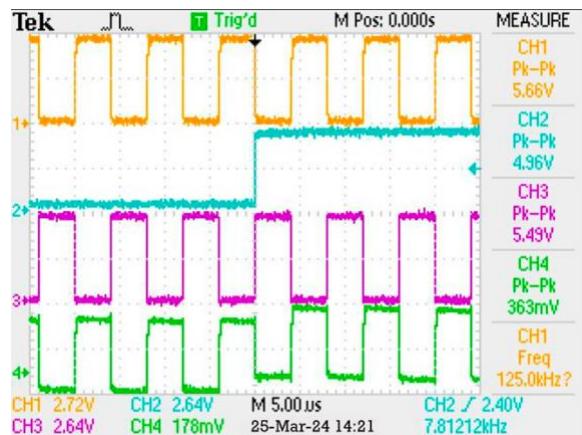
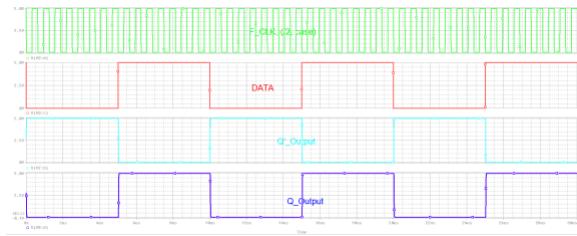


Figure 5.11: Simulation and Experimental I/p – O/p CMOS D-Latch Design applying a 5V rectangular waveform input with a frequency 100kHz and Clock divided by 16

I.VI. DISCUSSION AND CONCLUSION

This experiment presented several challenges for us. Initially, we had to determine whether the circuit was experiencing random noise due to shorts or incorrect grounds, or if the issue stemmed from the CD4007 chip itself.

After rebuilding the circuit multiple times, we deduced that the problem lay with the chip, either due to burnout or internal shorting. Upon using different integrated circuits (ICs), our input/output (I/O) behavior closely mirrored the PSpice graph, confirming that our waveform aligned with the truth table. This validation affirmed the results of our experiment.

I.VII. REFERENCES

- [1] ECE442 Lab Report
- [2] Jaeger, R. C., Blalock, T. N., & Blalock, B. J. (2023). *Microelectronic Circuit Design*. McGraw Hill LLC.
- [3] Supporting Slides on CMOS Transition Theory – Sequare Daniel-Berhe, Ph.D

CMOS NAND BASED S-R LATCH DESIGN, SIMULATION AND EXPERIMENTAL TEST AS WELL AS ANALYSIS

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I.I. ABSTRACT

The CMOS NAND-based S-R latch is a mix of a NAND gate and an S-R latch design. It's made using CMOS technology, which uses two types of transistors. This latch stores one bit of information by connecting two NAND gates in a loop.

It works in two stages: hold and set/reset. In the hold stage, it keeps its current state and ignores inputs. In the set/reset stage, the NAND gates get turned on, allowing input signals to change its state.

I.II. KEY WORDS

NMOS, PMOS, CMOS, Rectangular Waveform, Frequency

I.III. INTRODUCTION

The CMOS NAND-based S-R latch is valuable in sequential circuits for storing binary data. By merging NAND and S-R latch designs, it minimizes the transistor count, enhancing efficiency. Its application extends to high-speed operations.

This latch boasts numerous benefits, including its compact size, straightforwardness, and compatibility with

contemporary circuits. As a fundamental component, it plays a crucial role in various digital applications and system designs.

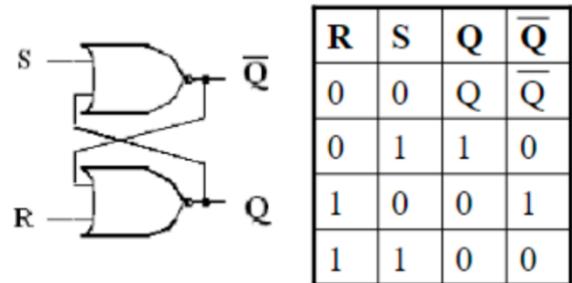


Figure 6.1 NOR RS Flip-flop Schematic

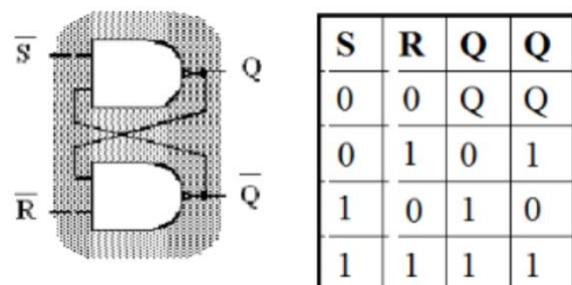


Figure 6.2 NAND RS Flip-flop Schematic

I.IV. EXPERIMENTAL AND SIMULATION SETUPS

The experiment involved various scenarios with different frequency ranges, all using the same circuit depicted in Figure 1b. The frequency ranges are outlined as follows:

- 1) Frequencies ranging from 100 kHz to 200 kHz
- 2) Frequencies ranging from 300 kHz to 500 kHz
- 3) Frequencies ranging from 600 kHz to 800 kHz
- 4) Frequencies ranging from 900 kHz to 1.2 MHz

I.V. EXPERIMENTAL AND SIMULATION DATA AND RESULTS

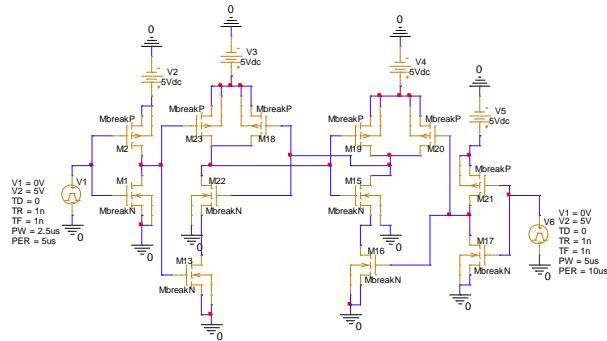


Figure 6.3 Schematic of 5V Rectangular Waveform Input with a Frequency of 126 kHz

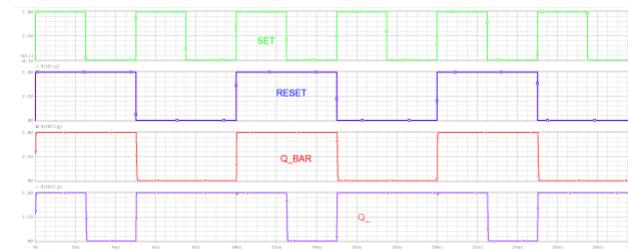


Figure 6.4 Simulation of 5V Rectangular Waveform Input with a Frequency of 126 kHz

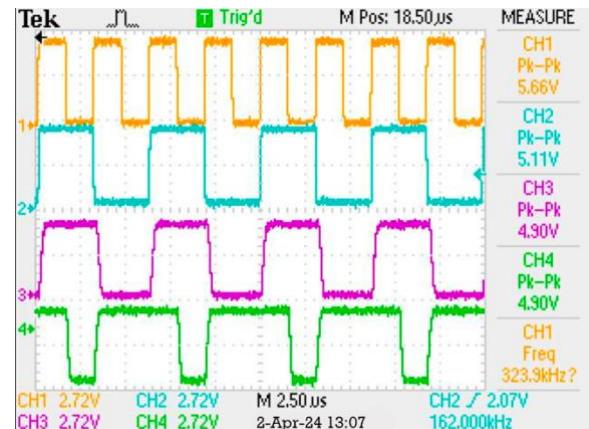


Figure 6.5 Experimental with a 5V Rectangular Waveform Input with a Frequency of 126 kHz

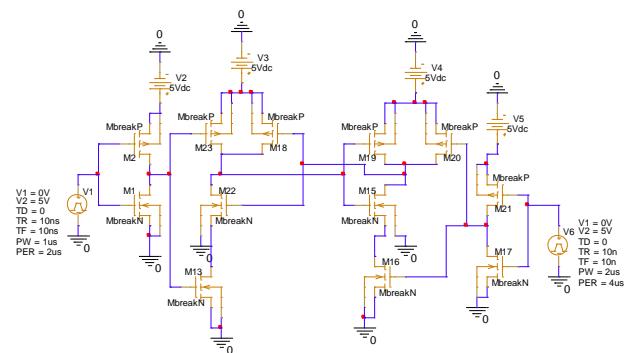


Figure 6.6 Schematic of 5V Rectangular Waveform Input with a Frequency of 324 kHz

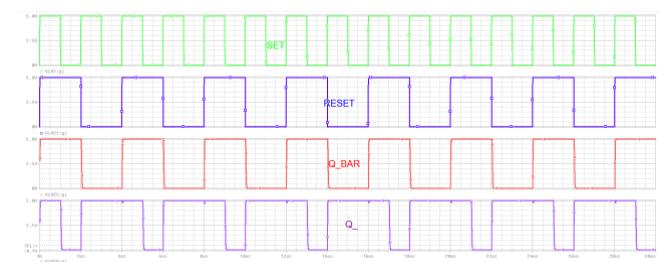


Figure 6.7 Simulation of 5V Rectangular Waveform Input with a Frequency of 324 kHz

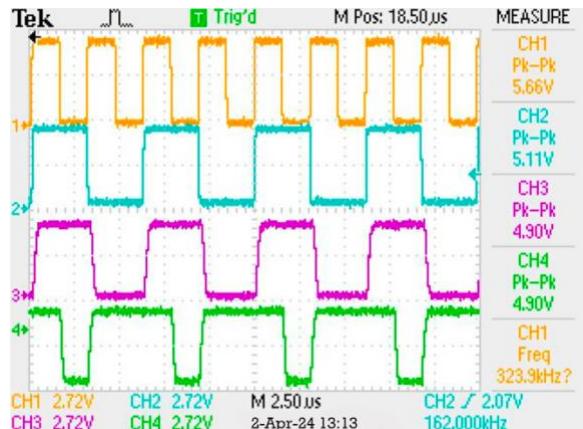


Figure 6.8 Experimental with a 5V Rectangular Waveform Input with a Frequency of 324 kHz

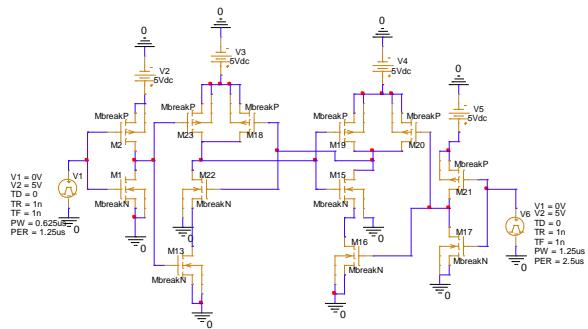


Figure 6.9 Schematic of 5V Rectangular Waveform Input with a Frequency of 624 kHz

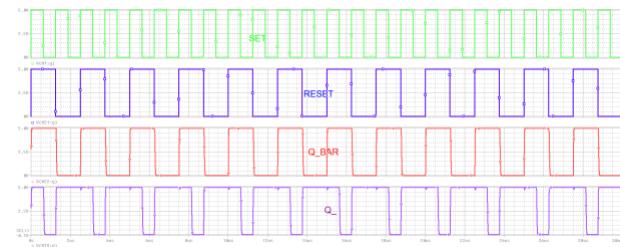


Figure 6.10 Simulation of 5V Rectangular Waveform Input with a Frequency of 624 kHz

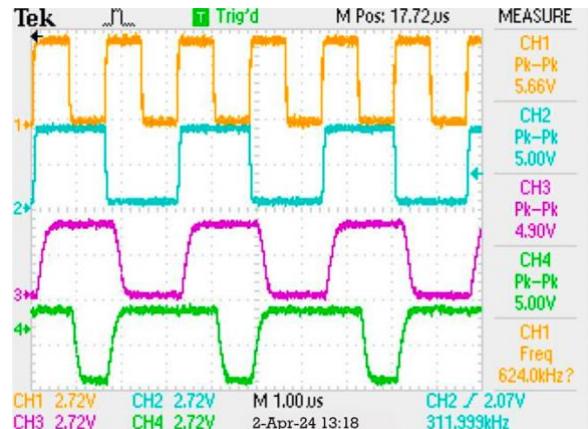


Figure 6.11 Experimental with a 5V Rectangular Waveform Input with a Frequency of 624 kHz

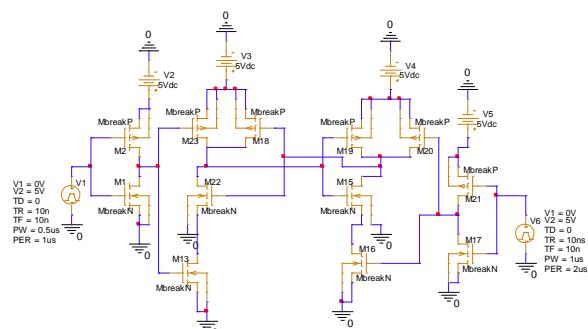


Figure 6.12 Schematic of 5V Rectangular Waveform Input with a Frequency of 1.2 MHz

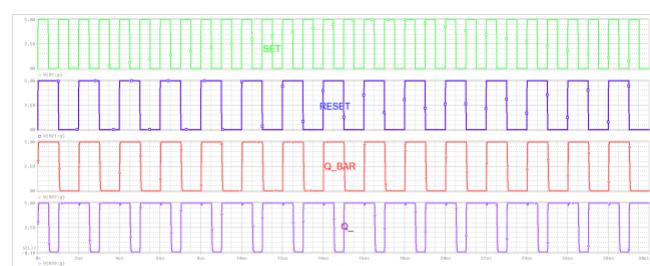


Figure 6.13 Simulation of 5V Rectangular Waveform Input with a Frequency of 1.2 MHz

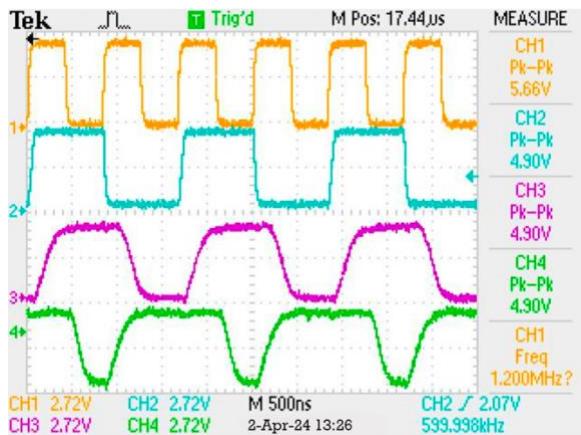


Figure 6.14 Experimental with a 5V Rectangular Waveform Input with a Frequency of 1.2 MHz

I.VI. DISCUSSION AND CONCLUSION

We achieved the correct logic outputs for Q and Q', yet, as the frequency increased, we encountered significant distortion due to the chips' low quality. This distortion became noticeable as early as 600KHz, and particularly evident at 900KHz, causing the square waveforms of our Q and Q' readings to become distorted and weakened. Despite this challenge, we successfully completed the experiment, and its validity was confirmed by the output graphs aligning with the logic diagram of the SR latch.

I.VII. REFERENCES

- [1] ECE442 Lab Report
- [2] Jaeger, R. C., Blalock, T. N., & Blalock, B. J. (2023). *Microelectronic Circuit Design*. McGraw Hill LLC.
- [3] Supporting Slides on CMOS Transition Theory – Sequare Daniel-Berhe, Ph.D.

CMOS 4X4 NOR ROM ARRAY DESIGN, SIMULATION AND EXPERIMENTAL TEST AS WELL AS ANALYSIS

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I.I. ABSTRACT

The CMOS 4x4 NOR ROM configuration comprises 4 rows and 4 columns of NOR gates, serving as a memory arrangement for predetermined data. Address bits inputted determine the cell within this matrix. Upon matching the input address to a specific row and column, the corresponding NOR gate outputs a logical high "1," while the rest produce logical lows "0." Memory access to a particular cell involves activating the word line with a high signal. Subsequently, the transistor connected to the bit line being activated facilitates reading from that cell. It works in two stages: hold and set/reset. In the hold stage, it keeps its current state and ignores inputs. In the set/reset stage, the NAND gates get turned on, allowing input signals to change its state.

I.II. KEY WORDS

NMOS, PMOS, CMOS, Load Capacitance, Oscillation, Frequency, and Voltage

I.III. INTRODUCTION

The CMOS 4x4 NOR ROM comprises a grid of 4 rows and 4 columns of NOR gates, forming a memory system for pre-set data. By inputting address bits, one can pinpoint a specific cell, causing its corresponding NOR

gate to produce a unique logic output while the others generate different values. This setup establishes a memory lookup table, enabling the array to yield distinct outputs according to input addresses. With its fixed data storage, the array eliminates the need for additional storage, thereby enhancing efficiency.

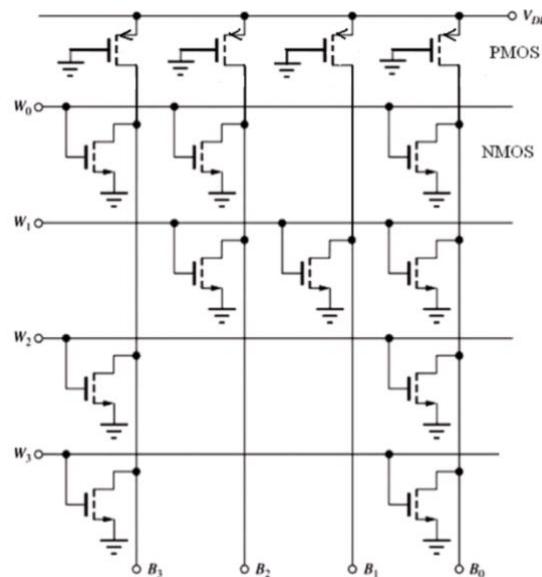


Figure 7.1 NMOS static ROM with 4-bit words

W0	W1	W2	W3	B3	B2	B1	B0
1	0	0	0	0	0	1	0
0	1	0	0	1	0	0	0
0	0	1	0	0	1	1	0
0	0	0	1	0	1	1	0

Figure 7.2 NMOS static ROM with 4-bit words truth table

I.IV. EXPERIMENTAL AND SIMULATION SETUPS

The experiment involved various scenarios with different frequency ranges, all using the same circuit depicted in Figure 7.1. The frequency ranges are outlined as follows:

- 1) Frequencies ranging from 100 kHz to 200 kHz
- 2) Frequencies ranging from 300 kHz to 500 kHz
- 3) Frequencies ranging from 600 kHz to 800 kHz
- 4) Frequencies ranging from 900 kHz to 1.2 MHz

I.V. EXPERIMENTAL AND SIMULATION DATA AND RESULTS

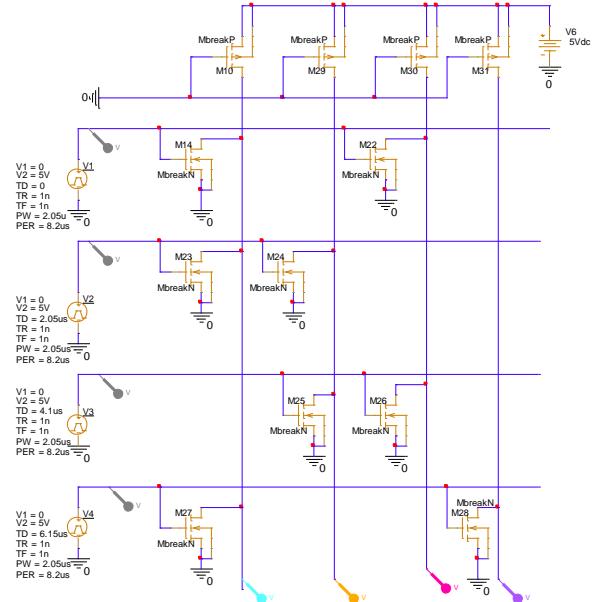
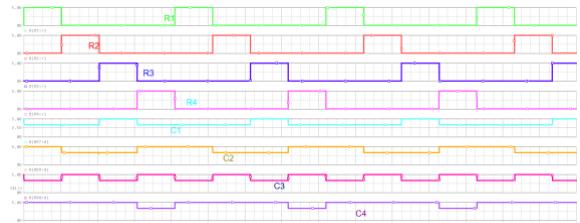
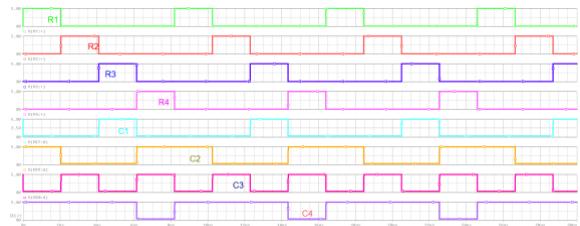


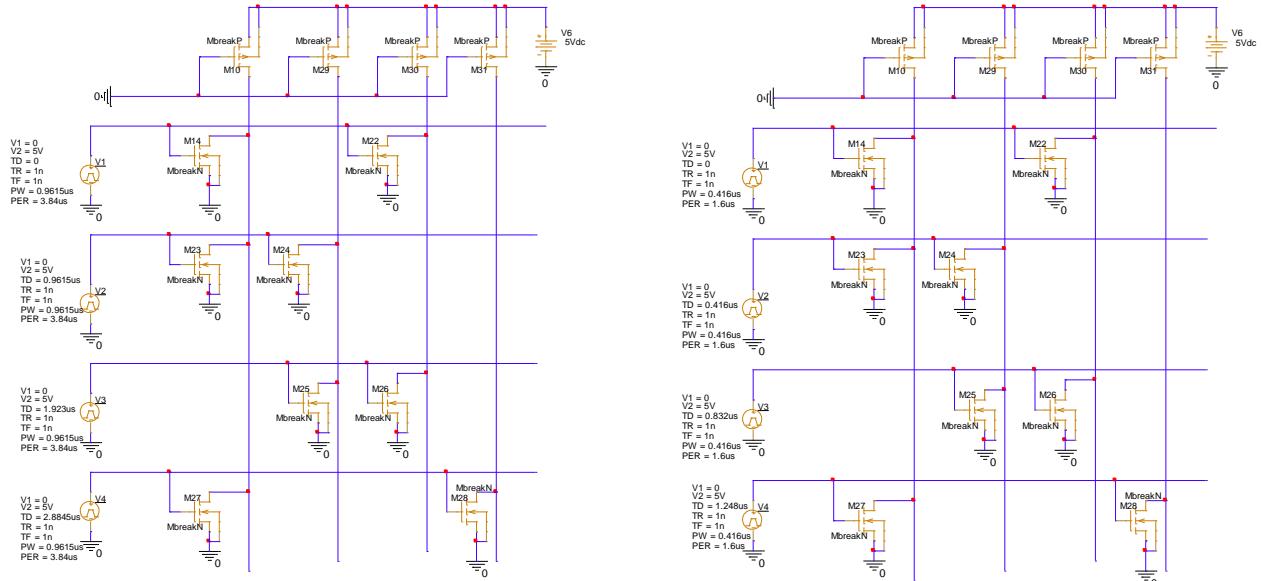
Figure 7.3 Schematic of CMOS 4x4 NOR ROM 5V Rectangular Waveform Input with a Frequency of 126 kHz



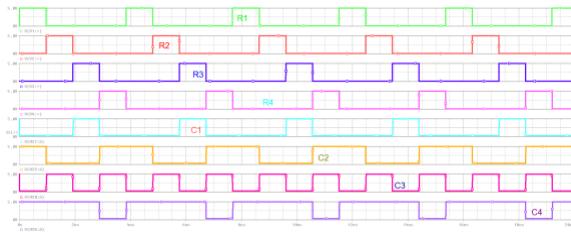
7.4 Simulation I of CMOS 4x4 NOR ROM 5V Rectangular Waveform Input with a Frequency of 126 kHz



7.5 Simulation II of CMOS 4x4 NOR ROM 5V Rectangular Waveform Input with a Frequency of 126 kHz

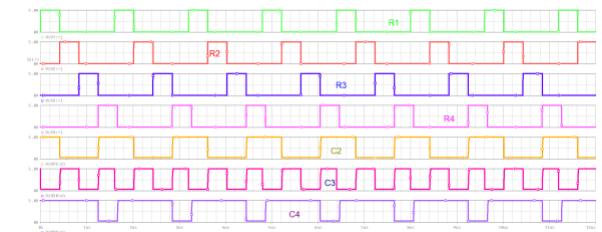


7.6 Schematic of CMOS 4x4 NOR ROM 5V Rectangular Waveform Input with a Frequency of 324 kHz

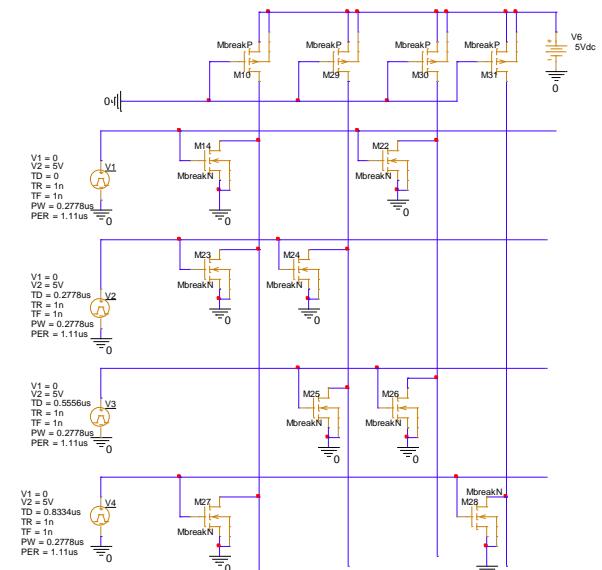


7.7 Simulation of CMOS 4x4 NOR ROM 5V Rectangular Waveform Input with a Frequency of 324 kHz

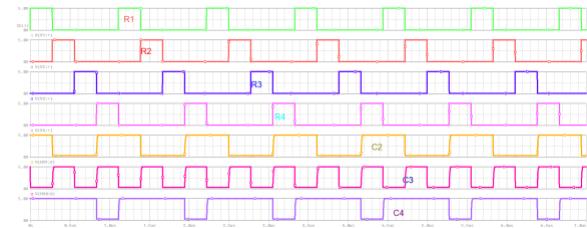
Figure 7.8 Schematic of CMOS 4x4 NOR ROM 5V Rectangular Waveform Input with a Frequency of 624 kHz



7.9 Simulation of CMOS 4x4 NOR ROM 5V Rectangular Waveform Input with a Frequency of 624 kHz



**7.10 Schematic of CMOS 4x4 NOR ROM
5V Rectangular Waveform Input with a
Frequency of 1.2 MHz**



**7.11 Simulation of CMOS 4x4 NOR ROM
5V Rectangular Waveform Input with a
Frequency of 1.2 MHz**

I.VI. DISCUSSION AND CONCLUSION

Reviewing the lab schematic revealed a lack of clarity regarding the necessity for repeatedly dividing the input. Troubles arose particularly with the D flip-flop, where even minor errors necessitated circuit reworking. Regrettably, we were unable to fully achieve circuit functionality. On the positive side, no apparent issues arose with the PSPICE simulation. The instructions were straightforward to follow and execute.

I.VII. REFERENCES

- [1] ECE442 Lab Report
- [2] Jaeger, R. C., Blalock, T. N., & Blalock, B. J. (2023). *Microelectronic Circuit Design*. McGraw Hill LLC.
- [3] Supporting Slides on CMOS Transition Theory – Sequare Daniel-Berhe, Ph.D.

CMOS SEVEN RING VOLTAGE CONTROL OSCILLATOR DESIGN, SIMULATION AND EXPERIMENTAL TEST AS WELL AS ANALYSIS

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I.I. ABSTRACT

In this experiment, we'll be using a specific electronic component called a CMOS seven ring. It's similar to what we used in Lab 3, but this time we'll be changing the voltage. As we move the voltage from 2V to 5V, we'll take pictures with our oscilloscope, create a table, and draw a graph showing how VDD (voltage) affects frequency. It's important to keep our mistakes to less than 1% before we start lowering the voltage.

I.II. KEY WORDS

NMOS, PMOS, CMOS, Load Capacitance, Oscillation, Voltage and Frequency

I.III. INTRODUCTION

The CMOS inverter holds significance within digital circuits, leveraging the Boolean logic of an inverter. However, the significance escalates when multiple CMOS inverters are arranged in series or cascaded. This configuration proves crucial as it offers a straightforward method for generating a primary clock signal.

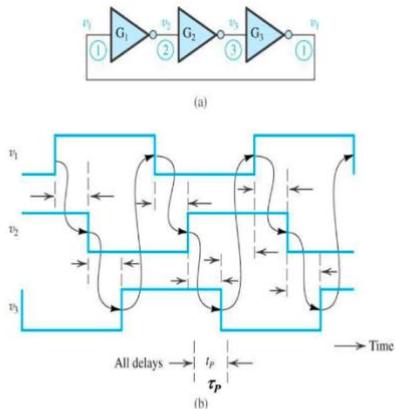


Fig. 1 CMOS Inverted Ring Oscillator and Gate Operations

Figure 8.1 CMOS Inverted Ring Oscillator and Gate Operations

Figure 1.a depicts the fundamental circuit, comprising a series arrangement of CMOS inverters. Another requirement specified is that the circuit must include an odd number of inverters, as illustrated in Figure 1.b. An interesting observation is that the gate path initiates with a rising edge at the first gate, traverses through subsequent gates, and eventually returns to the original rising clock. A ring oscillator, characterized by an odd number of inverter stages, generates oscillating signals at each node. The oscillation period is determined by the delay inherent in each stage and the total number of stages, which in this case is denoted as $3 t_p$ in

the figure. Nonetheless, the resultant clock signal may exhibit significant variations depending on the manufacturing process, rendering it process-dependent and potentially unstable.

Odd number of stages

$$\tau_{PHL} \cong 2R_{onN}C \left\{ \ln \left[4 \left(\frac{V_{DD} - V_{TN}}{V_{DD} + V_L} \right) - 1 \right] + \frac{1}{2} \right\}$$

$$\tau_{PLH} \cong 2R_{onP}C \left\{ \ln \left[4 \left(\frac{V_{DD} + V_{TP}}{V_H} \right) - 1 \right] + \frac{1}{2} \right\}$$

$$f_{osc} = \frac{1}{n(\tau_{PHL} + \tau_{PLH})} = \frac{1}{2n\tau_p} \quad \& \quad \tau_p = \frac{1}{2nf_{osc}}$$

Figure 8.2 Formulas for Path delay and Frequency of Oscillation of the Ring Oscillator

This report will discuss the simulations conducted on cascading CMOS inverters, along with the related equations. The simulations encompass the assessment of propagation delay and oscillating frequency, both of which can be deduced by computing the delays at individual signals, as illustrated in Figure 3.

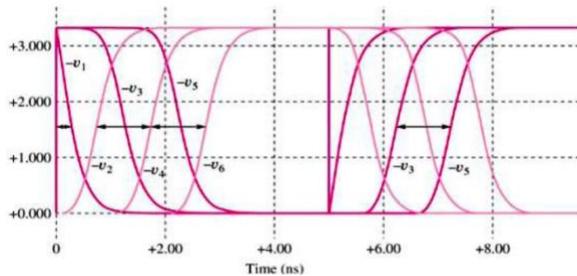


Figure 8.3 Oscillating Frequency Output

Furthermore, this lab experiment will employ the CD4007 CMOS chip, with each NMOS and PMOS arranged in series and in an odd number of stages. The layout of the circuit can be observed in Figure 4.

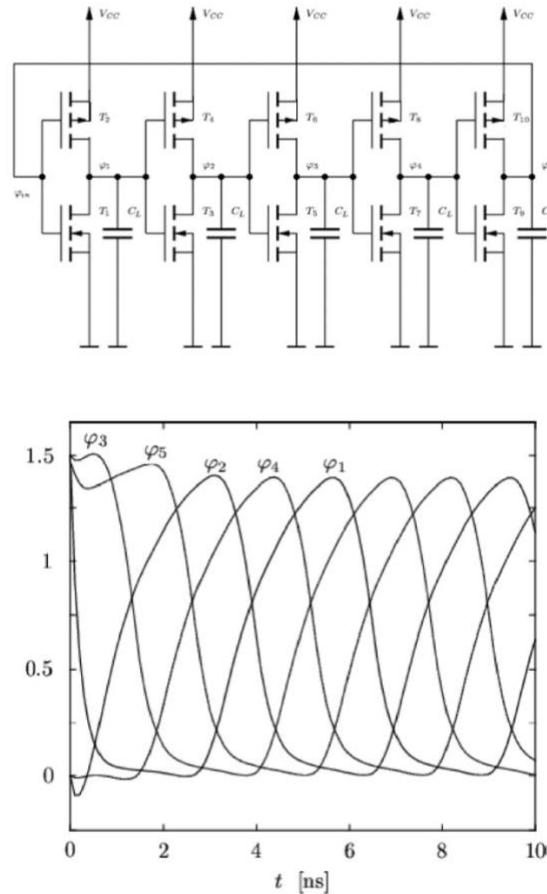


Figure 8.4 Ring Oscillator Circuit and Output

I.IV. EXPERIMENTAL AND SIMULATION SETUPS

Once we set up the circuit, we made different clock signals by changing the power supply voltage. We started at 5 volts and lowered it to 2 volts in steps of 0.25 volts. To make sure we had less than a 1% mistake, we added the right load capacity to each inverter's output. This let us figure out the error percentage, which needed to be below 1% before we

continued with the experiment. Then, we measured the supply voltage (VDD), the time it took for each cycle, and how often it repeated for each channel.

I.V. EXPERIMENTAL AND SIMULATION DATA AND RESULTS

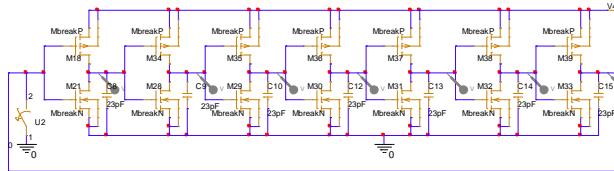


Figure 8.5 Ring Voltage Control Oscillator Circuit with 7 inverters at 5V bias

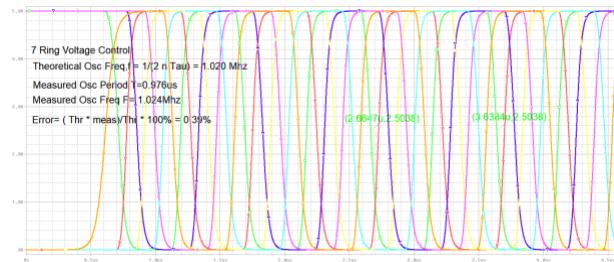


Figure 8.6 I/p – O/p Waveform of the Ring Voltage Control Oscillator circuit with 7 inverters at 5V bias

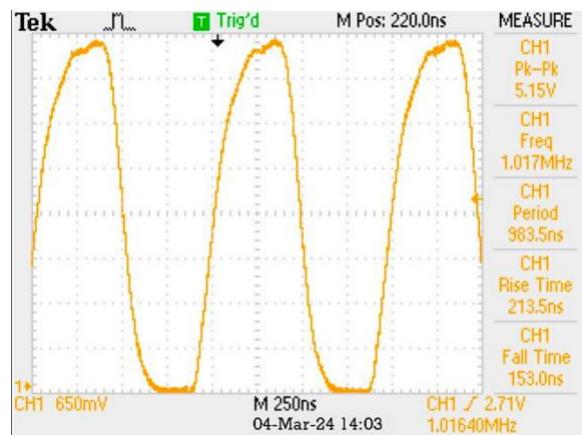


Figure 8.7 Simulation of 7 Ring Oscillation Circuit with an Error Percentage of 0.49%

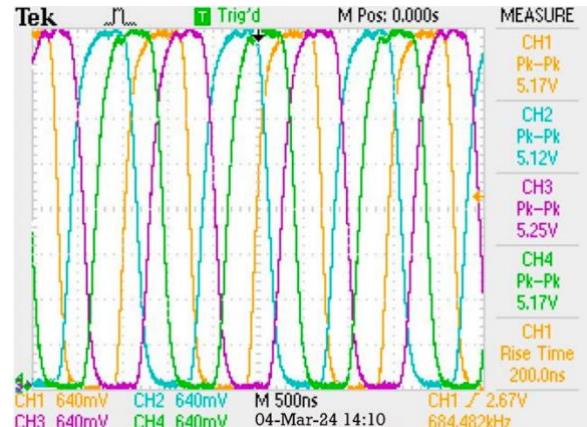


Figure 8.8 The Full First Half Simulation of 7 Ring Oscillation Circuit with an Error Percentage of 0.49%

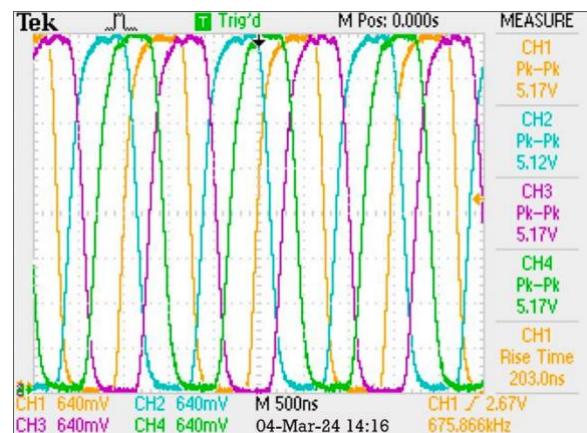


Figure 8.9 The Full Last Half Simulation of 7 Ring Oscillation Circuit with an Error Percentage of 0.49%

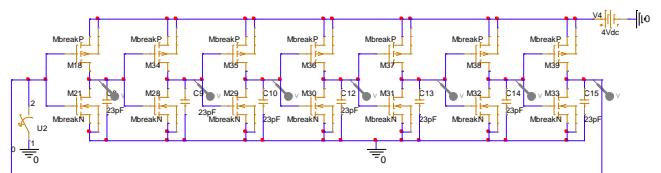


Figure 8.10 Ring Voltage Control Oscillator Circuit with 7 inverters at 4V bias

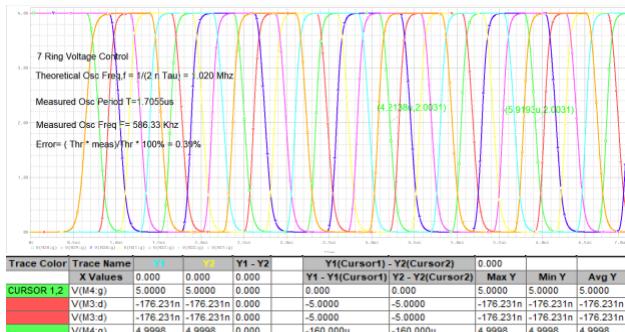


Figure 8.11 I/p – O/p Waveform of the Ring Voltage Control Oscillator circuit with 7 inverters at 4V bias

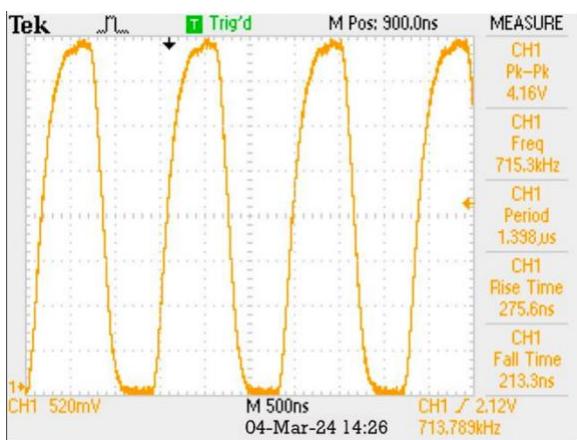


Figure 8.12 Simulation of 7 Ring Oscillation Circuit for 4V

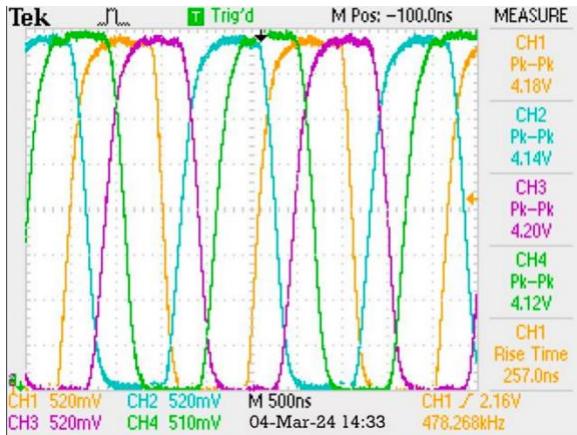


Figure 8.13 The Full First Half Simulation of 7 Ring Oscillation Circuit for 4V

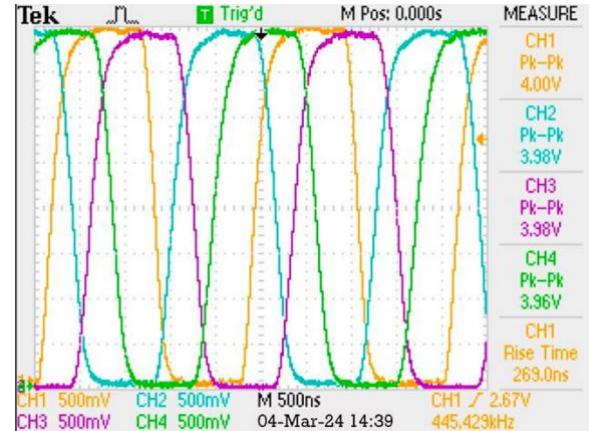


Figure 8.14 The Full Last Half Simulation of 7 Ring Oscillation Circuit for 4V

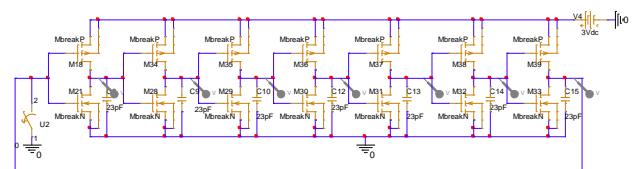


Figure 8.15 Ring Voltage Control Oscillator Circuit with 7 inverters at 3V bias

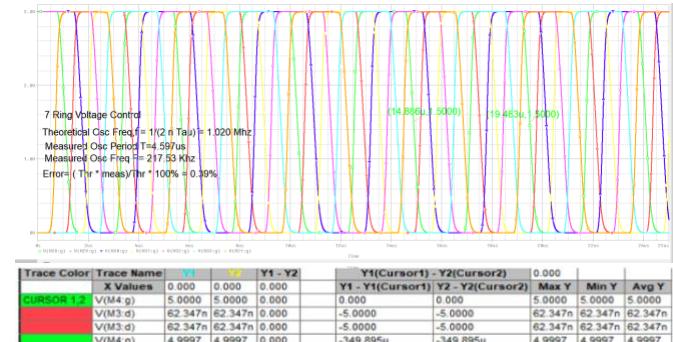


Figure 8.16 I/p – O/p Waveform of the Ring Voltage Control Oscillator circuit with 7 inverters at 3V bias

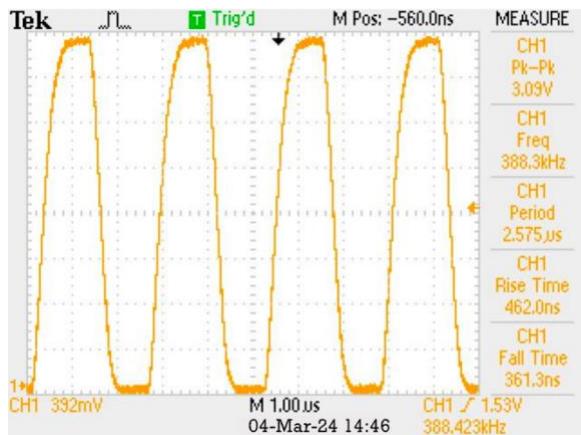


Figure 8.17 Simulation of 7 Ring Oscillation Circuit for 3V

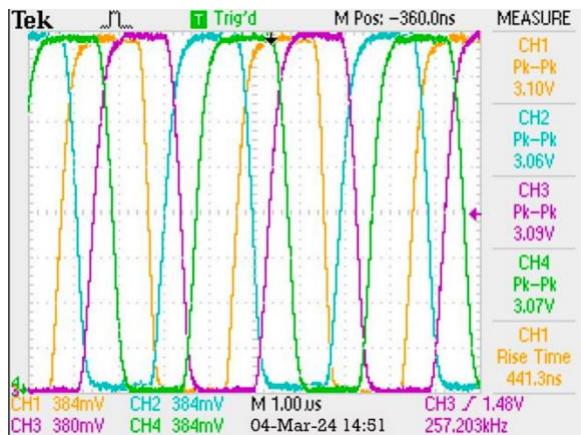


Figure 8.18 The Full First Half Simulation of 7 Ring Oscillation Circuit for 3V

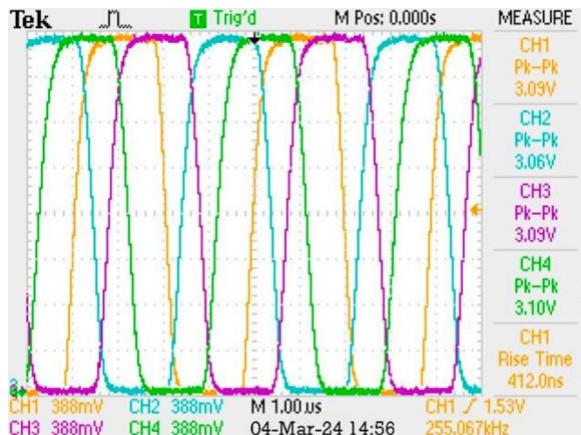


Figure 8.19 The Full Last Half Simulation of 7 Ring Oscillation Circuit for 3V

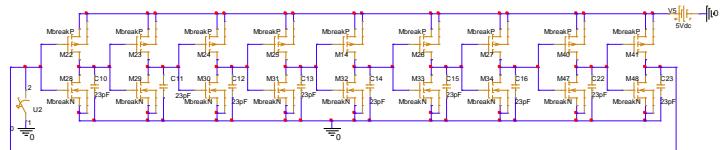


Figure 8.20: Ring Voltage Control Oscillator Circuit with 7 inverters at 2V bias

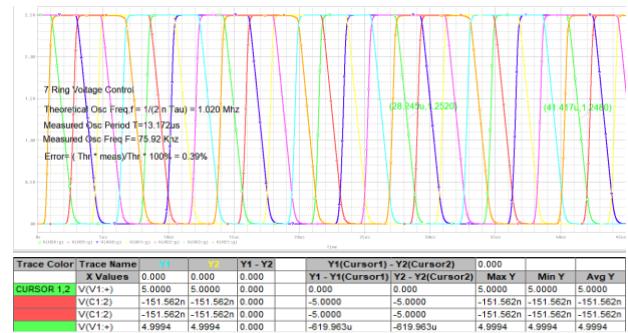


Figure 8.21 I/p – O/p Waveform of the Ring Voltage Control Oscillator circuit with 7 inverters at 2V bias

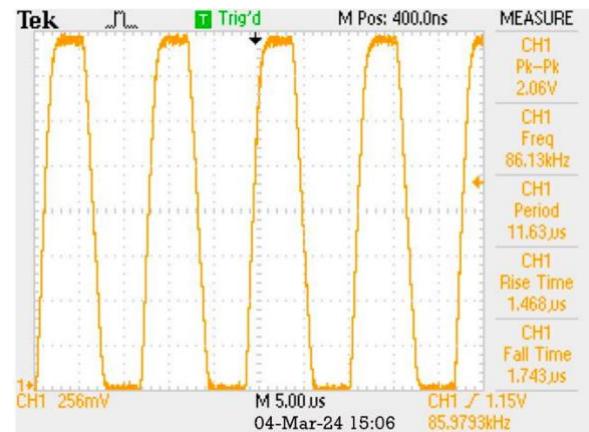


Figure 8.22 Simulation of 7 Ring Oscillation Circuit for 2V

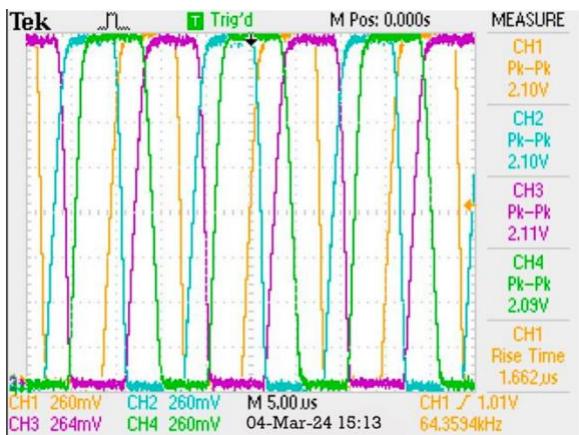


Figure 8.23 The Full First Half Simulation of 7 Ring Oscillation Circuit for 2V

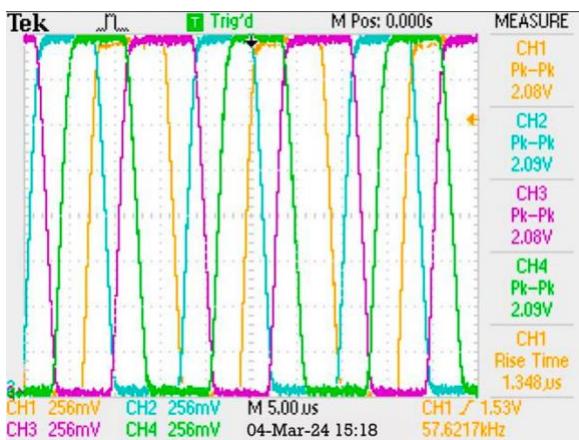


Figure 8.24 The Full Last Half Simulation of 7 Ring Oscillation Circuit for 2V

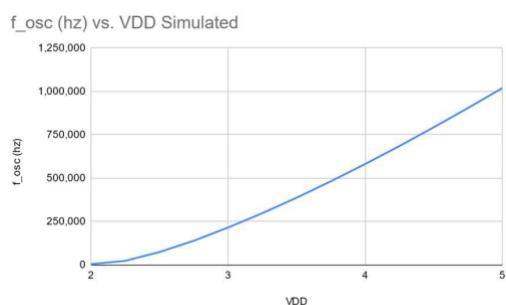


Figure 8.25 Frequency vs VDD plot for 7 ring Voltage Control Oscillator, simulated.

VDD	f_osc (hz)	Period T_osc (sec)
5	1,019,400	0.000009809691976
4.75	904,810	0.00001105204408
4.5	793,520	0.00001260207682
4.25	685,780	0.0000145819359
4	581,940	0.00001718390212
3.75	482,490	0.00002072581815
3.5	387,840	0.00002578382838
3.25	298,630	0.00003348625389
3	215,940	0.00004630915995
2.75	139,660	0.00007160246312
2.5	74,722	0.0001338293943
2.25	23,986	0.0004169098641
2	4,725	0.002116626098

Figure 8.26 Frequency vs VDD table for 7 ring Voltage Control Oscillator, simulated.

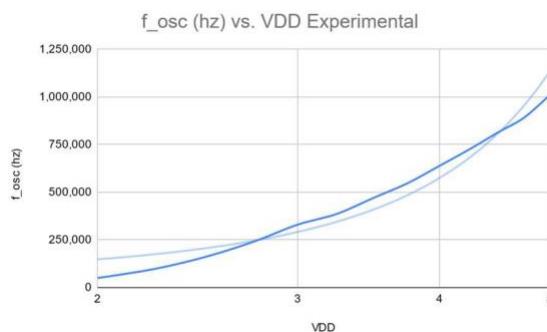


Figure 8.27 Frequency vs VDD plot for 7 ring Voltage Control Oscillator, experimental.

VDD	f_osc (hz)	Period T_osc (sec)
5	1,010,000	0.0000009900990099
4.75	892,500	0.000001120448179
4.5	813,084	0.000001229885227
4.25	725,300	0.000001378739832
4	638,700	0.000001565680288
3.75	547,800	0.000001825483753
3.5	470,800	0.00000212404418
3.25	386,900	0.000002584647196
3	330,000	0.00000303030303
2.75	242,600	0.000004122011542
2.5	164,100	0.000006093845216
2.25	98,720	0.00001012965964
2	50,150	0.00001994017946

Figure 8.28 Frequency vs VDD table for 7 ring Voltage Control Oscillator, experimental.

I.VI. DISCUSSION AND CONCLUSION

In this experiment, we built a CMOS circuit with seven rings that oscillate. This was akin to what we did in Lab 3, except this time we reduced the voltage supply gradually from 5V to 2V in increments of 0.25V. It was crucial to keep the error under 1% for accurate results. Once we collected all the necessary data, we plotted our findings, revealing an exponential increase.

Since this experiment resembled Lab 3, our PSPICE simulation proceeded smoothly, allowing us to simulate the seven-ring CMOS at voltage points ranging from 5V to 2V. Compared to previous labs, this one was particularly smooth because we had already prepared the seven-ring circuit in simulation and physically set it up before the lab session. Additionally, with the assistance of fellow classmates, we managed to complete the lab on schedule and verify our calculations.

I.VII. REFERENCES

- [1] ECE442 Lab Report
- [2] Jaeger, R. C., Blalock, T. N., & Blalock, B. J. (2023). *Microelectronic Circuit Design*. McGraw Hill LLC.
- [3] Supporting Slides on CMOS Transition Theory – Sequare Daniel-Berhe, Ph.D.

CASCODE VOLTAGE SWITCH LOGIC DESIGN, SIMULATION AND EXPERIMENTAL TEST AS WELL AS ANALYSIS

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I.I. ABSTRACT

The Cascade Voltage Switch Logic employs interconnected pull-up PMOS transistors to accelerate transitions between logic levels. This design can be adapted to NOR or NAND gates, accommodating multiple Boolean expressions of varying complexity. In this lab, we'll build and simulate a Cascade Voltage Switch Logic. We'll compare the outputs of our PSPICE design with our circuit design, utilizing a 5V rectangular waveform input and testing across frequencies ranging from 100 kHz to 1.2 MHz.

I.II. KEY WORDS

NMOS, PMOS, CMOS, Load Capacitance, Oscillation, Frequency, and Voltage.

I.III. INTRODUCTION

The Cascade Voltage Switch Logic blends static and dynamic logic to make things faster and use less power. It uses special transistors and clever feedback to switch between voltages quickly without wasting power when idle. This logic is great for handling weak signals in noisy places and can be handy for advanced sensors in noisy areas. For example, it could be used in wireless sensors that monitor volcanic eruptions.

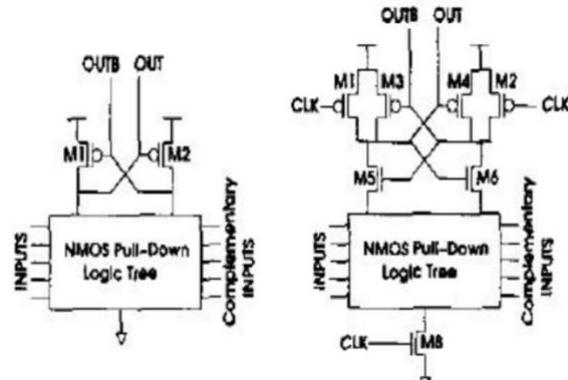


Figure 9.1 Cascode Voltage Switch Logic Schematic

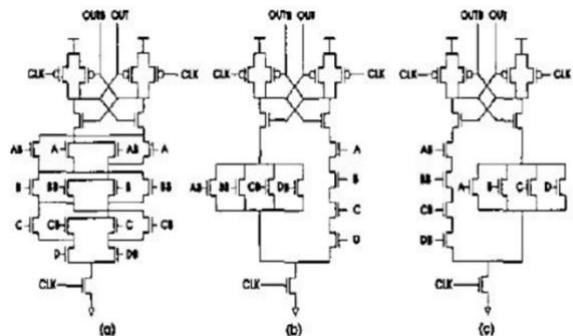


Figure 9.2 Cascode Voltage Switch Logic Circuits

I.IV. EXPERIMENTAL AND SIMULATION SETUPS

The experiment tests the circuit with different frequency ranges. The first set goes from 100kHz to 200kHz, the second from 300kHz to 500kHz, the third from 600kHz to 800kHz,

and the fourth from 900kHz to 1.2MHz. Each time, we use a 5V square wave input.

I.V. EXPERIMENTAL AND SIMULATION DATA AND RESULTS

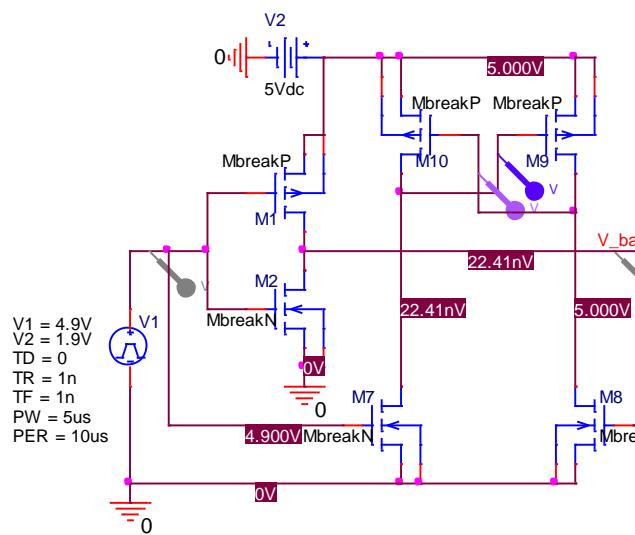


Figure 9.3 Schematic of Cascode Voltage Switch Logic Design Circuit with 1.9V – 4.9V square wave input and $F = 100$ KHz

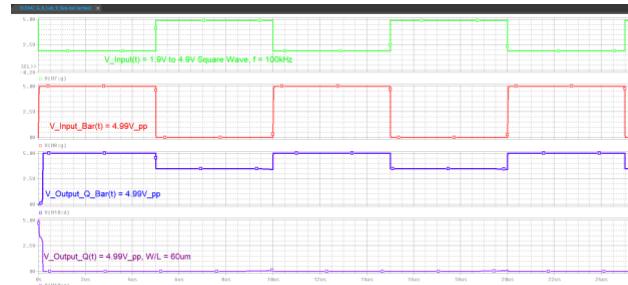


Figure 9.4 I/p – O/p Waveform of the Cascode Voltage Switch Logic Design Circuit with 1.9V – 4.9V square wave input and $F = 100$ KHz Unsized

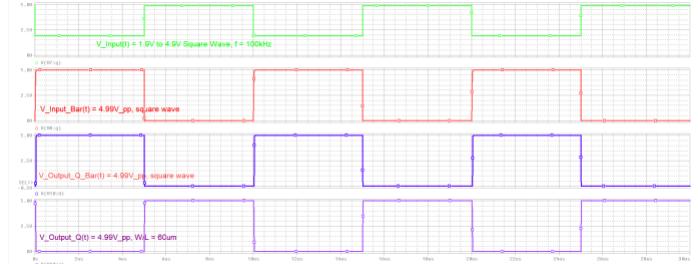


Figure 9.5 I/p – O/p Waveform of the Cascode Voltage Switch Logic Design Circuit with 1.9V – 4.9V square wave input and $F = 100$ KHz Sized

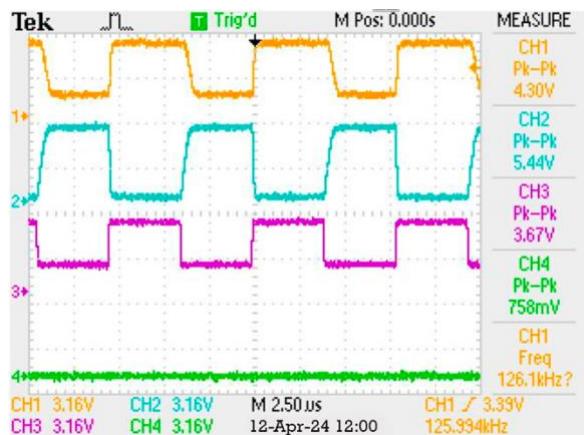


Figure 9.6 Experimental of Cascode Voltage Switch Logic with a Frequency of 126 KHz Unsized

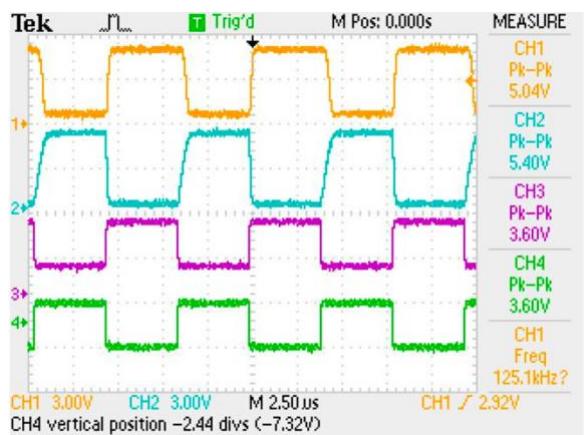


Figure 9.7 Experimental of Cascode Voltage Switch Logic with a Frequency of 126 KHz Sized

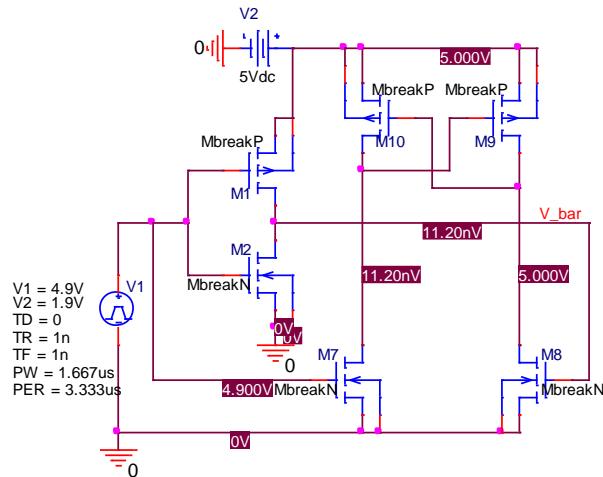


Figure 9.8 Schematic of Cascode Voltage Switch Logic Design Circuit with 1.9V – 4.9V square wave input and $F = 300$ KHz

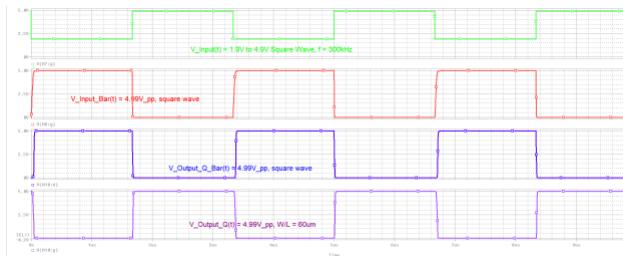


Figure 9.9: I/p – O/p Waveform of the Cascode Voltage Switch Logic Design Circuit with 1.9V – 4.9V square wave input and $F = 300$ KHz Sized

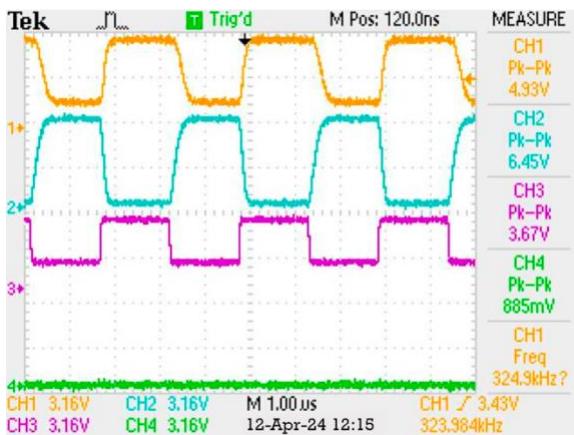


Figure 9.10 Experimental of Cascode Voltage Switch Logic with a Frequency of 324 KHz Unsized

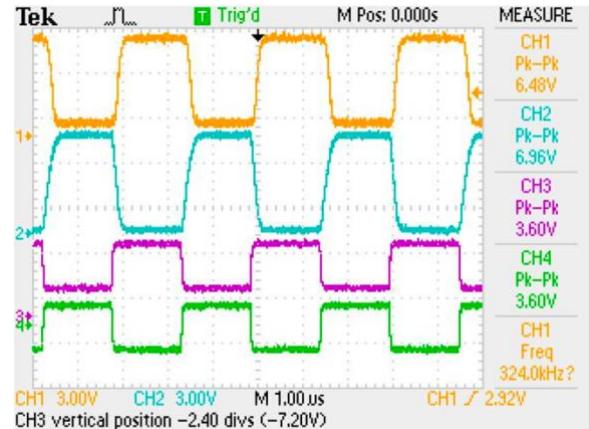


Figure 9.11 Experimental of Cascode Voltage Switch Logic with a Frequency of 324 KHz Sized

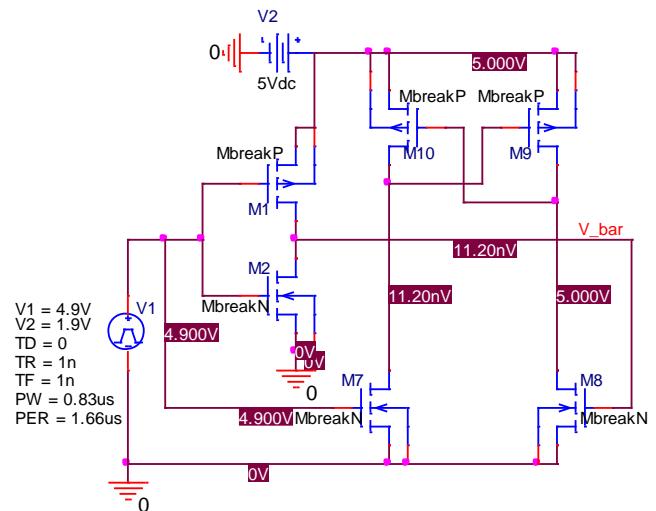


Figure 9.12 Schematic of Cascode Voltage Switch Logic Design Circuit with 1.9V – 4.9V square wave input and $F = 600$ KHz

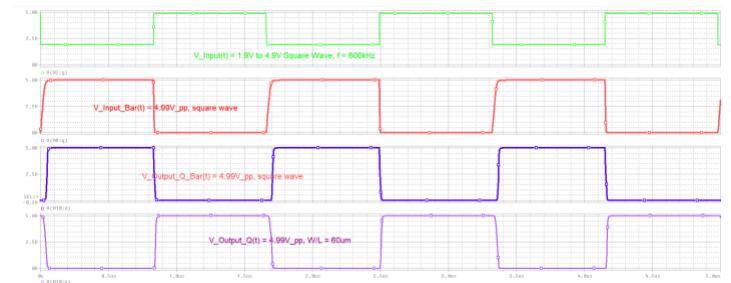


Figure 9.13 I/p – O/p Waveform of the Cascode Voltage Switch Logic Design

Circuit with 1.9V – 4.9V square wave input and F = 600 KHz Sized

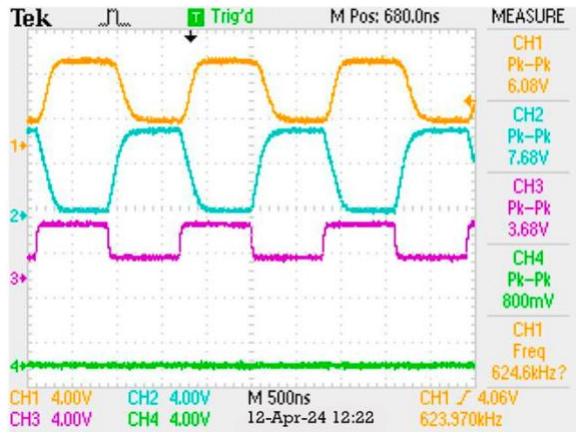


Figure 9.14 Experimental of Cascode Voltage Switch Logic with a Frequency of 624 KHz Unsized

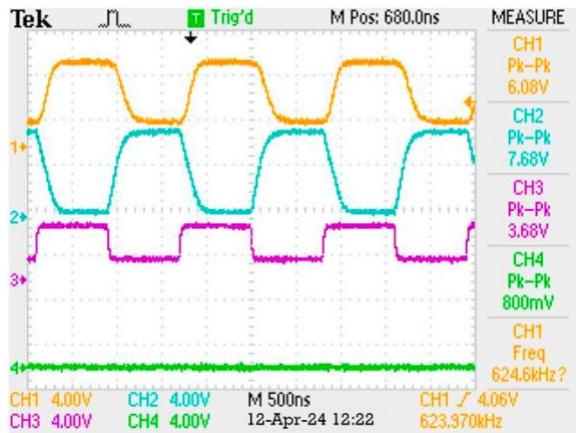


Figure 9.15 Experimental of Cascode Voltage Switch Logic with a Frequency of 624 KHz Sized

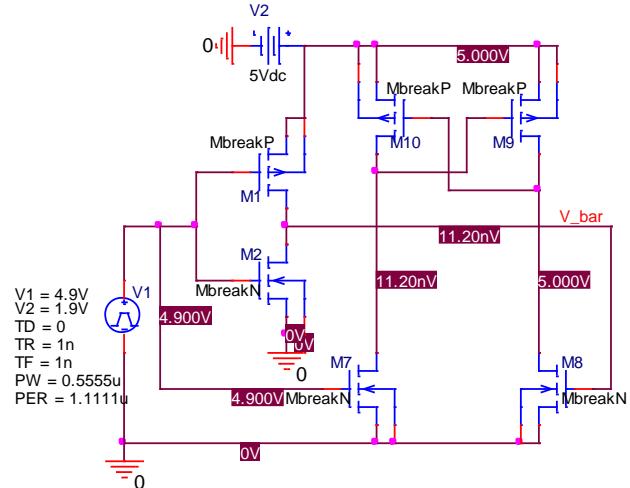


Figure 9.16 Schematic of Cascode Voltage Switch Logic Design Circuit with 1.9V – 4.9V square wave input and F = 900 KHz

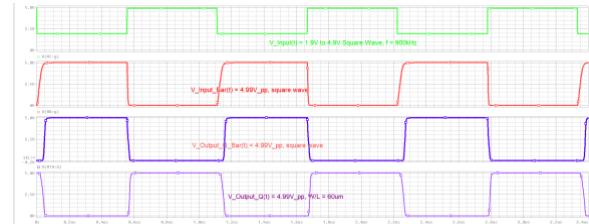


Figure 9.17 I/p – O/p Waveform of the Cascode Voltage Switch Logic Design Circuit with 1.9V – 4.9V square wave input and F = 900 KHz Sized

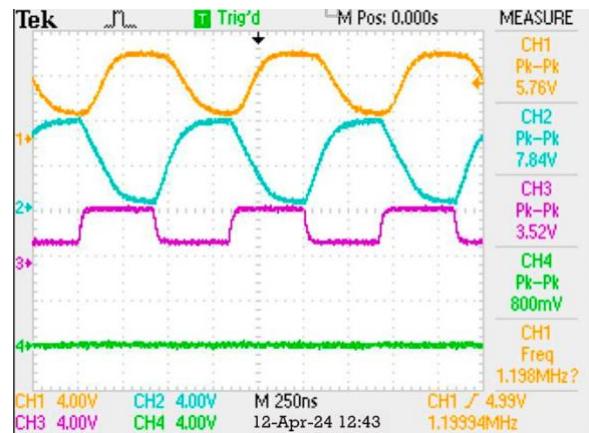


Figure 9.18 Experimental of Cascode Voltage Switch Logic with a Frequency of 1.2 MHz Case 4 Unsized

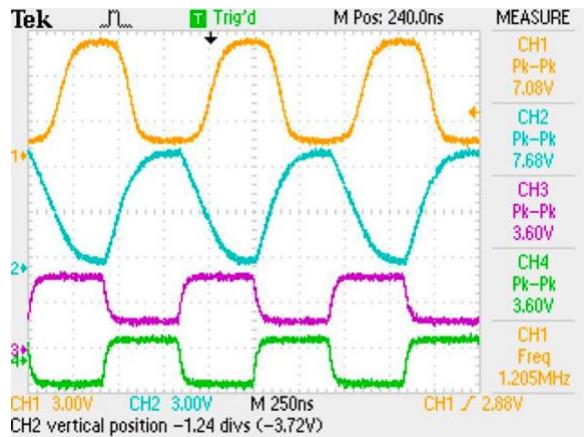


Figure 9.19 Experimental of Cascode Voltage Switch Logic with a Frequency of 1.2 MHz Case 4 Sized

I.VI. DISCUSSION AND CONCLUSION

In this lab, we discovered that the Cascode switch can replace a NAND or NOR gate, offering similar switching behavior or outputs with a much simpler circuit. However, we encountered issues with the PSpice simulation. Despite trying different sizes (2x, 3x, or 4x), we consistently got graphs showing 0V or 5V on outputs 2 and 4. This problem didn't occur in the lab, where we only used 2x sizing as a reference.

I.VII. REFERENCES

- [1] ECE442 Lab Report
- [2] Jaeger, R. C., Blalock, T. N., & Blalock, B. J. (2023). *Microelectronic Circuit Design*. McGraw Hill LLC.
- [3] Supporting Slides on CMOS Transition Theory – Sequare Daniel-Berhe, Ph.D