Repository: https://github.com/Mikey597/VDIC

Test specification:

1. “Sunny day scenario”.
2. Multiply two maximum operands and check result.
3. Multiply two minimum operands and check result.
4. Multiply by zero.
5. Check if results have correct signs.
6. Multiply operands with different size and check result.
7. Wrong parity bit input for first operand and check result.
8. Wrong parity bit input for second operand and check result.
9. Wrong parity bit input for both operands and check result.
10. Check if reset works correctly.
11. Keep req signal always high and check result.
12. Req signal going high for very short moment and check result.
13. Change input data before ack signal output goes high (if possible) and check result.
14. Check if result_parity works correctly.
15. Check different clock frequencies.
16. Check if output flags and result are active for the right amount of time.
17. Check if result is set to 0 when parity error occurs.