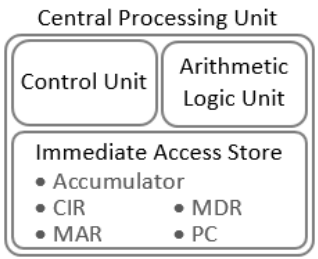
CPU and von Neumann Architecture

A	CPU structure		
Control Unit		CU	Communicates with the ALU, immediate access store and main memory to perform the functions of the CPU.
Immediate access store			A collection of registers with specific roles in the CPU
1	**Accumulator**		Stores data to be operated on, or the result of any operation carried out by the ALU
2	**Current Instruction Register**	CIR	Stores the instruction to be used next
3	**Memory Address Register**	MAR	Stores the address to be used next (all stages)
4	**Memory Data (or Buffer) Register**	MDR MBR	Stores data which has been retrieved from or is about to be sent to RAM
5	**Program Counter**	PC	Stores the next address in the program (Fetch stage)
Arithmetic and Logic Unit		ALU	Takes two operands from the Accumulator and an operator from the CIR and returns a single result to the Accumulator



D	CPU vocab
Boot Process	Set of instructions required to make the computer start
Clock speed	The frequency which the CPU runs at, and the number of instructions which can be processed per second (Hz)
Overclock	Run the CPU at a higher clock speed than its default

B	Key vocab
Systems Architecture	The way the components of a computer are arranged.
von Neumann architecture	System architecture where the data is stored in the same place as the instructions
Fetch-Decode-Execute cycle	The cycle followed by the von Neumann architecture

C	CPU hardware
Bus	A connector which transfers data between components. Three types are data, address and control
Cache	Fast, expensive memory which is loaded from RAM and called by the CPU
Clock generator	A circuit which produces a square wave, which is the maximum frequency a CPU can perform instructions
Core	A processing unit which can run simultaneously with others. It will have its own L1 and L2 cache, but share L3 cache and RAM
Single-core	Only one core
Dual-core	Two cores
Quad-core	Four cores
Multi-core	More than one core
Register	A section of high speed memory