CPU and von Neumann Architecture

	Α	CPU structure						В	Key vocab			
Control Unit		CU	Con	Communicates with the ALU, immediate			Systems		1	The way the components of a		
				acce	access store and main memory to perform			Architecture		e 0	computer are arranged.	
				the	the functions of the CPU.			von Neuma		nn S	System architecture where the data	
Immediate access				A collec		tion of registers with specific roles	а	architecture		e i	s stored in the same place as the	
store				in th	in the CPU					i	nstructions	
1	1 Accumulator			Stor	Stores data to be operated on, or the result			Fetch-Deco		de- T	The cycle followed by the von	
				of a	of any operation carried out by the ALU					le N	Neumann architecture	
2		ent Instruction		Stor	Stores the instruction to be used next			С		CPU hardware		
2	Register 3 Memory Address		MAR	Cto	Stores the address to be used next (all stages)			Bus		A conn	ector which transfers data	
3			IVIAN							betwe	en components. Three types are	
4	Register		MDE							data, address and control		
4	1 111011101 / 2 4144 (01		MDF MBR	0.0.	Stores data which has been retrieved from			Cache		Fast, expensive memory which is loaded		
_	_	er) Register		OF IS	or is about to be sent to RAM					from RAM and called by the CPU		
5	5 Program Counter		PC		Stores the next address in the program			Clock		A circu	it which produces a square wave,	
•	A .** th				(Fetch stage)			genera	or	which	is the maximum frequency a CPU	
Arithmetic and			ALU			s two operands from the Accumulator			(can pe	rform instructions	
Logic Unit					and an operator from the CIR and returns a single result to the Accumulator			Core		A proc	essing unit which can run	
									:	simulta	aneously with others. It will have	
	Central Processing Uni			D		CPU vocab Set of instructions required to make			l	its owr	n L1 and L2 cache, but share L3	
Control Unit Arithmet Logic Un Immediate Access Stor			tic]	Boot			:		(cache	and RAM	
			it	Process		the computer start		Single		re	Only one core	
			<u></u>	Clock		The frequency which the CPU runs at, and the number of instructions which		Dual-co Quad-co		е	Two cores	
- 11	Accumulator			speed						re	Four cores	
	• CIR • MDR					an be processed per second (Hz)		Multi	-cor	re	More than one core	
• MAR • PC				Over	Overclock Run the CPU at a higher clock speed than its default		R	Register A		A sectio	n of high speed memory	
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