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NTE2114
Integrated Circuit
MOS, Static 4K RAM, 300ns

Description:

The NTE2114 1024–word 4–bit static random access memory is fabricated using N–channel silicon–gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The separate chip select input ($\overline{CS}$) allows easy memory expansion by OR–tying individual devices to a data bus.

Features

- All Inputs and Outputs Directly TTL Compatible
- Static Operation: No Clocks or Refreshing Required
- Low Power: 225mW Typ
- High Speed: Down to 300ns Access Time
- TRI–STATE Output for Bus interface
- Common Data In and Data Out Pins
- Single 5V Supply
- Standard 18–Lead DIP Package

Absolute Maximum Ratings:

Voltage at Any Pin . . . . . –0.5V to +7V
Power Dissipation, P_D 1W
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +300°C

Recommended Operating Conditions:

Parameter	Symbol	Test Conditions	Min	Max	Units
Supply Voltage	V_{CC}		4.75	5.25	V
Ambient temperature	T_A		0	+70	°C

DC Electrical Characteristics: (T_A = 0° to +70°, V_{CC} = 5V ±5% unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Units
Logical “1” Input Voltage	V_{IH}		2.0	V_{CC}	V
Logical “0” Input Voltage	V_{IL}		–0.5	0.8	V
Logical “1” Output Voltage	V_{OH}	I_{OH} = –1.0mA	2.4	–	V
Logical “0” Output Voltage	V_{OL}	I_{OL} = 2.1mA	–	0.4	V
Input Load Current	I_{LI}	V_{IN} = 0 to 5.25V	–10	10	µA
Output Leakage Current	I_{LO}	V_O = 4V to 0.4V, $\overline{CS}$ = V_{IH}	–10	10	µA
Power Supply Current	I_{CC1}	All Inputs = 5.25V, T_A = 25°C	–	95	mA
Power Supply Current	I_{CC2}	All Inputs = 5.25V, T_A = 0°C	–	100	mA

AC Electrical Characteristics: (T_A = 0°C to +70°C, V_{CC} = 5V ±5%, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Units
READ CYCLE					
Read Cycle Time ($\overline{WE}$ = V_{IH})	t_{RC}		300	–	ns
Access Time	t_A		–	300	ns
Chip Select to Output Valid	t_{CO}		–	100	ns
Chip Select to Output Active	t_{CX}		20	–	ns
Chip Select to Output TRI–STATE	t_{COT}		0	80	ns
Output Hold from Address Change	t_{OHA}		10	–	ns
WRITE CYCLE					
Write Cycle Time	t_{WC}		300	–	ns
Write Pulse Width	t_{WP}		150	–	ns
Write Recovery Time	t_{WR}		0	–	ns
Data Set–Up Time	t_{DS}		150	–	ns
Data Hold Time	t_{DH}		0	–	ns
Write Enable to Output TRI–STATE	t_{WOT}		0	80	ns
Write Enable to Output Valid	t_{WO}		–	100	ns

Capacitance: (T_A = +25°C, f = 1 MH_Z, Note 3 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Units
Input Capacitance	C_{IN}	All Inputs V_{IN} = 0V	–	5	pF
Output Capacitance	C_{OUT}	V_O = 0V	–	10	pF

Note 1: Typical values at T_A = +25°C.

Note 2: All input transitions ≤ 10ns.Timing referenced to $V_{IL(MAX)}$ or $V_{IH(MIN)}$ for inputs, 0.8V and 2V for output. For test purposes, input levels should swing between 0V and 3V. Output load = 1 TTL gate and C_L = 100 pF.

Note 3: This parameter is guaranteed by periodic testing.

Truth Table:

$\overline{CS}$	$\overline{WE}$	I/O	MODE
H	X	Hi–Z	Not Selected
L	L	H	Write 1
L	L	L	Write 0
L	H	D_{OUT}	Read

Functional Description:

Two pins control the operation of the NTE2114. Chip Select ($\overline{CS}$) enables write and read operations and controls TRI–STATING of the data–output buffer. Write Enable ($\overline{WE}$) chooses between READ and WRITE modes and also controls output TRI–STATING. The truth table details the states produced by combinations of the $\overline{CS}$ and $\overline{WE}$ controls.

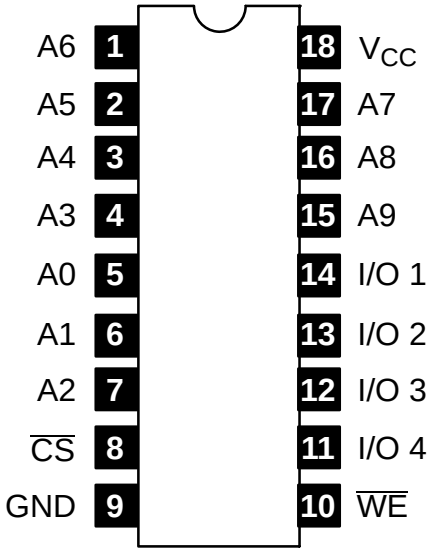
During READ–cycle timing, $\overline{WE}$ is kept high. Independent of $\overline{CS}$, any change in address code causes new data to be fetched and brought to the output buffer. $\overline{CS}$ must be low, however, for the output buffer to be enabled and transfer the data to the output pin.

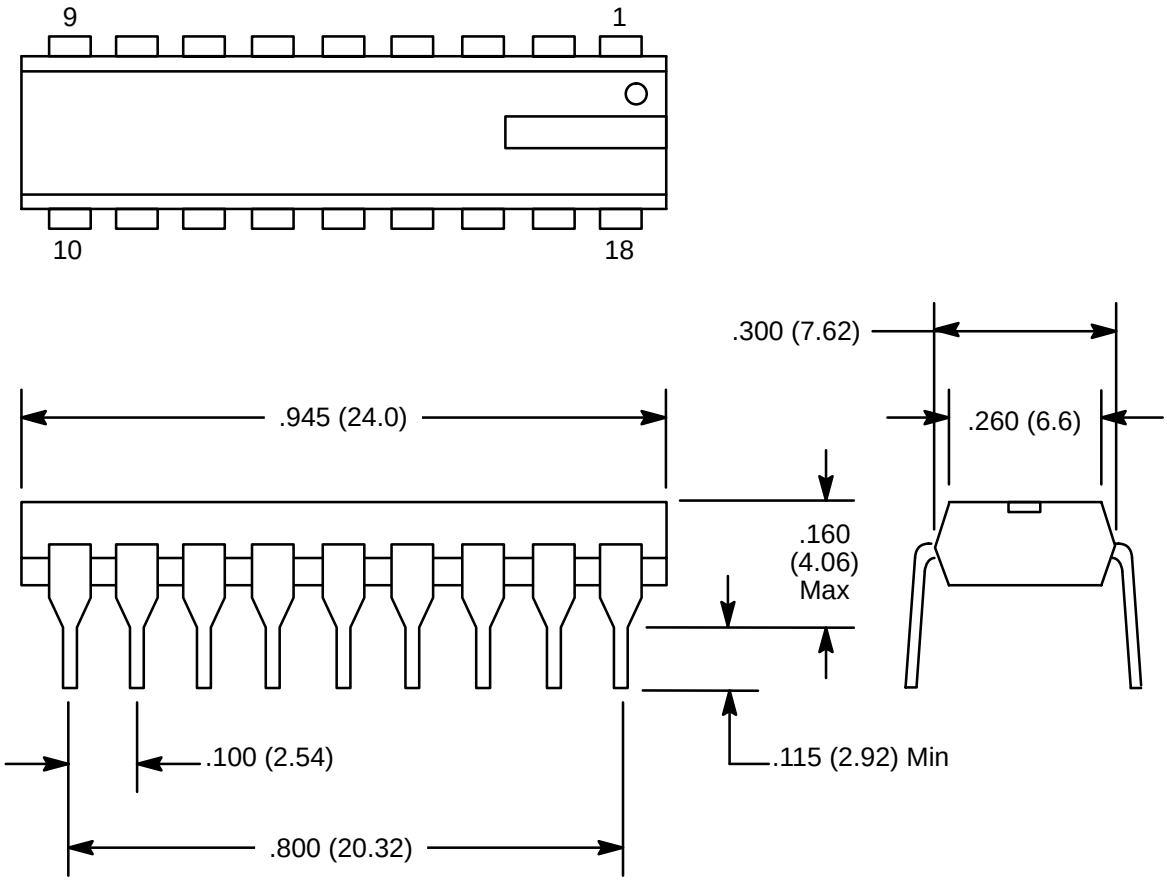
Address access time, t_A, is the time required for an address change to produce new data at the output pin, assuming $\overline{CS}$ has enabled the output buffer prior to data arrival. Chip Select–to–output delay, t_{CO}, is the time required for $\overline{CS}$ to enable the output buffer and transfer previously fetched data to the output–pin. Operation with $\overline{CS}$ continuously held low is permissible.

Writing occurs only during the time both $\overline{CS}$ and $\overline{WE}$ are low. Minimum write pulse width, t_{WP}, refers to this simultaneous low region. Data set–up and hold times are measured with respect to whichever control first rises. Successive write operations may be performed with $\overline{CS}$ continuously held low. $\overline{WE}$ then is used to terminate WRITE between address changes. Alternatively, $\overline{WE}$ may be held low for successive WRITES and $\overline{CS}$ used for WRITE interruption between address change.

In any event, either $\overline{WE}$ or $\overline{CS}$ (or both) must be high during address transitions to prevent erroneous WRITE.

Pin Connection Diagram




9
1
10
18
.300 (7.62)
.945 (24.0)
.260 (6.6)
.160
(4.06)
Max
.100 (2.54)
.115 (2.92) Min
.800 (20.32)