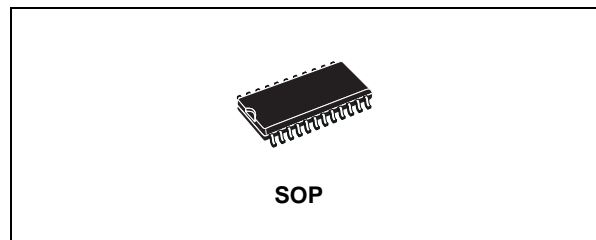# HCF40181B

4-BIT ARITHMETIC LOGIC UNIT

- FULL LOOK-AHEAD CARRY FOR SPEED OPERATIONS ON LONG WORDS
- GENERATES 16 LOGIC FUNCTIONS OF TWO BOOLEAN VARIABLES
- GENERATES 16 ARITHMETIC FUNCTIONS OF TWO 4-BIT BINARY WORDS
- A = B COMPARATOR OUTPUT AVAILABLE
- RIPPLE-CARRY INPUT AND OUTPUT AVAILABLE
- TYPICAL ADDITION TIME 200ns AT V_{DD} = 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIF. UP TO 20V
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

DESCRIPTION

HCF40181B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in SOP packages.

HCF40181B is a low-power 4-bit parallel arithmetic logic unit (ALU) capable of providing 16 binary arithmetic operations on two 4-bit words
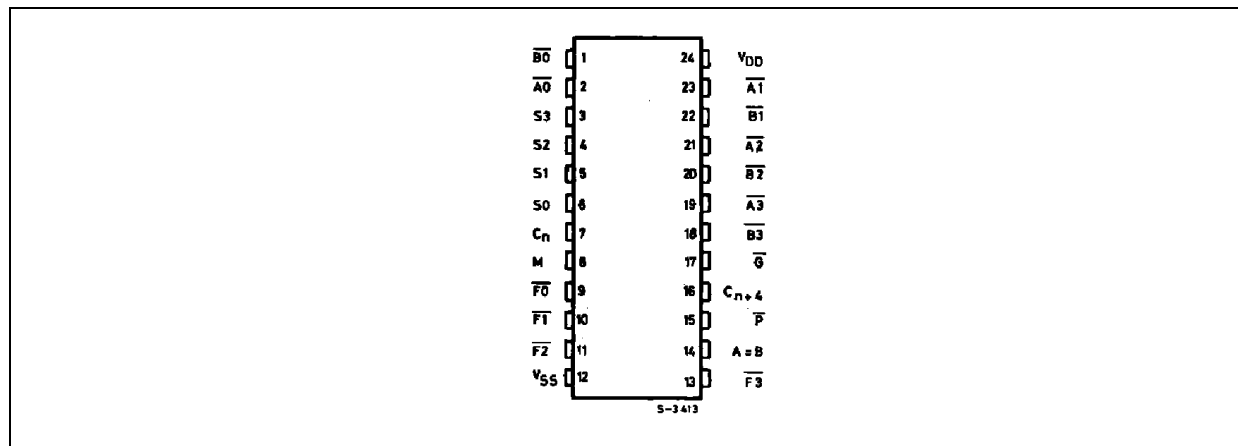
SOP

ORDER CODES

PACKAGE	TUBE	T & R
SOP	HCF40181BM1	HCF40181M013TR

and 16 logical functions of two Boolean variables. The mode control input M selects logical (M = High) or arithmetic (M = Low) operations. The four select inputs (S0, S1, S2, and S3) select the desired logical or arithmetic functions, which include AND, OR, NAND, NOR, and exclusive-OR and NOR in the logical mode, and addition, subtraction, decrement, left-shift and straight transfer in the arithmetic mode, according to the truth table. HCF40181B operations may be interpreted with either active-low or active-high data at the A and B word inputs and the function outputs F, by using the appropriate truth table. HCF40181B contains logic for full look-ahead carry operations for fast carry generations using the carry-generate and carry propagate outputs $\overline{G}$

PIN CONNECTION

| Pin		Pin	
$\overline{B0}$	1	24	V_{DD}
$\overline{A0}$	2	23	$\overline{A1}$
S3	3	22	$\overline{B1}$
S2	4	21	$\overline{A2}$
S1	5	20	$\overline{B2}$
S0	6	19	$\overline{A3}$
C_n	7	18	$\overline{B3}$
M	8	17	$\overline{G}$
$\overline{F0}$	9	16	C_{n+4}
$\overline{F1}$	10	15	$\overline{P}$
$\overline{F2}$	11	14	A = B
V_{SS}	12	13	$\overline{F3}$

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and $\overline{P}$ for the four bits of HCF40181B. Use of the HCF40182B look-ahead carry generator in conjunction with multiple HCF40181Bs permits high-speed arithmetic operations on long words. A ripple carry output C_{n+4} is available for use in systems where speed is not of primary importance. Also included in HCF40181B is a comparator output A = B, which assumes a high level whenever the two four-bit input words A and B are equal and the device is in subtract mode. In addition, relative magnitude information may be derived from the carry-in input C_n and ripple carry-out output C_{n+4} by placing the unit in the subtract mode and externally decoding using the information in table II. HCF40181B is similar to industry types MC14581 and 74181.

INPUT EQUIVALENT CIRCUIT

CS03790
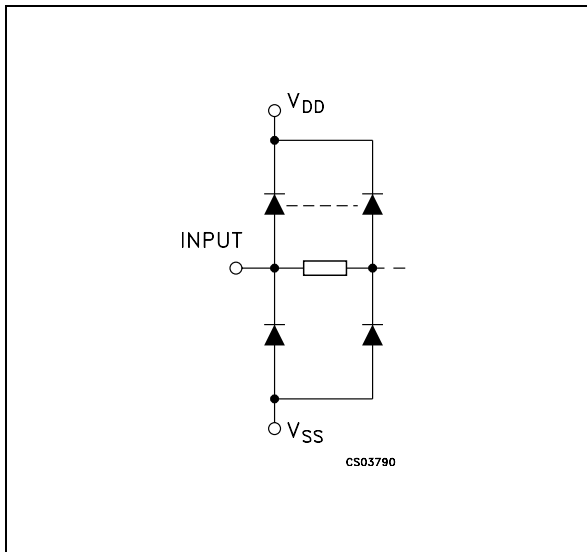
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 22, 20, 18	$\overline{B0}$ to $\overline{B3}$	Word $\overline{B}$
2, 23, 21, 19	$\overline{A0}$ to $\overline{A3}$	Word $\overline{A}$
6, 5, 4, 3	S0 to S3	Function Select Inputs
9, 10, 11, 13	$\overline{F0}$ to $\overline{F3}$	Output Function
7	Cn	Carry Input
8	M	Mode Control
14	A = B	Compare Output
15	$\overline{P}$	Look Ahead Carry Outputs
16	Cn+4	Ripple Carry Output
17	$\overline{G}$	Look Ahead Carry Outputs
12	V_{SS}	Negative Supply Voltage
24	V_{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM
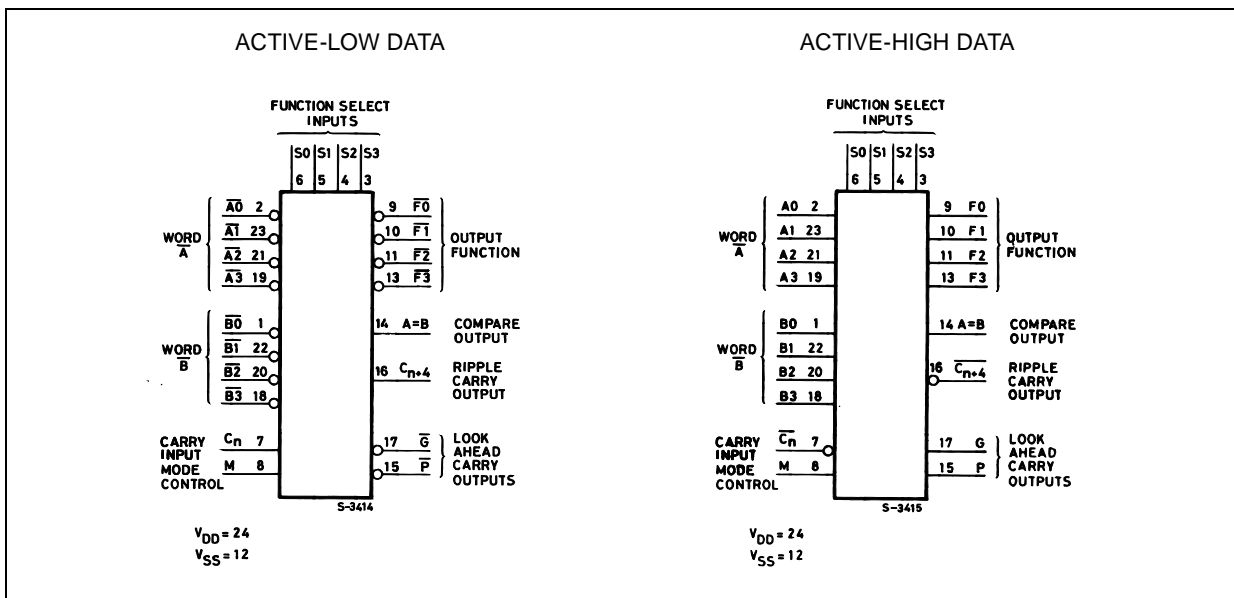
LOGIC DIAGRAM (ACTIVE-LOW DATA)

*ALL INPUTS PROTECTED
BY COS/MOS PROTECTION
NETWORK

S-3415
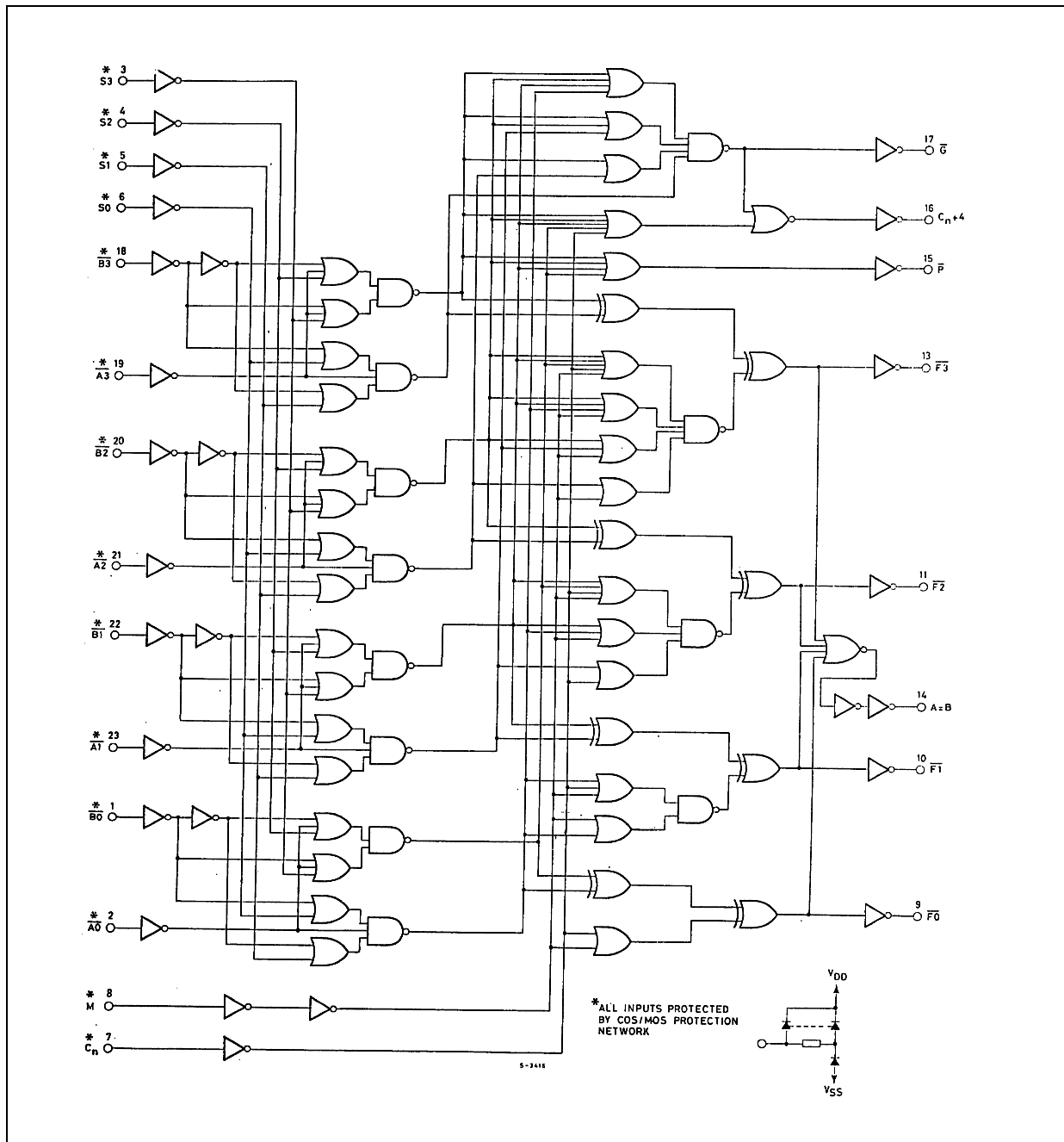
TRUTH TABLE 1

FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE LOW		INPUTS/OUTPUTS ACTIVE HIGH	
S3	S1	S2	S0	Logic Function (M = H)	Arithmetic* Function (M = L, Cn = L)	Logic Function (M = H)	Arithmetic* Function (M = L, $\overline{Cn}$ = H)
L	L	L	L	$\overline{A}$	A minus 1	A	A
L	L	L	H	$\overline{AB}$	AB minus 1	A + B	A + B
L	L	H	L	$\overline{A}$ + B	$A\overline{B}$ minus 1	$A\overline{B}$	A + $\overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A + B}$	A plus (A + $\overline{B}$)	$\overline{A}B$	A plus AB
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)	$\overline{B}$	(A + B) plus AB
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	A ⊕ B	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H	L	L	L	$\overline{AB}$	A plus (A + B)	$\overline{A}$ + B	A plus AB
H	L	L	H	A ⊕ B	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)	B	(A + $\overline{B}$) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A	Logic 1	A plus A
H	H	L	H	$A\overline{B}$	AB plus A	A + $\overline{B}$	(A + $\overline{B}$) plus A
H	H	H	L	AB	AB plus A	A + B	(A + B) plus A
H	H	H	H	A	A	A	A minus 1

● : Expressed as two's complement. For arithmetic function with Cn in the opposite state, the resulting function is as show plus 1.

TRUTH TABLE 2: MAGNITUDE COMPARISON

ACTIVE-HIGH DATA			ACTIVE-LOW DATA		
INPUT C_n	OUTPUT C_{n+4}	MAGNITUDE	INPUT C_n	OUTPUT C_{n+4}	MAGNITUDE
H	H	A ≤ B	L	L	A ≤ B
L	H	A < B	H	L	A < B
H	L	A > B	L	H	A > B
L	L	A ≥ B	H	H	A ≥ B

TRUTH TABLE 3: AC TEST SETUP REFERENCE (ACTIVE-LOW DATA)

TEST DELAY TIMES	AC PATHS		DC DATA INPUTS		MODE*
	INPUTS	OUTPUTS	TO V_{SS}	TO V_{DD}	
SUM_{IN} to SUM_{OUT}	$\overline{B0}$	Any $\overline{F}$	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$, M, C_n	All $\overline{A}$'s	ADD
SUM_{IN} to P	$\overline{A0}$	$\overline{P}$	$\overline{A1}$, $\overline{A2}$, $\overline{A3}$, M, C_n	All $\overline{B}$'s	ADD
SUM_{IN} to G	$\overline{B0}$	$\overline{G}$	All $\overline{A}$'s, M, C_n	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	ADD
SUM_{IN} to C_{n+4}	$\overline{B0}$	C_{n+4}	All $\overline{A}$'s, M, C_n	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	ADD
C_n to SUM_{OUT}	C_n	Any $\overline{F}$	All $\overline{A}$'s, M	All $\overline{B}$'s	ADD
C_n to C_{n+4}	C_n	C_{n+4}	All $\overline{A}$'s, M	All $\overline{B}$'s	ADD
SUM_{IN} to A = B	$\overline{B0}$	A = B	All A's, B1, B2, B3, M	C_n	SUBTRACT
SUM_{IN} to SUM_{OUT} (logic mode)	All $\overline{B}$,s	Any $\overline{F}$	All $\overline{A}$'s, C_n	M	EXCLUSIVE OR

● ADD Mode: S0, S3 = V_{DD}; S1, S2 = V_{SS}. SUBTRACT Mode: S0, S3 = V_{SS}; S1, S2 = V_{DD}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	$\pm$ 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$|I_{OI}|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm10^{-5}$	±0.1		±1		±1	μA
I_{OZ}	3-State Output Leakage Current	0/18	Any Input		18		$\pm10^{-4}$	±0.4		±12		±12	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

## DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PHL} t_{PLH}	Propagation Delay Time A or B to F (logic mode) A or B to G or P	5			400	800	ns
		10			160	320	
		15			120	240	
	A or B to F, C_{n+4}, or A = B	5			500	1000	ns
		10			200	400	
		15			140	280	
	C_n to F	5			320	640	ns
		10			135	270	
		15			100	200	
	C_n to C_{n+4}	5			200	400	ns
		10			100	200	
		15			70	140	
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C

(1) : If more than one unit is cascaded. tr should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TEST CIRCUIT
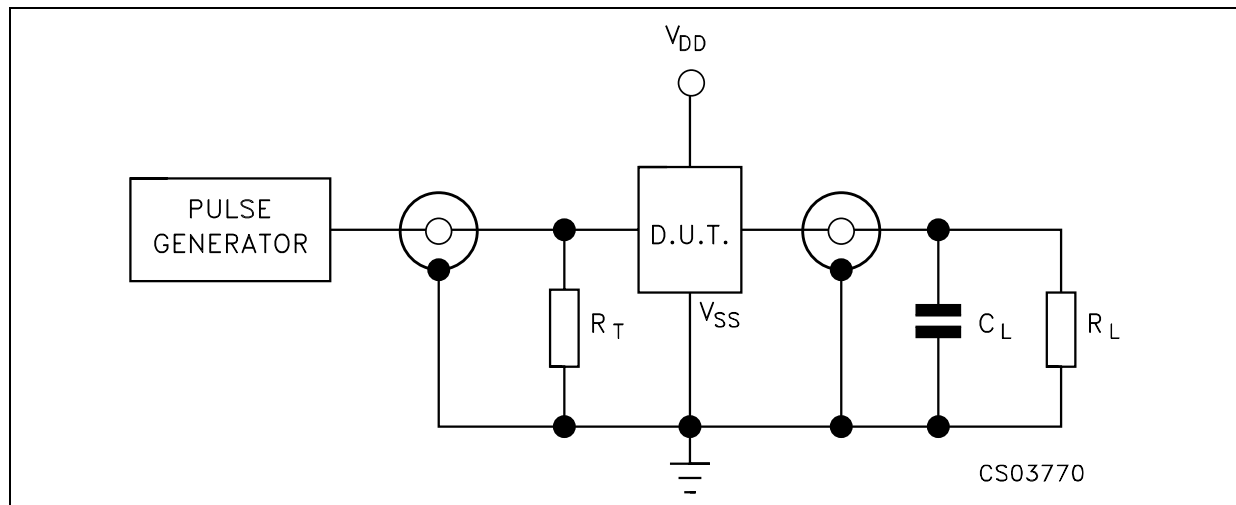
C_L = 50pF or equivalent (includes jig and probe capacitance)

R_L = 200KΩ

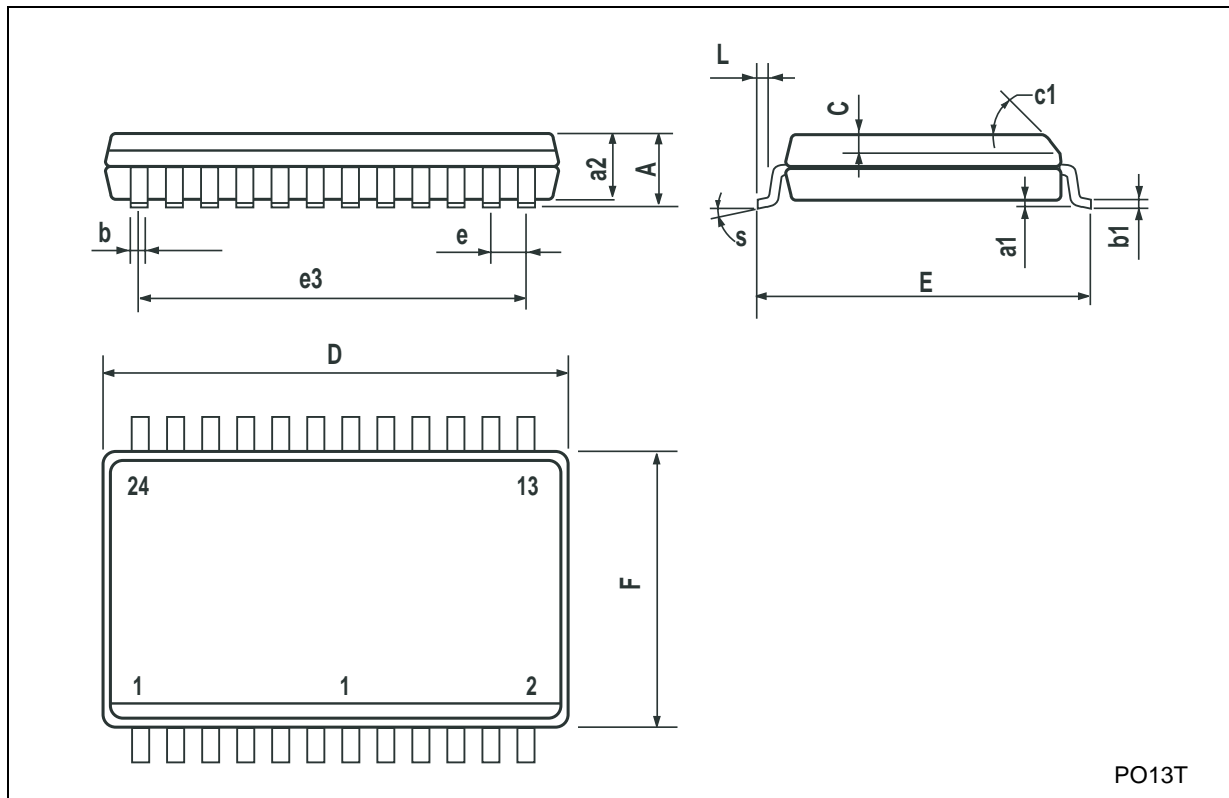R_T : Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM : PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)

S-10041
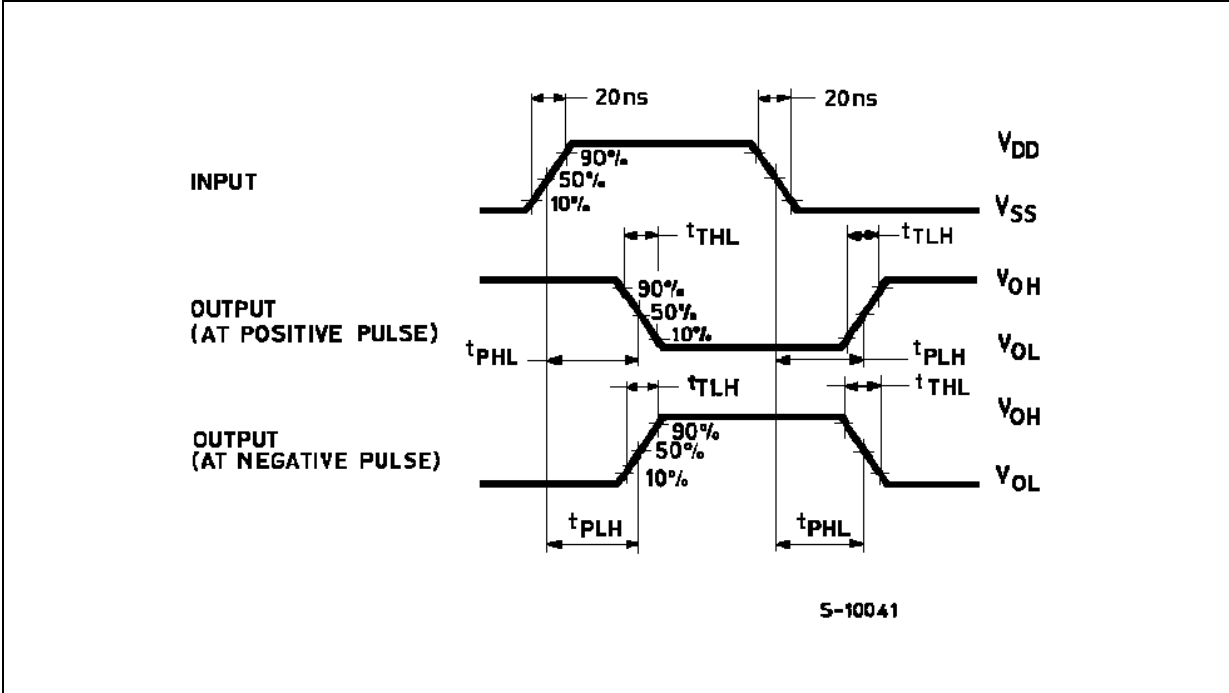
SO-24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	8° (max.)					

PO13T