**Problem Description:** Given a 32-bit binary number b31b30b29......b2b1b0 that represents a MIPS instruction, identify the following fields from it. a. The format of the instruction (e.g., R-Format/I-Format/J-Format) b. Operation (e.g., add, sub, and, or, etc.)

c. The Source register number/s (in decimal, separated by comma if two operands exist)

d. The destination register number (in decimal)

e. Shift amount (in decimal)

If a field does not exist for a given input, print "none" for that field. You may only consider the add, addi, sub, and, or, slt, lw, sw, #### and beq instructions of the MIPS architecture. You must show your outputs for the following test cases. You will not get any

f. Constant/Offset (in decimal)

points even if you miss a single test case. Test cases (inputs):

0000010001100100100000000100000 00100010001010000000000000000101

00000010010100111000100000100010

10001110010100010000000001100100

0000001010010111001000000100101 0000001001010101001100000100100

0000001010010110100100000101010 10101110001100110000000001100100

00010010001100100000000001100100

In [126... # putting the input in list inputList = ['0000001000110010010000000100000' '001000100010100000000000000000101',

'00000010010100111000100000100010', '10001110010100010000000001100100'

'10101110001100110000000001100100', '00010010001100100000000001100100'] Various R-Format instructions:

Mnemonic

add

and

slt

sll

sltu

addu

'00000001010010111001000000100101', '00000001001010101001100000100100', '00000001010010110100100000101010',

Add

Add unsigned

Set on less than

Shift left logical

Bitwise and

Bitwise nor nor Bitwise or or

		2		
	srl	Shift right logical	0	2
	sra	Shift right arithmetic	0	3
	sub	Subtract	0	34
	subu	Subtract unsigned	0	35
<pre>In [128  def r_type_func(entry):     if (int(entry[-6:], 2)) == 32:         print('Operation: addu')     elif (int(entry[-6:], 2)) == 33:         print('Operation: addu')     elif (int(entry[-6:], 2)) == 36:         print('Operation: and')     elif (int(entry[-6:], 2)) == 39:         print('Operation: nor')     elif (int(entry[-6:], 2)) == 37:         print('Operation: or')     elif (int(entry[-6:], 2)) == 42:         print('Operation: slt')     elif (int(entry[-6:], 2)) == 43:         print('Operation: sltu')     elif (int(entry[-6:], 2)) == 0:         print('Operation: sltu')     elif (int(entry[-6:], 2)) == 0:         print('Operation: sll')     elif (int(entry[-6:], 2)) == 3:         print('Operation: srl')     elif (int(entry[-6:], 2)) == 34:         print('Operation: srl')     elif (int(entry[-6:], 2)) == 35:         print('Operation: subu')     elif (int(entry[-6:], 2)) == 35:         print('Operation: subu') </pre>				

Meaning

Set on less than immediate unsigned

Meaning

Set on less than unsigned

Opcode

0

0

0

0

0

0

0

0

Funct

32

33

36

39

37

42

43

Opcode

4

5

15

35

13

10

11

43

0

print('Operation: addiu') elif (int(entry[0:6], 2)) == 12: print('Operation: andi') elif (int(entry[0:6], 2)) == 4: print('Operation: beq') **elif** (int(entry[0:6], 2)) == 5: print('Operation: bne') elif (int(entry[0:6], 2)) == 15: print('Operation: lui') elif (int(entry[0:6], 2)) == 35: print('Operation: lw') elif (int(entry[0:6], 2)) == 13: print('Operation: ori') **elif** (int(entry[0:6], 2)) == 10: print('Operation: slti') elif (int(entry[0:6], 2)) == 11: print('Operation: sltiu') elif (int(entry[0:6], 2)) == 43: print('Operation: sw')

For R-Type Operations:

Recall

op

6 bits

operation

Various I-Format instructions:

Add immediate

Branch if equal

Load word

Store word

Add immediate unsigned

Bitwise and immediate

Branch if not equal

Load upper immediate

Bitwise or immediate

Set on less than immediate

R-type format

rd

5 bits

- shamt is "shift amount" and is only used for shift instructions

rd

5 bits

op is an operation code or opcode that selects a specific

rs and rt are the first and second source registers

func is used together with op to select an arithmetic

00010

rt

5 bits

shamt

5 bits

00100 00000

shamt

5 bits

func

6 bits

10 0000

func

6 bits

2

rt

5 bits

rs

5 bits

rd is the destination register

rs

5 bits

Mnemonic

addi

addiu

andi

beq

bne

lui

lw

ori

SW

In [129.

slti

sltiu

def i\_type\_func(entry):

if (int(entry[0:6], 2)) == 8: print('Operation: addi') **elif** (int(entry[0:6], 2)) == 9:

## • For example: add \$4, \$3, \$2

op

6 bits

Functions for R-Type Operations:

For I-Type Operations:

000100

op

6 bits

def i\_source\_reg(entry):

op

6 bits

In [130..

In [131..

In [132...

instruction

000000 00011

## def r\_source\_reg(entry): print(f"Source Registers: {int(entry[6:11], 2)}, {int(entry[11:16], 2)}") def r\_destination\_reg(entry): print(f"Destination Register: {int(entry[16:21], 2)}") def r\_shamt(entry): print(f"Shift amount: {int(entry[21:26], 2)}")

## 100011 00101 00110

00010

• For Example: 1w \$5, 8 (\$6)

for the other I-type instructions

def i\_destination\_reg(entry): print(f"Destination Register: {int(entry[11:16], 2)}") def i\_constant\_or\_offset(entry): print(f"Constant/Offset: {int(entry[-16:], 2)}") For J-Type Operations: J-Type Instructions These instructions are identified and differentiated by their opcode numbers (2 and 3). Jump instructions use pseudo-absolute addressing, in

00111

## **if** int(entry[0:6], 2) == 0: r\_type\_func(entry)

j\_type\_func(entry)

print("Instruction Format: J")

else: print("Instruction Format: I") i\_type\_func(entry) i\_source\_reg(entry) i\_destination\_reg(entry) print("Shift amount: none") i\_constant\_or\_offset(entry) For the bit string 00000010001100100100000000100000: Instruction Format: R Operation: add Source Registers: 17, 18 Destination Register: 8 Shift amount: 0

Operation: lw Source Register: 18 Shift amount: none Constant/Offset: 100 Instruction Format: R

Operation: or

Source Registers: 10, 11 Destination Register: 18 Shift amount: 0 Constant/Offset: none Instruction Format: R Operation: and Source Registers: 9, 10 Destination Register: 19 Shift amount: 0 Constant/Offset: none

For the bit string 00000001010010110100100000101010: Instruction Format: R Operation: slt Source Registers: 10, 11 Destination Register: 9 Shift amount: 0 Constant/Offset: none For the bit string 10101110001100110000000001100100: Instruction Format: I Operation: sw Source Register: 17 Destination Register: 19 Shift amount: none Constant/Offset: 100 For the bit string 0001001000110010000000001100100: Instruction Format: I Operation: beq Source Register: 17 Destination Register: 18 Shift amount: none

address rt rs 5 bits 5 bits 16 bits Functions for I-Type Operations: print(f"Source Register: {int(entry[6:11], 2)}")

I-type format rt 5 bits 5 bits

address 16 bits - rs is a source register-an address for loads and stores, or an

operand for branch and immediate arithmetic instructions rt is a source register for branches, but a destination register

0000 0000 0000 1000 bne \$7, \$2, skip\_next\_4 0000 0000 0000 0100

Constant/Offset: 5 For the bit string 00000010010100111000100000100010: Instruction Format: R

print('Operation: jump') **elif** (int(entry[0:6], 2)) == 3: print('Operation: jump and link') Main Function: In [135.. for entry in inputList: print(f"For the bit string {entry}:") print("Instruction Format: R")

which the upper 4 bits of the computed address are taken relatively from the program counter. Instruction RTL  $PC \leftarrow \{(PC + 4)[31:28], address, 00\}$ j address jal address  $R[31] \leftarrow PC + 8$  $PC \leftarrow \{(PC + 4)[31:28], address, 00\}$ 

Load, store, branch, & immediate instrs are I-type

Function for J-Type Operation: def j\_type\_func(entry): **if** (int(entry[0:6], 2)) == 2: r\_source\_reg(entry) r\_destination\_reg(entry) r\_shamt(entry) print("Constant/Offset: none") elif int(entry[0:6], 2) == 2 or int(entry[0:6], 2) == 3:

Constant/Offset: none For the bit string 00100010001010000000000000000101: Instruction Format: I Operation: addi Source Register: 17 Destination Register: 8 Shift amount: none

For the bit string 00000001010010111001000000100101: For the bit string 0000000100101010001100000100100:

Operation: sub Source Registers: 18, 19 Destination Register: 17 Shift amount: 0 Constant/Offset: none For the bit string 1000111001010001000000001100100: Instruction Format: I Destination Register: 17

Constant/Offset: 100 In [ ]: