nexperia

Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of http://www.nxp.com, http://www.philips.com/ or http://www.semiconductors.philips.com/, use **http://www.nexperia.com**

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:
- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved
Should be replaced with:
- **© Nexperia B.V. (year). All rights reserved**.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

AN11599

Using power MOSFETs in parallel

Rev. 1 — 7 July 2015

Application note

Revision history

Rev	Date	Description
01	20150707	initial version

Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

1. Introduction

One much publicized benefit of power MOSFETs (compared to other semiconductor devices) is that it is easy to parallel them to create a group with increased capability. Although this feature is superficially true, there are several potential problems that can catch out the unwary circuit designer.

A MOSFET consists of a group of paralleled 'cells' fabricated on the surface of a silicon die. All the cells are created at the same time under the same conditions. When the MOSFET is fully enhanced and conducts channel current, the temperatures of all the cells are very similar. As the cells are structurally and thermally closely matched, they share current and power well and the parameters of the MOSFET can be well-defined.

There is a range of values for the parameters of the MOSFET dies on a wafer. There is a wider range for MOSFET dies on different wafers in the same production batch. The range is even wider for all batches even though the MOSFETs are the same type. MOSFETs with parameter values outside the data sheet limits are rejected.

The MOSFETs in a paralleled group should all be the same type, but their parameters could be anywhere within the data sheet range. Their die temperatures are unlikely to be the same. Consequently their power sharing is not perfect.

This document contains guidelines on how to design a group of MOSFETs to get the best performance from them. The design must accommodate MOSFET variations within the data sheet limits. It must also allow for MOSFET parameter variations over the range of electrical and environmental conditions. If all the MOSFETs in the group work within their safe maximum limits, the paralleled group of MOSFETs operates reliably.

It is technically and commercially undesirable to have to select MOSFETs and it should be unnecessary. The circuit should be designed to accommodate any MOSFET within the worst case $R_{DS(on)}$ range.

The key data sheet limit which must not be exceeded is the maximum junction temperature $T_{j(max)}$ of 175 °C.

2. Static (DC) operation

This situation is the simplest condition where current flows through a group of paralleled MOSFETs that are fully enhanced (switched ON). A proportion of the total current flows through each MOSFET in the group. At the initial point of turn on, the die temperatures of all the MOSFETs in the group are the same. The drain current I_D flowing in each MOSFET is inversely proportional to its $R_{DS(on)}$ (the drain-source voltage V_{DS} across all the MOSFETs is the same).

The MOSFET with the lowest $R_{DS(on)}$ takes the highest proportion of the current and dissipates the most power (power dissipation $P = V_{DS} \times I_D$).

All the MOSFETs heat up, but the MOSFET with the lowest $R_{DS(on)}$ heats up most (assuming the $R_{th(j-a)}$ of all the MOSFETs is the same).

AN11599

Application note **Rev. 1 — 7 July 2015** **3 of fm**

MOSFET $R_{DS(on)}$ has a positive temperature coefficient. $R_{DS(on)}$ increases as T_j increases. The die temperatures and $R_{DS(on)}$ values of all MOSFETs in the group rise, but the die temperature of the lowest $R_{DS(on)}$ MOSFET increases disproportionately. The effect of this behavior is to redistribute the current towards the other (higher $R_{DS(on)}$) MOSFETs in the group.

Stable thermal equilibrium is reached after a period of operation. The lowest $R_{DS(on)}$ MOSFET is the hottest, but carries a lower proportion of the current than it did initially.

The Positive Temperature Coefficient (PTC) of $R_{DS(on)}$ is a stabilizing influence that promotes power sharing between the MOSFETs in the group. However, as stated earlier the most important criterion is that the maximum junction temperature of any MOSFET in the group must not exceed 175 °C.

The cooling of each MOSFET in the group depends on its thermal resistance from junction to ambient. Die temperature influences the heat flow from adjacent MOSFETs. Rather than considering the thermal resistance paths between the MOSFET dies, the main influence is the temperature of the common heatsink. All the MOSFET mounting bases are bonded electrically and thermally to this heatsink.

The lowest $R_{DS(on)}$ MOSFET could be located anywhere in the group. The thermal resistance from mounting base to ambient of all the MOSFETs in the group should be as similar as possible and as low as possible. Cooling is optimized and independent of location.

This thermal resistance solely depends on the thermal characteristics and design of the assembly [Printed-Circuit Board (PCB) or heatsink] to which the MOSFET is thermally bonded.

Sometimes a value for $R_{th(j-a)}$ is given in data sheets but this parameter is of very limited value. It cannot be treated as a well-defined parameter because it also depends on other external factors such as PCB construction, PCB orientation and air flow. The only guaranteed thermal parameter is the thermal resistance from the MOSFET junction to mounting base $R_{th(j-mb)}$.

2.1 Worked examples for static operation

The worked examples that follow are based on the BUK764R0-40E.

Table 1.   Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.82	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a PCB	-	50	-	K/W

A typical group of MOSFETs has a range of $R_{DS(on)}$ values. The distribution has a peak at around the typical data sheet $R_{DS(on)}$ value; none should have an $R_{DS(on)}$ higher than the data sheet maximum. The $R_{DS(on)}$ of about half of the samples is less than the typical value.

Minimum $R_{DS(on)}$ is not given in the data sheet, but a good estimate is

$$R_{DS(on)(min)} \approx R_{DS(on)(max)} - 2(R_{DS(on)(max)} - R_{DS(on)(typ)}) \tag{1}$$

The $R_{DS(on)}$ value range means that a group of typical MOSFETs is very unlikely to share power equally when they are operated in parallel.

The worst case would be when one of the MOSFETs has the minimum $R_{DS(on)}$ and all the others have the maximum $R_{DS(on)}$.

Modeling of the electro-thermal system is complex because its electrical and thermal characteristics are mutually dependent. However, an electro-thermally convergent Excel model can be used to estimate the performance characteristics of a paralleled group. As an example, in a worst case situation three BUK764R0-40E MOSFETs are connected in parallel; two have maximum $R_{DS(on)}$ of 4 mΩ. The other has a lower than typical $R_{DS(on)}$ of 2.6 mΩ.

The MOSFET with the lowest $R_{DS(on)}$ value takes the highest proportion of the current. It therefore has the highest power dissipation.

The target is to keep the junction temperature of the hottest MOSFET below 175 °C under worst case operating conditions.

These estimations are simplified illustrations. The thermal representation of the MOSFET group is less complex than a real application. In a real application, there are other factors such as neighboring components and orientation that would influence cooling. However, they show the approximate behavior of the group with two different $R_{th(j-a)}$ values.

The first scenario shows the system with the thermal resistance from junction to ambient for each MOSFET ($R_{th(j-a)}$ = 20 K/W; T_{amb} = 125 °C).
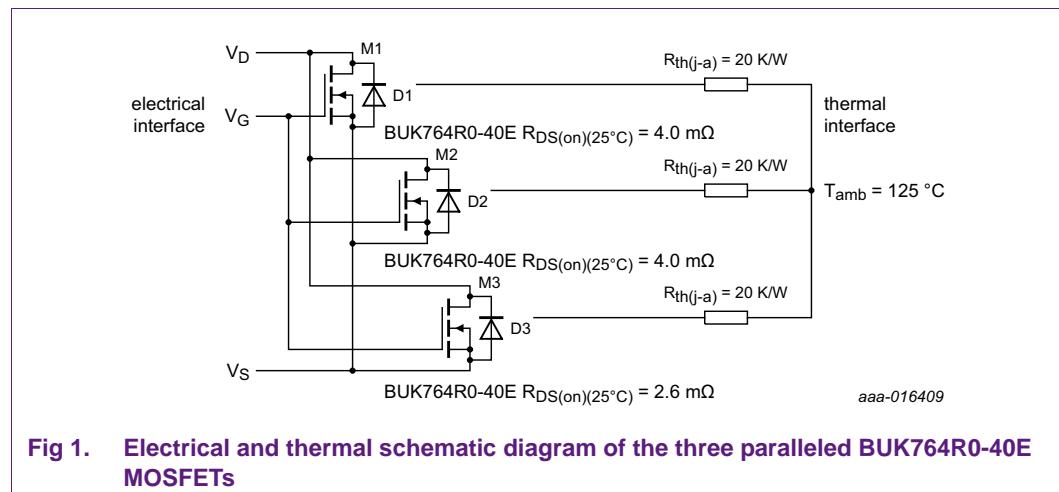
Fig 1. Electrical and thermal schematic diagram of the three paralleled BUK764R0-40E MOSFETs

Table 2 shows the maximum safe limits of V_{DS}, I_D, P and T_j for all the MOSFETs at thermal equilibrium. At this point, the junction temperature of the hottest MOSFET is almost 175 °C.

Table 2. MOSFET maximum conditions for $R_{th(j-a)}$ = 20 K/W and T_{amb} = 125 °C

MOSFET	V_{DS} [V]	$R_{th(j-a)}$ [K/W]	$R_{DS(on)(25°C)}$ [mΩ]	Initial $R_{DS(on)(125°C)}$ [mΩ]	Initial current I_D [A]	Initial power P [W]	Initial power share [%]	Final $R_{DS(on)}$ [mΩ]	Final current I_D [A]	Final power P [W]	Final T_j [°C]	Final power share [%]
M1	0.11	20	2.6	4.16	42.31	4.65	43.5	4.92	22.36	2.46	174	42.3
M2	0.11	20	4	6.4	27.50	3.03	28.3	7.21	15.26	1.68	159	28.9
M3	0.11	20	4	6.4	27.50	3.03	28.3	7.21	15.26	1.68	159	28.9

Total initial power P(M1 + M2 + M3) = 10.70 W

Total final power P(M1 + M2 + M3) = 5.82 W

The second scenario relates to the same electrical system, but with ideal thermal characteristics. The thermal resistance $R_{th(j-a)}$ of each MOSFET is 0.82 K/W. This situation corresponds to the ideal but unrealistic situation where each MOSFET is perfectly thermally bonded to an infinite heatsink (a heatsink with zero thermal resistance).
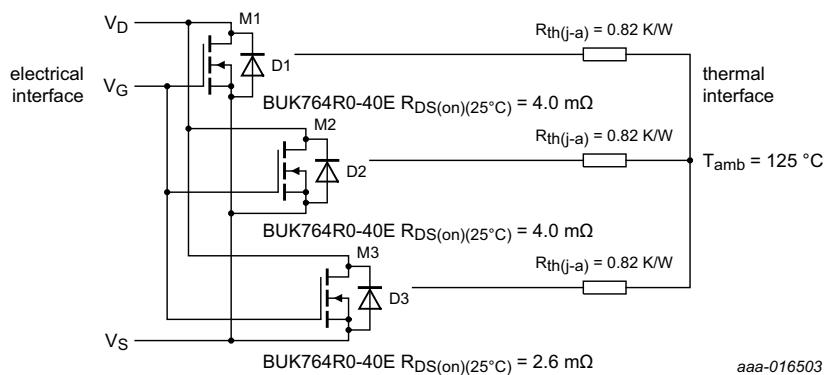

Fig 2. Electrical and thermal schematic diagram of the three paralleled BUK764R0-40E MOSFETs with ideal thermal conditions

Table 3 shows the values of V_{DS}, I_D, P and T_j for all the MOSFETs at thermal equilibrium. At this point, the junction temperature of the hottest MOSFET is almost 175 °C.

Table 3. MOSFET maximum conditions for $R_{th(j-a)}$ = 0.82 K/W and T_{amb} = 125 °C

MOSFET	V_{DS} [V]	$R_{th(j-a)}$ [K/W]	$R_{DS(on)(25°C)}$ [mΩ]	Initial $R_{DS(on)(125°C)}$ [mΩ]	Initial current I_D [A]	Initial power P [W]	Initial power share [%]	Final $R_{DS(on)}$ [mΩ]	Final current I_D [A]	Final power P [W]	Final T_j [°C]	Final power share [%]
M1	0.55	0.82	2.6	4.16	211.54	116.35	43.5	4.92	111.79	61.48	174	42.3
M2	0.55	0.82	4	6.4	137.50	75.63	28.3	7.21	76.28	41.96	159	28.9
M3	0.55	0.82	4	6.4	137.50	75.63	28.3	7.21	76.28	41.96	159	28.9

Total initial power P(M1 + M2 + M3) = 267.60 W

Total final power P(M1 + M2 + M3) = 145.39 W

Note: This scenario is ideal and unrealistic. It is included to illustrate the benefit of reducing $R_{th(j-a)}$ to maximize the usage of the MOSFET capabilities.

In practice, $R_{th(j-a)}$ is always greater than $R_{th(j-mb)}$. The thermal bonding between the MOSFET mounting base and the heatsink is never perfect and an infinite heatsink does not exist in the real world.

In this case, the drain current (I_D) of the MOSFETs becomes the limiting factor (the data sheet maximum I_D is 75 A).

To optimize MOSFET utilization, the MOSFETs must be able to dissipate as much power as possible. At the same time, the junction temperature of the hottest MOSFET must remain below the maximum safe temperature of 175 °C.

The following conclusions can be drawn from Table 2 and Table 3:

1. It is beneficial to reduce $R_{th(j-a)}$ as much as possible to optimize the MOSFET die cooling.

2. It is beneficial to reduce the maximum ambient temperature to increase the available thermal 'headroom'.

3. As a result of Table 2 and Table 3, it is clear that junction temperature difference between the MOSFETs depends only on their $R_{DS(on)}$ values (assuming the $R_{th(j-a)}$ for each MOSFET is the same).

4. When the paralleled (fully enhanced) MOSFETs heat up during use, their power distribution changes such that the cooler MOSFETs take a greater proportion of the power. This effect is due to the PTC of $R_{DS(on)}$ and it acts to promote thermal stability.

3. MOSFET mounting for good thermal performance and power sharing

To get the most from the MOSFET group, the individual MOSFET should be mounted in a way that causes their mounting base temperatures to be as similar as possible and also as low as possible.

To realize this goal, the thermal resistance between each MOSFET (mounting base) and the mounting bases of all the other MOSFETs in the group should be matched and minimized. They should be mounted symmetrically and as close together as possible on a thermally conductive surface.

Heat flow can be considered to be analogous to electric current flow; so the thermal bonding points of the MOSFETs (usually the drain tabs) should be on a thermal 'ring main'. The low thermal resistance path allows heat to flow easily between the MOSFETs. When heat flows easily between all the MOSFETs in the group, their mounting base temperatures track together closely.

Note: This arrangement does not promote equal current sharing, but promotes better die temperature matching. The temperatures of all the MOSFETs in the group can rise more before the temperature of the hottest MOSFET reaches 175 °C. Hence the power dissipation capability of the group is maximized.

There are practical limits to the physical extent of the thermal ring main; ideally each MOSFET should be next to all its neighbors. This condition limits the group to two or three MOSFETs.

AN11599

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2015. All rights reserved.

Application note **Rev. 1 — 7 July 2015** **7 of fm**
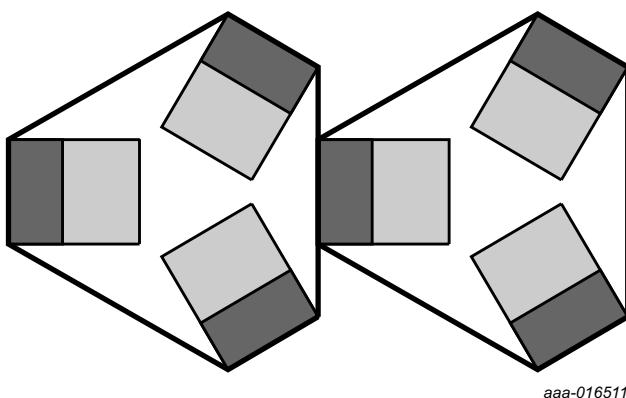
This layout suits standard packaged MOSFETs (e.g. D2PAK, LFPAK and TO-220). The dark shaded area corresponds to the drain tab of the device.

Fig 3.   A layout for six paralleled MOSFETs to promote good power sharing
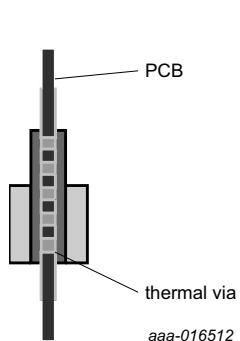
a. Two paralleled MOSFETS where both devices are located directly opposite each other on the two faces of a PCB
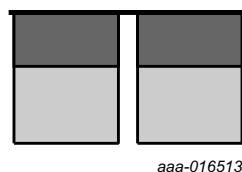
b. Two paralleled MOSFETS where the devices are located next to each other on the same face of a PCB
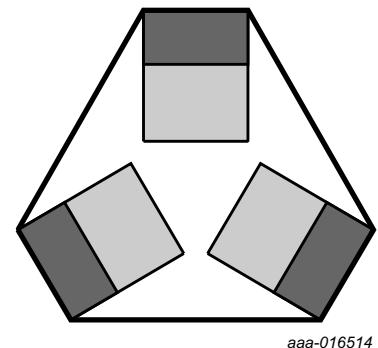
c. Three paralleled MOSFETS where the devices are located in a symmetrical loop other on one face of a PCB

Fig 4.   Good layout arrangements for two paralleled MOSFETs and three paralleled MOSFETs

A good way to parallel a pair of MOSFETs is to locate them on opposite faces of a PCB forming a PCB 'sandwich' as in Figure 4a. Thermal vias between the copper 'land' areas on the PCB reduce the electrical and thermal resistances between their mounting bases.

To parallel a pair of MOSFETs on the same face of a PCB, they can be mounted next to each other as in Figure 4b.

A good way to parallel three MOSFETs is in a ring as in Figure 4c. This arrangement allows all the MOSFET sources in the group to be connected to a 'star' point. The electrical and thermal paths between the MOSFET drains match due to their symmetrical connections to the drain loop.

Minimizing and matching the electrical impedances in the source paths is more important than matching the electrical impedance in the drain paths. This difference is because their gate drives are related to the sources. Good impedance matching in both drain and source is more important in high frequency switching circuits.

If similar electrical and thermal matching can be achieved, larger paralleled groups could be considered. Groups of more than four or five become unwieldy so grouped sub groups should be used.

aaa-016511

aaa-016518

a. Six paralleled MOSFETs based on two sub groups of three MOSFETs

b. Nine paralleled MOSFETs based on three sub groups of three MOSFETs
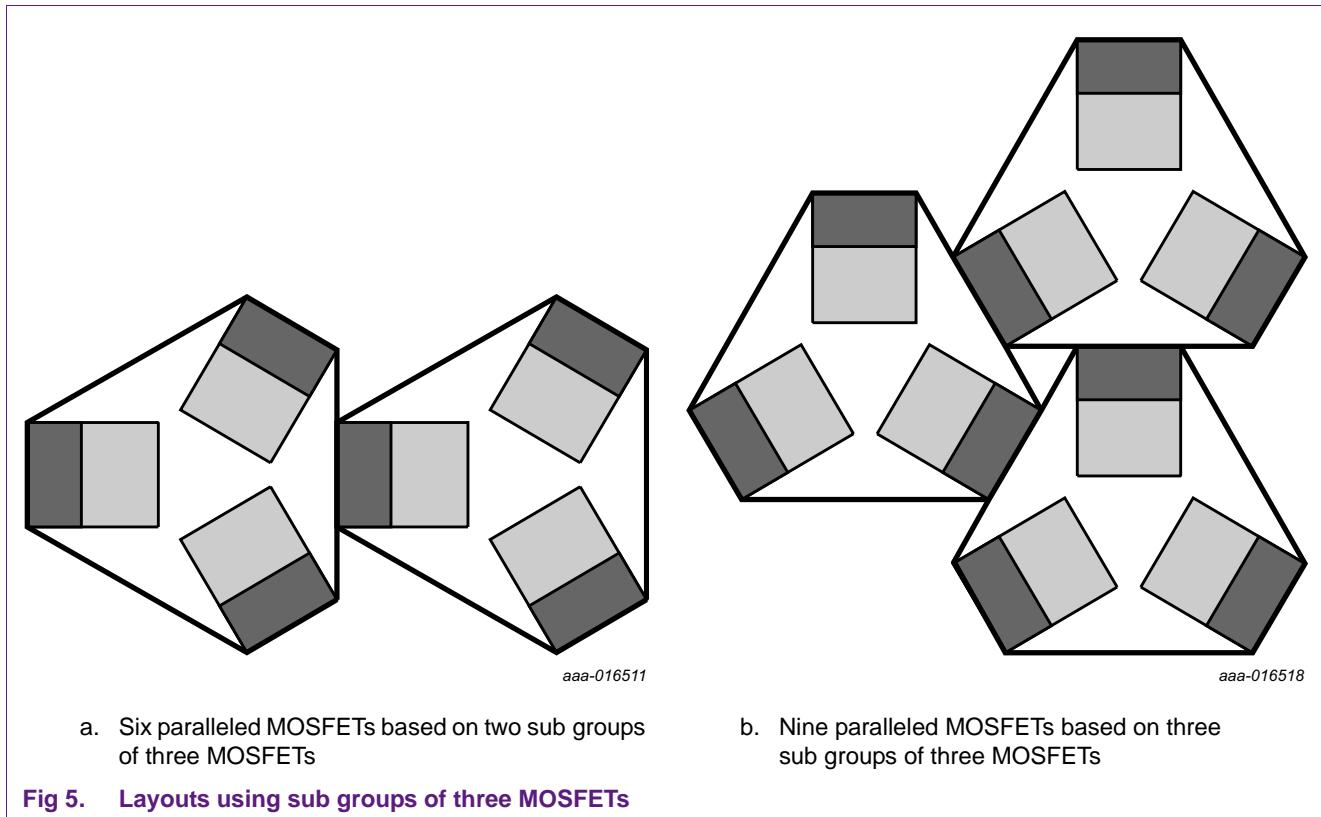
Fig 5.   Layouts using sub groups of three MOSFETs

In this group of 9 (3 groups of 3), there is a natural drain star point at the center of the group. There are separate source star points at the centers of each sub group. The source star points can be connected on a layer of a multi-layer PCB.

There is a compromise between optimizing layout for power sharing and maximizing PCB usage.

Electrically and thermally optimized layouts always use more PCB area than the minimum possible, but utilization of MOSFET capability should be better. Areas of PCB that are unoccupied by MOSFETs or gate drive components are useful for thermal interfaces with heat sink or cooling air.

AN11599

Application note **Rev. 1 — 7 July 2015** **9 of fm**

4. Power sharing in dynamic operation [pulse and Pulse Width Modulation (PWM) circuits]

Many MOSFET circuits are designed to operate in systems where they are switched repetitively (such as DC-to-DC converters). Paralleled MOSFETs can be used as the switching elements in the system, but in addition to the guidelines set out for optimal steady state power sharing. Some additional points must be considered so that the MOSFETs share current during the switching transitions.

Good circuit and layout design is important. It influences the proportion of current carried by each MOSFET in the group during and after the switching event.
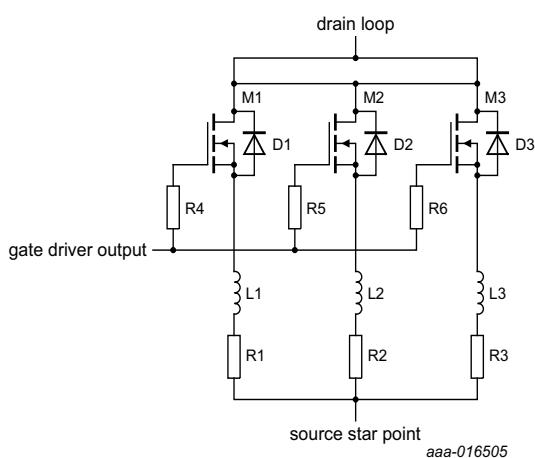

Fig 6. **Schematic diagram showing the stray source inductances and source resistances**
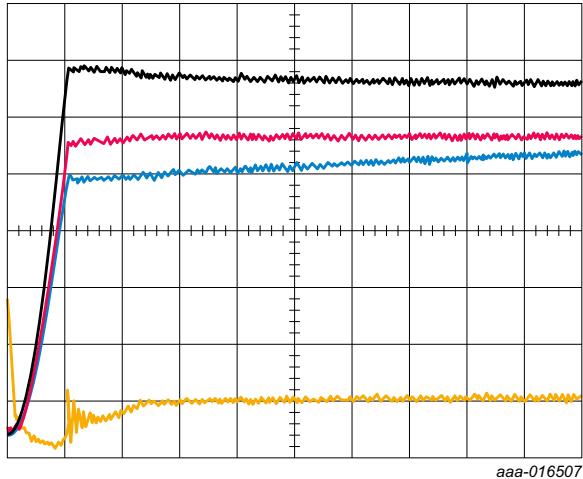
a. MOSFET drain current distribution immediately after turn on. The time base scale is 100 ns/division.
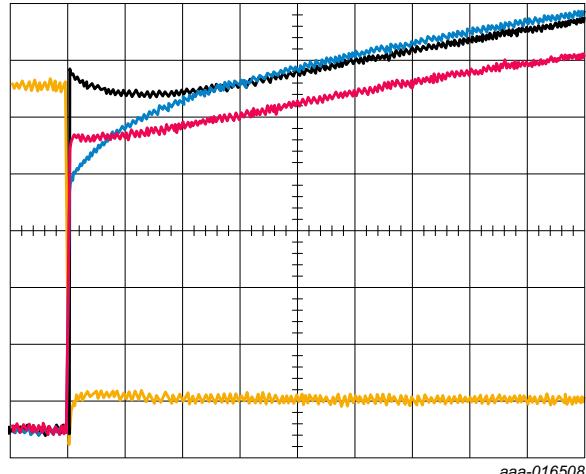
b. The same MOSFET drain current distribution as in Figure 7a showing the changes as time progress. The time base scale is 100 μs/division.

Fig 7. **Oscilloscope plots showing the MOSFET drain currents (black, red and blue) and drain source voltage (yellow) after turn on**

AN11599

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2015. All rights reserved.

Application note

Rev. 1 — 7 July 2015

10 of fm

Figure 7a and Figure 7b show how the current distribution in three paralleled MOSFETs initially depends on the source inductances in the MOSFET current paths, namely L1, L2 and L3. As time progresses the resistances in the MOSFET current paths, namely $R_{DS(on)}$ + R1, $R_{DS(on)}$ + R2 and $R_{DS(on)}$ + R3 determine the current distribution.

The same principles hold about impedance matching of the current paths to the MOSFETs in the group. In this case, it is more important for the rates of change of current in the MOSFETs to match. The source inductances are the key impedance as they affect the gate-source voltages (gate drives) of the MOSFETs in the group.

This effect dominates more in high frequency and short duty cycle applications (e.g. switched-mode power supplies). It may be insignificant in lower frequency applications such as motor drives.

5. Partially enhanced (linear mode) power sharing

If a group of MOSFETs must operate in linear (partially enhanced) mode, great caution is needed. MOSFETs simply paralleled together as they are for fully enhanced conduction are very unlikely to share power or current well.

This behavior is due to the Negative Temperature Coefficient (NTC) of gate threshold voltage $V_{GS(th)}$. As the group of MOSFETs starts to enhance, the MOSFET with the lowest $V_{GS(th)}$ starts to conduct channel current first. It dissipates more power than the others and heat up more. Its $V_{GS(th)}$ decreases even further which causes it to enhance further.

This unbalanced heating causes the hottest MOSFETs to take a greater proportion of the power (and get even hotter). This process is unsustainable and can result in MOSFET failure if the power is not limited. Great care is needed when designing paralleled power MOSFET circuits that operate in the partially enhanced (linear mode) condition.

If all the MOSFETs in the group operate within their Safe Operating Area (SOA), they work reliably. The SOA must be adjusted for the worst case mounting base temperature that occurs in the application. Remember that the data sheet SOA graph applies only if the MOSFET mounting base temperature is 25 °C or less.

Adding external source resistors (R1 to R4 in the schematic; see Figure 8) provides the negative feedback needed for stable operation. The gate-source voltage applied to $V_{GS}(M1) = V_G - I_D(M1) \times R1$.

If the MOSFETs must also operate in fully enhanced mode (e.g. in 'Hot Swap' or 'Soft Start' applications), the inclusion of these resistors is an efficiency disadvantage.

As the MOSFET channel current increases, its gate drive voltage reduces.

As the MOSFETs are operating in partial enhancement (where MOSFET $R_{DS(on)}$ is not important), there is no adverse effect caused by including these resistors. If the MOSFETs must operate in both modes (as with active clamping after fully enhanced conduction), the inclusion of source resistors does have a negative impact.

AN11599

Application note **Rev. 1 — 7 July 2015** **11 of fm**
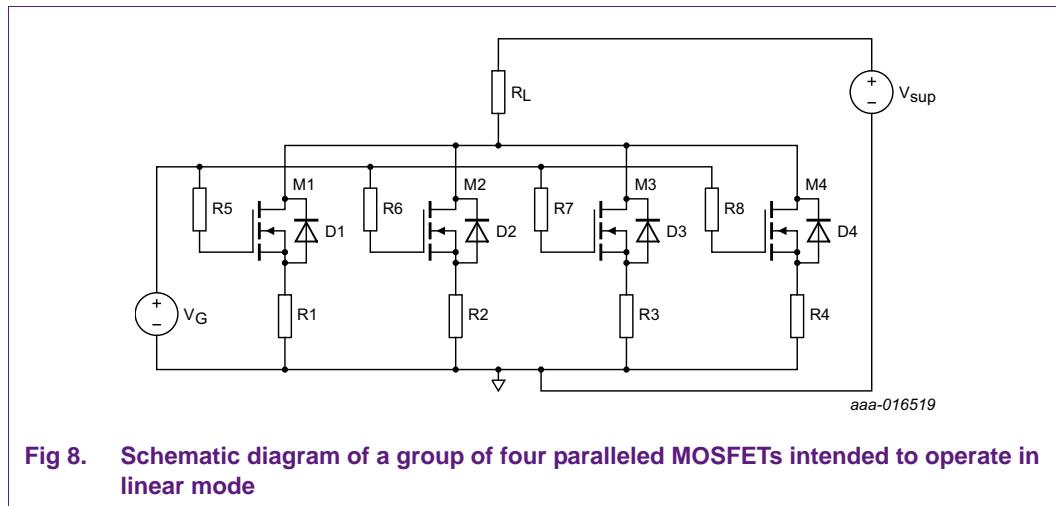
Fig 8. **Schematic diagram of a group of four paralleled MOSFETs intended to operate in linear mode**

MOSFETs developed specifically for linear mode operation are available from NXP. They can simplify the design of paralleled groups of MOSFETs intended for linear mode operation.

6. Gate drive considerations

It is preferable to fit low value gate resistors between the gate driver and the gate of each MOSFET in the group.

Their main function is to decouple the MOSFET gates from each other so they all receive similar gate drive signals. Without these resistors, at turn on the Miller plateau of the MOSFET with the lowest threshold voltage would act to clamp the gate-source voltages of the other MOSFETs in the group. This clamping effect tends to inhibit and delay the turning on of the other MOSFETs in the group. At turn off a similar process occurs.

Without these resistors, the MOSFET with the lowest threshold voltage would switch on first and switch off last. The consequences of this effect may be insignificant in low frequency high duty cycle applications. In higher frequency PWM applications, it could cause a significant power imbalance between the MOSFETs. Positive feedback also occurs in this case which increases the imbalance and could ultimately cause MOSFET failure.

Gate resistors also help to damp out oscillatory transients on V_{GS}. They also swamp any effects caused by variations in the internal gate resistance $R_{G(int)}$ of the MOSFETs.

6.1 Should individual gate drivers be used for each MOSFET in the group?

Using individual gate drivers for each MOSFET in the group is usually unnecessary. They may be necessary in applications where fast switching of a large group of large die MOSFETs is needed. Here the MOSFETs should be arranged in smaller sub groups, each sub group driven by an individual gate driver. Care should be taken to balance the circuit so the propagation delays of all the gate drivers are similar. This matching ensures that the switching of all the MOSFETs in the group is synchronized. Usually it is sufficient to

drive the gate of each MOSFET in the group from the same gate driver. However, it is important to have a gate resistor between the gate driver output and the gate of each MOSFET as mentioned earlier.

7. MOSFET packaging considerations for paralleled groups

Conventionally packaged surface-mounted MOSFETs (DPAK and D2PAK) are the most widely available types so they are considered first for paralleled groups. However, KGD and LFPAK (power SO8) MOSFETs could offer better solutions.

7.1 Bare die (KGD) MOSFETs

These MOSFETs offer the densest and most flexible options for paralleled groups; they are designed to suit a specific application. The die aspect ratio and gate pad location can be designed specifically to suit the application. More source wire bonds can be fitted to the die than can be fitted in a conventionally packaged MOSFET, so overall $R_{DS(on)}$ can be reduced. Maximum drain current can be increased to achieve better performance from a paralleled group of MOSFETs. Special manufacturing facilities are required for KGD assembly.

7.2 LFPAK MOSFETs

The power SO8 (LFPAK) MOSFETs offer the opportunity to manufacture the paralleled MOSFET circuit conventionally. Higher component density and power capability are possible (approaching that of KGDs). The connections to the source and gate are made using copper clips which give better electrical and thermal performance than aluminum wire bonds in conventional packages.

8. Inductive energy dissipation in paralleled MOSFETs

8.1 Avalanching - low side MOSFET group driving a high side inductive load

If the group of paralleled MOSFETs is driving an inductive load, energy stored in this load must be safely dissipated when the current is switched off. A good way to manage this energy is to connect a 'freewheel diode' across the load; see Figure 9. Current flowing in the MOSFET channel diverts into the diode when the MOSFETs switch off and the energy is dissipated in the circuit resistances. However, it is not always possible and energy must then be dissipated safely in the MOSFETs.

If the battery polarity (V_{sup}) is reversed, the low impedance path through the freewheel diode and the body diode can carry large damaging currents. Freewheel diodes are often not used for this reason.

When the group of MOSFETs is switched off, the back e.m.f. from the inductive load may be high enough to cause the drain-source voltage across the group of MOSFETs to exceed the drain-source breakdown voltage $V_{(BR)DSS}$ of one of the MOSFETs. It likely that MOSFETs in the group have a range of $V_{(BR)DSS}$ values (even though they are the same type). The current then flows through the body diode of the MOSFET with the lowest $V_{(BR)DSS}$ in reverse (avalanche) conduction. This condition causes high-power dissipation and temperature rise in the MOSFET die ($P = I_D \times V_{(BR)DSS}$). If the maximum 175 °C junction temperature is exceeded, the thermal stress on the die could degrade or destroy the MOSFET.

In the worst case, all the current which was flowing through the group of MOSFETs could be diverted into the body diode of one MOSFET in the group. If this scenario is possible, it is vital that a single MOSFET in the group can safely handle the total avalanche current under worst case thermal conditions. $V_{(BR)DSS}$ has a positive temperature coefficient which tends to redistribute the current towards other MOSFETs with higher $V_{(BR)DSS}$ values.
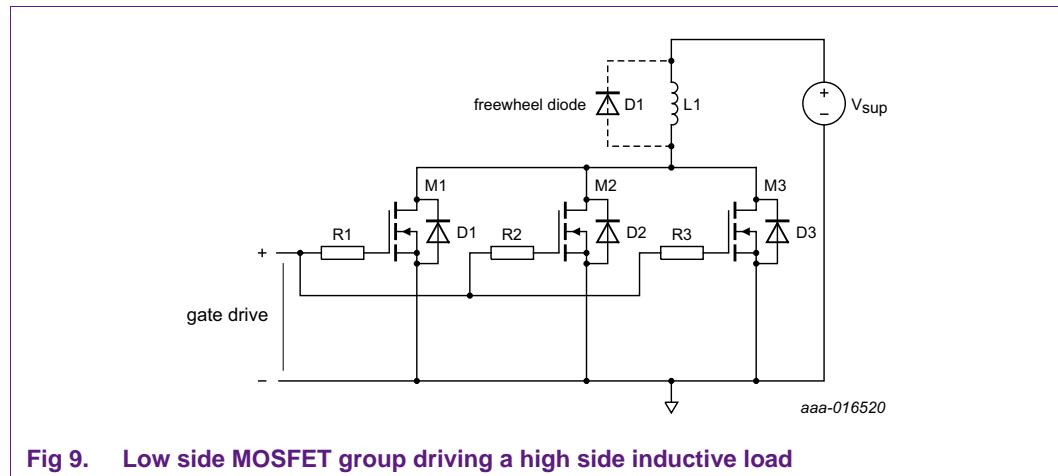

Fig 9.   Low side MOSFET group driving a high side inductive load

8.2   Active clamping - high side MOSFET group driving a low side inductive load

This configuration (see Figure 10) is often used in automotive applications. This topology is useful because the vehicle chassis can be used as the negative supply return path to the battery.
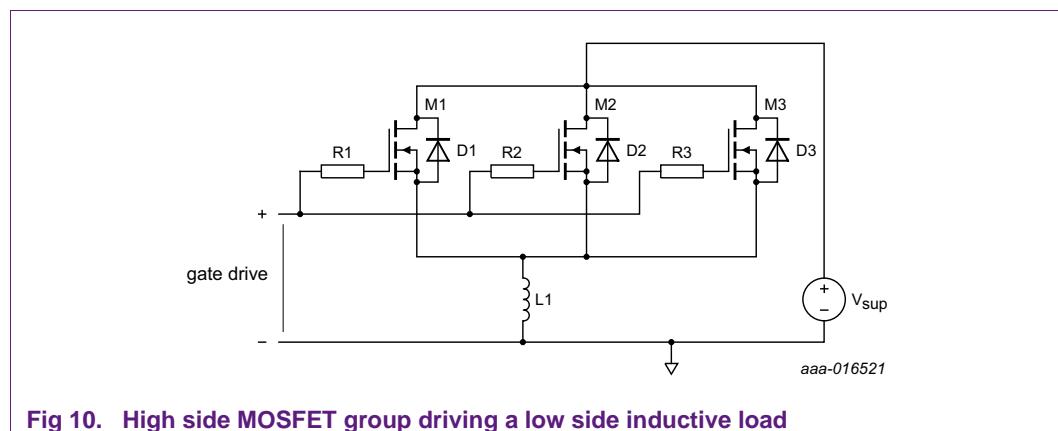

Fig 10.   High side MOSFET group driving a low side inductive load

In this circuit, the difference between the threshold voltages rather than $V_{(BR)DSS}$ spread determines where the load current flows. The MOSFET with the lowest threshold voltage conducts the greatest proportion of the current. The drain-source voltage across the MOSFET group is $V_{sup} + V_{GS}$ and the power dissipation of the group is $(V_{sup} + V_{GS}) \times I_D$. As with the avalanche case, all the current (and hence all the power dissipation) could be diverted into a single MOSFET in the group.

This situation is worse than the avalanche case because MOSFET threshold voltage has a negative temperature coefficient. This characteristic tends to direct the current flow initially to the hottest MOSFET. This MOSFET then gets even hotter so that it retains the current.

9. Summary

1. It is better to use a single large MOSFET rather than a group of smaller MOSFETs.
2. The power capability of a group of n MOSFETs never achieves n times the power capability of a single MOSFET.
3. If it is necessary to use paralleled MOSFETs, use the lowest number possible as the basic group size (3 maximum).
4. If a larger number is needed, use a group of basic groups i.e. 4 = 2 groups of 2; 6 = 2 groups of 3.
5. The circuit layout is a very important factor determining how well a group of paralleled MOSFETs share power dissipation, particularly in higher frequency repetitive switching circuits.
6. Consider LFPAKs (for repetitive switching applications) because of their small size, good thermal performance and low package impedances.
7. Special care is needed when designing groups of MOSFETs that could operate in avalanche or active clamping mode.

10. Abbreviations

Table 4.   Abbreviations

Acronym	Description
KGD	Known Good Die
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NTC	Negative Temperature Coefficient
PCB	Printed-Circuit Board
PTC	Positive Temperature Coefficient
PWM	Pulse Width Modulation
SOA	Safe Operating Area

AN11599

Application note **Rev. 1 — 7 July 2015** **15 of fm**

11. Legal information

11.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

11.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

11.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

12. Contents

Date of release: 7 July 2015
Document identifier: AN11599