Scientific Conference of Young Researchers 2012

12th Scientific Conference of Young Researchers

May 15th, 2012
Herľany, Slovakia

# Proceedings from Conference

Faculty of Electrical Engineering and Informatics
Technical University of Košice




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**12th Scientific Conference of Young Researchers**
**of Faculty of Electrical Engineering and Informatics**
**Technical University of Košice**

Proceedings from Conference

Published: Faculty of Electrical Engineering and Informatics
Technical University of Košice
I. Edition, 440 pages

Available: http://web.tuke.sk/scyr/data/templates/Proceedings_2012.pdf

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**ISBN 978-80-553-0943-9**

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# Foreword

Dear Colleagues,

SCYR (Scientific Conference of Young Researchers) is a Scientific Event focused on exchange of information among young scientists from Faculty of Electrical Engineering and Informatics at Technical University of Košice - series of annual events that was founded in 2000. Since 2000 the conference has been hosted by FEI TUKE with rising technical level and unique multicultural atmosphere. The Eleventh Scientific Conference of Young Researchers (SCYR 2012), conference of Graduates and Young researchers, was held on 15$^{th}$ May 2012. The primary aims of the conference, to provide a forum for dissemination of information and scientific results relating to research and development activities at the Faculty of Electrical Engineering and Informatics has been achieved. 110 participants mostly by doctoral categories were active in the conference.

Faculty of Electrical Engineering and Informatics has a long tradition of students participating in skilled labor where they have to apply their theoretical knowledge. SCYR is opportunities for doctoral and graduating students use this event to train their scientific knowledge exchange. Nevertheless, the original goal to represent a forum for the exchange of information between young scientists from academic communities on topics related to their experimental and theoretical works in the very wide spread field of electronics, telecommunication, electrotechnics, computers and informatics, cybernetics and Artificial intelligence, electric power engineering, remained unchanged.

12$^{th}$ Scientific Conference of Young Researchers at Faculty of Electrical Engineering and Informatics Technical University of Košice (SCYR 2012) was organized in a beautiful village Herľany. The Conference was opened in the name of dean prof. Ing. Liberios Vokorokos, PhD. by the vicedean of faculty, doc. Ing. Roman Cimbala, PhD. In his introductory address he noted the importance of the Conference as a forum for exchange of information and a medium for broadening the scientific horizons of its participants and stressed the scientific and practical value of investigations being carried out by young researchers.

The program of conferences traditionally includes two parallel sessions (both consist of oral and poster part):

- Electrical & Electronics Engineering
- Informatics & Telecommunications

with approximately 110 technical papers dealing with research results obtained mainly in university environment. This day was filled with a lot of interesting scientific discussions among the junior researchers and graduate students, and the representatives of the Faculty of Electrical Engineering and Informatics. This Scientific Network included various research problems and education, communication between young scientists and students, between students and professors. Conference was also a platform for student exchange and a potential starting point for scientific cooperation. The results presented in papers demonstrated that the investigations being conducted by young scientists are making a valuable contribution to the fulfillment of the tasks set for science and technology at Faculty of Electrical Engineering and Informatics at Technical University of Košice.

We want to thank all participants for contributing to these proceedings with their high quality manuscripts. We hope that conference constitutes a platform for a continual dialogue among young scientists.

It is our pleasure and honor to express our gratitude to our sponsors and to all friends, colleagues and committee members who contributed with their ideas, discussions, and sedulous hard work to the success of this event. We also want to thank our session chairs for their co-operation and dedication throughout the whole conference.

Finally, we want to thank all the attendees of the conference for fruitful discussions and a pleasant stay in our event.

Liberios VOKOROKOS
dean of FEI TUKE

May 15$^{th}$ 2012, Herľany

# Application binary state arithmetic encoding in JPEG

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***Abstract*— This paper shortly describes basic image JPEG format. This paper also describes issue of decomposition of DCT image spectral coefficients to its bit levels and their encoding using binary state arithmetic code. In the conclusion, the advantage for replacement of conventionally used Huffmann code by binary state arithmetic encoding of the picture´s bit levels DCT spectral coefficients image is contemplated .**

***Keywords*— JPEG, DCT compression, bit plane and arithmetic encoding.**

## I. INTRODUCTION

The transmission speed of connection has been increasing, but given the fact that the amount of data transferred also increases, it is compulsory to enhance the methods of compression applied to the multimedia data.

This article is focused on an algorithm of source encoding in JPEG. In JPEG, the Huffman encoding is being used. We will try to replace this algorithm using the binary state arithmetic encoding.

## II. JPEG WITH DISSIPATION ENCODING

Block diagram of image encoder is on figure 2.1. There can be colorful or grey scale image on the input. This structure corresponds with intern-image transformation encoding with DCT block size 8x8 pixels and with entropic encoding.[1]

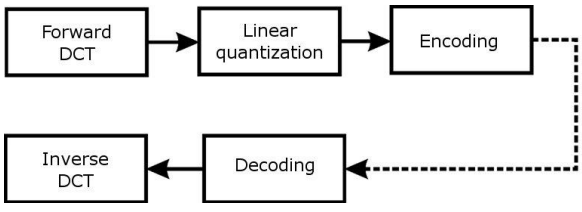



Fig. 2.1. Block diagram image codec JPEG with dissipation encoding.

At the beginning, the image is divided to 8x8 block pixels and after this, DCT is applied. All spectral coefficients (SC) are quantized with different or equal quantization step, which changes, depending on statistical properties or application. Quantized SC are scanned in a diagonal order called with quantization step. [2] Quantized SC are scanned in diagonal order called Zig-zag scanning. Zig-zag is showed on figure 2.2. By using this scanning, we achieve that SC with high energy end small frequency will be scanned before SC with high frequency but small energy do so. SC with zero energy are detected and counted. This allows making couples "number of zeros and non-zero values of SC". These couples are entropic encoded by Huffman code. [3]

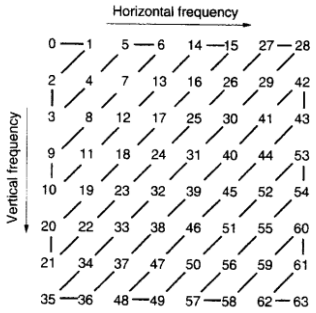



Fig. 2.2 Zig-zag scanning

Each one dimensionally represented block must be ended with special couple [0][0] called EOB (end of block).

### A. Used quantizers

By quantization in space of SC, each of SC is quantized, using its own quantizer. This is showed on figure 2.3.

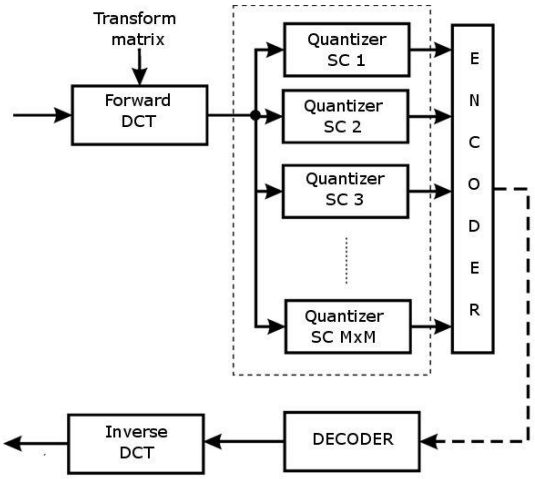



Fig. 2.3 Block diagram of transformation encoding system

In this letter we will use two types of quantizers. We will use one for DC spectral coefficients (DSC) and one for AC spectral coefficients (ASC).

*1) ASC quantization*

For quantization of ASC, the used algorithm is described by the equation 2.1

$$q_{ij} = 8Y_{ij}//MK\Delta_{ij} \quad (2.1)$$

Where $q_{ij}$ represents an index of quantization and takes its values on interval <-255,255>. $Y_{ij}$ is a value of original spectral coefficient and MK is a scaling factor. $\Delta_{ij}$ is quantization step. Operation // means dividing with rounding on nearest integer.
Results of this operation are quantization indexes. [2]
Reverse operation is described by equation 2.2.

$$\tilde{Y}_{ij} = q_{ij}MK\Delta_{ij}/8 \quad (2.2)$$

*2) DSC quantization*

For quantization DSC, algorithm represented by equation 2.3, is used.

$$q_{00} = Y_{00}//8 \quad (2.3)$$

Usually quantization of DSC is performed with fix set step. The obtained quantization level is showed in equation 2.4.

$$\tilde{Y}_{00} = 8q_{00} \quad (2.4)$$

## III. IMAGE DECOMPOSITION TO BIT PLANE

In general, each image can be expressed like two dimension rasters of pixels and each pixel can be described by N bits as follows:

$$\text{pixel} = p_0 2^0 + p_1 2^1 + p_2 2^2 + \ldots\ldots + p_{N-1} 2^{N-1}$$

Individual bits $P_i$ correspond to the respective weights $2^i$ for i=0,1, ... ,N-1. If we pick up only $P_0$ from in a such way expressed pixel from entire polytonal image, we get its bit plane of zero weight ($BP_0$). Using the same process all other bit-planes until $BP_{N-1}$ are created.

In a transformed space, there are not only spectral coefficients with positive value. Because of this fact, there are two various ways for decomposition [2].

- *Decomposition of the real bit-plane (RBP)*
- *Decompositions of the absolute bit-plane and plane of sign (ABP)*

We not decompose image of spectral coefficients, but image of quantization indexes in range <-255; 255>.

### *A. Decomposition of the real bit-plane (RBP)*

In this decomposition, we get bit-planes $-BP_{N-1}$ ... $-BP_0$, .... $BP_0$ ... $BP_{N-1}$. Figure 3.1. shows the block diagram of RBP decomposer.

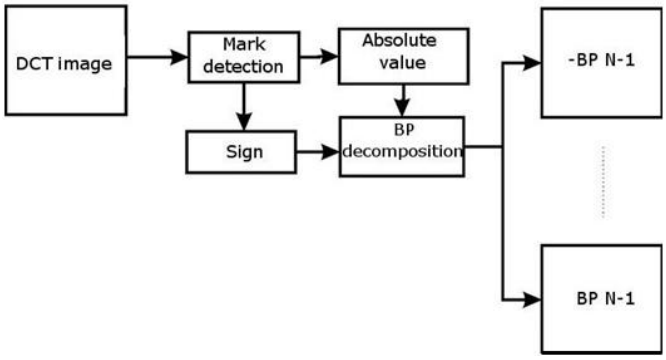



Fig. 3.1 Block diagram of RBP decomposer

Each of spectral coefficients of transformed image is tested on a sign and the result of this is a mark defining either positive or negative bit plane. After this, the image is transformed into absolute value and decomposed with identical method like decomposition of image in Gaussian space.

### *B. Decompositions of the absolute bit-plane and plane of sign (ABP)*

In this decomposition, we get bit-planes $BP_0$, $BP_1$ ... $BP_{N-1}$ and $BP_s$. Block diagram of ABP decomposer is showed on figure 3.2.

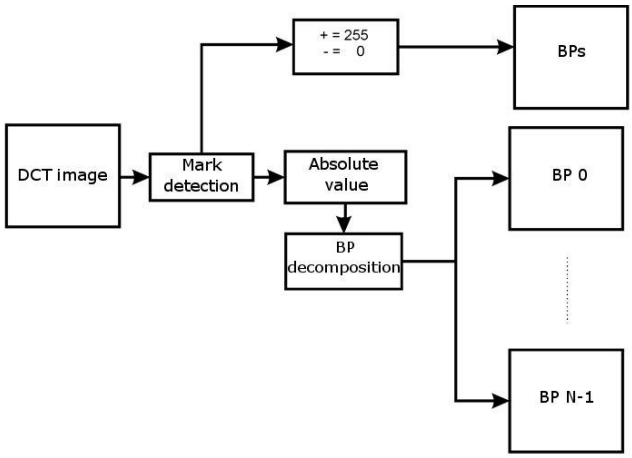



Fig. 3.2 Block diagram of ABP decomposer

Each of spectral coefficients of transformed image is tested on the sign and the result shows value of pixel in bit-plane $BP_s$. This value is 255, or white for positive and 0, or black for negative mark. After this, the image is transformed on absolute value and decomposed with identical method like in previous case.

## IV. ARITHMETIC ENCODING

### A. Arithmetic code without using multiplication

#### 1) Encoding

Procedure of the arithmetic encoding (AE) without using multiplications is described with equations 4.1 – 4.4. [4]

$$A(sk) = A(s).2^{-Q} \quad (4.1)$$
$$A(sm) = < A(s) - A(sk) > \quad (4.2)$$
$$C(sm) = C(s) \quad (4.3)$$
$$C(sk) = C(s) + A(sm) \quad (4.4)$$

Where **C(s)** represents binary variable of sequence **S** with 0 initial value before encoding first symbol, and expresses low limit of probabilistic subinterval. **C(sm)** is binary variable of sequence **S** for the more probable symbol and **C(sk)** for less probable symbol of sequence **S**.

Size of probabilistic subinterval is extended by variable **A(s)**, which initial value is 0.111…..11. Variables **A(sk)** and **A(sm)** are binary variables of size of probabilistic subinterval for more and less probable symbol.

This method is based on approximation of probability of less probable symbol by value of $2^{-Q}$. Variable **C(s)** is obtained by gradual encoding of symbols of binary variable **S**. When all symbols of binary variable **S** are encoded we get two binary variables, **C(s)** and **A(s)**. Resulting arithmetic code is a binary value from interval <C(s), C(s) + A(s)). This value is made, so it contained the smallest possible amount of valid binary numbers.

#### 2) Decoding

Procedure of decoding is described by equations 4.5 – 4.8.

$$A(sk) = A(s).2^{-Q} \quad (4.5)$$
$$A(sm) = < A(s) - A(sk) > \quad (4.6)$$
$$C(s) < A(sm) => y = m; C(sy) = C(s) \quad (4.7)$$
$$C(s) \geq A(sm) => y = k; C(sy) = C(s) - A(sm) \quad (4.8)$$

Input encoded sequence is decoded with gradual recursion of equations 4.5 – 4.8. Decoder must have information about length of encoded word. This information could be broadcasted in transmission channel separated from encoded sequence, or the length can be given in advance.

### B. Binary state arithmetic encoding (BSAC) of binary images

In arithmetic encoding without using multiplications, it is necessary to know value of **Q** from expression $2^{-Q}$.

This value must be given for each symbol of sequence. This information is contained in the model [5]. Model is practically an estimator estimating probability of actual symbol occurrence. JBIG algorithm is used For binary images. Ten points template of JBIG algorithm is on figure 4.1.

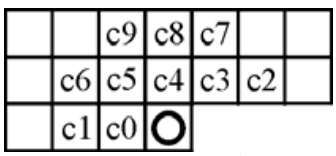



Figure. 4.1. Ten points template of JBIG algorithm.

State **S(y)** of actual point (indicated by circles) is estimated by equation 4.9.

$$S(y) = \sum_{i=0}^{n-1} ci.2^i \quad (4.9)$$

Where **n** is a number of elements in template and **y** is an actual point. After testing the whole image, it is evaluated how many times a particular state occurred and which value actual point had. After that, the most frequent occurred value is determined Finally, conditional probability will be calculated (eq. 4.10.) of point with value "1" or "0" in individual states.

$$p(c = v \mid S_k) = p(S_{v,k}) = \frac{n_{v,k}}{n_k} \quad (4.10)$$

$\mathbf{S_k}$ is value given by equation 4.9 and mean value of actual pixel. $\mathbf{S_{v,k}}$ is state of $\mathbf{S_k}$ with value of pixel equal to **v**.

$\mathbf{n_k}$ is a number of states $\mathbf{S_{v,k}}$. The final model of image is formed by the resulting probabilities. Conditional probability $\mathbf{S_{v,k}}$ are approximated by value $2^{-Q}$.

## V. EXPERIMENTAL RESULTS

Experimental images LENA and BABOON fig. 5.1 and 5.2, respectively, were transformed by DCT in to images of spectral coefficients fig. 5.3 and 5.4. After that, they were quantized with two scales. Lower value of scale is set so that the IDCT (inverse discrete cosine transform) subjective quality would by approximately the same as the original images. High level is set to maximum possible value therefore 32. On fig. 5.5 and 5.6 images after quantization and IDCT are showed.

Fig. 5.1 Image Lena

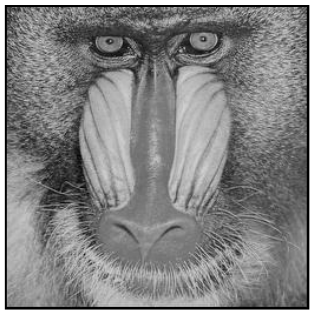


Fig. 5.2 Image Baboon

Fig. 5.3 DCT image Lena

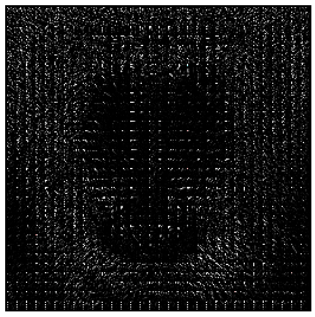
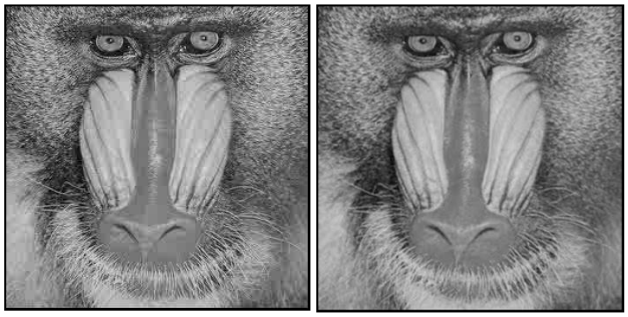


Fig. 5.4 DCT image Baboon

a) b)

Fig. 5.5 IDCT image Lena a) MK = 15 b) MK = 32



a) b)

Fig. 5.6 IDCT image Baboon a) MK = 17 b) MK = 32

Table 1 shows middle length of code words of images encoded by BSAC and HC and also differences between middle lengths of code words.

TABLE I
DIFFERENCE BETWEEN MIDDLE LENGTH OF CODE WORD OF HC AND BSAC

| Image | | | Middle length of code word | | Difference between HC and BSAC | |
|---|---|---|---|---|---|---|
| Image | | Scale | BSAC bit/sc | HC bit/sc | Reduction of code word | Extension of code word |
| RBP | LENA | 15 | 1,7679 | 1,8800 | 0,1121 | - |
| | | 32 | 1,1489 | 1,4680 | 0,3192 | - |
| | BABBON | 17 | 2,3959 | 2,2130 | - | 0,1829 |
| | | 32 | 1,6004 | 1,6100 | 0,0096 | - |
| ABP | LENA | 15 | 1,7982 | 1,8800 | 0,0818 | - |
| | | 32 | 1,2082 | 1,4680 | 0,2598 | - |
| | BABBON | 17 | 2,4980 | 2,2130 | - | 0,2850 |
| | | 32 | 1,7526 | 1,6100 | - | 0,1426 |

From the table, it can be concluded that maximum saving is achieved by using BSAC aplicated on RBP for images with low frequency content therefore for an image with lot of monotone areas.

For an image with high frequency content, it is better to use conventional encoding, therefore Huffman encoding.

BSAC implicated on the image decomposed to ABP is possible, but it gets lower compression like application on RBP. From the table, it is also evident that with the increase of MK there is increasing compression in both encoding methods compression. This increase is stronger in BSAC than in HC. This is illustrated in table 2.

TABLE II
INCREASING OF COMPRESSION FOR BSAC AND HC WITH INCREASING OF SCALE OF QUANTIZATION

| | | Middle length of code word | | | Increasing of compression | | |
|---|---|---|---|---|---|---|---|
| | | BSAC | | HC bit/sc | HC | BSAC | |
| Image | Scale | RBP | ABP | | | ABP | RBP |
| LENA | 15 | 1,7679 | 1,7982 | 1,880 | | | |
| | 32 | 1,1489 | 1,2082 | 1,468 | 0,412 | 0,590 | 0,6191 |
| BABOON | 17 | 2,3959 | 2,4980 | 2,213 | | | |
| | 32 | 1,6004 | 1,7526 | 1,610 | 0,603 | 0,7454 | 0,7955 |

## VI. CONCLUSION

In the article, we discussed the modification of standard JPEG using arithmetic binary-state encoding applied on bit-planes of DCT image instead common used Huffman code. With experiments we arrive at the results which suggest that increased degree of compression for images with low frequency content. Conversely, this encoding doesn't achieve satisfactory results for images with high frequency content. It was found out that it is better to encode the real bit-plane of DCT image than absolute bit-plane. We achieved the best results using BSAC on image quantized with high MK. It can be inferred, that this modification of JPEG can be used, but it is necessary to add other algorithms which detect level of details of image and decides what kind of encoding to use. Another disadvantage is the necessary decomposition of the image to bit-plane and encoding of these using more difficult arithmetic code and a need to determine actual state and conditional probability. These disadvantages cause increased demands on hardware performance.

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# ADC test stand with exponential excitation signal using LabVIEW

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***Abstract*—The paper deals with design and implementation of the testing system for testing analogue-to-digital converters. The system itself takes advantage of exponential excitation signal and the programming environment LabVIEW. The main part of the paper is creation of the functions library (subroutines) which can be used not only within the final program, but also within further development and testing of the measuring method if needed. Measurements were done at chosen converters using the final program. The same converters were tested by standard testing method. The results acquired by both methods are compared to validate the above mentioned implementation of the testing method.**

***Keywords*—LabVIEW, AD convertor, testing, exponential stimulus**

## I. INTRODUCTION

Each AD (analog-digital) / DA (digital-analog) conversion deteriorates signal by additional errors. The basic requirement at application of AD or DA conversion is that these errors should be as small as possible.

Today's market offers a wide range of ADC's with high quality (with respect to their use). In their common applications it is not necessary to choose the "better" one. But if such a need occurs, it is necessary to use a method to do a qualitative analysis. In most cases, we get to the final INL (integral nonlinearity) graph of the converter.

In standard [7] a dynamic method for testing AD converters is described in order to determine their INL. This method is standardized and in our experiments, the results obtained with it will be considered as correct (reference). Of course, other methods of testing have been developed, each of which has its advantages and disadvantages [2]. At our department one such proposal of a test method is also developed. It is a dynamic histogram method, using an exponential bidirectional signal as a test stimulus. Initial proposals and experiments were published in [3]. This paper was focused on the generation of the exponential test signal. The final version of the proposed method is described in [4] and [1]. We implemented in our programs the mathematical procedures that were derived in [1].

Our goal was to develop software for test stand in form of library with subroutines allowing, if necessary, to be used in continued developing, or use them in other programs. The final program was tested on real ADC's in order to verify its functionality and metrological validity.

The paper is organized as follows: chapter II describes the theoretical basis of the measuring method and its mathematical apparatus. Chapter III is a description of the implementation and of the main programs. Chapter IV discusses measured results obtained from measurements with the standard method and the results obtained from the histogram method using exponential excitation signal. These are then compared.

## II. THEORETICAL FUNDAMENTS

The histogram test method with exponential test signal is derived from the histogram method described in the standards [7]. It is mainly focused on the determination of INL and DNL of ADC under test. The exponential signal occurs in "nature", so it is also easier to generate a good exponential test signal using common, components than to create high-quality harmonic signal. Therefore hardware implementation of the proposed method is simpler than the method described in the standards. Steps in the data processing are similar to the standard method:

- to generate a test signal
- to acquire a data record
- to build (calculate) a histogram from the record
- to determine the parameters of the test signal from the histogram
- to calculate the DNL and INL

### A. Description of the method

The signal, which is used to excite ADC under test is generated by following way: the DAC generates a square wave signal with 50% duty cycle, which is then integrated by the integrating circuit that produce the final exponential signal by the charging and discharging of integrating capacitor. Output dual slope exponential signal is used as excitation signal for the ADC under test (DUT). The principle of generation is shown in Fig. 1, and the generated excitation signal in Fig. 2. The mathematical representation of the signal is given by (1)

$$u_{in}(t) = \begin{cases} (F_2 - B_f)\cdot e^{\frac{t_1 - t}{\tau_f}} + B_f, \; for \; (t_1 < t < t_2) \\ B_r - (B_r - F_1)\cdot e^{\frac{t_3 - t}{\tau_r}}, \; for \; (t_3 < t < t_4) \end{cases} \quad (1)$$

where $F_1$ and $F_2$ are the minimum and maximum voltages of the ADC (DUT) input full scale range, $\tau_r$ *and* $\tau_f$ are the time constants of the exponential pulse, $B_f$ and $B_r$ are the final values of exponential signal for $t \to \infty$ for decreasing and increasing exponential part of the signal, respectively (i.e. the maximum and minimum voltage of the rectangular signal generated in the DAC), and $t_1$, $t_2$, $t_3$, $t_4$ are times when the signal crosses the ADC input range limits F1 or F2 (see Fig. 2).

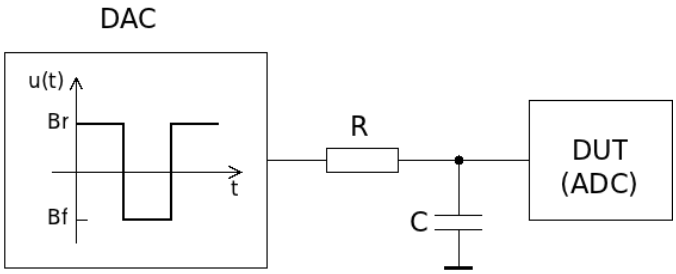


Fig. 1 Generation of the exponential test signal

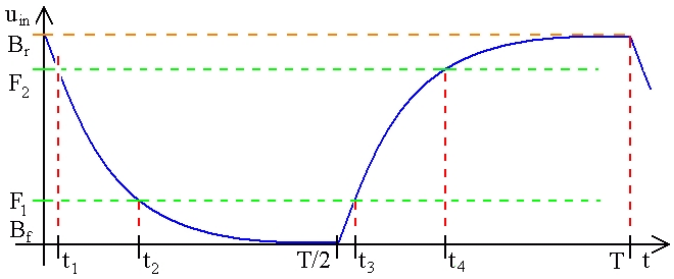


Fig. 2 Exponential excitation signal in time domain

To meet the requirements for quality of the exponentional signal, we need to fulfill only simple rules:

- generated rectangular signal must have short switching times between high and low level;
- capacitor C must be of high quality (dielectricum!), so that it does not cause any additional shape distortion of the generated signal.

The best capacitor for the integration circuit was selected on the basis of experiments performed in [3]. A capacitor with a polypropylene sheet type dielectric (No. MKP X2 SH) 470nF/275VAC from the company ARCOTRONICS was used. The resistor has negligible effect on the quality of the generated signal. We used an older type of carbon film resistor 80MJIT with a resistance of 82kΩ. It is appropriate to shield the entire integration circuit to achieve a good signal to noise ratio.

The record has to contain an integer number of signal periods. Then two independent histograms are calculated from the record for the rising and for the falling part of recorded signal. The histograms have to be normalized according to the following equation

$$H_n(i) = \frac{H(i)}{\sum_{l=0}^{2^N-1} H(l)}. \tag{2}$$

where $H(i)$ is a histogram calculated from the record.

### B. Model of the histogram

The INL and DNL can be computed from the measured and ideal histogram. For the ideal histogram we use a recurrent model introduced in [3]. It is defined as shown in (3), where $b$ is the only parameter we need to estimate. This is a great advantage of this recurrent histogram model. This model has also small errors as it was shown in [5] and is easy to compute, because we need to perform just basic arithmetical operations.

$$\hat{H}_{nid}(k) = \frac{\hat{S}}{k - \frac{1}{2} - b}, \quad \hat{S} = \frac{1}{\sum_{l=1}^{2^N-2} \frac{1}{l - \frac{1}{2} - b}}, \tag{3}$$

$$\hat{H}_{cnid}(k) = \sum_{i=1}^{k} \hat{H}_{nid}(i) = \sum_{i=1}^{k} \frac{\hat{S}}{i - \frac{1}{2} - b}.$$

### C. Excitation signal parameters estimation

The mail goal of this method is to estimate the parameters of the excitation signal from the measured histogram. Parameters that we need to estimate are the voltages in infinite time, separate for rising and falling part of the excitation signal ($b_r$, $b_f$). We achieve this by fitting measured data using the recurrent model. It is done by Newton's iteration algorithm that is used to minimize the cost function

$$\min(CF) = \min(\phi(b_r, b_f)) = \min\left(\sum_{i=1}^{2^N-2} (INL(i, b_r) - INL(i, b_f))^2\right) \tag{4}$$

where $\phi(b_r,b_f)$ is the cost function, and $b_r$ and $b_f$ are the unknown parameters. The INL and DNL are computed as

$$DNL(i, b_r) = \frac{H_{nr}(i) - H_{nrid}(i, b_r)}{H_{nrid}(i, b_r)} = \frac{H_{nr}(i)}{H_{nrid}(i, b_r)} - 1,$$
$$DNL(i, b_f) = \frac{H_{nf}(i) - H_{nfid}(i, b_f)}{H_{nfid}(i, b_f)} = \frac{H_{nf}(i)}{H_{nfid}(i, b_f)} - 1, \tag{5}$$
$$INL(i, b_r) = INL(i-1, b_r) + DNL(i, b_r),$$
$$INL(i, b_f) = INL(i-1, b_f) + DNL(i, b_f).$$

where $H_{nr}(i)$ a $H_{nf}(i)$ are the measured normalized histograms, and $b_r$, $b_f$ are the normalized parameters $B_f$, $B_r$. Because we do not take into account the actual voltage at the ADC input and record only codes from the ADC output (raw data) and also the calculations are made in code domain, we can assume that $b = B$.

The local minimum of the function (4) is given by

$$\frac{\partial \phi(b_r, b_f)}{\partial b_r} = 0, \quad \frac{\partial \phi(b_r, b_f)}{\partial b_f} = 0. \tag{6}$$

The Newton iteration process for this system of equations is given by (7). To simplify the calculations we don't use the exact values of the partial derivations needed in (7), but just their approximations with the corresponding Taylor series, when we suppose that $h_r \approx h_f \approx h$. They are not described here due to space limitations for this paper. You can find them in [1]. The STOP criterion is, according to [4], derived from assumption:

$$\varepsilon \approx h^3, h \approx \varepsilon^{1/3} \tag{8}$$

where $\varepsilon$ is the machine epsilon (it represents the round-off error for a floating-point number with a given precision) and $h$ is the increment. Finally the new parameters $b_r$ and $b_f$ are computed as shown in (9).

$$\begin{aligned}
&\frac{\partial^2\phi(b_r,b_f)}{\partial b_r\partial b_f}h_r+\frac{\partial^2\phi(b_r,b_f)}{\partial b_r\partial b_f}h_f=-\frac{\partial\phi(b_r,b_f)}{\partial b_r},\\
&\frac{\partial^2\phi(b_r,b_f)}{\partial b_r\partial b_f}h_r+\frac{\partial^2\phi(b_r,b_f)}{\partial b_r\partial b_f}h_f=-\frac{\partial\phi(b_r,b_f)}{\partial b_f},\\
&b_r^{[n]}=b_r^{[n-1]}+h_r,\quad b_f^{[n]}=b_f^{[n-1]}+h_f.
\end{aligned}\tag{7}$$

$$\begin{aligned}
b_r^{[n+1]}&=b_r^{[n]}-\frac{\frac{\partial\phi}{\partial b_r}\cdot\frac{\partial^2\phi}{\partial b_f^2}-\frac{\partial\phi}{\partial b_f}\cdot\frac{\partial^2\phi}{\partial b_r b_f}}{\Delta},\\
b_f^{[n+1]}&=b_f^{[n]}-\frac{\frac{\partial\phi}{\partial b_f}\cdot\frac{\partial^2\phi}{\partial b_r^2}-\frac{\partial\phi}{\partial b_r}\cdot\frac{\partial^2\phi}{\partial b_r b_f}}{\Delta},\\
\Delta&=\begin{vmatrix}\frac{\partial^2\phi}{\partial b_r^2} & \frac{\partial^2\phi}{\partial b_r b_f}\\ \frac{\partial^2\phi}{\partial b_r b_f} & \frac{\partial^2\phi}{\partial b_f^2}\end{vmatrix}=\frac{\partial^2\phi}{\partial b_r^2}\cdot\frac{\partial^2\phi}{\partial b_f^2}-\left(\frac{\partial^2\phi}{\partial b_r b_f}\right)^2.
\end{aligned}\tag{9}$$

The STOP criterion of the iteration process is $\left|b_i^{[n+1]}-b_i^{[n]}\right|\le\varepsilon_i$, where $\varepsilon_i$ in (8) is the chosen residual uncertainty. The final $b_r^{[n+1]}, b_f^{[n+1]}$ are used to calculate $DNL_r(k)$, $DNL_f(k)$, $INL_r(k)$ a $INL_f(k)$ of the tested ADC using (5). The final INL and DNL (i. e. main result) is calculated as

$$\begin{aligned}
DNL(k)&=\frac{DNL_r(k)+DNL_f(k)}{2},\\
INL(k)&=\frac{INL_r(k)+INL_f(k)}{2}.
\end{aligned}\tag{10}$$

## III. Implementation of the Method

The generator was built on multifunction DAQ card PCI-6289 with the termination unit BNC-2120 by NI. The integration circuit was shielded with a metal box. All connections were realized by coaxial cables.

Two separate software routines VI (Virtual Instruments, programs in LabVIEW, see [6]) were developed. One VI collected data and calculated histograms. The other VI performed analysis and final calculations of the DNL and INL. The programs communicated using two files contain separated histograms for the rising and falling exponential signal slopes.

### A. Program MEASURE.VI

This program enables setting test conditions, such as sample rate, Hi and Lo levels of the generated square wave, etc. The program shows in real time the collected histograms as they grow and automatically stops the data collecting after achieving the required number of samples (or after the user presses the STOP button).

### B. Program ANALYZE.VI

This is the main program for this method. It performs fitting of the model histogram and calculates the final INL. The main parts of it are the output graph windows. It can also save the results in a specified file.

The complete documentation of these programs, including screenshots of the GUIs and the source code is in [1].

## IV. Experimental Results

To test the new implementation in LabVIEW and to verify its metrological performance we have performed a number of tests on real ADCs. The results have been compared with reference results acquired by the standardized histogram test method using the precise generator STANFORD DS360 and software developed in [3]. Because of space limitations we show here only test results of the following tested ADCs: USB6009 (14bit), ADC0804LCN (8bit). Test conditions are briefly described in the following figures captions.

### A. USB6009

It is an external measurement card from NI, with a USB connection. The Fig. 5 shows the difference between the reference result, and the result obtained by the new method.

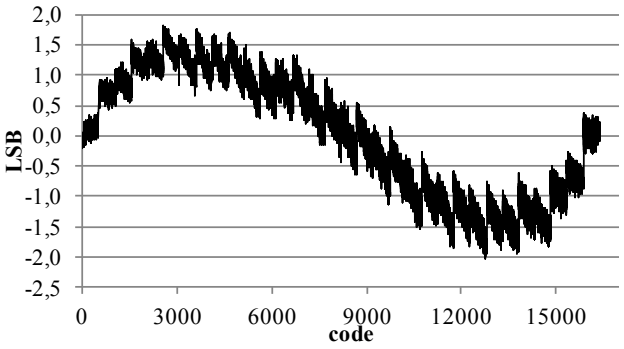


Fig. 3 INL of USB6009 using standardized method (frequency of excitation signal: 111.111Hz, resolution: 14bit, input range: ±1V, sampling rate: 48 000Ss, # of samples in record: $8\times10^6$)

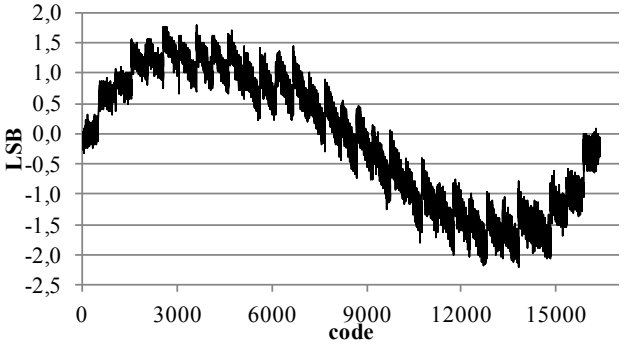


Fig. 4 INL of USB6009 using the discussed method (frequency of excitation signal: 23.5Hz, resolution: 14bit, input range: ±1V, sampling rate: 48 000Ss, # of samples in record: $8\times10^6$)

The theoretical maximal difference shown in Fig. 5 according to the number of samples in record should be 0.6LSB (according to [3]). The requirement is accomplished, what is a positive proof of the validity of the discussed method.

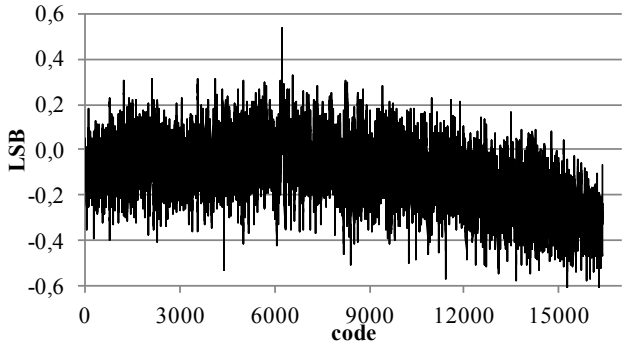


Fig. 5 Difference of INLs in Fig. 4 and Fig. 3

### B. ADC0804LCN

It is one chip ADC. The connection to the PC and whole setup was made according to [8]. Fig. 8 shows the difference between the reference result and the result obtained by the new method.

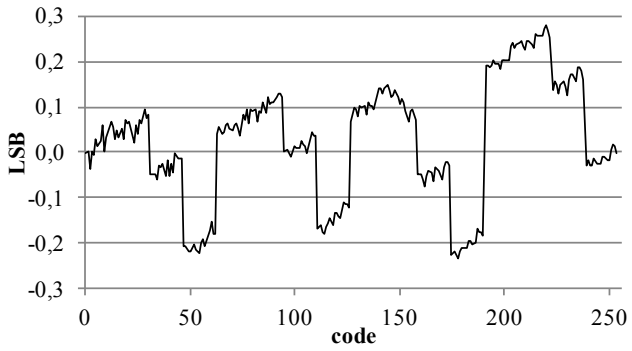


Fig. 6 INL of ADC0804LCN using standardized method (frequency of excitation signal: 111.111Hz, resolution: 8bit, input range: 0÷5V, sampling rate: 8 110Ss, # of samples in record: $2\times10^6$)

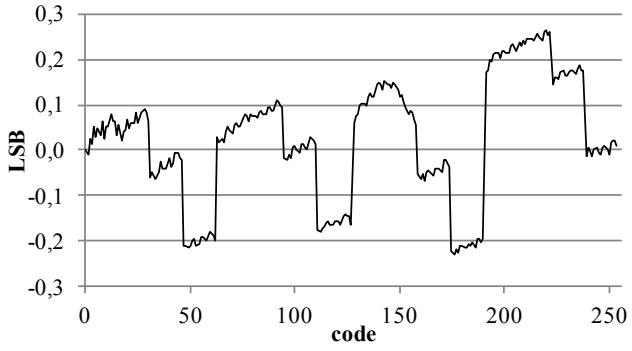


Fig. 7 INL of ADC0804LCN using the discussed method (frequency of excitation signal: 16.5Hz, resolution: 8bit, input range: 0÷5V, sampling rate: 8 110Ss, # of samples in record: $2\times10^6$)

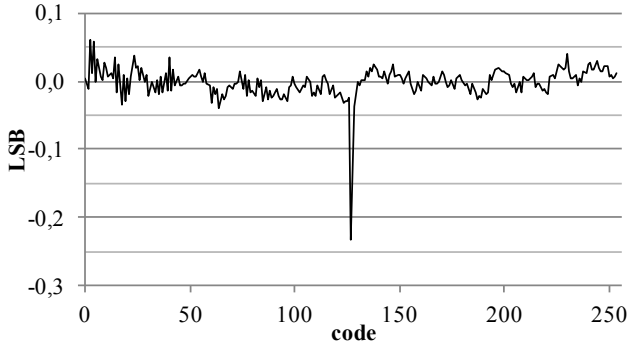


Fig. 8 Difference of INLs in Fig. 7 and Fig. 6

This ADC had the biggest difference in the acquired INLs in the code 127. This difference exceeds the theoretical measurement inaccuracy that should be max. 0.12LSB. The code 127 of this ADC appears to have a build-in/construction error because the same effect was observed also in earlier experiments, including static tests.

The differences of INLs shown in Fig. 5 and Fig. 8 have a noise-like character, what proofs, that there is no systematic error interleaved into the testing, and the difference is caused just due statistic uncertainty of both test methods.

## V. Conclusion

This method has great potential, because using the methods described in the standards it is already unrealistic to test present high-resolution ADC. The development of new testing methods is therefore necessary.

In the future we would like to modify the GUI of the main program. Another desired modification of the program for obtaining histograms is that it should automatically recognize the format of the raw data obtained from the tested ADC. The comfort of the operating personnel would improve, if the program ANALYZE.VI had an algorithm that guaranteed even without entering the initial *Bf*, *Br*, that the program returned a result. Due to problems with convergence of the proposed minimization in the test method it is sometimes necessary to repeatedly change the initial value of *Bf*, *Br* to get the right results.

## Acknowledgment

This work is the result of the project implementation: Development of the Center of Information and Communication Technologies for Knowledge Systems (ITMS project code: 26220120030) supported by the Research & Development Operational Program funded by the ERDF.

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# A Novel Multiphase Boost Converter with High Efficiency of Energy Conversion

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***Abstract* — This article introduce a novel concept of boost converter with high efficiency of energy conversion. This new concept allows effective utilization of energy from photovoltaic solar cell. The effective utilization of energy is ensured by adding five parallel legs to the conventional boost converter with one leg. The simulation model has been built and the simulation results obtained to verify the theoretical properties of multiphase boost converter.**

***Keywords* — multiphase boost converter, photovoltaic, SLPS interface, energy conversion, CCM mode**

## I. INTRODUCTION

This paper presents the novel concept of multiphase boost converter with high efficiency of energy conversion. The high efficiency of energy conversion is ensured by adding five more parallel legs to the conventional boost converter with one leg. The suitable algorithm of switches control in particular legs ensures that the almost whole PV output energy from the PV panel is effective utilized.

## II. EFFICIENCY OF ENERGY CONVERSION

Fig.1. explains the problem of efficiency of energy conversion. The impinging sun energy $P_{INsun}$ is converted by PV module direct to the electric energy. According to the material which PV module is build this conversion efficiency moving from 5% (a-Si) to 30% (GaAs), [1]. The output PV energy $P_{OUT\_PV}$ equals the input energy to the converter $P_{IN\_con}$.

$$P_{OUT\_PV} = P_{IN\_con} \tag{1}$$

Only a part of this input energy $P_{IN\_con}$ is drawn by the converter system. The converter works in switching mode with any set value of duty cycle *z*. According to the set value of duty cycle *z*, the real amount of input energy to the converter is

$$P_{IN\_con}{}^{*} = P_{IN\_con}.z \tag{2}$$

It can be seen that the real amount of input energy to the converter $P_{IN\_con}{}^{*}$ is less that the $P_{IN\_con}$ because the duty cycle *z* is theoretically moving from 0 to 1.

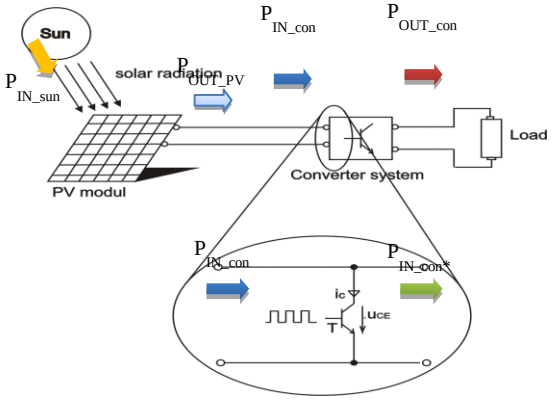


Fig. 1. Overview at efficiency of energy conversion.

The three different efficiencies we can define as:

The conversion efficiency of PV module

$$\eta_{PV} = \frac{P_{OUT\_PV}}{P_{IN\_sun}} \tag{3}$$

The converter efficiency

$$\eta_{con} = \frac{P_{OUT\_con}}{P_{IN\_conv}{}^{*}} \tag{4}$$

The efficiency of energy conversion

$$\eta_{E} = \frac{P_{OUT\_con}}{P_{OUT\_PV}} \tag{5}$$

where $P_{OUT\_con}$ is the output converter energy.

Nowadays, the efficiency of the soft switching DC/DC converters $\eta_{con}$ is very well. It is moving around the 97%. But on the other hand the efficiency of energy conversion $\eta_E$ is in comparison with converter efficiency $\eta_{con}$ much lower. This fact belongs between one of major factor of long-term energy recovery and high cost of PV modules. One way to reduce the long –term energy recovery and so high cost of PV cells is proposed multiphase boost converter which ensures the

equality of converter efficiency $\eta_{con}$ and the efficiency of energy conversion $\eta_E$.

## III. THE PROPOSED CONCEPT OF MULTIPHASE BOOST CONVERTER

The proposed topology of multiphase boost converter is in fig.2. The multiphase boost converter has, in comparison with the conventional boost converter with one leg, five more parallel legs with five inductors ($L_2$ - $L_6$), five rectifier diodes ($D_{21}$ - $D_{61}$) and five switches ($S_{21}$ – $S_{61}$). There are also six auxiliary switches $S_{12}$ – $S_{62}$ on the converter input. The auxiliary switches $S_{12}$ – $S_{62}$ ensure the connection of the input voltage $U_{IN}$ to the load $Z$. The topology of multiphase converter is also complemented by six auxiliary diodes $D_{12}$ – $D_{62}$ which serve as freewheeling diodes. The freewheeling diodes $D_{12}$ – $D_{62}$ return the inductor storage energy $W_{L1}$ – $W_{L6}$ back to the load $Z$ after the particular complementarily switches $S_{a1}$ – $S_{a2}$ are turned off (where a $\in$ <1 - 6>).

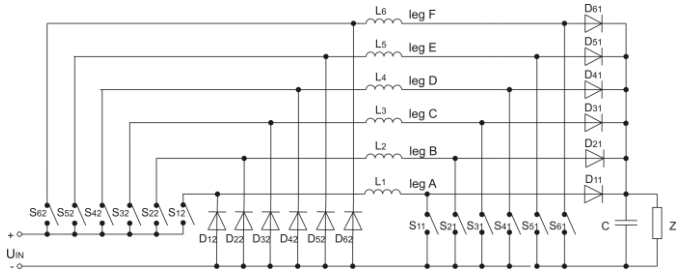


Fig. 2. Multiphase boost converter.

## IV. PRINCIPLE OF OPERATION

The proposed multiphase boost converter has 6 operating cycles within each period. The corresponding operation waveforms are shown in fig.3.

***Mode 1 ($t_0$–$t_1$):*** The switches $S_{11}$ and $S_{12}$ (leg A) are turned on at the time $t_0$. The energy in form of magnetic field begins to accumulate in inductor $L_1$. The diode $D_{12}$ is reverse biased so the whole input current is closed in loop $+U_{IN}$ –$S_{12}$ – $L_1$ – $S_{11}$ – $-U_{IN}$. In this mode the switches $S_{51}$, $S_{52}$ (leg E) and $S_{61}$, $S_{62}$ (leg F) are in on-state. The input energy is delivering to the inductor $L_5$ and $L_6$ in particular legs, too. The switches $S_{21}$, $S_{22}$ (leg B) and $S_{31}$, $S_{32}$ (leg C) are in off-state. The inductor energy $W_{L2}$ and $W_{L3}$ is delivered through diodes $D_{21}$ and $D_{31}$ to the load $Z$. The equivalent equations are:

The inductor voltages $u_{L1}(t)$, $u_{L5}(t)$ and $u_{L6}(t)$ are

$$u_{L1}(t) = u_{L5}(t) = u_{L6}(t) = U_{IN} = L_{1(5,6)} \frac{di_{L1(5,6)}(t)}{dt} \qquad (6)$$

The inductor voltage $u_{L2}(t)$, $u_{L3}(t)$ and $u_{L4}(t)$ are

$$u_{L2}(t) = u_{L3}(t) = u_{L4}(t) = -U_{OUT} = L_{2(3,4)} \frac{di_{L2(3,4)}(t)}{dt} \qquad (7)$$

The currents flow through inductors $L_1$, $L_5$, $L_6$ and co-operating switches $S_{11}$ - $S_{12}$, $S_{51}$ – $S_{52}$, $S_{61}$ – $S_{62}$ are

$$\begin{aligned} &i_{S11}(t) = i_{S12}(t) = i_{S51}(t) = i_{S52}(t) = i_{S61}(t) = \\ &i_{S62}(t) = i_{L1}(t) = i_{L5}(t) = i_{L6}(t) = \\ &\frac{1}{L_{1(5,6)}} \int_{t0}^{t1} u_{L1(5,6)}(t)dt + I_{L1(5,6)}(t_0) = \\ &\frac{U_{IN}}{L_{1(5,6)}} (t_1 - t_0) + I_{L1(5,6)}(t_0) \end{aligned} \qquad (8)$$

The currents flow through inductors $L_2$, $L_3$, $L_4$ and couple of diodes $D_{21}$ – $D_{22}$, $D_{31}$ – $D_{32}$, $D_{41}$ – $D_{42}$ are

$$\begin{aligned} &i_{D21}(t) = i_{D22}(t) = i_{D31}(t) = i_{D32}(t) = i_{D41}(t) = \\ &i_{D42}(t) = i_{L2}(t) = i_{L3}(t) = i_{L4}(t) = \\ &\frac{1}{L_{2(3,4)}} \int_{t0}^{t1} u_{L2(3,4)}(t)dt + I_{L2(3,4)}(t_0) = \\ &-\frac{U_{OUT}}{L_{2(3,4)}} (t_1 - t_0) + I_{L2(3,4)}(t_0) \end{aligned} \qquad (9)$$

The inductor current $i_{L1}(t)$ exponentially increase from initial value $I_{L1}$ to the maximum value $I_{L1max}$ (reached at the time $t_3$) with time constant $\tau_1 = L_1/R$.

*Mode 2 ($t_1$–$t_2$)* and *mode 3 ($t_2$–$t_3$)* are the same as *mode1*. Only another co-operating switches $S_{21}$ - $S_{22}$ (leg B, *mode 2*) and $S_{31}$ - $S_{32}$ (leg C, *mode 3*) are turned on, on-state $S_{11}$, $S_{12}$, $S_{61}$, $S_{62}$ (leg A and leg F, *mode 2*) and $S_{11}$ – $S_{12}$, $S_{21}$ – $S_{22}$ (legs A and B, *mode 3*) and off-state $S_{41}$ – $S_{42}$, $S_{51}$ – $S_{52}$ (legs D and E, *mode 3*) and $S_{31}$, $S_{32}$, $S_{41}$, $S_{42}$ (leg D and leg C, *mode 2*). The corresponding equations are the same. Only subscript are changed.

***Mode 4 ($t_3$–$t_4$):*** The switches $S_{11}$ and $S_{12}$ are turned off and $S_{41}$ and $S_{42}$ are turned on the beginning of this mode at the time $t_3$. The inductor energy $W_{L1}$ begins to deliver through diode $D_{11}$ to the load $Z$. The polarity of inductor voltage $u_{L1}(t)$ is reversed so the diode $D_{12}$ is in on-state. The output current $i_Z(t)$ is enclosed in the loop $L_1$ – $D_{11}$ – $Z$ – $D_{12}$. The switches $S_{21}$, $S_{22}$ (leg B) and $S_{31}$, $S_{32}$ (leg C) are on-state and the input energy is delivering to the inductor $L_2$ and $L_3$. The switches $S_{51}$, $S_{52}$ (leg E) and $S_{61}$, $S_{62}$ (leg F) are in off-state. The inductor energy $W_{L5}$ and $W_{L6}$ is delivered through diodes $D_{51}$ and $D_{61}$ to the load $Z$. The equivalent equations are:

The inductor voltages $u_{L4}(t)$, $u_{L2}(t)$ and $u_{L3}(t)$ are

$$u_{L4}(t) = u_{L2}(t) = u_{L3}(t) = U_{IN} = L_{4(2,3)} \frac{di_{L4(2,3)}(t)}{dt} \qquad (10)$$

The inductor voltages $u_{L1}(t)$, $u_{L5}(t)$ and $u_{L6}(t)$ are

$$u_{L1}(t) = u_{L5}(t) = u_{L6}(t) = -U_{OUT} = L_{1(5,6)} \frac{di_{L1(5,6)}(t)}{dt} \qquad (11)$$

The currents flow through inductors $L_4$, $L_2$, $L_3$ and co-operating switches $S_{41} – S_{42}$, $S_{21} – S_{22}$, $S_{31} – S_{32}$ are

$$\begin{aligned} &i_{S41}(t) = i_{S42}(t) = i_{S21}(t) = i_{S22}(t) = i_{S31}(t) = \\ &i_{S32}(t) = i_{L4}(t) = i_{L2}(t) = i_{L3}(t) = \\ &\frac{1}{L_{4(2,3)}} \int_{t3}^{t4} u_{L4(2,3)}(t)dt + I_{L4(2,3)}(t_3) = \\ &\frac{U_{IN}}{L_{4(2,3)}} (t_4 - t_3) + I_{L4(2,3)}(t_3) \end{aligned} \quad (12)$$

The currents flow through inductors $L_1$, $L_5$, $L_6$ and couple of diodes $D_{11} – D_{12}$, $D_{51} – D_{52}$, $D_{61} – D_{62}$ are

$$\begin{aligned} &i_{D11}(t) = i_{D12}(t) = i_{D51}(t) = i_{D52}(t) = i_{D61}(t) = \\ &i_{D62}(t) = i_{L1}(t) = i_{L5}(t) = i_{L6}(t) = \\ &\frac{1}{L_{1(5,6)}} \int_{t3}^{t4} u_{L1(5,6)}(t)dt + I_{L1(5,6)}(t_3) = \\ &-\frac{U_{OUT}}{L_{1(5,6)}} (t_4 - t_3) + I_{L1(5,6)}(t_3) \end{aligned} \quad (13)$$

*Mode 5* ($t_4$–$t_5$) and *mode 6* ($t_5$–$t_6$) are the same as *mode4*. Only another co-operate switches $S_{61} – S_{62}$ (leg F, *mode 6*) and $S_{51}$ - $S_{52}$ (leg E, *mode 5*) are turned on, on-state $S_{31}$, $S_{32}$, $S_{41}$, $S_{42}$ (leg C and leg D, *mode 5*) and $S_{41} – S_{42}$, $S_{51} – S_{52}$ (legs D and E, *mode 6*) and off-state $S_{11} – S_{12}$, $S_{21} – S_{22}$ (legs A and B, *mode 6*) and $S_{11}$, $S_{12}$, $S_{61}$, $S_{62}$ (leg A and leg F, *mode 5*). The corresponding equations are the same. Only subscript are changed.

If we assume that the average value inductor voltage $U_{L(AV)}$ has to be zero for period $T$, equation (14), then the average value of the output voltage $U_{OUT(AV)}$ of proposed topology of boost converter in CCM can be easily derived.

$$U_{L(AV)} = \frac{1}{T} \int_0^T u_L(t)dt = 0 \quad (14)$$

The average value of the output voltage $U_{OUT(AV)}$ of proposed topology of multiphase boost converter in CCM.

$$U_{OUT(AV)} = \frac{z}{1-z} U_{IN}. \quad (15)$$

It is clear that the minimum setting of value for duty cycle $z$ has to be 0,5 respectively 50% of period $T$. If the value of duty cycle $z$ is less that the 0,5 than the average value of the output voltae $U_{OUT(AV)}$ will be smaller than the input voltage $U_{IN}$. The function of multiphase boost converter will be incorrect in this case.

## V. Simulation Results

The simulation model of multiphase boost converter shown in fig.4 was created in simulation environment OrCAD Capture CSI to verify its theoretical properties.

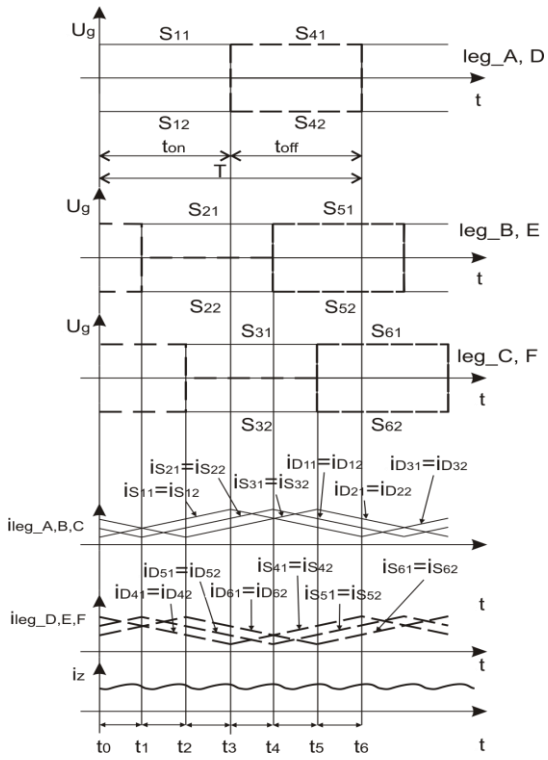


Fig. 3. Theoretical waveforms of proposed multiphase boost converter.

Parameters:

| | |
|---|---|
| Switching frequency | $f_S$ = 50 kHz, |
| output voltage | $U_{bat}$ = 14V, |
| input voltage | $U_{PV}$ = 10V, |
| inductance | $L_1 = L_2 = L_3 = L_4 = L_5 = L_6$ = 50uH, |
| capacitance | C = 22uF |
| duty cycle | z = 0,6. |

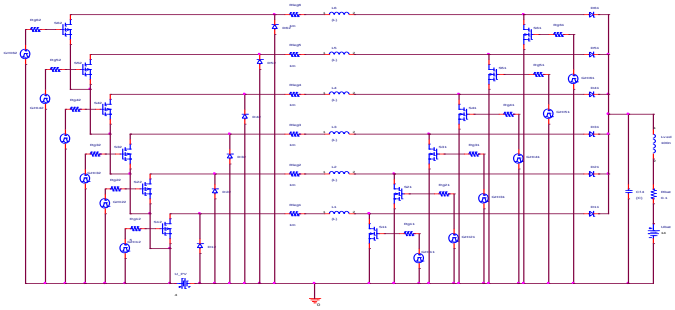

Fig.4. Simulation model of proposed multiphase boost converter.

Fig.5. shows the inductor currents $i_{L1}(t)$ - $i_{L6}(t)$, diode currents $i_{D11}(t)$, $i_{D12}(t)$ - $i_{D61}(t)$, $i_{D62}(t)$ and transistor currents $i_{S11}(t)$, $i_{S12}(t)$ - $i_{S61}(t)$, $i_{S62}(t)$ in particular legs. It can be seen that after turning on co-operating transistors in given leg the inductor begins to accumulate energy in form of magnetic field. This energy is consequently delivered to the load $Z$ till these couples of transistors are turned-off.

Control structure created in Simulink environment is shown in fig.6. On this purpose the PSpice SLPS (SimuLink PSpice) simulation environment, supports the substitution of

an actual Simulink block with an equivalent analog PSpice electrical circuit, was used.

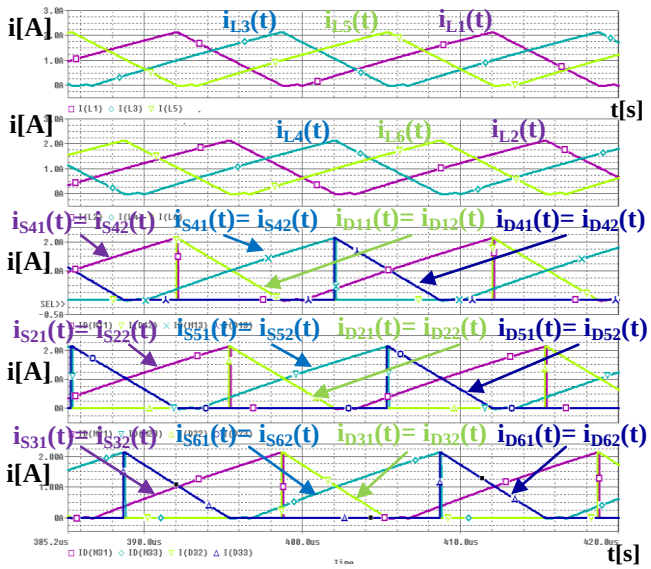


Fig.5. Waveforms of inductor currents $i_{L1}(t)$ till $i_{L6}$(t), diode currents $i_{D11}(t)$, $i_{D12}(t)$ till $i_{D61}(t)$, $i_{D62}(t)$ and transistor currents $i_{S11}(t)$, $i_{S12}(t)$ till $i_{S11}(t)$, $i_{S12}(t)$.

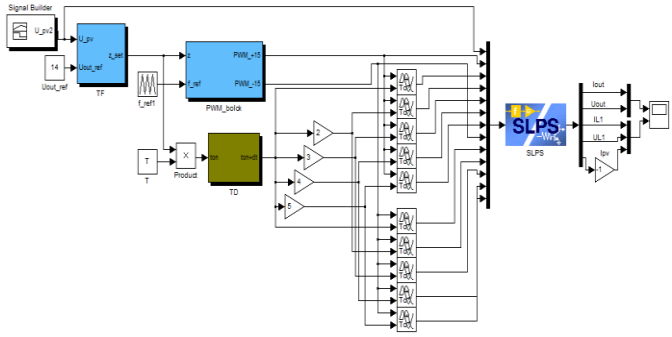


Fig.6. Simulink model of control structure of six phase boost converter.

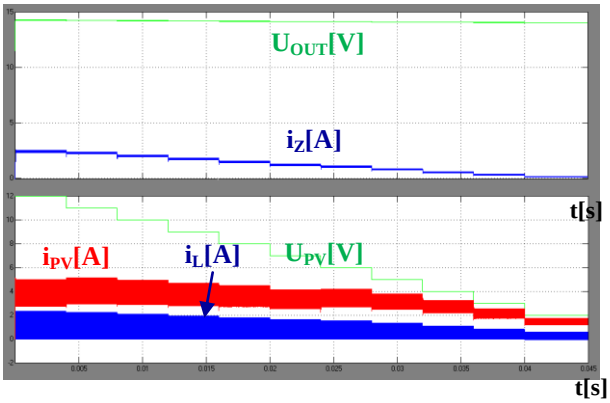


Fig.7. Waveforms of load current $i_Z(t)$, output voltage $U_{OUT}$ (upper part), inductor and PV currents $i_{PV}(t)$ and $i_L(t)$ and PV voltage (lower part).

Fig.7. shows overview of load current $i_Z(t)$, inductor current $i_L(t)$, input photovoltaic current $i_{PV}(t)$, input and output voltage $u_{out}(t)$ at different values of photovoltaic voltage $U_{PV}$. The PV voltage is moving in range from 12V to 2V, with decrement 1V. In comparison with conventional boost converter with one leg the load current $i_Z(t)$ works in CCM for whole range of input voltages $U_{PV}$ including the minimum value $U_{PV}$ = 2V, Fig.8.

The extended waveforms of inductor current $i_L(t)$, load current $i_Z(t)$ and photovoltaic current $i_{PV}(t)$ are shown in fig.9. The peak-to-peak values of load ripple current $\Delta i_Z$ are very small for whole range of input PV voltage $U_{PV}$. The peak-to-peak values of load ripple current $\Delta i_Z$ is moving around = 150 mA .

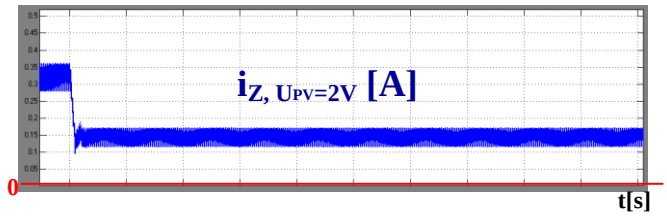


Fig.8. Load current $i_Z(t)$.

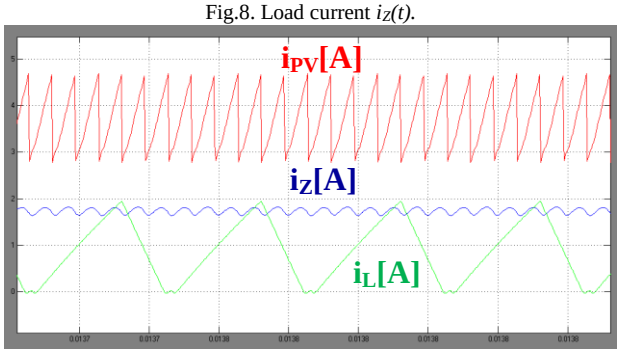


Fig.9. Extended waveforms of inductor current $i_L(t)$, load current $i_Z(t)$ and photovoltaic current $i_{PV}(t)$.

## VI. Conclusion

The simulation results confirm the theoretical assumes. The efficiency of energy conversion of proposed multiphase converter is very high because the output PV energy is continually delivered to the load by means of six phases of multiphase converter. This new concept of proposed converter ensures utilization of the full range of energy supplied from the PV module.

## Acknowledgment

The paper has been prepared under support of Slovak grant projects KEGA No. 005TUKE-4/2012, KEGA No.024TUKE-4/2012 and VEGA No. 1/0559/12.

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Published: Faculty of Electrical Engineering and Informatics
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I. Edition, 440 pages

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**ISBN 978-80-553-0943-9**