ADC test stand with exponential excitation signal using LabVIEW

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***Abstract*—The paper deals with design and implementation of the testing system for testing analogue-to-digital converters. The system itself takes advantage of exponential excitation signal and the programming environment LabVIEW. The main part of the paper is creation of the functions library (subroutines) which can be used not only within the final program, but also within further development and testing of the measuring method if needed. Measurements were done at chosen converters using the final program. The same converters were tested by standard testing method. The results acquired by both methods are compared to validate the above mentioned implementation of the testing method.**

***Keywords*—LabVIEW, AD convertor, testing, exponential stimulus**

I. INTRODUCTION

Each AD (analog-digital) / DA (digital-analog) conversion deteriorates signal by additional errors. The basic requirement at application of AD or DA conversion is that these errors should be as small as possible.

Today's market offers a wide range of ADC's with high quality (with respect to their use). In their common applications it is not necessary to choose the "better" one. But if such a need occurs, it is necessary to use a method to do a qualitative analysis. In most cases, we get to the final INL (integral nonlinearity) graph of the converter.

In standard [7] a dynamic method for testing AD converters is described in order to determine their INL. This method is standardized and in our experiments, the results obtained with it will be considered as correct (reference). Of course, other methods of testing have been developed, each of which has its advantages and disadvantages [2]. At our department one such proposal of a test method is also developed. It is a dynamic histogram method, using an exponential bidirectional signal as a test stimulus. Initial proposals and experiments were published in [3]. This paper was focused on the generation of the exponential test signal. The final version of the proposed method is described in [4] and [1]. We implemented in our programs the mathematical procedures that were derived in [1].

Our goal was to develop software for test stand in form of library with subroutines allowing, if necessary, to be used in continued developing, or use them in other programs. The final program was tested on real ADC's in order to verify its functionality and metrological validity.

The paper is organized as follows: chapter II describes the theoretical basis of the measuring method and its mathematical apparatus. Chapter III is a description of the implementation and of the main programs. Chapter IV discusses measured results obtained from measurements with the standard method and the results obtained from the histogram method using exponential excitation signal. These are then compared.

II. THEORETICAL FUNDAMENTS

The histogram test method with exponential test signal is derived from the histogram method described in the standards [7]. It is mainly focused on the determination of INL and DNL of ADC under test. The exponential signal occurs in "nature", so it is also easier to generate a good exponential test signal using common, components than to create high-quality harmonic signal. Therefore hardware implementation of the proposed method is simpler than the method described in the standards. Steps in the data processing are similar to the standard method:

- to generate a test signal
- to acquire a data record
- to build (calculate) a histogram from the record
- to determine the parameters of the test signal from the histogram
- to calculate the DNL and INL

A. Description of the method

The signal, which is used to excite ADC under test is generated by following way: the DAC generates a square wave signal with 50% duty cycle, which is then integrated by the integrating circuit that produce the final exponential signal by the charging and discharging of integrating capacitor. Output dual slope exponential signal is used as excitation signal for the ADC under test (DUT). The principle of generation is shown in Fig. 1, and the generated excitation signal in Fig. 2. The mathematical representation of the signal is given by (1)

$$u_{in}(t) = \begin{cases} (F_2 - B_f)\cdot e^{\frac{t_1 - t}{\tau_f}} + B_f, \; for \; (t_1 < t < t_2) \\ B_r - (B_r - F_1)\cdot e^{\frac{t_3 - t}{\tau_r}}, \; for \; (t_3 < t < t_4) \end{cases} \quad (1)$$

where F_1 and F_2 are the minimum and maximum voltages of the ADC (DUT) input full scale range, τ_r *and* τ_f are the time constants of the exponential pulse, B_f and B_r are the final values of exponential signal for $t \to \infty$ for decreasing and increasing exponential part of the signal, respectively (i.e. the maximum and minimum voltage of the rectangular signal generated in the DAC), and t_1, t_2, t_3, t_4 are times when the signal crosses the ADC input range limits F1 or F2 (see Fig. 2).

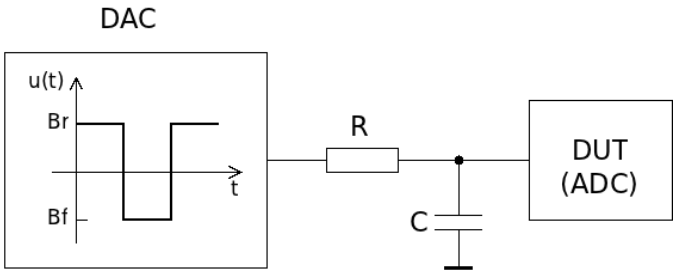

Fig. 1 Generation of the exponential test signal

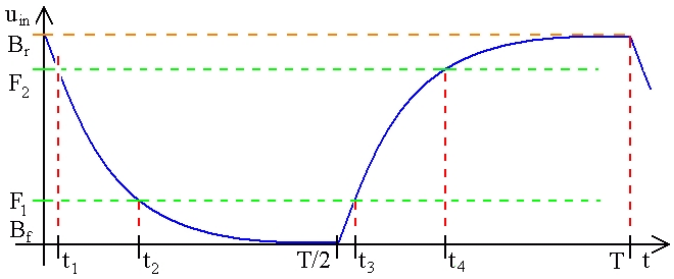

Fig. 2 Exponential excitation signal in time domain

To meet the requirements for quality of the exponentional signal, we need to fulfill only simple rules:

- generated rectangular signal must have short switching times between high and low level;
- capacitor C must be of high quality (dielectricum!), so that it does not cause any additional shape distortion of the generated signal.

The best capacitor for the integration circuit was selected on the basis of experiments performed in [3]. A capacitor with a polypropylene sheet type dielectric (No. MKP X2 SH) 470nF/275VAC from the company ARCOTRONICS was used. The resistor has negligible effect on the quality of the generated signal. We used an older type of carbon film resistor 80MJIT with a resistance of 82kΩ. It is appropriate to shield the entire integration circuit to achieve a good signal to noise ratio.

The record has to contain an integer number of signal periods. Then two independent histograms are calculated from the record for the rising and for the falling part of recorded signal. The histograms have to be normalized according to the following equation

$$H_n(i) = \frac{H(i)}{\sum_{l=0}^{2^{N-1}} H(l)}. \tag{2}$$

where $H(i)$ is a histogram calculated from the record.

B. Model of the histogram

The INL and DNL can be computed from the measured and ideal histogram. For the ideal histogram we use a recurrent model introduced in [3]. It is defined as shown in (3), where b is the only parameter we need to estimate. This is a great advantage of this recurrent histogram model. This model has also small errors as it was shown in [5] and is easy to compute, because we need to perform just basic arithmetical operations.

$$\hat{H}_{nid}(k) = \frac{\hat{S}}{k - \frac{1}{2} - b}, \quad \hat{S} = \frac{1}{\sum_{l=1}^{2^N-2} \frac{1}{l - \frac{1}{2} - b}}, \qquad \hat{H}_{cnid}(k) = \sum_{i=1}^{k} \hat{H}_{nid}(i) = \sum_{i=1}^{k} \frac{\hat{S}}{i - \frac{1}{2} - b}. \tag{3}$$

C. Excitation signal parameters estimation

The mail goal of this method is to estimate the parameters of the excitation signal from the measured histogram. Parameters that we need to estimate are the voltages in infinite time, separate for rising and falling part of the excitation signal (b_r, b_f). We achieve this by fitting measured data using the recurrent model. It is done by Newton's iteration algorithm that is used to minimize the cost function

$$\min(CF) = \min(\phi(b_r, b_f)) = \min\left(\sum_{i=1}^{2^N-2} (INL(i, b_r) - INL(i, b_f))^2\right) \tag{4}$$

where $\phi(b_r,b_f)$ is the cost function, and b_r and b_f are the unknown parameters. The INL and DNL are computed as

$$DNL(i, b_r) = \frac{H_{nr}(i) - H_{nrid}(i, b_r)}{H_{nrid}(i, b_r)} = \frac{H_{nr}(i)}{H_{nrid}(i, b_r)} - 1,$$
$$DNL(i, b_f) = \frac{H_{nf}(i) - H_{nfid}(i, b_f)}{H_{nfid}(i, b_f)} = \frac{H_{nf}(i)}{H_{nfid}(i, b_f)} - 1, \tag{5}$$
$$INL(i, b_r) = INL(i-1, b_r) + DNL(i, b_r),$$
$$INL(i, b_f) = INL(i-1, b_f) + DNL(i, b_f).$$

where $H_{nr}(i)$ a $H_{nf}(i)$ are the measured normalized histograms, and b_r, b_f are the normalized parameters B_f, B_r. Because we do not take into account the actual voltage at the ADC input and record only codes from the ADC output (raw data) and also the calculations are made in code domain, we can assume that $b = B$.

The local minimum of the function (4) is given by

$$\frac{\partial \phi(b_r, b_f)}{\partial b_r} = 0, \quad \frac{\partial \phi(b_r, b_f)}{\partial b_f} = 0. \tag{6}$$

The Newton iteration process for this system of equations is given by (7). To simplify the calculations we don't use the exact values of the partial derivations needed in (7), but just their approximations with the corresponding Taylor series, when we suppose that $h_r \approx h_f \approx h$. They are not described here due to space limitations for this paper. You can find them in [1]. The STOP criterion is, according to [4], derived from assumption:

$$\varepsilon \approx h^3, h \approx \varepsilon^{1/3} \tag{8}$$

where ε is the machine epsilon (it represents the round-off error for a floating-point number with a given precision) and h is the increment. Finally the new parameters b_r and b_f are computed as shown in (9).

$$\begin{aligned}
&\frac{\partial^2\phi(b_r,b_f)}{\partial b_r \partial b_f}h_r + \frac{\partial^2\phi(b_r,b_f)}{\partial b_r \partial b_f}h_f = -\frac{\partial\phi(b_r,b_f)}{\partial b_r},\\
&\frac{\partial^2\phi(b_r,b_f)}{\partial b_r \partial b_f}h_r + \frac{\partial^2\phi(b_r,b_f)}{\partial b_r \partial b_f}h_f = -\frac{\partial\phi(b_r,b_f)}{\partial b_f},\\
&b_r^{[n]} = b_r^{[n-1]} + h_r, \quad b_f^{[n]} = b_f^{[n-1]} + h_f .
\end{aligned} \tag{7}$$

$$\begin{aligned}
b_r^{[n+1]} &= b_r^{[n]} - \frac{\frac{\partial\phi}{\partial b_r}\cdot\frac{\partial^2\phi}{\partial b_f^2} - \frac{\partial\phi}{\partial b_f}\cdot\frac{\partial^2\phi}{\partial b_r b_f}}{\Delta},\\
b_f^{[n+1]} &= b_f^{[n]} - \frac{\frac{\partial\phi}{\partial b_f}\cdot\frac{\partial^2\phi}{\partial b_r^2} - \frac{\partial\phi}{\partial b_r}\cdot\frac{\partial^2\phi}{\partial b_r b_f}}{\Delta},\\
\Delta &= \begin{vmatrix} \frac{\partial^2\phi}{\partial b_r^2} & \frac{\partial^2\phi}{\partial b_r b_f} \\ \frac{\partial^2\phi}{\partial b_r b_f} & \frac{\partial^2\phi}{\partial b_f^2} \end{vmatrix} = \frac{\partial^2\phi}{\partial b_r^2}\cdot\frac{\partial^2\phi}{\partial b_f^2} - \left(\frac{\partial^2\phi}{\partial b_r b_f}\right)^2 .
\end{aligned} \tag{9}$$

The STOP criterion of the iteration process is $\left|b_i^{[n+1]} - b_i^{[n]}\right| \le \varepsilon_i$, where ε_i in (8) is the chosen residual uncertainty. The final $b_r^{[n+1]}, b_f^{[n+1]}$ are used to calculate $DNL_r(k)$, $DNL_f(k)$, $INL_r(k)$ a $INL_f(k)$ of the tested ADC using (5). The final INL and DNL (i. e. main result) is calculated as

$$\begin{aligned}
DNL(k) &= \frac{DNL_r(k) + DNL_f(k)}{2},\\
INL(k) &= \frac{INL_r(k) + INL_f(k)}{2}.
\end{aligned} \tag{10}$$

III. Implementation of the Method

The generator was built on multifunction DAQ card PCI-6289 with the termination unit BNC-2120 by NI. The integration circuit was shielded with a metal box. All connections were realized by coaxial cables.

Two separate software routines VI (Virtual Instruments, programs in LabVIEW, see [6]) were developed. One VI collected data and calculated histograms. The other VI performed analysis and final calculations of the DNL and INL. The programs communicated using two files contain separated histograms for the rising and falling exponential signal slopes.

A. Program MEASURE.VI

This program enables setting test conditions, such as sample rate, Hi and Lo levels of the generated square wave, etc. The program shows in real time the collected histograms as they grow and automatically stops the data collecting after achieving the required number of samples (or after the user presses the STOP button).

B. Program ANALYZE.VI

This is the main program for this method. It performs fitting of the model histogram and calculates the final INL. The main parts of it are the output graph windows. It can also save the results in a specified file.

The complete documentation of these programs, including screenshots of the GUIs and the source code is in [1].

IV. Experimental Results

To test the new implementation in LabVIEW and to verify its metrological performance we have performed a number of tests on real ADCs. The results have been compared with reference results acquired by the standardized histogram test method using the precise generator STANFORD DS360 and software developed in [3]. Because of space limitations we show here only test results of the following tested ADCs: USB6009 (14bit), ADC0804LCN (8bit). Test conditions are briefly described in the following figures captions.

A. USB6009

It is an external measurement card from NI, with a USB connection. The Fig. 5 shows the difference between the reference result, and the result obtained by the new method.

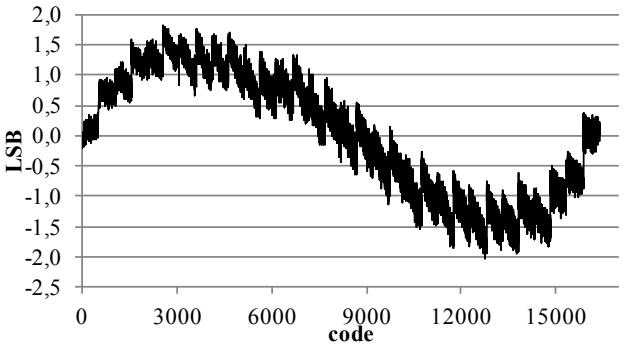

Fig. 3 INL of USB6009 using standardized method (frequency of excitation signal: 111.111Hz, resolution: 14bit, input range: ±1V, sampling rate: 48 000Ss, # of samples in record: 8×10^6)

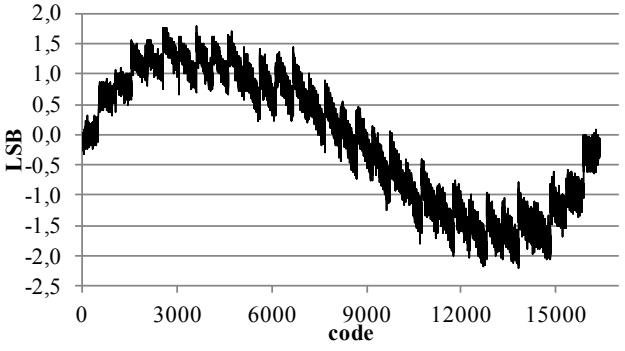

Fig. 4 INL of USB6009 using the discussed method (frequency of excitation signal: 23.5Hz, resolution: 14bit, input range: ±1V, sampling rate: 48 000Ss, # of samples in record: 8×10^6)

The theoretical maximal difference shown in Fig. 5 according to the number of samples in record should be 0.6LSB (according to [3]). The requirement is accomplished, what is a positive proof of the validity of the discussed method.

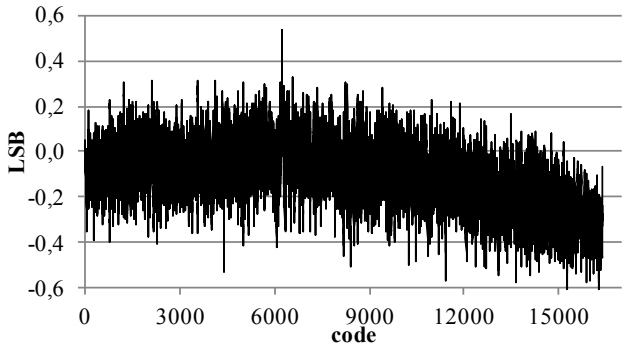

Fig. 5 Difference of INLs in Fig. 4 and Fig. 3

B. ADC0804LCN

It is one chip ADC. The connection to the PC and whole setup was made according to [8]. Fig. 8 shows the difference between the reference result and the result obtained by the new method.

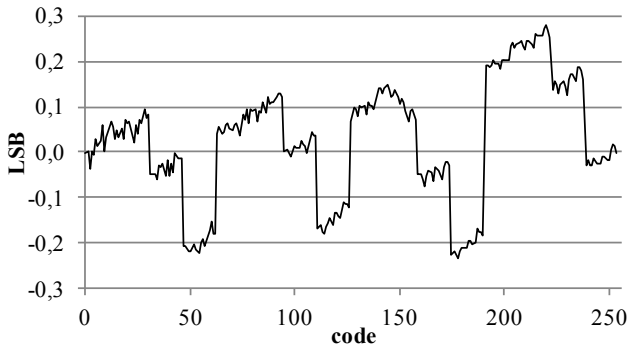

Fig. 6 INL of ADC0804LCN using standardized method (frequency of excitation signal: 111.111Hz, resolution: 8bit, input range: 0÷5V, sampling rate: 8 110Ss, # of samples in record: 2×10^6)

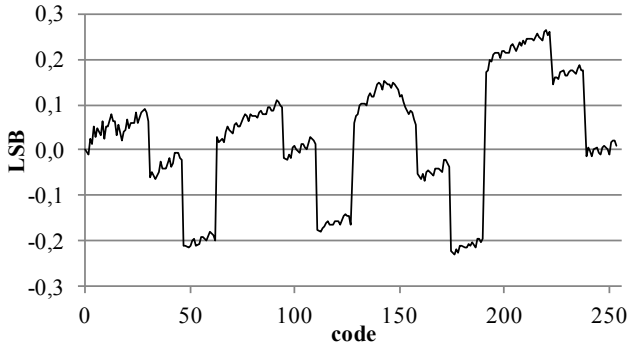

Fig. 7 INL of ADC0804LCN using the discussed method (frequency of excitation signal: 16.5Hz, resolution: 8bit, input range: 0÷5V, sampling rate: 8 110Ss, # of samples in record: 2×10^6)

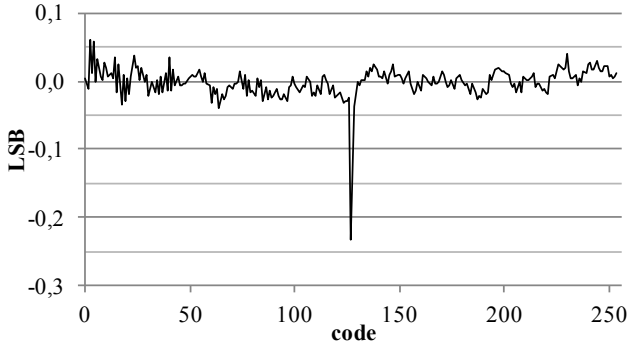

Fig. 8 Difference of INLs in Fig. 7 and Fig. 6

This ADC had the biggest difference in the acquired INLs in the code 127. This difference exceeds the theoretical measurement inaccuracy that should be max. 0.12LSB. The code 127 of this ADC appears to have a build-in/construction error because the same effect was observed also in earlier experiments, including static tests.

The differences of INLs shown in Fig. 5 and Fig. 8 have a noise-like character, what proofs, that there is no systematic error interleaved into the testing, and the difference is caused just due statistic uncertainty of both test methods.

V. Conclusion

This method has great potential, because using the methods described in the standards it is already unrealistic to test present high-resolution ADC. The development of new testing methods is therefore necessary.

In the future we would like to modify the GUI of the main program. Another desired modification of the program for obtaining histograms is that it should automatically recognize the format of the raw data obtained from the tested ADC. The comfort of the operating personnel would improve, if the program ANALYZE.VI had an algorithm that guaranteed even without entering the initial *Bf*, *Br*, that the program returned a result. Due to problems with convergence of the proposed minimization in the test method it is sometimes necessary to repeatedly change the initial value of *Bf*, *Br* to get the right results.

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References

[1] LIPTÁK, Jozef : Testovanie AČ prevodníkov. Diplomová práca. Košice: Technická univerzita v Košiciach, Fakulta elektrotechniky a informatiky, 2011. 57 s.

[2] SAKMÁR, Michal : Testovanie analógovo-číslicových prevodníkov. Diplomová práca. Košice: Technická univerzita v Košiciach, FAKULTA ELETROTECHNIKY A INFORMATIKY, 2006. 51 s.

[3] SAKMÁR, Michal : Využitie netradičných signálov pre testovanie analógovo-číslicových prevodníkov. Dizertačná práca. Košice: Technická univerzita v Košiciach, FAKULTA ELETROTECHNIKY A INFORMATIKY, 2009. 103 s.

[4] ŠALIGA, Ján et al. : Processing of bidirectional exponential stimulus in ADC testing. In: Measurement, Kidlington: Elsevier, 2010. s. 1061 - 1068.

[5] MICHAELI, Linus et al. : New approximation models for processing exponential stimulus histogram test of ADC, In: 16th IMEKO TC-4 Symposium, Florence, Italy, September 22–24, 2008.

[6] National Instruments Corporation : LabVIEW™ Help. [LabVIEW program help]. Actualized 6-2011, under number 371361H-01 [cit 2012-02-19].

[7] IEEE Std. 1057 IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters, 2007.

[8] National Semiconductor : ADC0801/ADC0802/ADC0803/ADC0804/ /ADC0805 8-Bit µP Compatible A/D Converters. [integrated circuit datasheet]. Actualized 11-1999, under number DS005671 [cit 2011-03-10].