

Product Specification _

NHD-2.4-240320DA-CTXN

TFT Liquid Crystal Display Module

NHD- Newhaven Display

2.4- 2.4" Diagonal

240320- 240 x 320 Pixels

DA- Model

C- Built-in Controller

T- White LED Backlight

X- TFT

N- TN, 6:00 Optimal View, Wide Temperature







Table of Contents

| Document Revision History | 2 |
|--------------------------------|----|
| Mechanical Drawing | |
| Pin Description | 4 |
| MCU Interface Mode Selection | |
| RGB Interface Mode Selection | ε |
| Electrical Characteristics | 7 |
| Optical Characteristics | 7 |
| Controller Information | 7 |
| Timing Characteristics for TFT | 8 |
| Example Initialization Code | 14 |
| Quality Information | 16 |

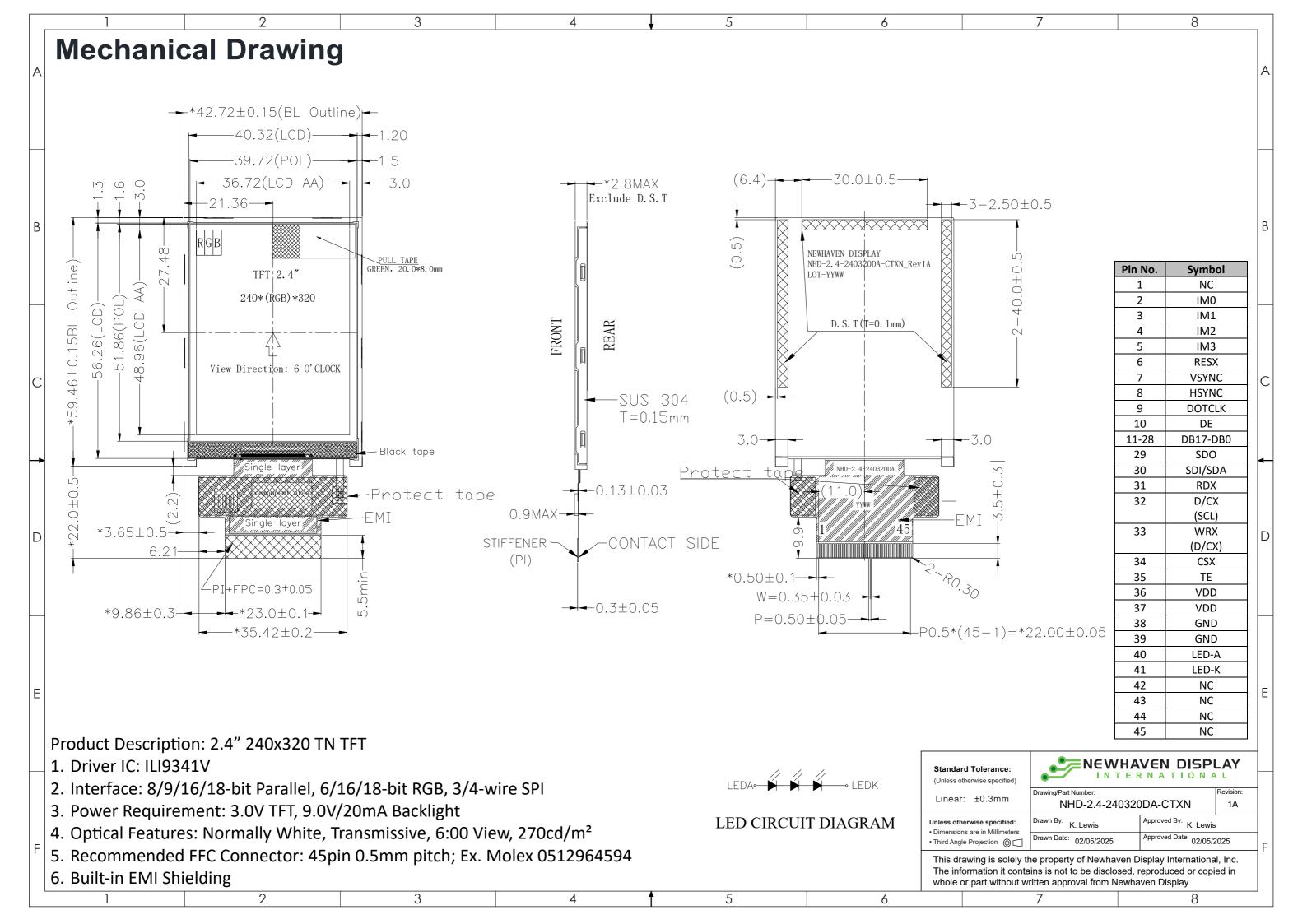
Additional Resources

- Support Forum: https://support.newhavendisplay.com/hc/en-us/community/topics
- ➤ **GitHub:** https://github.com/newhavendisplay
- **Example Code:** https://support.newhavendisplay.com/hc/en-us/categories/4409527834135-Example-Code/
- ➤ Knowledge Center: https://www.newhavendisplay.com/knowledge center.html
- ➤ Quality Center: https://www.newhavendisplay.com/quality_center.html
- Precautions for using LCDs/LCMs: https://www.newhavendisplay.com/specs/precautions.pdf
- ➤ Warranty / Terms & Conditions: https://www.newhavendisplay.com/terms.html



Document Revision History

| Revision | Date | Description | Changed By |
|----------|------------|-----------------|------------|
| - | 02/05/2025 | Initial Release | KL |





Pin Description

| Pin No. | Symbol | External Connection | Function Description |
|---------|----------|---------------------|--|
| 1 | NC | - | No Connect |
| 2 | IM0 | MPU | Interface Mode select |
| 3 | IM1 | MPU | Interface Mode select |
| 4 | IM2 | MPU | Interface mode select |
| 5 | IM3 | MPU | Interface mode select |
| 6 | RESX | MPU | Active LOW Reset signal |
| 7 | VSYNC | MPU | Vertical (Frame) sync signal for RGB interface |
| 8 | HSYNC | MPU | Horizontal (Line) sync signal for RGB interface |
| 9 | DOTCLK | | Dot Clock signal for RGB interface (Rising Edge) |
| 10 | DE | MPU | Data Enable signal for RGB interface |
| 11-28 | DB17-DB0 | MPU | Bi-directional data bus |
| 29 | SDO | MPU | Serial Data Out |
| 30 | SDI/SDA | MPU | Serial Data In |
| 31 | RDX | MPU | Active LOW Read signal |
| 32 | D/CX | MPU | Parallel Interface: |
| | (SCL) | | Data/command selection: 1 = Data; 0 = Command |
| | | | Serial Interface: |
| | | | Serial Clock signal |
| 33 | WRX | MPU | Parallel Interface: |
| | (D/CX) | | Active LOW write signal |
| | | | Serial Interface: |
| | | | Data/command selection: 1 = Data; 0 = Command |
| 34 | CSX | MPU | Active LOW Chip Select signal |
| 35 | TE | MPU | Tearing Effect output signal to synchronize MPU to frame |
| 36 | VDD | Power Supply | Supply Voltage for LCD and Logic (3.0V) |
| 37 | VDD | Power Supply | Supply Voltage for LCD and Logic (3.0V) |
| 38 | GND | Power Supply | Ground |
| 39 | GND | Power Supply | Ground |
| 40 | LED-A | Power Supply | Backlight Anode (9.0V/20mA) |
| 41 | LED-K | Power Supply | Backlight Cathode (Ground) |
| 42 | NC | - | No Connect |
| 43 | NC | - | No Connect |
| 44 | NC | - | No Connect |
| 45 | NC | - | No Connect |

Recommended LCD connector: 45-pin, 0.5mm pitch FFC connector Molex P/N: 0512964594or similar



MCU Interface Mode Selection

| Pin | | | Interface | e Mode I | | | | | Interface | Mode II | | |
|------|-------|--------|-----------|----------|--------|--------|-------|--------|-----------|---------|--------|--------|
| Name | 8080 | 8080 | 8080 | 8080 | 3-wire | 4-wire | 8080 | 8080 | 8080 | 8080 | 3-wire | 4-wire |
| | 8-bit | 16-bit | 9-bit | 18-bit | SPI | SPI | 8-bit | 16-bit | 9-bit | 18-bit | SPI | SPI |
| IM0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| IM1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| IM2 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| IM3 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

MPU Interface Pin Assignment Summary

| Bus | | | | | | Dat | a/Con | nmand | Inter | face | | | | | | | | | | | Control | Signals | | |
|--------------|-------|-----|----|------|--------|-----|-------|--------|--------|------|---|---|------|-------|------|---|---|-----|------|------|---------|---------|-----|------|
| Interface | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | /WRX | /RDX | /csx | D/CX | SDO | SDI/ |
| | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | SDA |
| Interface Mo | de I | | | | | | | | | | | | | | | | | | | | | | | |
| 8080 8-bit | | | | | Tie LO | W | | | | | | | | D | [7:0 |] | | | /WRX | /RDX | /CSX | D/CX | NC | LOW |
| 8080 16-bit | Tie l | _OW | | | | | | [|) [15: | :0] | | | | | | | | | /WRX | /RDX | /CSX | D/CX | NC | LOW |
| 8080 9-bit | | | | Т | ie LOW | 1 | | | | | | | | D [8 | 3:0] | | | | /WRX | /RDX | /CSX | D/CX | NC | LOW |
| 8080 18-bit | | | | | | | | [17:0] |] | | | | | | | | | | /WRX | /RDX | /CSX | D/CX | NC | LOW |
| 3-wire SPI | | | | | | | T | ie LOV | / | | | | | | | | | | HIGH | HIGH | /CSX | SCL | NC | SDA |
| 4-wire SPI | | | | | | | T | ie LOV | / | | | | | | | | | | D/CX | HIGH | /CSX | SCL | NC | SDA |
| Interface Mo | de II | | | | | | | | | | | | | | | | | | | | | | | |
| 8080 8-bit | | | | D [1 | 7:10] | | | | | | | | Tie | LO\ | ٧ | | | | /WRX | /RDX | /CSX | D/CX | NC | LOW |
| 8080 16-bit | | | | D [1 | 7:10] | | | | | | | D | [8:1 | .] | | | | LOW | /WRX | /RDX | /CSX | D/CX | NC | LOW |
| 8080 9-bit | | | | С | [17:9] |] | | | | | | | | Tie l | .OW | | | | /WRX | /RDX | /CSX | D/CX | NC | LOW |
| 8080 18-bit | | | | | | | | [17:0] |] | | | | | | | | | | /WRX | /RDX | /CSX | D/CX | NC | LOW |
| 3-wire SPI | | | | | | | T | ie LOV | I | | | | | | | | | | HIGH | HIGH | /CSX | SCL | SDO | SDI |
| 4-wire SPI | | | | | | | Т | ie LOV | / | | | | | | | | | | D/CX | HIGH | /CSX | SCL | SDO | SDI |



RGB Interface Mode Selection

The Ilitek ILI9341V driver IC is user configurable for DE Mode and SYNC mode RGB interface.

DE Mode is enabled when the RCM [1:0] bits of B0h command are set to "10", and DE signal is high for valid pixel data. Data is clocked in using rising edge of DOTCLK signal. DE mode is recommended to enable the ILI9341V driver IC to synchronize the display image on TFT panel without depending on specific horizontal and vertical sync timing from host controller.

SYNC mode is enabled when the RCM [1:0] bits of B0h command are set to "11", DE signal is ignored, and HSYNC and VSYNC signals are used to explicitly define the horizontal and vertical sync timing to synchronize the display image on TFT panel. Data is clocked in using rising edge of DOTCLK signal. Any change to the HSYNC or VSYNC values may prevent the image from correctly appearing on the display.

ILI9341V supports several pixel formats that can be selected by DPI [2:0] bits of "Pixel Format Set (3Ah)" and RIM bit of F6h command.

| RCM | [1:0] | RIM | D | PI[2: | :0] | RGB Interface Mode | RGB Mode | Used Pins |
|-----|-------|-----|---|-------|-----|--------------------------------------|---|---|
| 1 | 0 | 0 | 1 | 1 | 0 | 18-bit RGB interface (262K colors) | | VSYNC, HSYNC, DE, DOTCLK,D[17:0] |
| 1 | 0 | 0 | 1 | 0 | 1 | 16-bit RGB interface (65K colors) | DE Mode | VSYNC, HSYNC, DE, DOTCLK, D[17:13] & D[11:1] |
| 1 | 0 | 1 | 1 | 1 | 0 | 6-bit RGB interface (262K colors) | Valid data is determined by the DE signal | VSYNC, HSYNC, DE, DOTCLK, D[5:0] |
| 1 | 0 | 1 | 1 | 0 | 1 | 6-bit RGB interface (65K colors) | | VSYNC, HSYNC, DE, DOTCLK, D[5:0] |
| 1 | 1 | 0 | 1 | 1 | 0 | 18-bit RGB interface (262K colors) | | VSYNC, HSYNC, DOTCLK, D[17:0] |
| 1 | 1 | 0 | 1 | 0 | 1 | 16-bit RGB interface (65K colors) | SYNC Mode In SYNC mode, DE signal is ignored; | VSYNC, HSYNC, DOTCLK, D[17:13] & D[11:1] |
| 1 | 1 | 1 | 1 | 1 | 0 | 6-bit RGB interface (262K colors) | blanking porch is determined by B5h command. | VSYNC, HSYNC, DOTCLK, D[5:0] |
| 1 | 1 | 1 | 1 | 0 | 1 | 6-bit RGB interface (65K colors) | | VSYNC, HSYNC, DOTCLK, D[5:0] |



Electrical Characteristics

| Item | Symbol | Condition | Min. | Тур. | Max. | Unit |
|-----------------------------|-----------------|---------------------------------------|-----------------------|--------|-----------------------|------|
| Operating Temperature Range | T _{OP} | Absolute Max | -20 | - | +70 | °C |
| Storage Temperature Range | T _{ST} | Absolute Max | -30 | - | +80 | °C |
| Supply Voltage for LCD | V_{DD} | - | 2.5 | 3.0 | 3.3 | V |
| Supply Current | I _{DD} | $V_{DD} = 3.0V$ | 5 | 10 | 15 | mA |
| "H" Level input | V_{IH} | - | 0.7 * V _{DD} | 1 | V_{DD} | V |
| "L" Level input | V_{IL} | - | V_{SS} | - | 0.3 * V _{DD} | V |
| "H" Level output | Voh | - | 0.8 * V _{DD} | - | V_{DD} | V |
| "L" Level output | V_{OL} | - | Vss | • | 0.2 * V _{DD} | V |
| | | | | | | |
| Backlight Supply Current | I_{LED} | - | 10 | 20 | 25 | mA |
| Backlight Supply Voltage | V_{LED} | I _{LED} = 20mA | 8.1 | 9.0 | 10.2 | V |
| Backlight Lifetime* | - | $I_{LED} = 20$ mA $T_{OP} = 25$ °C | 30,000 | 50,000 | - | Hrs. |

^{*}Backlight Lifetime is rated as Hours until **half-brightness**, under normal operating conditions. The LED of the backlight is driven by current drain; drive voltage is for reference only. Drive voltage must be selected to ensure backlight current drain is below MAX level stated.

Optical Characteristics

| | Item | | Symbol | Condition | Min. | Тур. | Max. | Unit |
|-------------------|--------|-------|----------------|-------------------------|-------|-------|-------|-------------------|
| Outine | Тор | | φΥ+ | | - | 20 | - | 0 |
| Optimal | Bottom | | φΥ- | CD > 10 | - | 45 | - | 0 |
| Viewing Angles | Left | | θХ- | CR ≥ 10 | - | 45 | - | 0 |
| Aligies | Right | | θХ+ | | - | 45 | - | 0 |
| Contrast Rat | io | | CR | - | - | 350 | - | - |
| Luminance | | | Lv | I _{LED} = 20mA | 220 | 270 | - | cd/m ² |
| Response Tir | ne | | $T_R + T_F$ | $T_{OP} = 25^{\circ}C$ | - | 30 | 45 | ms |
| | | Red | X_R | - | 0.525 | 0.575 | 0.625 | - |
| | | Red | Y_R | - | 0.297 | 0.347 | 0.397 | - |
| | | Croon | X _G | - | 0.282 | 0.332 | 0.382 | - |
| Chromo | tioit. | Green | Y _G | - | 0.556 | 0.606 | 0.656 | - |
| Chroma | licity | Dlug | X _B | - | 0.101 | 0.151 | 0.201 | - |
| | | Blue | Y _B | - | 0.026 | 0.062 | 0.126 | - |
| | | | Xw | - | 0.239 | 0.289 | 0.339 | - |
| | | White | Yw | - | 0.249 | 0.299 | 0.349 | - |

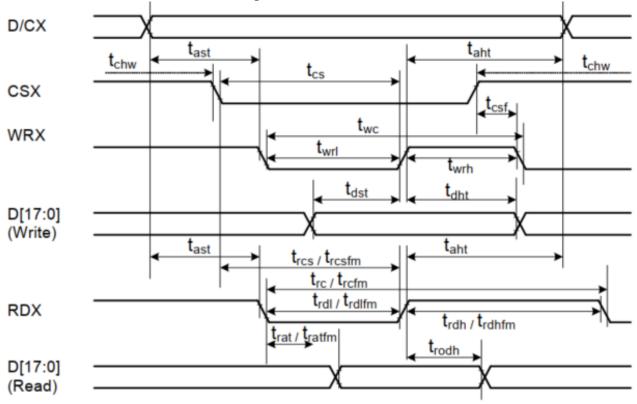
Controller Information

Built-in ILI9341V Controller: https://support.newhavendisplay.com/hc/en-us/articles/26623027048343-ILI9341V



Timing Characteristics for TFT

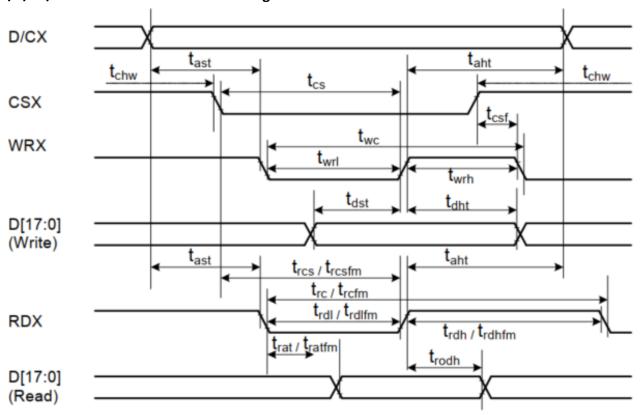
8/9/16/18-bit Parallel Interface I Timing Characteristics



| Signal | Symbol | Parameter | min | max | Unit | Description |
|-------------------|--------|------------------------------------|-----|-----|------|---------------------|
| DCX | tast | Address setup time | 0 | • | ns | |
| DCX | taht | Address hold time (Write/Read) | 0 | ١ | ns | |
| | tchw | CSX "H" pulse width | 0 | • | ns | |
| | tcs | Chip Select setup time (Write) | 15 | • | ns | |
| CSX | trcs | Chip Select setup time (Read ID) | 45 | • | ns | |
| | trcsfm | Chip Select setup time (Read FM) | 355 | ١ | ns | |
| | tcsf | Chip Select Wait time (Write/Read) | 10 | • | ns | |
| | twc | Write cycle | 66 | ١ | ns | |
| WRX | twrh | Write Control pulse H duration | 15 | ١ | ns | |
| | twrl | Write Control pulse L duration | 15 | ١ | ns | |
| | trcfm | Read Cycle (FM) | 450 | • | ns | |
| RDX (FM) | trdhfm | Read Control H duration (FM) | 90 | • | ns | |
| | trdlfm | Read Control L duration (FM) | 355 | • | ns | |
| | trc | Read cycle (ID) | 160 | • | ns | |
| RDX (ID) | trdh | Read Control pulse H duration | 90 | • | ns | |
| | trdl | Read Control pulse L duration | 45 | ٠ | ns | |
| D/47.03 | tdst | Write data setup time | 10 | • | ns | |
| D[17:0], | tdht | Write data hold time | 10 | • | ns | 5 |
| D[15:0], | trat | Read access time | - | 40 | ns | For maximum CL=30pF |
| D[8:0], D[7:0] | tratfm | Read access time | - | 340 | ns | For minimum CL=8pF |
| D[7.0] | trod | Read output disable time | 20 | 80 | ns | |



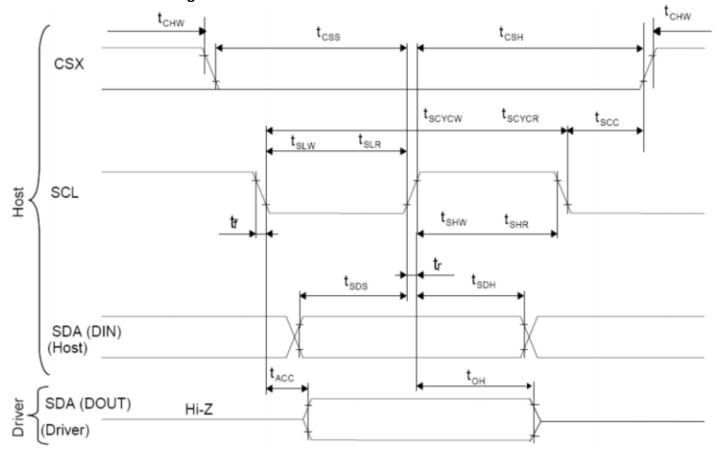
8/9/16/18-bit Parallel Interface II Timing Characteristics



| Signal | Symbo | Parameter | min | max | Unit | Description |
|----------------------|--------|------------------------------------|-----|-----|------|---------------------|
| DCX | tast | Address setup time | 0 | - | ns | |
| DCX | taht | Address hold time (Write/Read) | 0 | - | ns | |
| | tchw | CSX "H" pulse width | 0 | - | ns | |
| | tcs | Chip Select setup time (Write) | 15 | - | ns | |
| CSX | trcs | Chip Select setup time (Read ID) | 45 | - | ns | |
| | trcsfm | Chip Select setup time (Read FM) | 355 | - | ns | |
| | tcsf | Chip Select Wait time (Write/Read) | 10 | - | ns | |
| | twc | Write cycle | 66 | - | ns | |
| WRX | twrh | Write Control pulse H duration | 15 | - | ns | |
| | twrl | Write Control pulse L duration | 15 | - | ns | |
| | trcfm | Read Cycle (FM) | 450 | - | ns | |
| RDX (FM) | trdhfm | Read Control H duration (FM) | 90 | - | ns | |
| | trdlfm | Read Control L duration (FM) | 355 | - | ns | |
| | trc | Read cycle (ID) | 160 | - | ns | |
| RDX (ID) | trdh | Read Control pulse H duration | 90 | - | ns | |
| | trdl | Read Control pulse L duration | 45 | - | ns | |
| D. (T. 0) | tdst | Write data setup time | 10 | - | ns | |
| D[17:0], | tdht | Write data hold time | 10 | - | ns | F |
| D[17:10]&D[8:1], | trat | Read access time | - | 40 | ns | For maximum CL=30pF |
| D[17:10], D[17:9] | tratfm | Read access time | - | 340 | ns | For minimum CL=8pF |
| D[17.8] | trod | Read output disable time | 20 | 80 | ns | |



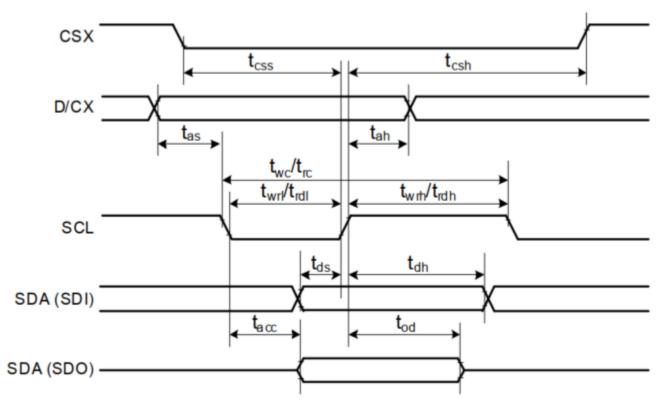
3-wire Serial interface Timing Characteristics



| Signal | Symbol | Parameter | min | max | Unit | Description |
|-----------|--------|-----------------------------|-----|------|------|--------------|
| | tscycw | Serial Clock Cycle (Write) | 100 | - | ns | 111 82 - 111 |
| | tshw | SCL "H" Pulse Width (Write) | 40 | - | ns | |
| 201 | tslw | SCL "L" Pulse Width (Write) | 40 | - | ns | |
| SCL | tscycr | Serial Clock Cycle (Read) | 150 | - | ns | |
| | tshr | SCL "H" Pulse Width (Read) | 60 | - | ns | |
| | tslr | SCL "L" Pulse Width (Read) | 60 | - | ns | |
| SDA / SDI | tsds | Data setup time (Write) | 30 | - | ns | |
| (Input) | tsdh | Data hold time (Write) | 30 | - | ns | |
| SDA/SDO | tacc | Access time (Read) | 10 | - 15 | ns | |
| (Output) | toh | Output disable time (Read) | 10 | 50 | ns | |
| | tscc | SCL-CSX | 20 | - | ns | |
| CSX | tchw | CSX "H" Pulse Width | 40 | - | ns | |
| CSX | tcss | CSV SCI Time | 60 | - | ns | |
| | tcsh | CSX-SCL Time | 65 | - 2 | ns | |



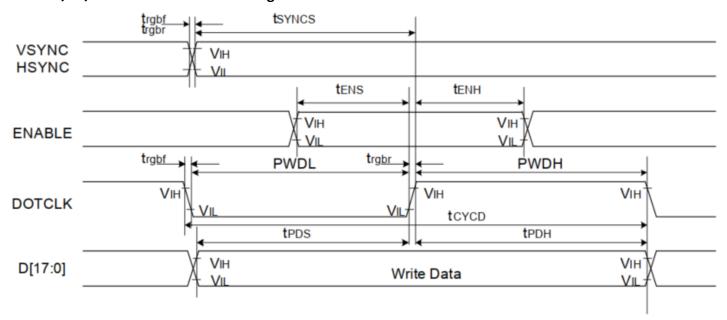
4-wire Serial interface Timing Characteristics



| Signal | Symbol | Parameter | min | max | Unit | Description |
|-----------|--------|-------------------------------|-----|-----|------|---------------------|
| CCV | tcss | Chip select time (Write) | 40 | | ns | |
| CSX | tcsh | Chip select hold time (Read) | 40 | - | ns | |
| | twc | Serial clock cycle (Write) | 100 | 55 | ns | |
| | twrh | SCL "H" pulse width (Write) | 40 | | ns | |
| 001 | twrl | SCL "L" pulse width (Write) | 40 | - | ns | |
| SCL | trc | Serial clock cycle (Read) | 150 | | ns | |
| | trdh | SCL "H" pulse width (Read) | 60 | - | ns | |
| | trdl | SCL "L" pulse width (Read) | 60 | - | ns | |
| DIOY | tas | D/CX setup time | 10 | - | | |
| D/CX | tah | D/CX hold time (Write / Read) | 10 | - | | X. |
| SDA / SDI | tds | Data setup time (Write) | 30 | - | ns | |
| (Input) | tdh | Data hold time (Write) | 30 | 17 | ns | |
| SDA/SDO | tacc | Access time (Read) | 10 | - | ns | For maximum CL=30pF |
| (Output) | tod | Output disable time (Read) | 10 | 50 | ns | For minimum CL=8pF |



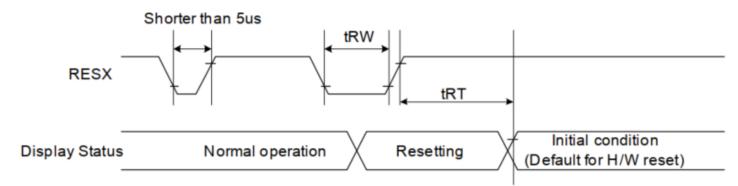
Parallel 6/16/18-bit RGB Interface Timing Characteristics



| Signal | Symbol | Parameter | min | max | Unit | Description |
|---------|---------------------------------------|-----------------------------------|-----|-----|------|-------------------|
| VSYNC / | tsyncs | VSYNC/HSYNC setup time | 15 | - | ns | |
| HSYNC | tsynch | VSYNC/HSYNC hold time | 15 | - | ns | |
| DE | t _{ENS} | DE setup time | 15 | • | ns | |
| | t _{ENH} | DE hold time | 15 | - | ns | |
| D[17:0] | t _{POS} | Data setup time | 15 | - | ns | 18/16-bit bus RGB |
| D[17:0] | t _{PDH} | Data hold time | 15 | - | ns | interface mode |
| | PWDH | DOTCLK high-level period | 15 | - | ns | |
| DOTCLK | PWDL | DOTCLK low-level period | 15 | • | ns | |
| DOTCLK | tcycD | DOTCLK cycle time | 100 | - | ns | |
| | t _{rgbr} , t _{rgbf} | DOTCLK,HSYNC,VSYNC rise/fall time | - | 15 | ns | |
| VSYNC / | tsyncs | VSYNC/HSYNC setup time | 15 | - | ns | |
| HSYNC | tsynch | VSYNC/HSYNC hold time | 15 | - | ns | |
| DE | t _{ENS} | DE setup time | 15 | - | ns | |
| DE | t _{ENH} | DE hold time | 15 | - | ns | |
| D[47:0] | t _{POS} | Data setup time | 15 | • | ns | 6-bit bus RGB |
| D[17:0] | t _{PDH} | Data hold time | 15 | - | ns | interface mode |
| | PWDH | DOTCLK high-level pulse period | 15 | - | ns | |
| DOTCLK | PWDL | DOTCLK low-level pulse period | 15 | - | ns | |
| | t _{CYCD} | DOTCLK cycle time | 50 | - | ns | |
| | t _{rgbr} , t _{rgbf} | DOTCLK,HSYNC,VSYNC rise/fall time | - | 15 | ns | |

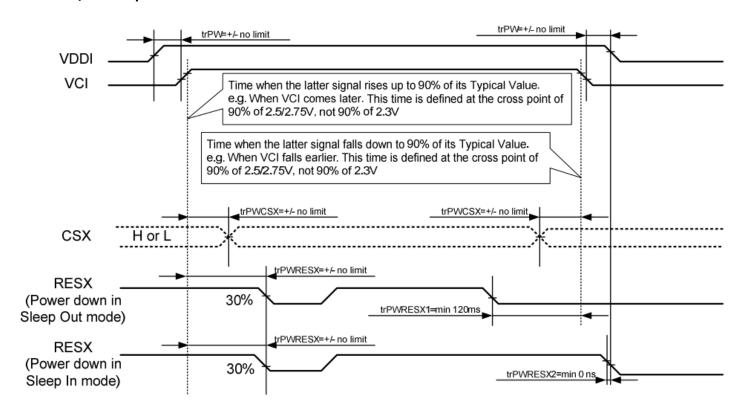


Reset Timing



| Signal | Symbol | Parameter | Min | Max | Unit |
|--------|--------|----------------------|-----|---------------------|------|
| RESX | tRW | Reset pulse duration | 10 | | uS |
| | tRT | Reset cancel | | 5 (note 1,5) | mS |
| | | | | 120 (note 1,6,7) | mS |

Power ON/OFF Sequence



trPWRESX1 is applied to RESX falling in the Sleep Out Mode trPWRESX2 is applied to RESX falling in the Sleep In Mode



Example Initialization Code

```
void TFT_Init() {
  command(0x28); // Display off
  command(0x11); // Exit SLEEP mode
  command(0xCB); // Power Control A
  data(0x39);
  data(0x2C);
  data(0x00);
  data(0x34);
  data(0x02);
  command(0xCF); // Power Control B
  data(0x00);
  data(0x81);
  data(0x30);
  command(0xC0); // Power Control 1
  data(0x26);
  data(0x04);
  command(0xC1); // Power Control 2
  data(0x11);
  command(0xC5); // VCOM Control 1
  data(0x35);
  data(0x3E);
  command(0x36); // Memory Access Control (BGR)
  data(0x88);
  command(0xB1); // Frame Rate Control
  data(0x00);
  data(0x18);
  command(0xB6); // Display Function Control
  data(0x0A);
  data(0xA2);
  command(0xC7); // VCOM Control 2
  data(0xBE);
  command(0x3A); // Pixel Format (16-bit)
  data(0x55);
  command(0xF2); // 3G Gamma Control (Off)
  data(0x02);
```



```
command(0x26); // Gamma Curve 3
data(0x01);

command(0x2A); // Column Address Set
data(0x00);
data(0x00);
data(0x00);
data(0xEF);

command(0x2B); // Page Address Set
data(0x00);
data(0x00);
data(0x01);
data(0x3F);

command(0x29); // Display ON
}
```



Quality Information

| Test Item | Content of Test | Test Condition | Note |
|--|---|---|------|
| High Temperature Storage | Endurance test applying the high storage temperature for a long time. | +80°C, 240hrs | 2 |
| Low Temperature Storage | Endurance test applying the low storage temperature for a long time. | -30°C, 240hrs | 1,2 |
| High Temperature Operation | Endurance test applying the electric stress (voltage & current) and the high thermal stress for a long time. | +70°C, 240hrs | 2 |
| Low Temperature Operation | Endurance test applying the electric stress (voltage & current) and the low thermal stress for a long time. | -20°C, 240hrs | 1,2 |
| High Temperature / Humidity Operation | Endurance test applying the electric stress (voltage & current) and the high thermal with high humidity stress for a long time. | +60°C, 90% RH, 240hrs | 1,2 |
| Thermal Shock resistance | Endurance test applying the electric stress (voltage & current) during a cycle of low and high thermal stress. | -30°C 30min -> 25°C 3min -> 80°C 30min = 1 cycle. For 100 cycles | |
| Vibration test | Endurance test applying vibration to simulate transportation and use. | 10Hz-55Hz,(1 min) 1.5mm amplitude. Accelerated Velocity:2G 30 min in each of 3 directions X,Y,Z | 3 |
| Static electricity test | Endurance test applying electric static discharge. | Air discharge: ±8kV 10 Times Contact discharge: ±4kV 10 Times (RS=330kΩ ,CS=150pF) | |

Note 1: No condensation to be observed.

Note 2: Conducted after 4 hours of storage at 25°C, 0%RH.

Note 3: Test performed on product itself, not inside a container.