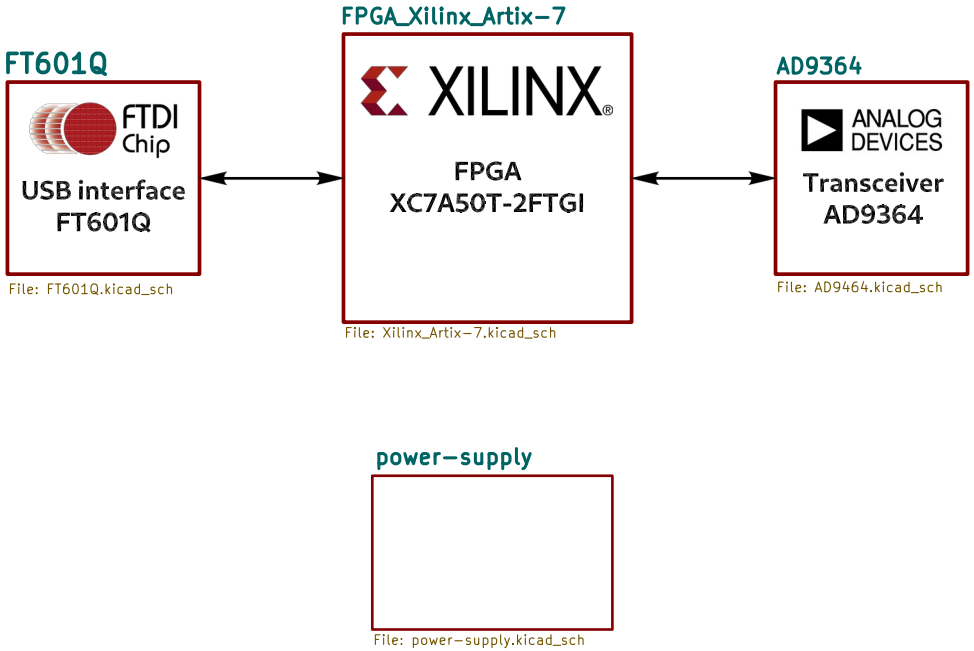
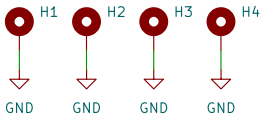


M3 mounting holes



MurPhy SDR

M.P Inc

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File: MurPhySDR.kicad_sch

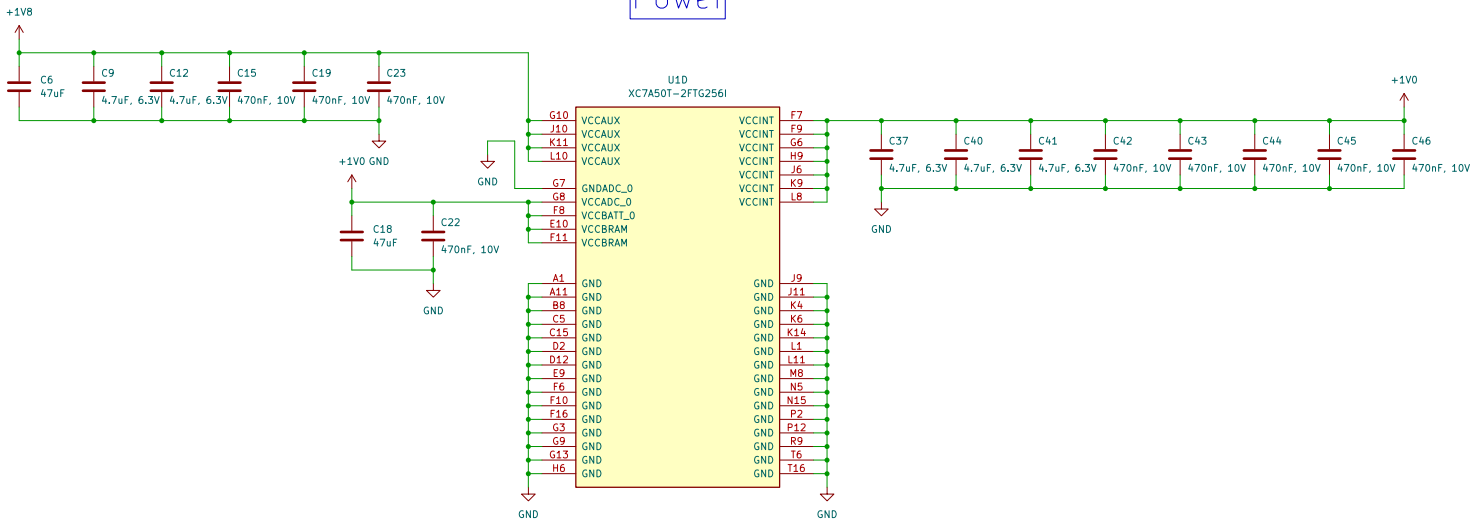
Title: MurPhy SDR

Size: A4	Date: 2024-04-22	Rev:
KiCad E.D.A. 8.0.2		Id: 1/10

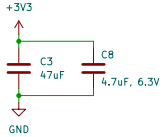
Package	Device	V_{CCINT}					V_{CCBRAM}				V_{CCAUX}			V_{CCO} Bank 0	V_{CCO} all other Banks (per Bank)		
		680 µF	330 µF	100 µF	47 µF	4.7 µF	0.47 µF	100 µF	47 µF	4.7 µF	0.47 µF	47 µF	4.7 µF	0.47 µF	47 µF	47 µF or 100 µF[1]	4.7 µF	0.47 µF
FTG256	XC7A50T	0	1	0	0	3	5	1	0	0	1	1	2	3	1	1	2	4

xilinx ug483 p15

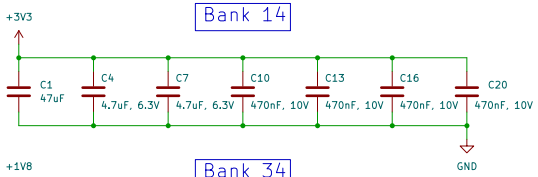
Power



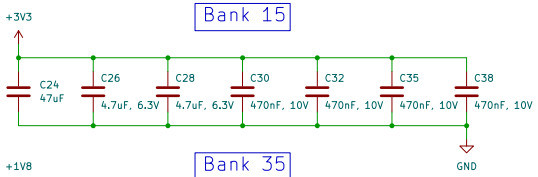
Bank 0



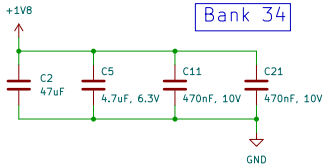
Bank 14



Bank 15



Bank 34



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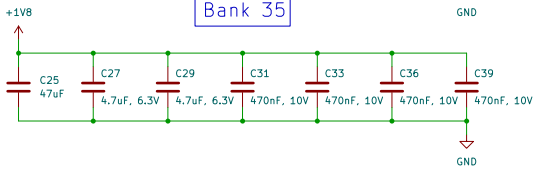

FPGA power

M.P Inc

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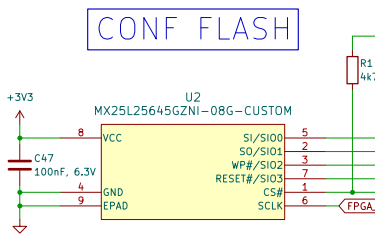
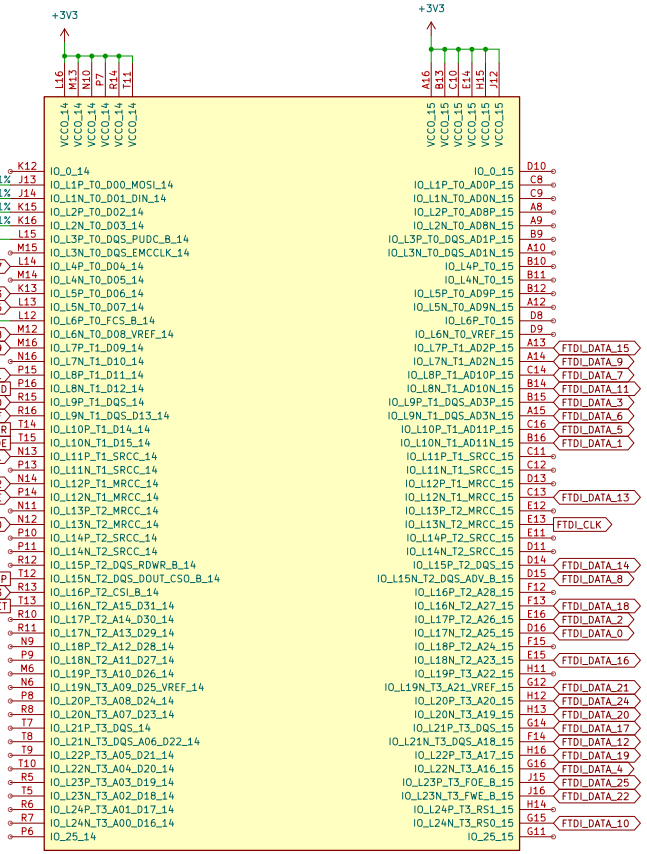
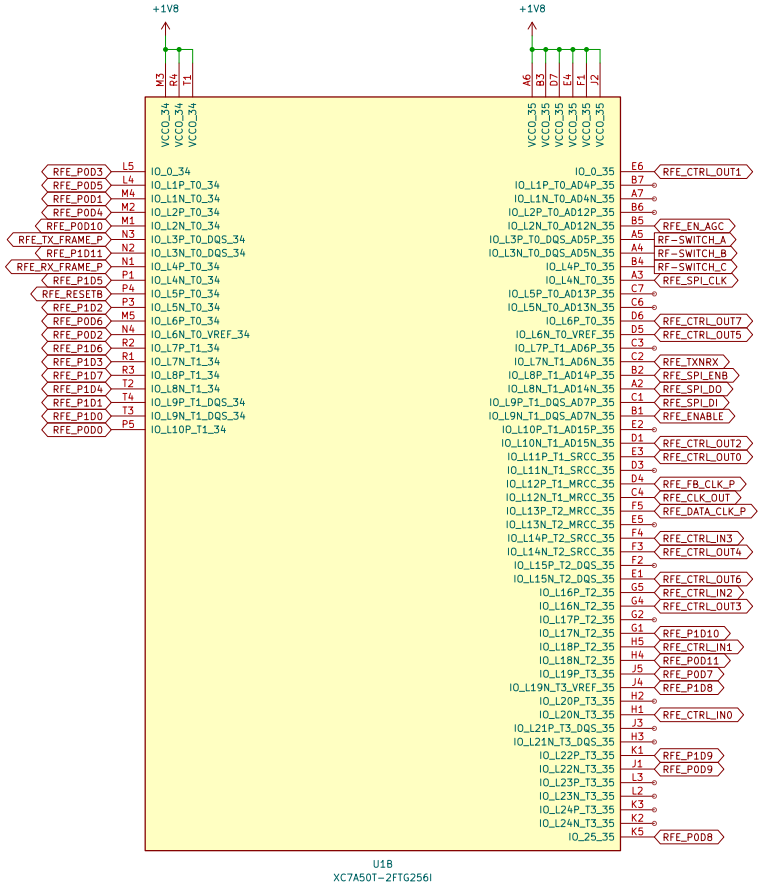
File: Xilinx_Artix-7_power-supply.kicad_sch

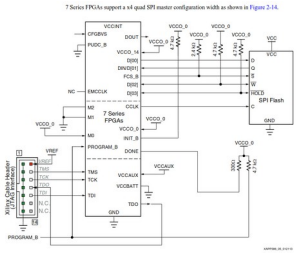
Title: MurPhy SDR

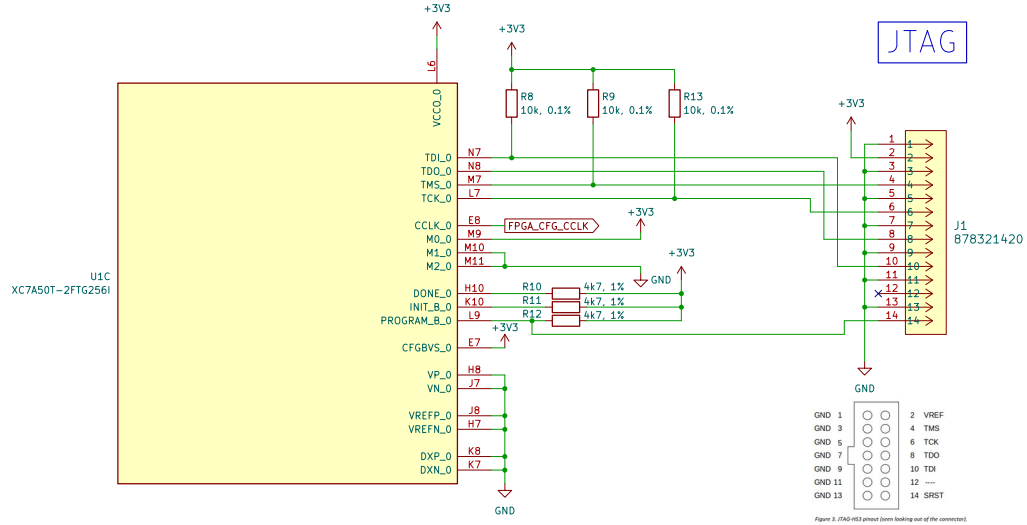
Size: A3	Date: 2024-04-22	Rev:
KiCad E.D.A. 8.0.2		Id: 3/10











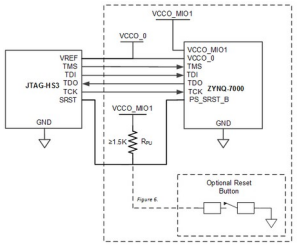


Figure 6. System board components.

Figure 3. JTAG-HS3 pinout (seen looking out of the connector).

FPGA banks, JTAG and FLASH

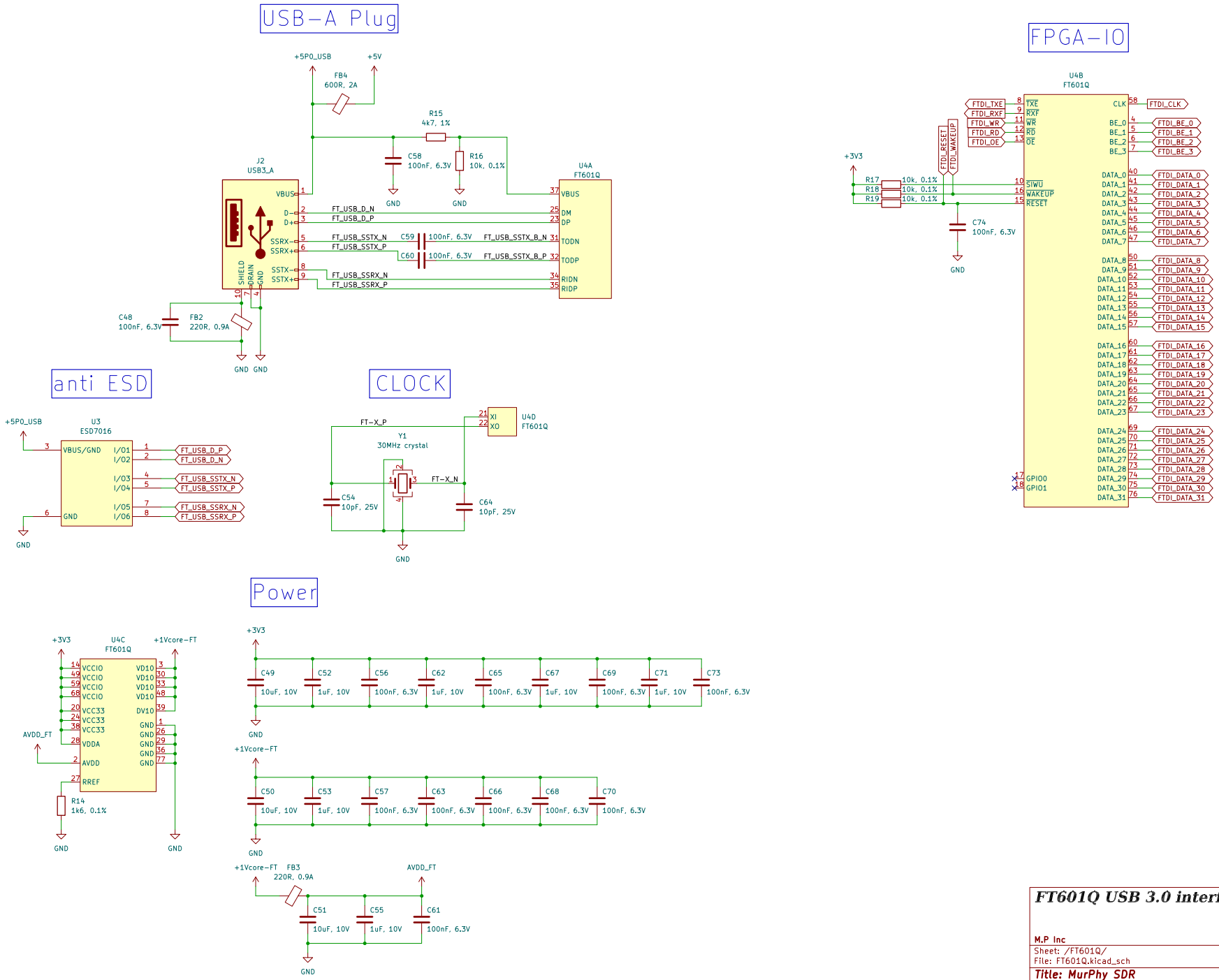
M.P Inc

Sheet: /FPGA_Xilinx_Artix-7/Banks/

File: Xilinx_Artix-7_Banks.kicad_sch

Title: MurPhy SDR

Size: A3	Date: 2024-04-22	Rev:
KiCad E.D.A. 8.0.2		Id: 4/10



FT601Q USB 3.0 interface

M.P Inc

Sheet: /FT601Q/

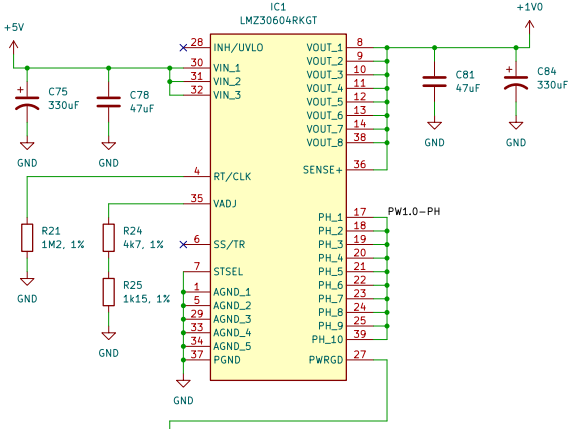
File: FT601Q.kicad_sch

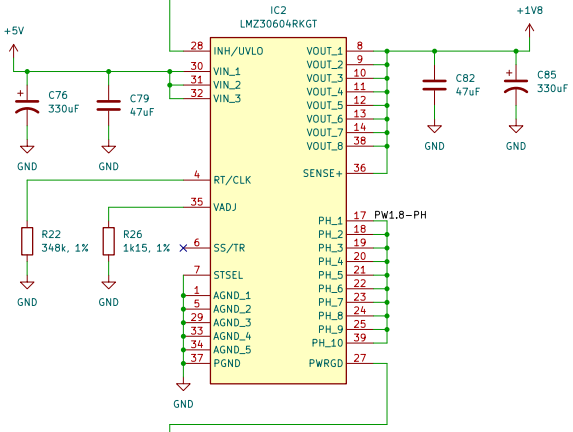
Title: MurPhy SDR

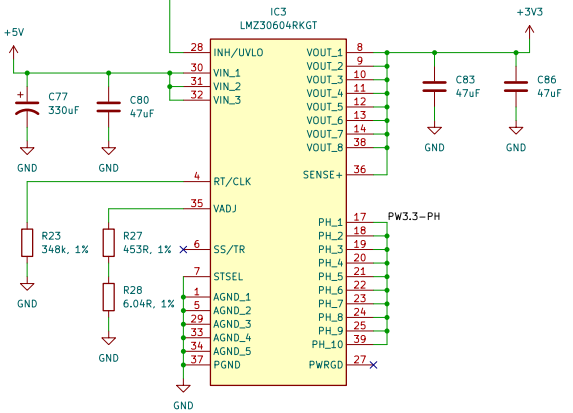
Size: A3	Date: 2024-04-22	Rev:
KiCad E.D.A. 8.0.2		Id: 5/10

switching regulators

PWR sequence: 1V0 -> 1V8 -> 3V3







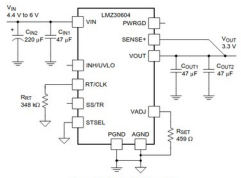
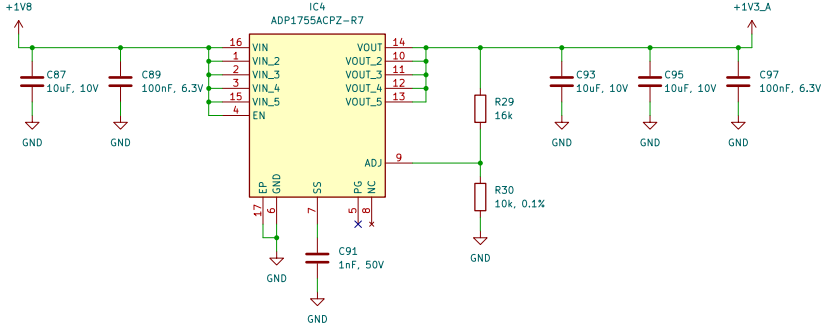
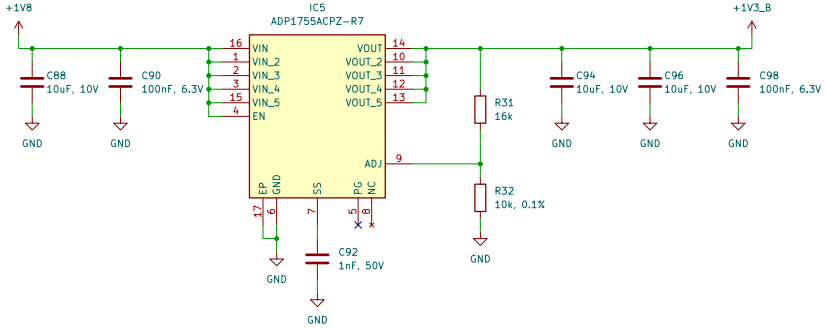


Figure 20. Typical Schematic
VIN = 4.4 V to 6.0 V, VOUT = 3.3 V

low-dropout regulators





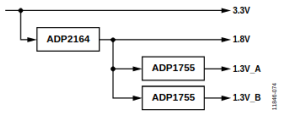


Figure 74. Low Noise Power Solution for the AD9364

Table 4. Standard R_{SET} Resistor Values

V_{OUT} (V)	R_{SET} (kΩ)	R_{FF}(kΩ)	f_{SW}(kHz)	V_{OUT} (V)	R_{SET} (kΩ)	R_{FF}(kΩ)	f_{SW}(kHz)
0.8	open	1200	650	2.3	0.768	348	1000
0.9	11.8	1200	650	2.4	0.715	348	1000
1.0	5.83	1200	650	2.5	0.673	348	1000
1.1	3.83	1200	650	2.6	0.634	348	1000
1.2	2.87	715	750	2.7	0.604	348	1000
1.3	2.32	715	750	2.8	0.576	348	1000
1.4	1.91	715	750	2.9	0.549	348	1000
1.5	1.65	348	1000	3.0	0.523	348	1000
1.6	1.43	348	1000	3.1	0.499	348	1000
1.7	1.27	348	1000	3.2	0.475	348	1000
1.8	1.15	348	1000	3.3	0.459	348	1000
1.9	1.05	348	1000	3.4	0.442	348	1000
2.0	0.953	348	1000	3.5	0.422	348	1000
2.1	0.845	348	1000	3.6	0.412	348	1000
2.2	0.825	348	1000				

Power supply

M.P Inc

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File: power-supply.kicad_sch

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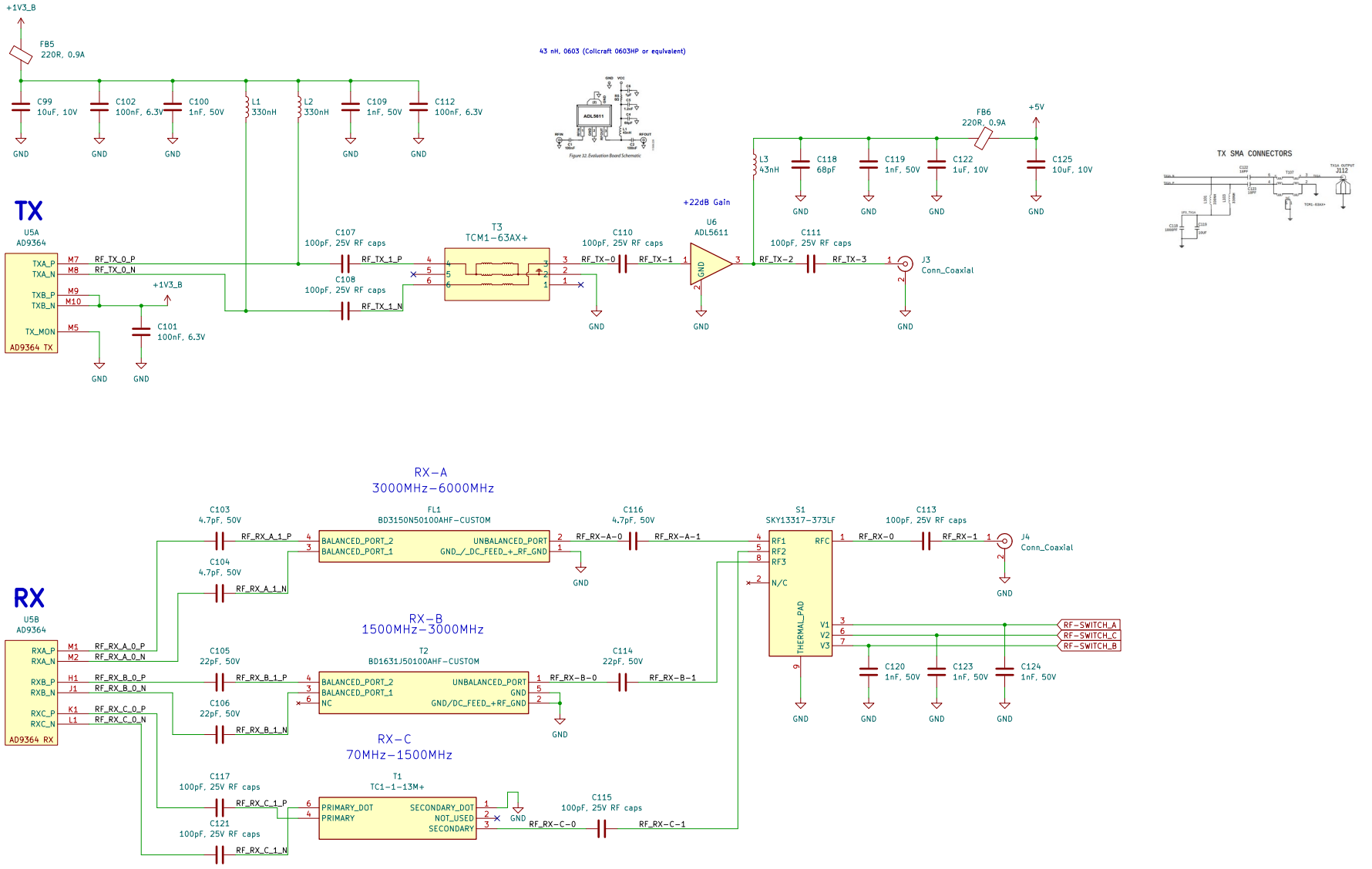
KiCad E.D.A. 8.0.2		Id: 6/10



RF frontend

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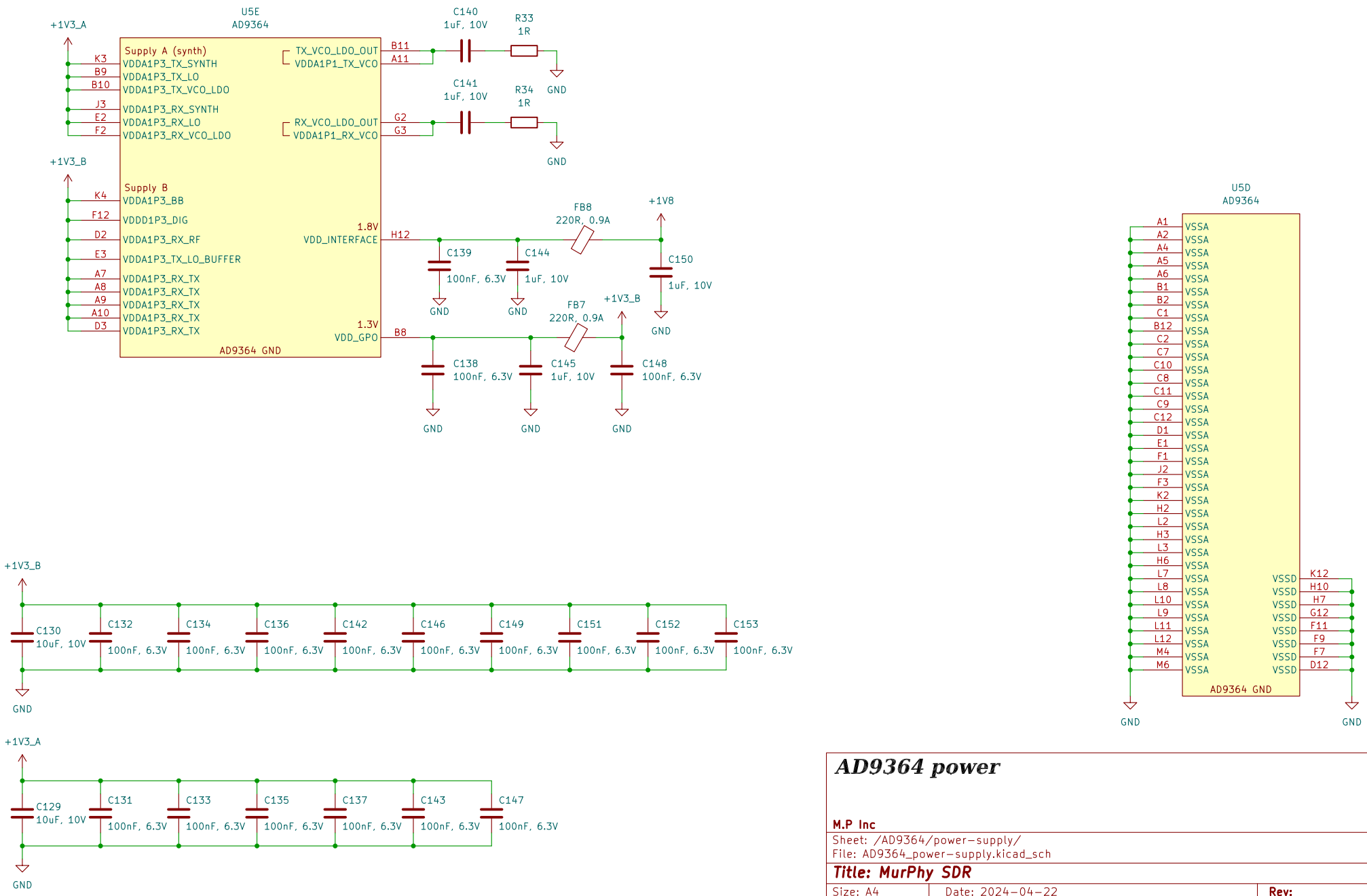

AD9364 power

M.P Inc

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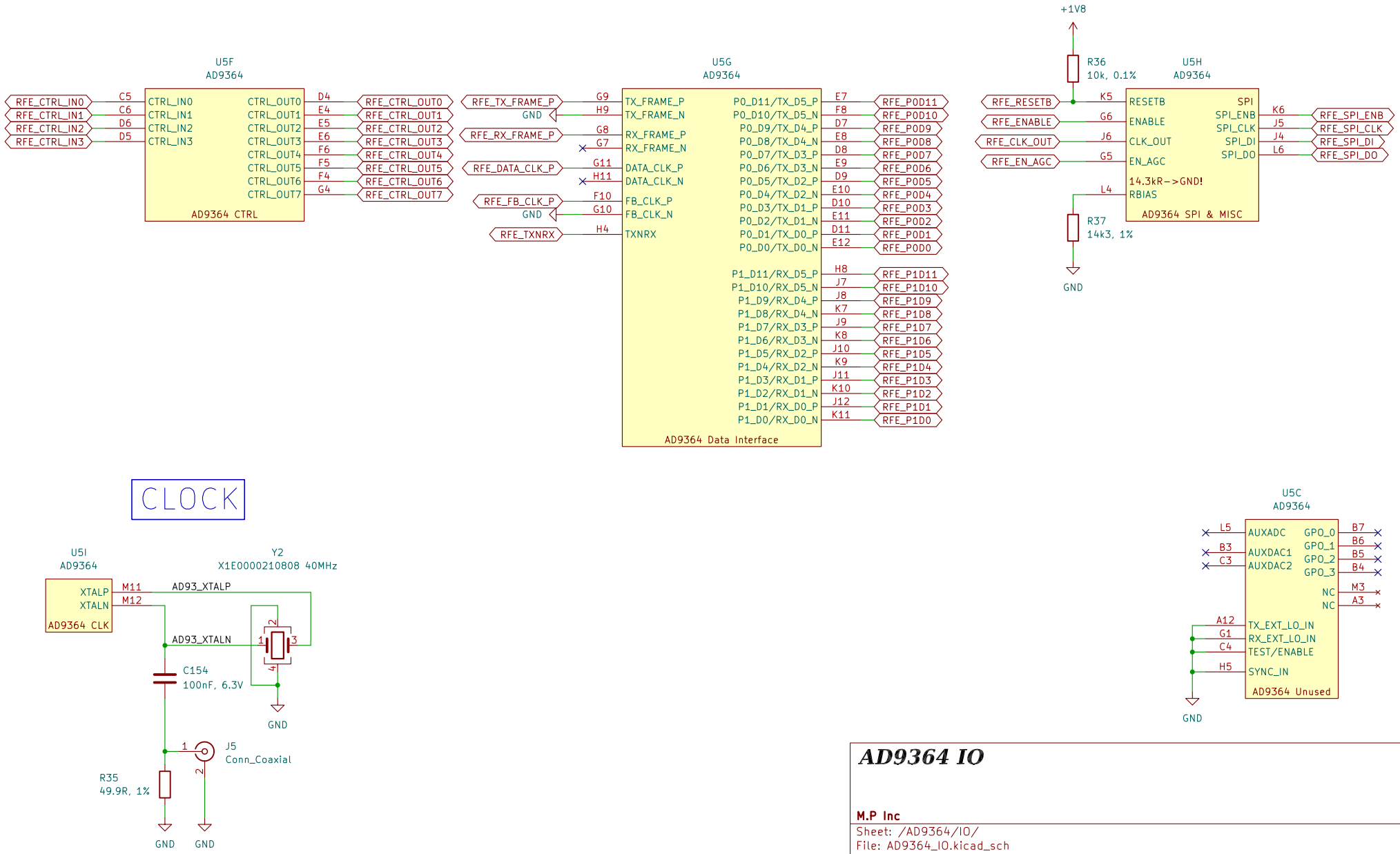

AD9364 IO

M.P Inc

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