The mute function is obtained during power-up of the device or by sending any binary data of 01001111 and above (to 11111111) serially to the device. The device may be placed into mute from a previous attenuation setting by sending any of the above data. This allows the designer to place a mute button onto his system which could cause a microcontroller to send the appropriate data to a µPot and thus mute any or all channels. Since this function is achieved through software, the designer has a great amount of flexibility in configuring the system.

DC INPUTS

Although the µPot was designed to be used as an attenuator for signals within the audio spectrum, the device is capable of tracking an input DC voltage. The device will track DC voltages to a diode drop above each supply rail.

One point to remember about DC tracking is that with a buffer at the output of the µPot, the resolution of DC tracking will depend upon the gain configuration of that output buffer and its supply voltage. It should also be remembered that the output buffer's supply voltage does not have to be the same as the µPot's supply voltage. This could allow for more resolution when DC tracking.

SERIAL DATA FORMAT

The LM1973 uses a 3-wire serial communication format that is easily controlled by a microcontroller. The timing for the 3-wire set, comprised of DATA-IN, CLOCK, and LOAD/SHIFT is shown in Figure 3. Figure 22 exhibits in block diagram form how the digital interface controls the tap switches which select the appropriate attenuation level. As depicted in Figure 3, the LOAD/SHIFT line is to go low at least 150 ns before the rising edge of the first clock pulse and is to remain low throughout the transmission of each set of 16 data bits. The serial data is comprised of 8 bits for channel selection and 8 bits for attenuation setting. For both address data and attenuation setting data, the MSB is sent first and the 8 bits of address data are to be sent before the 8 bits of attenuation data. Please refer to Figure 20 to confirm the serial data format transfer process.

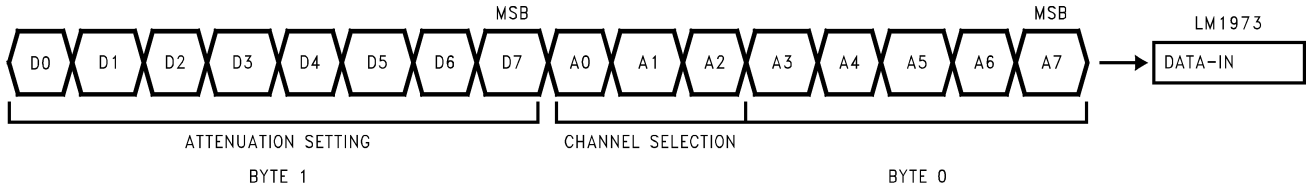

Figure 20. Serial Data Format Transfer Process

Table 1. LM1973 Micropot Attenuator Register Set Description

MSB: LSB	
Address Register (Byte 0)	
0000 0000	Channel 1
0000 0001	Channel 2
0000 0010	Channel 3
Data Register (Byte 1)	
Contents	**Attenuation Level dB**
0000 0000	0.0
0000 0001	0.5
0000 0010	1.0
0000 0011	1.5
: : : : :	: :
0001 1110	15.0
0001 1111	15.5
0010 0000	16.0
0010 0001	17.0
0010 0010	18.0

Table 1. LM1973 Micropot Attenuator Register Set Description (continued)

MSB: LSB	
Address Register (Byte 0)	
: : : : :	: :
0011 1110	46.0
0011 1111	47.0
0100 0000	48.0
0100 0001	50.0
0100 0010	52.0
: : : : :	: :
0100 1100	72.0
0100 1101	74.0
0100 1110	76.0
0100 1111	100.0 (Mute)
0101 0000	100.0 (Mute)
: : : : :	: :
1111 1110	100.0 (Mute)
1111 1111	100.0 (Mute)

µPot SYSTEM ARCHITECTURE

The µPot's digital interface is essentially a shift register, where serial data is shifted in, latched, and then decoded. As new data is shifted into the DATA-IN pin, the previously latched data is shifted out the DATA-OUT pin. Once the data is shifted in, the LOAD/SHIFT line goes high, latching in the new data. The data is then decoded and the appropriate switch is activated to set the desired attenuation level for the selected channel. This process is continued each and every time an attenuation change is made. Each channel is updated, only, when that channel is selected for an attenuator change or the system is powered down and then back up again. When the µPot is powered up, each channel is placed into the muted mode.

µPot LADDER ARCHITECTURE

Each channel of a µPot has its own independent resistor ladder network. As shown in Figure 21, the ladder consists of multiple R1/R2 elements which make up the attenuation scheme. Within each element there are tap switches that select the appropriate attenuation level corresponding to the data bits in Table 1. It can be seen in Figure 21 that the input impedance for the channel is a constant value regardless of which tap switch is selected, while the output impedance varies according to the tap switch selected.

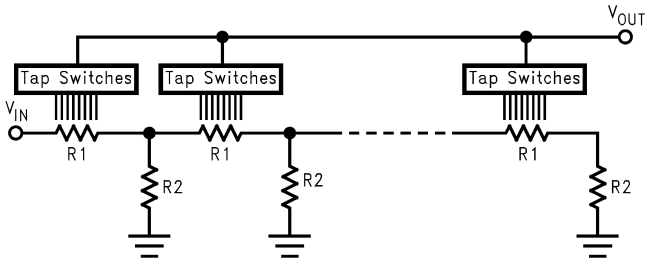

Figure 21. µPot Ladder Architecture

DIGITAL LINE COMPATIBILITY

The µPot's digital interface section is compatible with either TTL or CMOS logic due to the shift register inputs acting upon a threshold voltage of 2 diode drops or approximately 1.4V.